Challenges and Solutions in 3DIC Extractions

Dusan Petranovic
Design2Silicon Division

Mentor Graphics®

Agenda

I. Status of 3DIC integration
II. Die stacking configurations
III. Stack verification and extraction methodology
IV. New challenges in extraction and future work
V. Conclusion

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

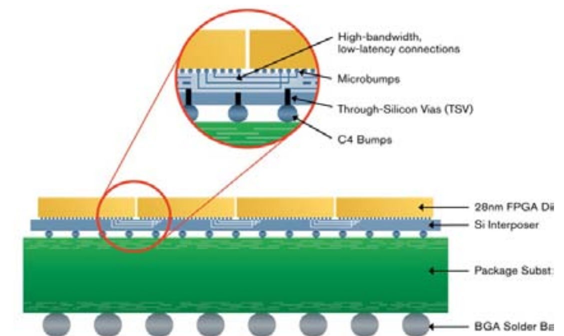
Status of TSV based 3D-IC

- 3D ICs are real. Lot of activities and announcements

Company	Interposers		3D with TSV	
TSMC	2H 2011	[2]	2012-2013	[3]
UMC			2H 2011	[4]
GlobalFoundries			2013	[5]
IBM	2011	[6]		
Samsung			2012	[7]
Elpida			2H 2011	[4]
Micron			2012	[8]
Nanya			2011-2012	[9]
ASE	2012-2013	[10]		
STATSChipPAC			2013	[11]
Amkor	2H 2011	[3]		
SPIL	2011	[12]	2012	[12]
Qualcomm			2013	[12]
Nokia			2012-2013	[12]
Xilinx	2H 2011	[2]		
Dell			2012	[13]

Source: P.Garrou, Micronews, Jan.2011.

- Driven by the customer demands for more functionality,
  larger bandwidth, low power, smaller size;
- Inability of 2D SoC to respond to the customer demands
  in cost effective and timely manner.
- Problems with further scaling and SoC are becoming more obvious
  ROI shrinks with every new technology node
  Fab cost, process R&D, mask set, Chip Design, EDA,…
- There are still challenges in 3DIC but no technological show stoppers

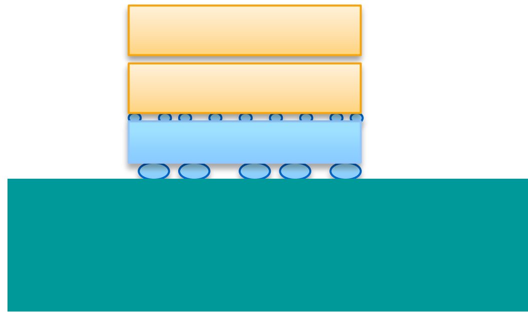


Source: www.xilinx.com/technology/roadmap/ssi-technology.htm

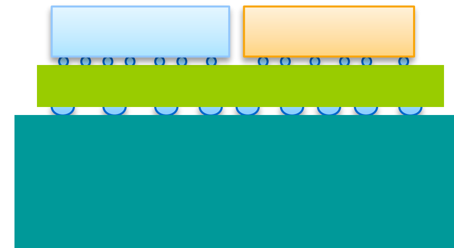
- Various configurations -- 2.5 D (interposer based) and 3D
  Interposers got into the center of attention due to the industry first stacked silicon (Xillinx Virtex FPGA)
- Will stay around long, but might not be sufficiently good for all applications

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

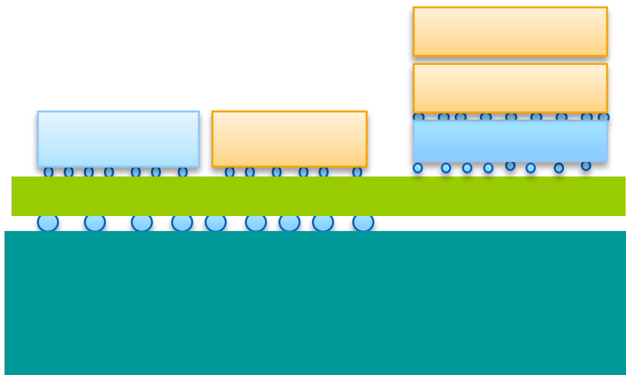
Some of the typical 3DIC configurations



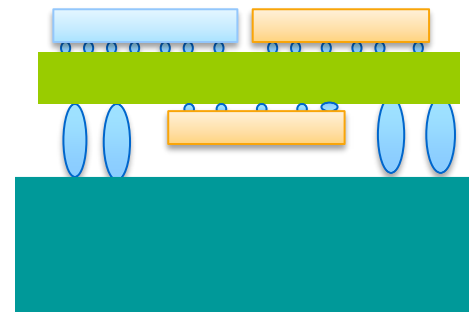
3D Memory on Logic
One or More DRAM die stacked directly on logic die



2.5D Side by side die stacked on a passive interposer that includes TSV's



3D + Interposer
Mix of side by side and stacked implementations on an interposer

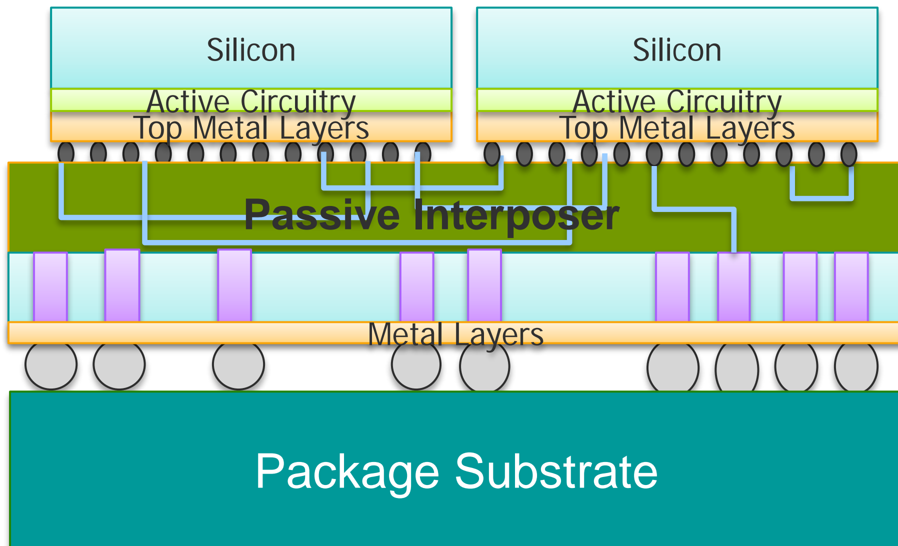


2.5D or 3D Interposer with top and bottom connection

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

2.5D vs. 3D configurations

2.5D Stacking, Interposer

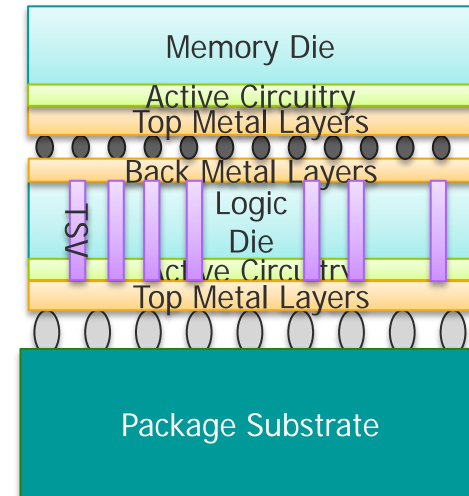


Advantage: No on-chip TSVs

Concern: Interposer size and cost

Applications: Not- Phone driven

3D Stacking, Die on Die



Advantage: Form factor, performance, power

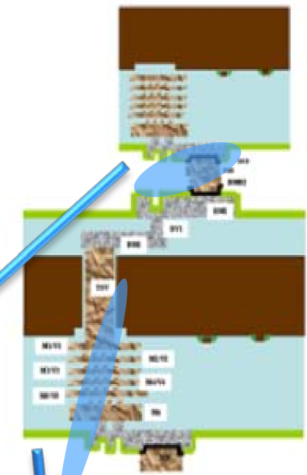
Concern: TSV integration, thermal, stress

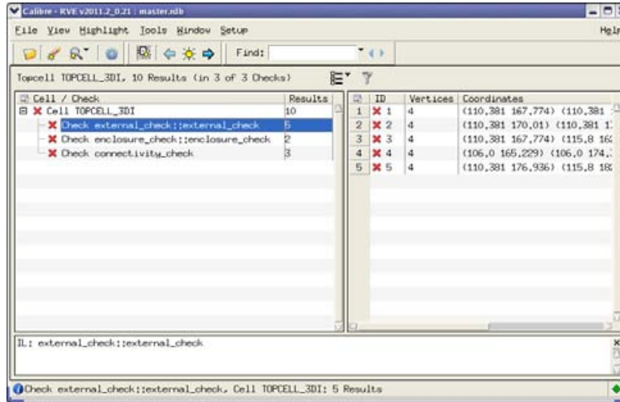
Applications : Mobile phone driven

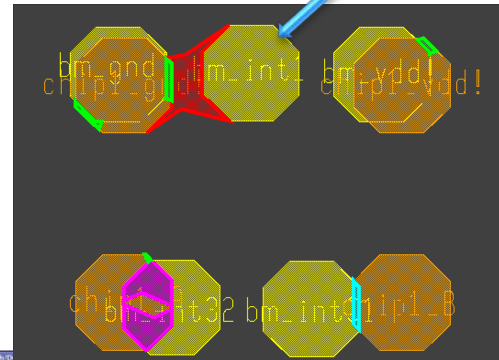
© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

3D-IC
Physical Verification

- DRC: verify micro-bumps are physically aligned
- LVS: verify proper electrical connectivity through die interfaces



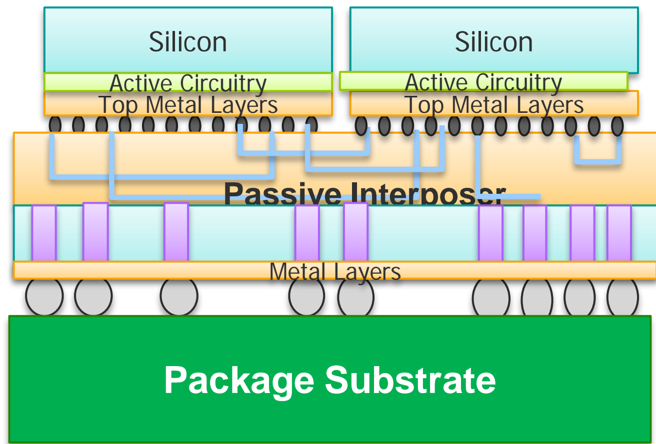




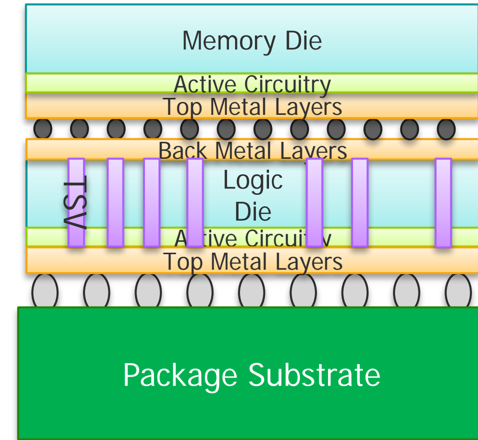
- PEX: Extracts parasitics of interconnect and BRDL
- Inserts provided TSV circuit into the netlists

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

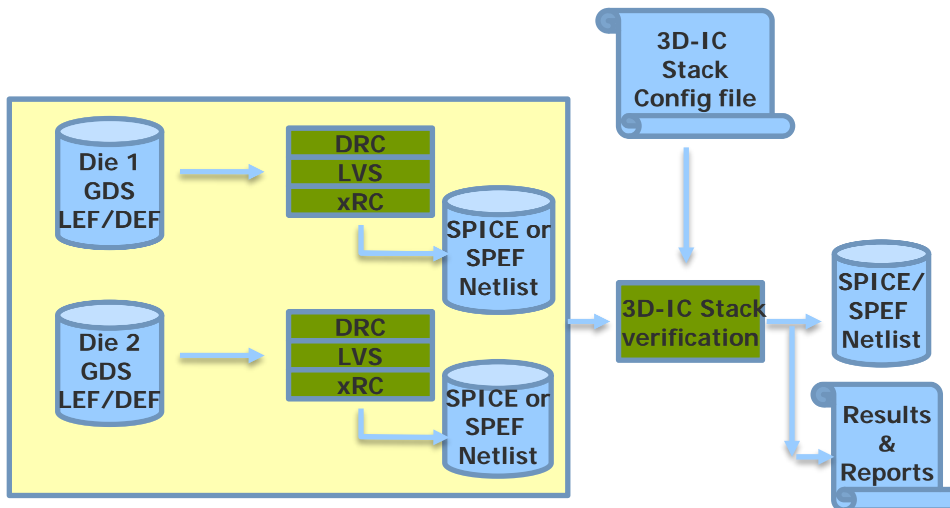
3D-IC Verification Flows



2.5D



3D



- Single net-list for double sided die (3D) including front metal parasitics, TSV and back metal parasitics stack including TSV and backside metal
- Separate Interposer netlist (2.5D)
- Combined netlist, if desired, for simulation across the dies in the stack

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Verification Flows: Analog vs. Digital

Analog flow

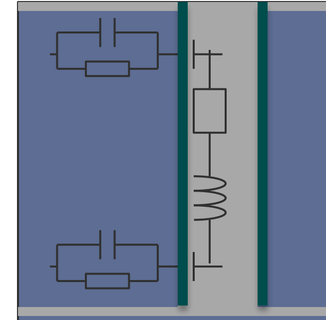
- Requires more accurate TSV model
- Treat TSV as a LVS device or as a via
- LVS device described by Spice sub-circuit
- Generates HSPICE, ELDO netlist
- Dynamic circuit simulation

Digital flow

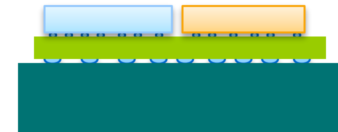
- Lower accuracy model requirements
- Treat TSV as a via
- Extraction tool generates R(C) model
  Can be replaced by provided model
- Generates SPEF or DSPF netlist
- Static timing analysis

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

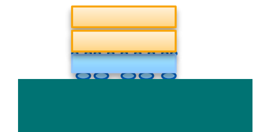
Issues in the existing verification solutions



- Present Solution
  - TSV as LVS device or as a VIA
  - Circuit for TSV provided
    - Typically obtained by S-parameter measurements and circuit parameter extraction
  - Model of arbitrary complexity supported for TSV in simulation
  - Double-sided die front and back metal parasitic extraction
  - Sufficiently good for some applications (regular layout, no RDL, low density TSVs)



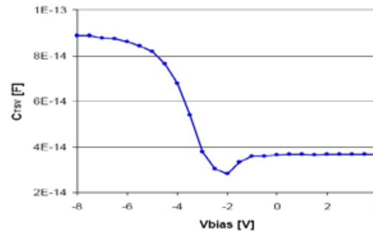
- Problems with the existing solutions
  - Not adequate for high density, high frequency applications
  - Problem with non-uniform environment around the TSVs
  - Does not account for TSV interactions with other TSVs, interconnect, devices
  - Does not consider inter-die interactions



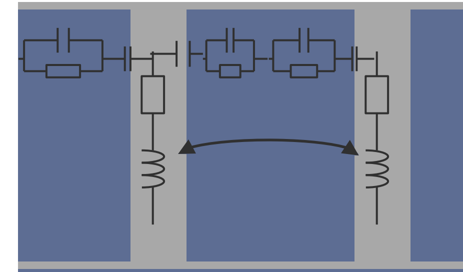
© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Issues in Modeling of TSVs and their interactions

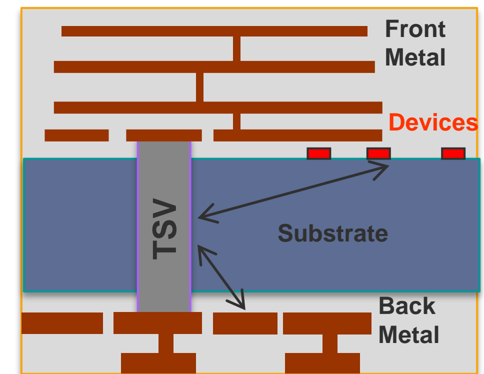
- TSD or TSV
  - Nonlinear behavior



- Interactions between the TSVs
  - Capacitive and Inductive couplings



- Interaction between TSV and interconnect
  - Interactions with RDL and metal lines

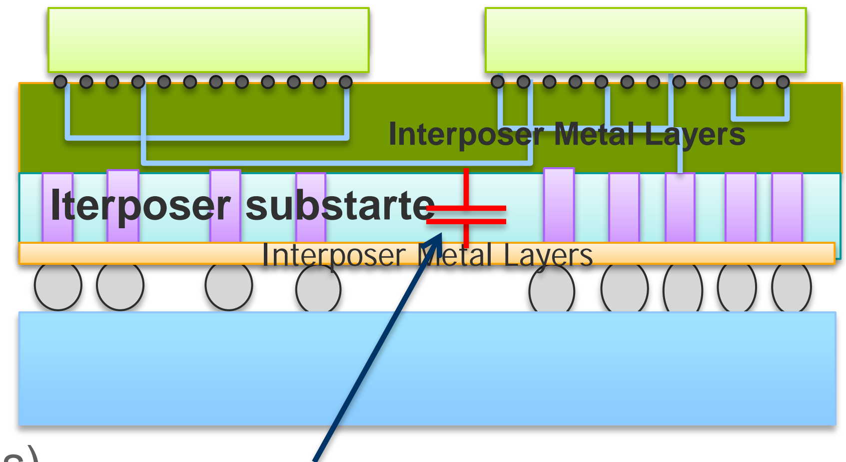


- Impact of TSVs on device performance
  - Proper substrate description and modeling is needed

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Interposer couplings

- Interposer metal coupling might be significant
- In 3D configurations substrate is grounded; Interposer substrate is floating
- Hard to take into account with rule based extraction due to semiconductor nature of the substrate and frequency dependence of couplings



- Substrate treated as
  - Dielectric (for higher frequencies)
  - Floating Metal (for lower frequencies)
- Not accurate for all frequencies of interest

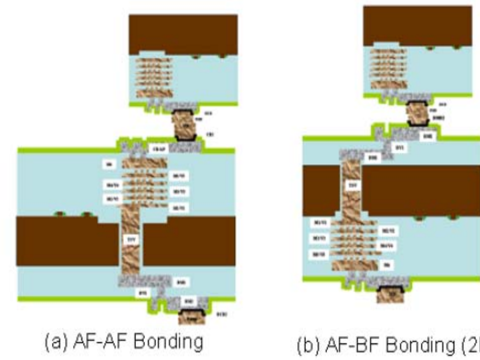
In 2.5D Configurations This coupling might need to be modeled!?

- Field Solver based solution might be needed

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Dies Interface modeling

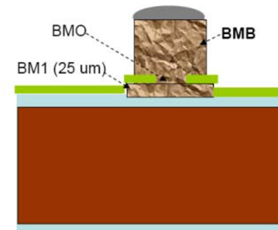
- Bump/Pillar bonding is common

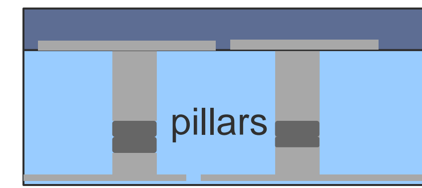


(a) AF-AF Bonding (b) AF-BF Bonding (2BM)

Source: Qualcomm

- Bump/Pillar modeling, interactions and shielding





- Other bonding techniques

  Typical for Monolithic 3DIC (3DIC Si Integration)
  - Cu-Cu bonding
  - Oxide bonding

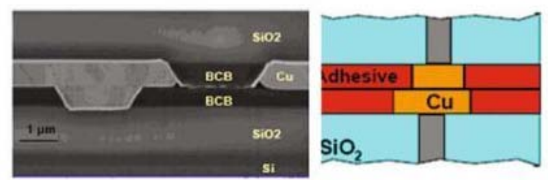
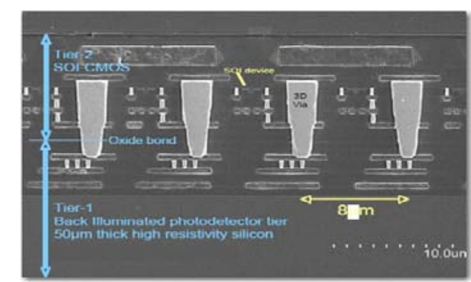


Fig. 1.35 A die-Stack using a combination of Cu-Cu and BCB adhesive bonding at RPI [14]

Source: RPI

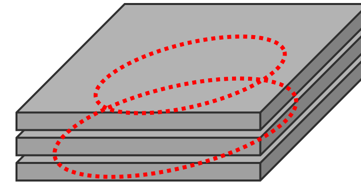


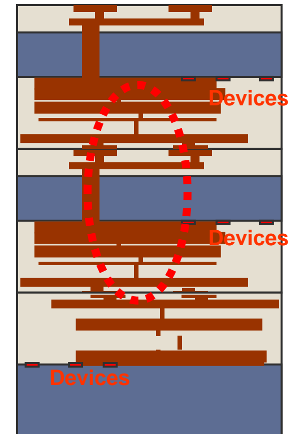
Source: Lincoln Lab

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Inter-die interactions

- Capacitive coupling might not be negligible between the dies, especially in Face-to-Face connection





- Magnetic coupling between the dies
  — The dies are getting closer together
  — Overlapping loops between the dies
- Full stack IR drop is needed
  — As number of TSVs is increasing, the interactions are becoming stronger, and IR drop analysis has to be done simultaneously for the entire stack
- The paths go across the dies and LVS, extraction and simulation have to go across the dies.

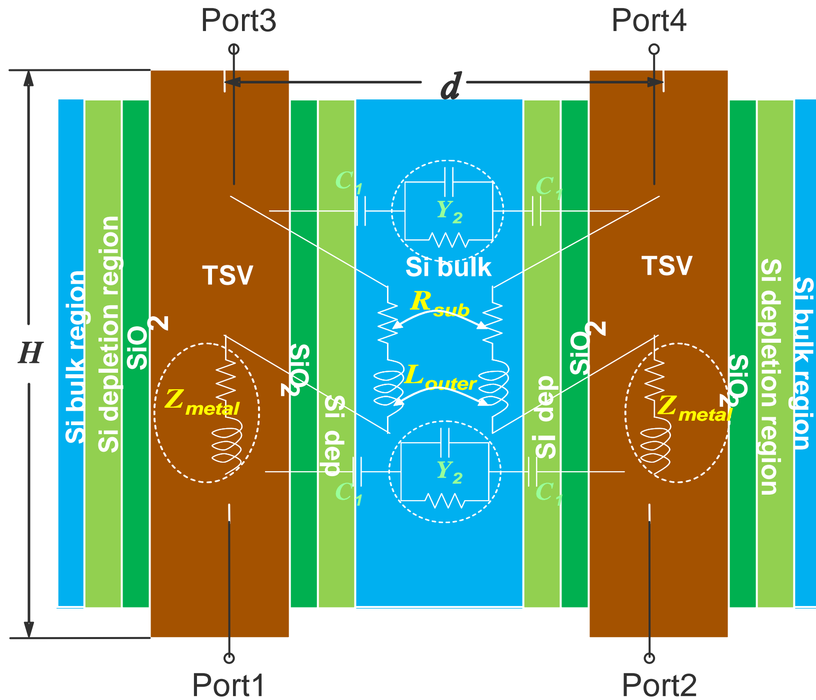
© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Alternative Modeling Approaches

- Single TSV models
  - Advantage
    - Easy to integrate into a flow ; Sufficient for present needs
  - Challenges
    - Not adequate for high density, high frequency applications
- Compact models
  - Advantage
    - Can account for some interactions; Faster than FS
  - Challenges
    - Hard to account for all situations, to parameterize for all important variables
- Field solver approach
  - Advantage
    - Most accurate
  - Challenges
    - Performance; Integration

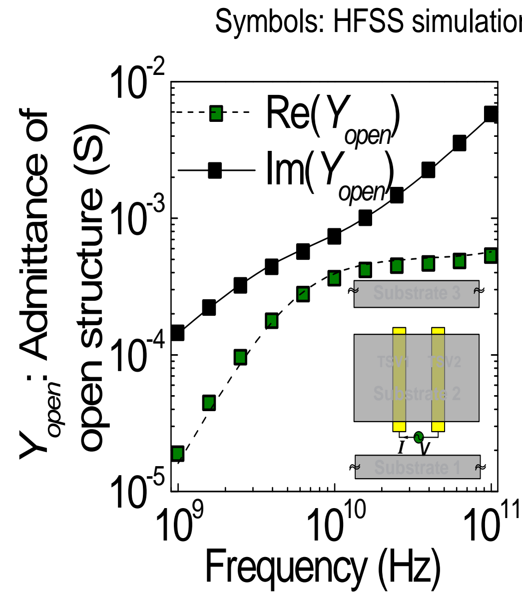
© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

TSV Modeling: Compact Model for a TSV Pair

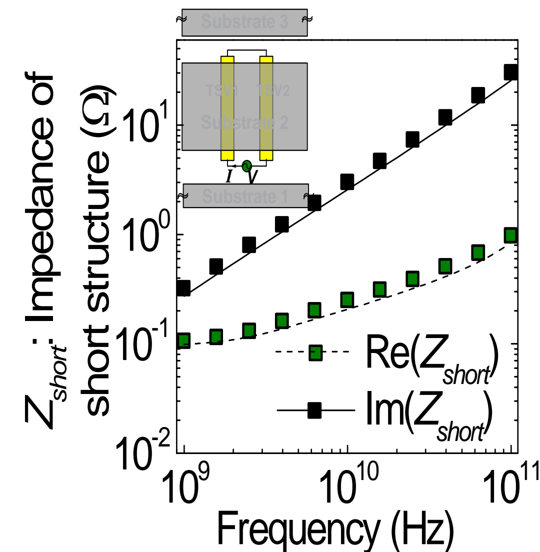


Models-based results show good agreement with Field solver results (HFSS)

Symbols: HFSS simulation   Lines: Analytical model



Open Structure



Short Structure

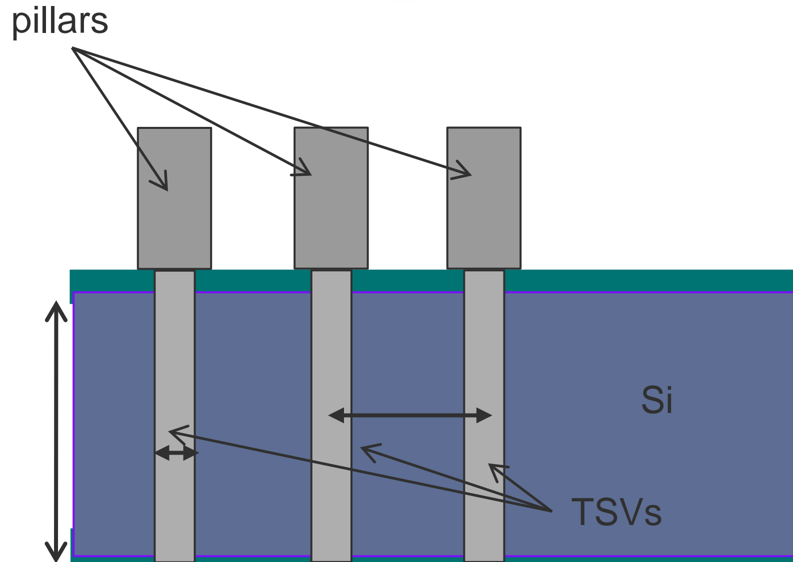
Compact RLGC Model accounts for

- Wide frequency range
- Skin effect
- Eddy currents in substrate
- MOS effect

Source: C. Xu, H. Li, R. Suaya, and K. Banerjee, "Compact AC Modeling and Analysis of Cu, W, and CNT Based Through-Silicon Vias (TSVs) in 3-D ICs," in /IEDM /Tech. Dig./, 2009, pp.521-524

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

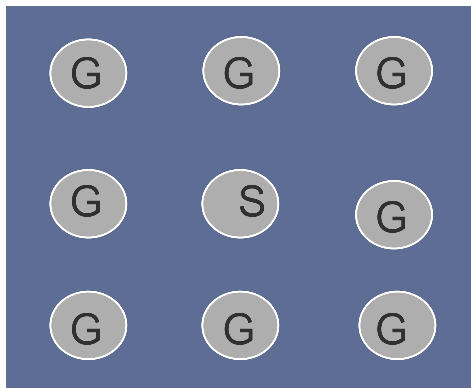
TSV Modeling: Fast Field Solver

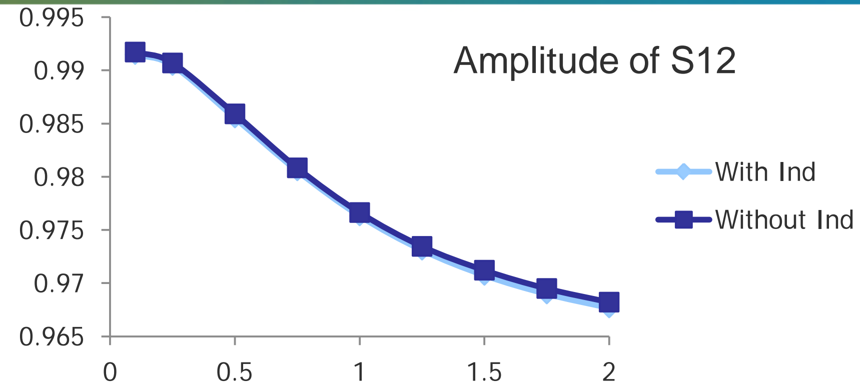


Two ports defined:

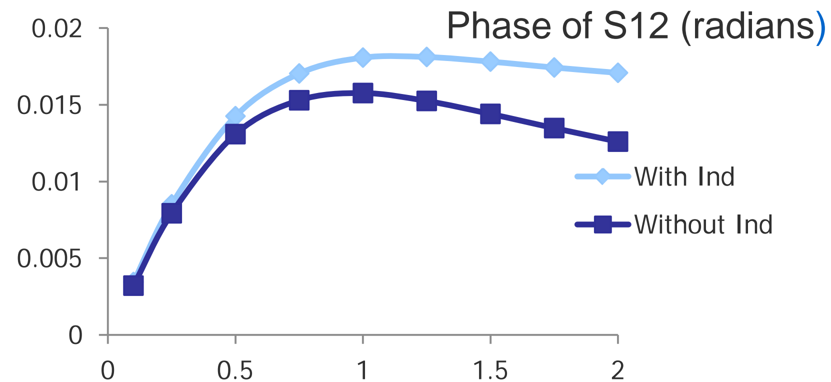
Port 1: Signal Pillar to Ground Pillars
Port 2: Signal TSV to Ground TSV
Ground TSVs are shortened together

Top View



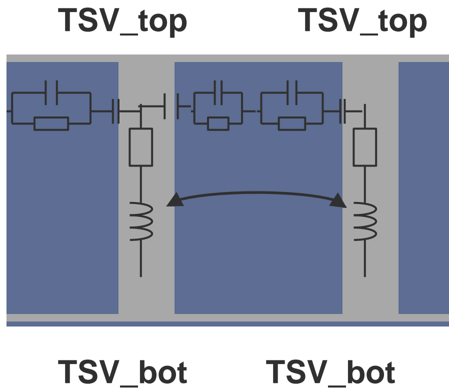


- Energy loss proportional to amplitude of $S12^2$
  - ~ 6% @ 1.5GHz
- Inductance effect begins to show divergence at ~ 500MHz

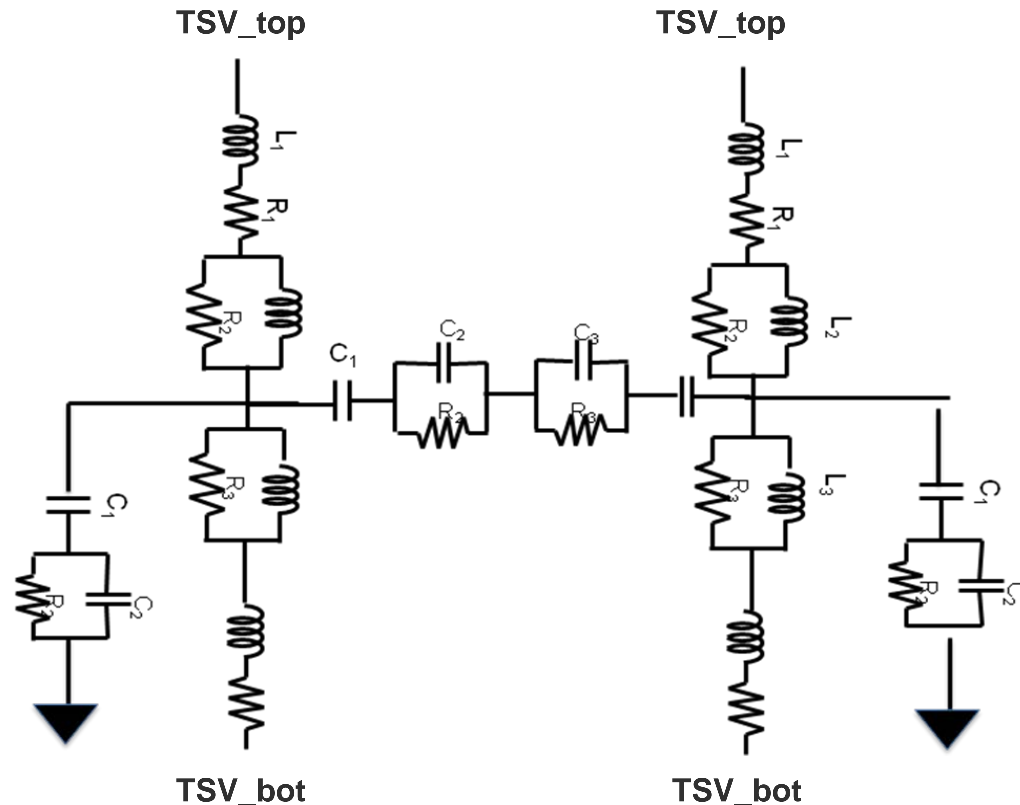


© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Fast Field Solver Output



Output:
Netlist of frequency-independent linear elements.
Values of those elements will be computed by fitting the frequency dependent results of the field solver



© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Conclusions

- Lot of challenges in design and verification of 3DICs, more in 3D then in 2.5D
- Present verification solutions inadequate for high TSV density and high frequency designs
- Challenges in parasitics extraction, not in DRC/LVS
- Determination of modeling/extraction accuracy needed to analyze TSV, intra and inter die interactions
- Need for modeling of TSVs and their interactions
- Fast field solver solution needed for accurate substrate effect modeling
- Efficient TSV model integration into the verification flows
- Analysis with inter die process variability

Source: Qualcomm

© 2011 Mentor Graphics Corp. All Rights Reserved
www.mentor.com
Mentor Graphics

Mentor Graphics®

www.mentor.com