

Mechanical Stresses and Reliability Study of Cu Through-Silicon Via (TSV) Samples Fabricated by SK Hynix vs. SEMATECH using Synchrotron X-Ray Microdiffraction for 3-D Integration and Reliability

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Outline

- **Background – Mechanical Stresses and Reliability/Performance Implications in 3-D Cu TSV Integration Schemes**
- **The Technique – Synchrotron X-Ray Submicron Diffraction (White and Monochromatic Beam)**
- **Experimental –**
 - **Mechanical Stresses in Cu TSV and Their Potential Impacts on 3-D Interconnect Reliability: SK Hynix vs. SEMATECH**
 - **Mechanical Stresses in Silicon Surrounding TSV and Their Potential Impacts on 3-D Interconnect Performance as well as Reliability: SK Hynix vs. SEMATECH**
- **Conclusions & Future Work**

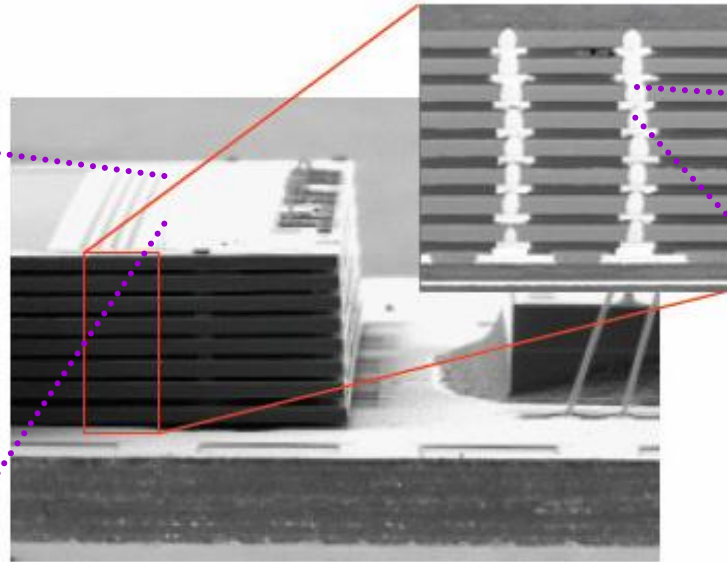
Impact to Reliability and Performance of Device

❖ Si stress

Keep-away zone

Device must be kept away from the zone in which mobility is changed.

Si cracking

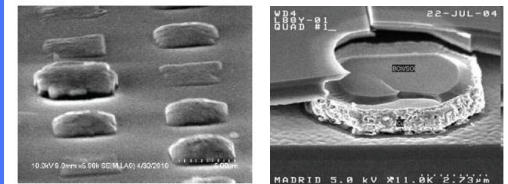


<Samsung Electronics>

❖ Cu stress

Debonding, TSV cracking

TSV Pop-up, Bulging-up → Integration Issues

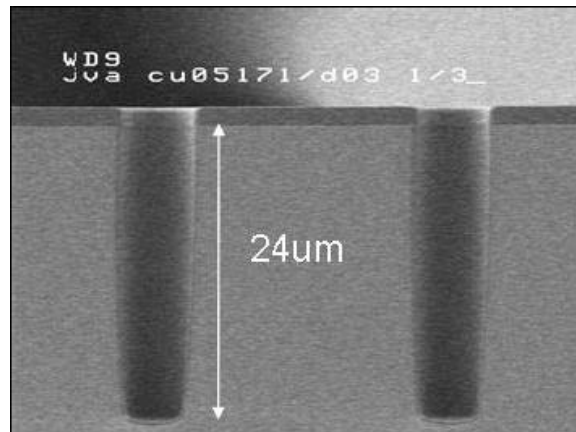
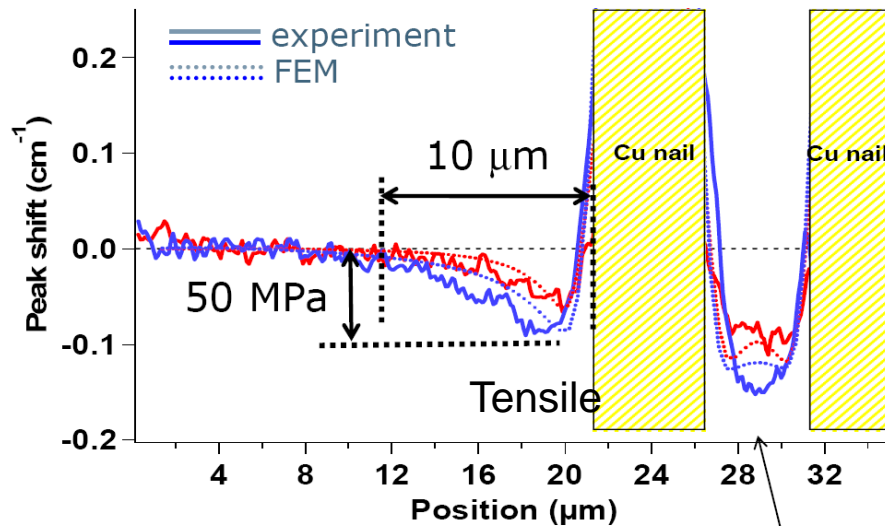


<Source: SEMATECH>

- Thermal stress of TSV → Si stress and Cu stress.
- Si stress (residual stress) → degradation of device performance.
- Cu stress (thermal stress) → mechanical failure of Cu TSV.

Stress of Si : μ -Raman spectroscopy

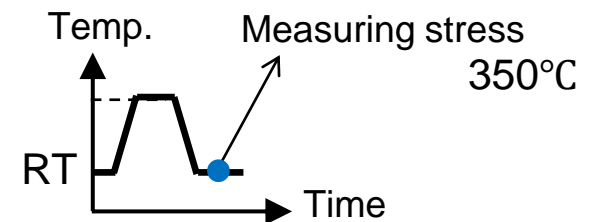
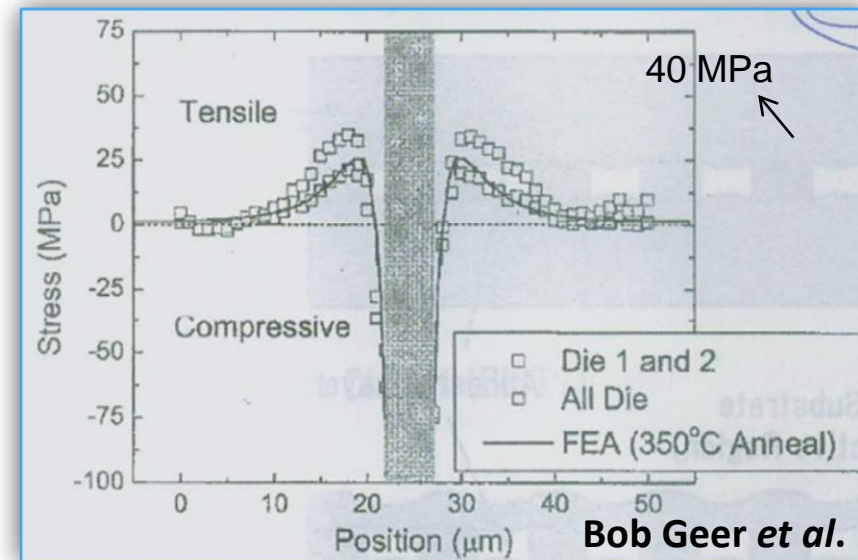
Okoro, *et al.*, IRPS, 2010



Diameter 5 μm ,
pitch 10 μm ,
depth 24 μm

- TSV-induced stress extends about 10 μm in Si
- 50 MPa **tensile stress in Si** after cycling

Lee, *et al.*, TSV 3D Packaging Technology Workshop, 2010

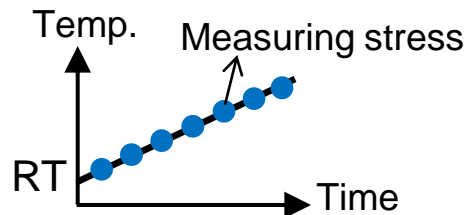
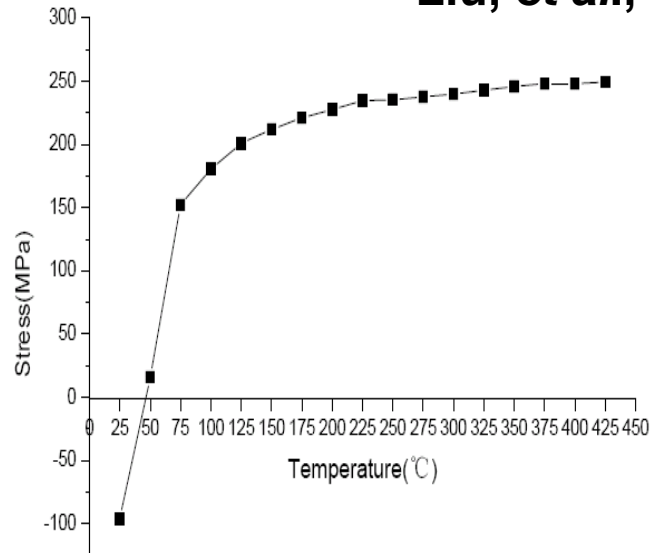


- 40 MPa **tensile stress in Si** was developed near Cu TSV after cycling.

Stress of Cu : Laboratory XRD

Lack of micron resolution

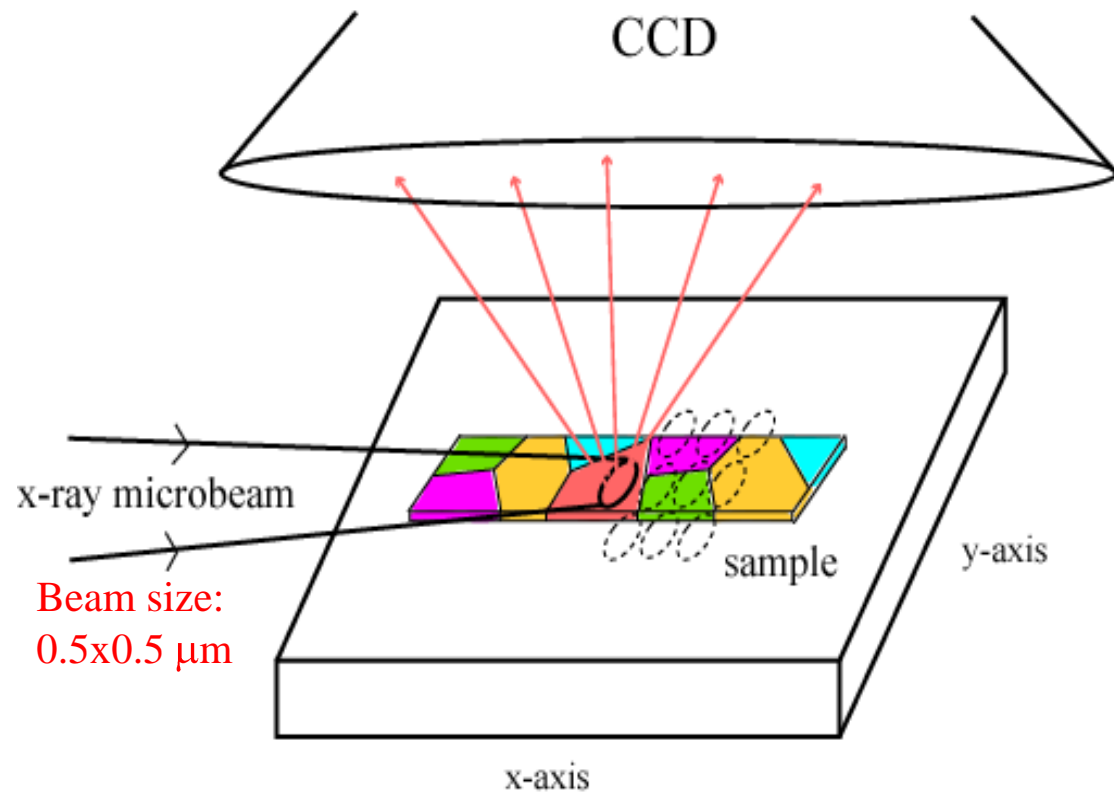
Liu, et al., ECTC, 2009



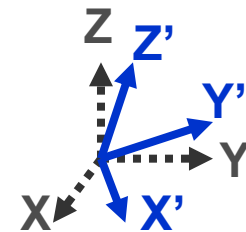
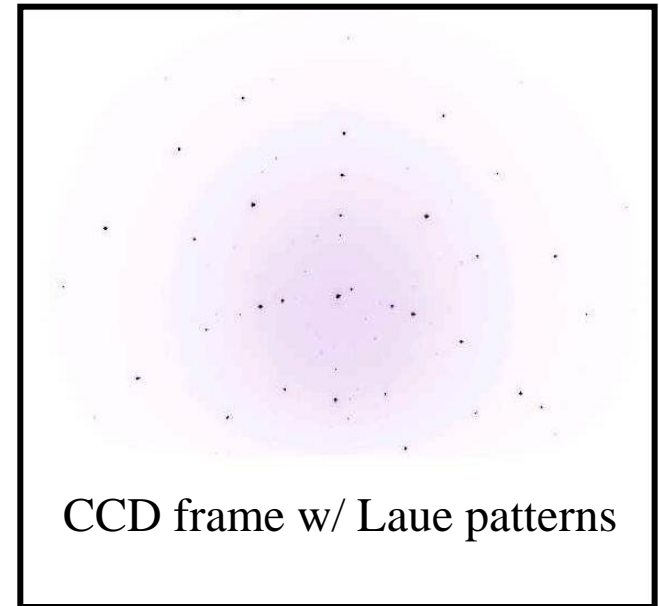
Diameter 70 μm , pitch
140 μm , depth 460 μm

- + 225 MPa at 200 °C.
- - 100 MPa at 25 °C.

Synchrotron X-Ray Sub-micron Diffraction

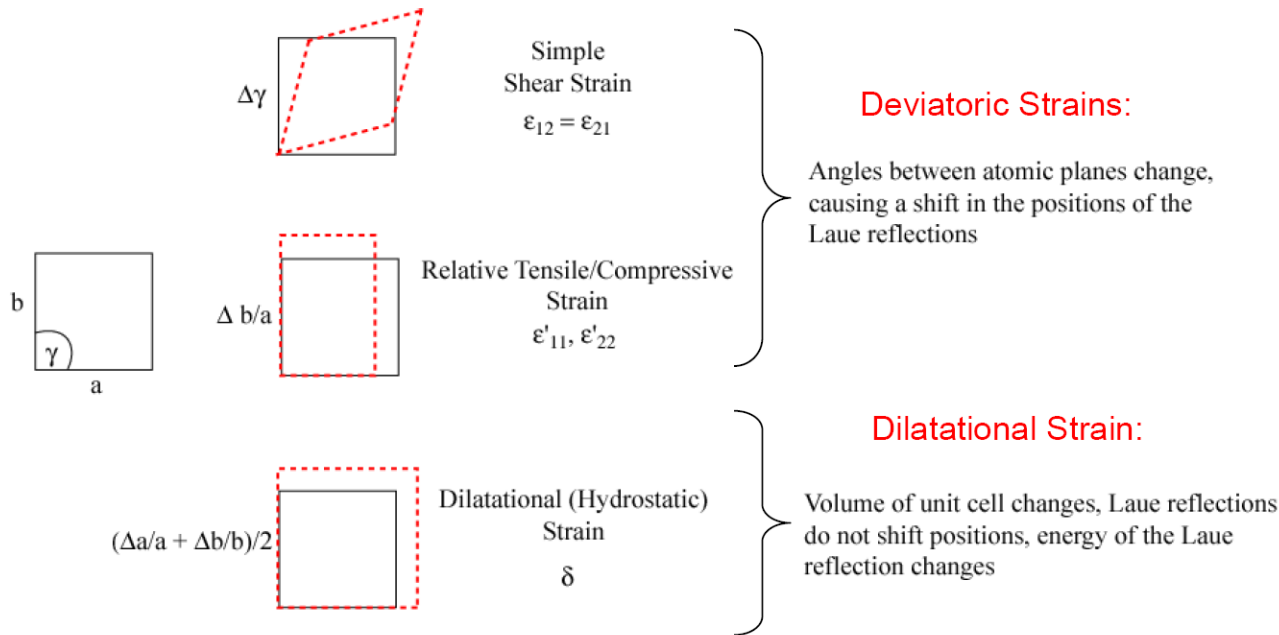


X-ray source: ALS Synchrotron,
Berkeley Lab (Beamline 12.3.2)



Deviatoric strain tensor: Small shifts in spot relative positions \rightarrow Crystal deformation at constant volume ($\sim 1 \times 10^{-4}$ accuracy)

Laue pattern and energy scanning analysis

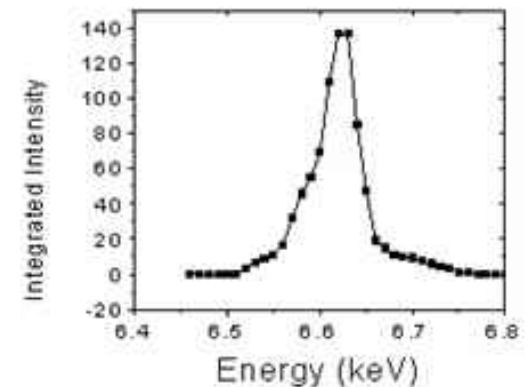


Laue
pattern

Energy
scanning

Total strain = dilatational + deviatoric
(Energy scan) + (Laue pattern)

$$\epsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \epsilon'_{11} & \epsilon_{12} & \epsilon_{13} \\ \epsilon_{21} & \epsilon'_{22} & \epsilon_{23} \\ \epsilon_{31} & \epsilon_{32} & \epsilon'_{33} \end{pmatrix}$$



Experimental

❖ Sample

Hynix: 20 μm TSV diameter, 90 μm pitch, 90 μm height

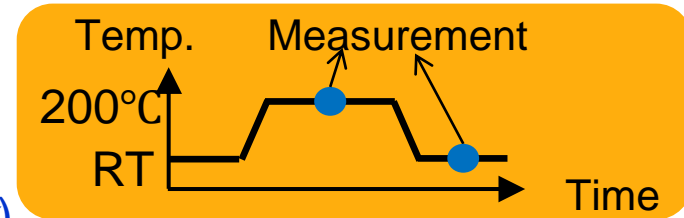
SEMATECH: 5.5 μm TSV diameter, 80 μm pitch, 50 μm height

❖ Condition of measurement

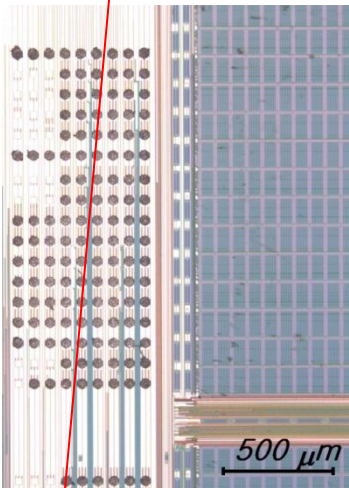
- Measurement of stress for : Si, Cu TSV
- Thermal treatment: *in situ* at 200 °C (**SK Hynix**)

ex situ post-annealed (200 °C for 1 hour) sample (**SK Hynix**)

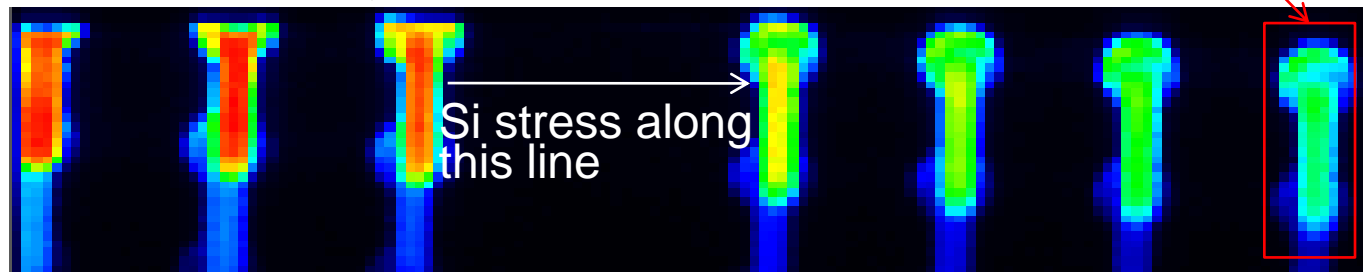
ex situ post-annealed (350 °C for 30 mins) - **SEMATECH**



Polished with angle



Cu stress within this area

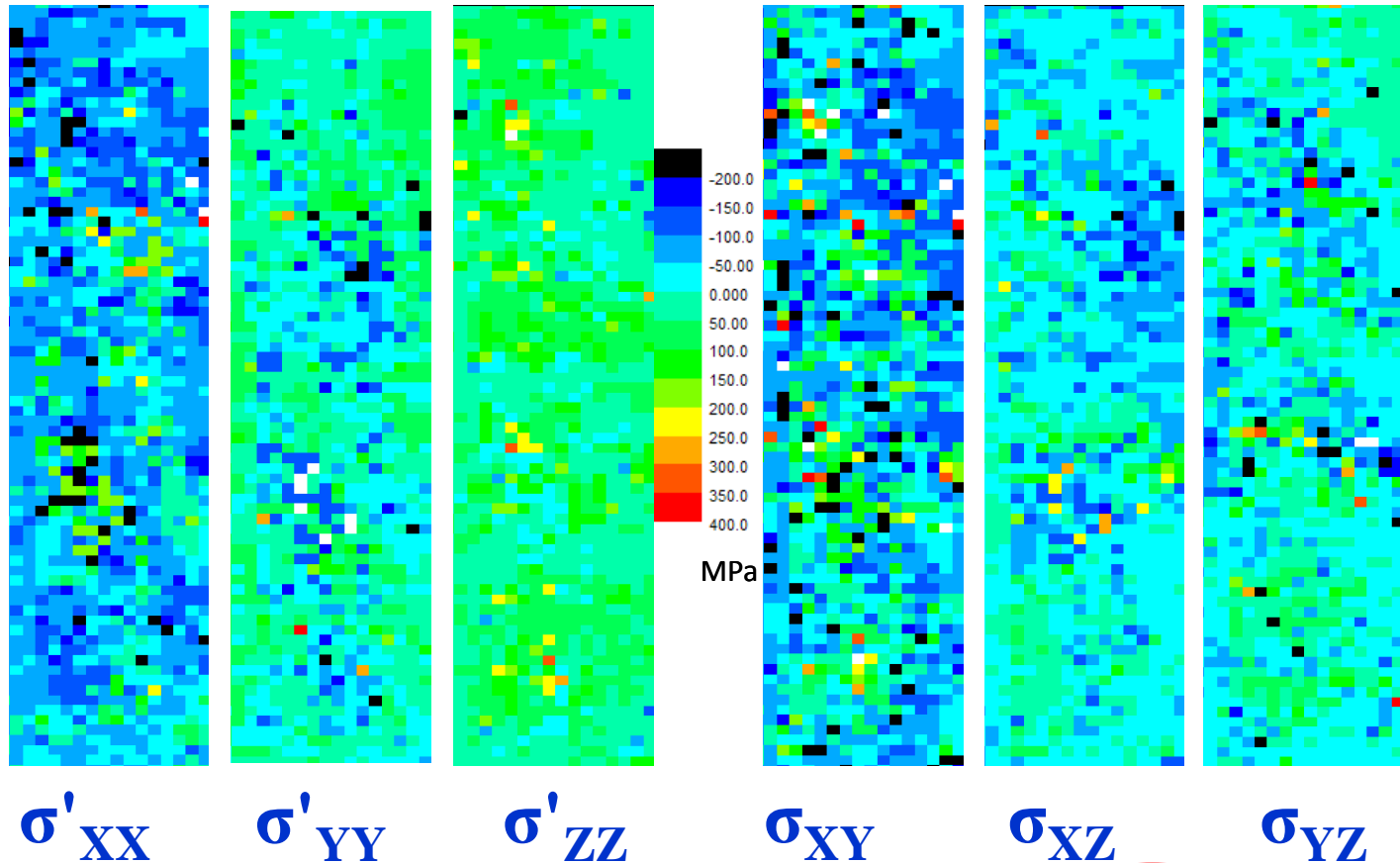
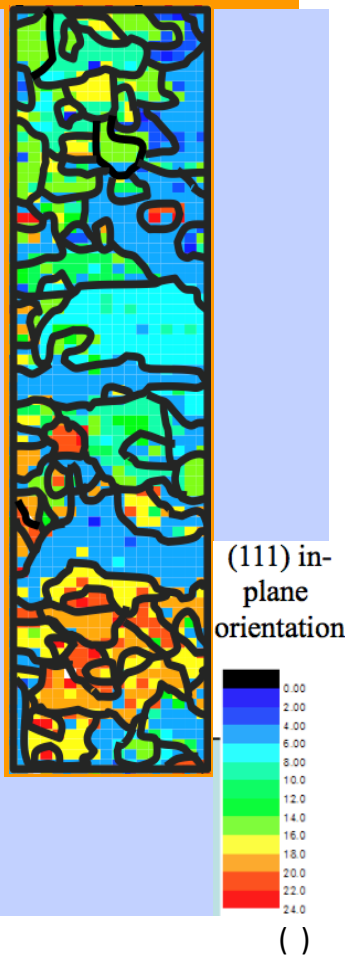
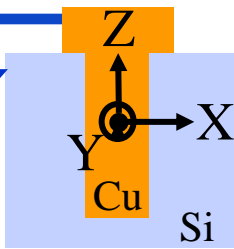


Top view of TSV array

XRF (from characteristic x-rays) image of TSV array

Cu Stress State in TSV – *SK Hynix*

- Post Annealed Sample (measure at RT)

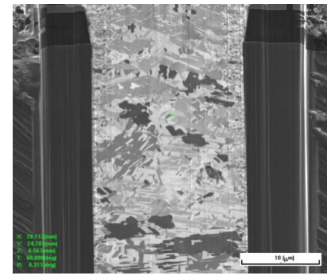
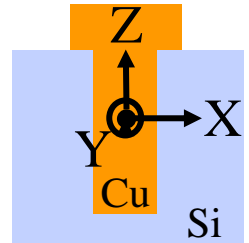
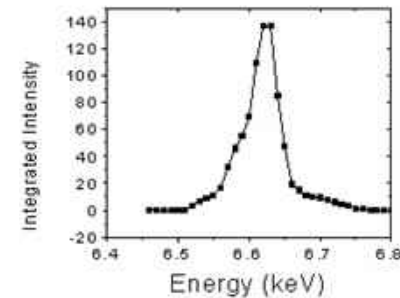
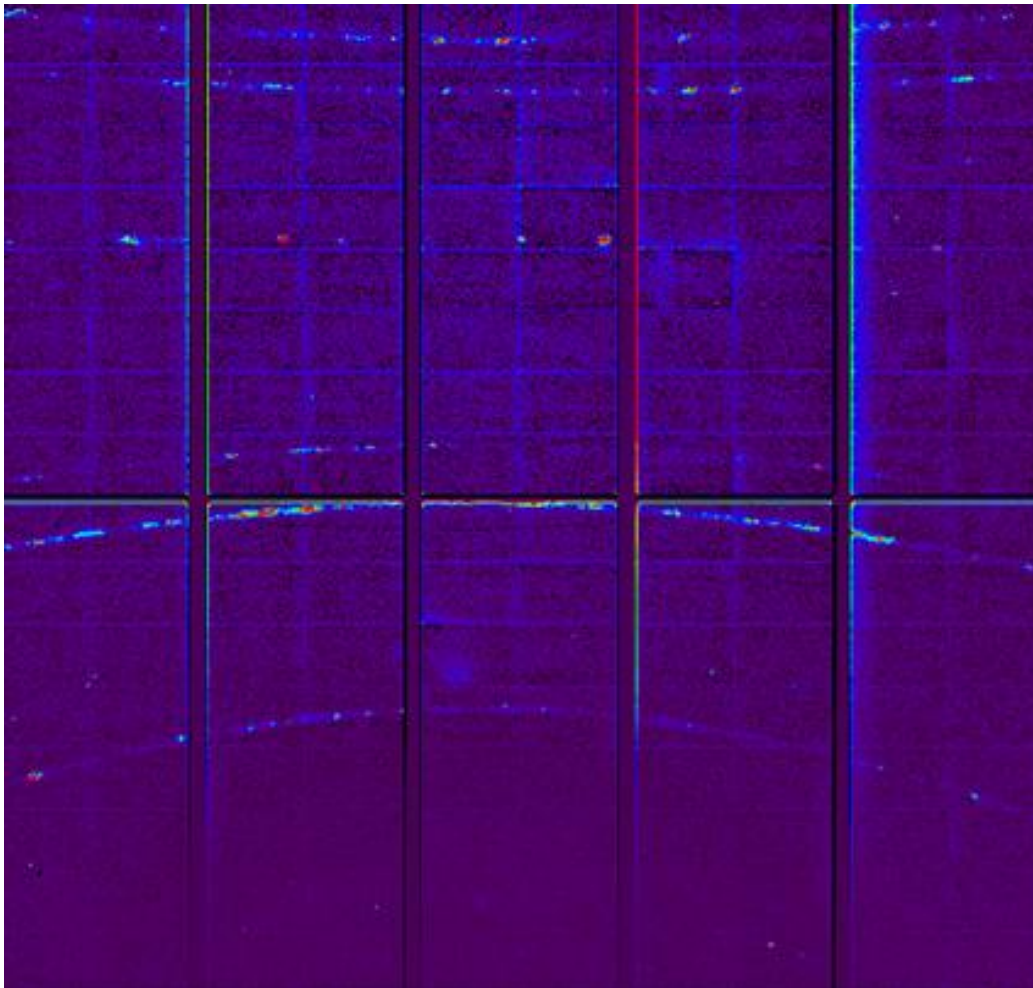


Only deviatoric components of stress

$$\varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon'_{12} & \varepsilon'_{13} \\ \varepsilon'_{21} & \varepsilon'_{22} & \varepsilon'_{23} \\ \varepsilon'_{31} & \varepsilon'_{32} & \varepsilon'_{33} \end{pmatrix}$$

Cu Hydrostatic Stress State in TSV – *SK Hynix*

- Post Annealed Sample (measure at RT)

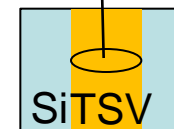


$$\varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon'_{12} & \varepsilon'_{13} \\ \varepsilon'_{21} & \varepsilon'_{22} & \varepsilon'_{23} \\ \varepsilon'_{31} & \varepsilon'_{32} & \varepsilon'_{33} \end{pmatrix}$$

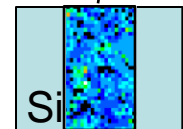
**Hydrostatic stress =
+166.6 MPa**

❖ Hydro + deviatoric

One area



All area scan



Stress Evolution in Cu TSV – *SK Hynix*

Cu hydrostatic stress

❖ As-received



233.8 MPa

❖ at 200°C

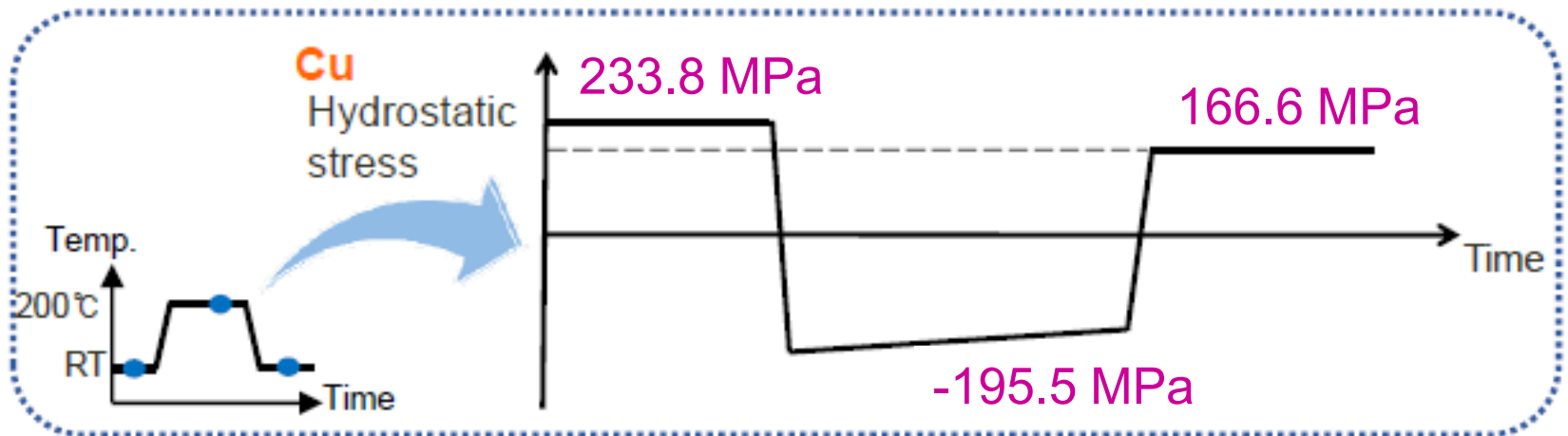


-195.5 MPa

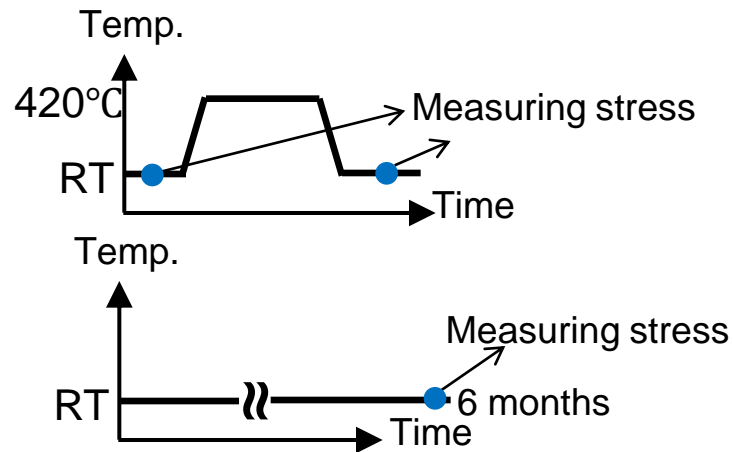
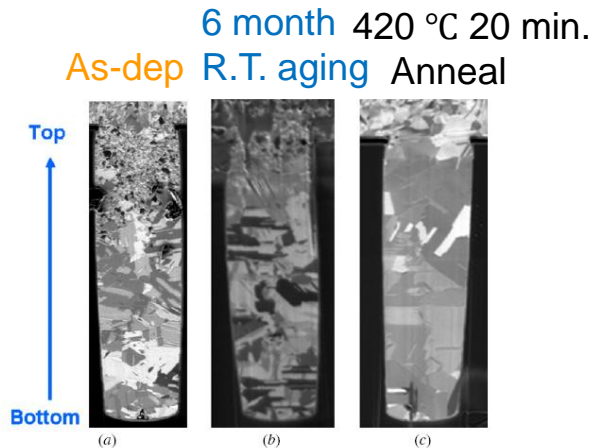
❖ After annealing



166.6 MPa

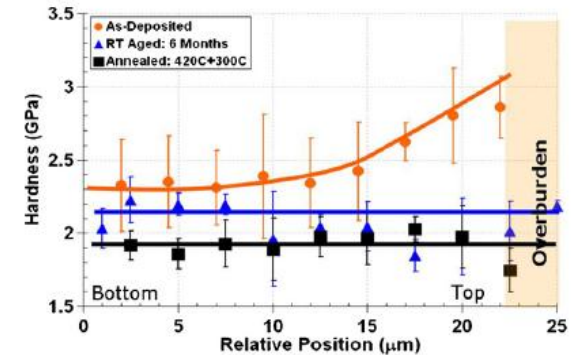


High Tensile in As-Received → Cu RT Grain Growth

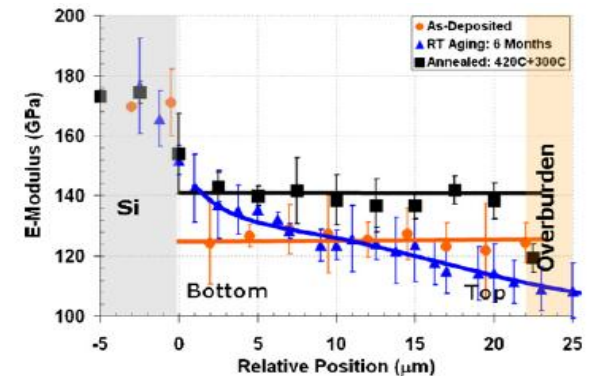


- Decreasing hardness → Cu stress toward **more tensile** stress after annealing and R. T. aging.

- Hardness change by annealing

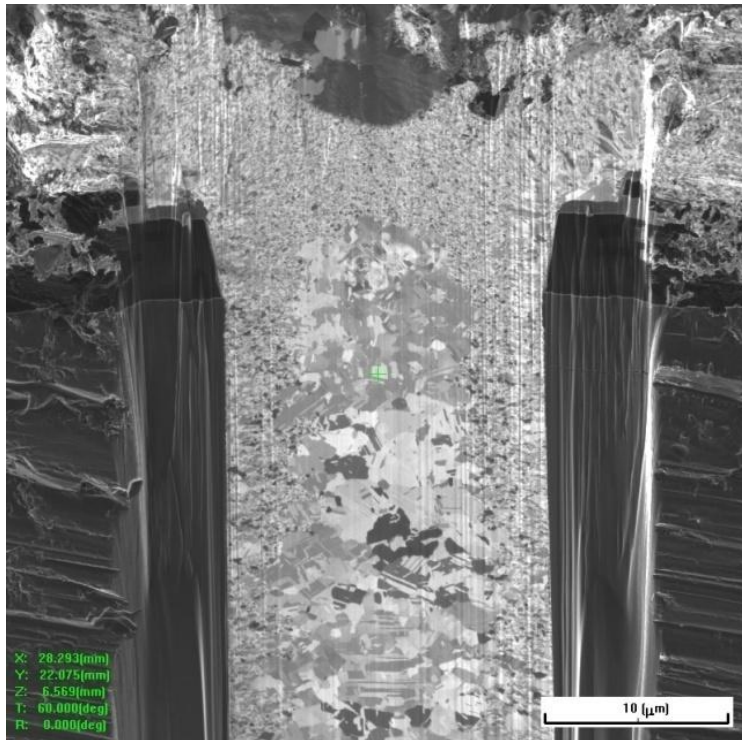


- Elastic modulus



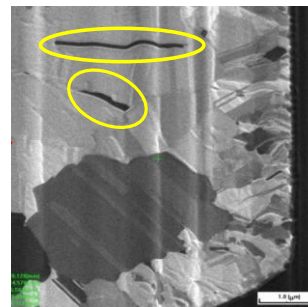
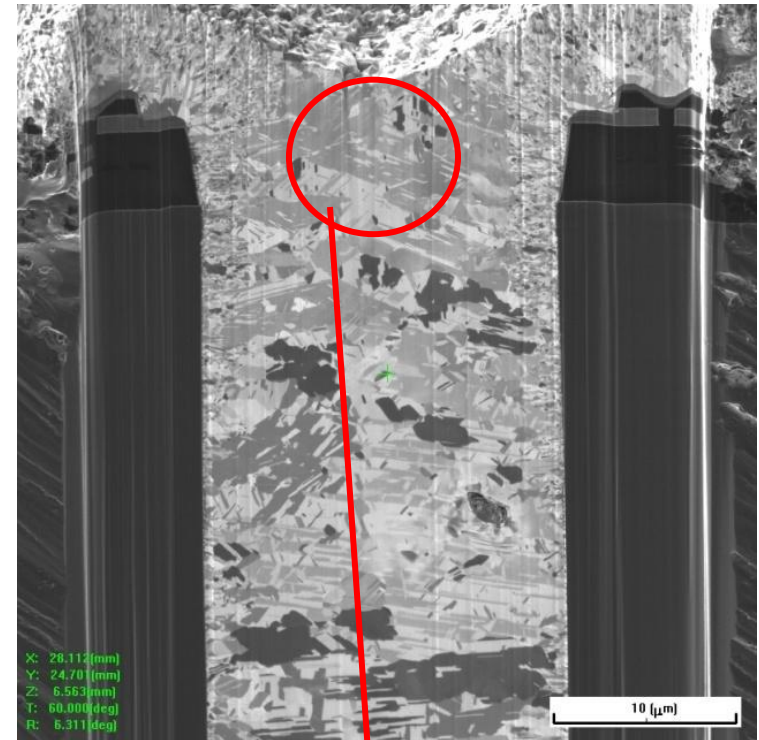
Microstructure change of Cu during annealing leads to tensile stress – SK Hynix

As received

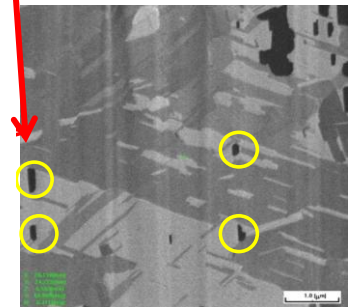


Grain growth

200°C 1hr annealing



Crack



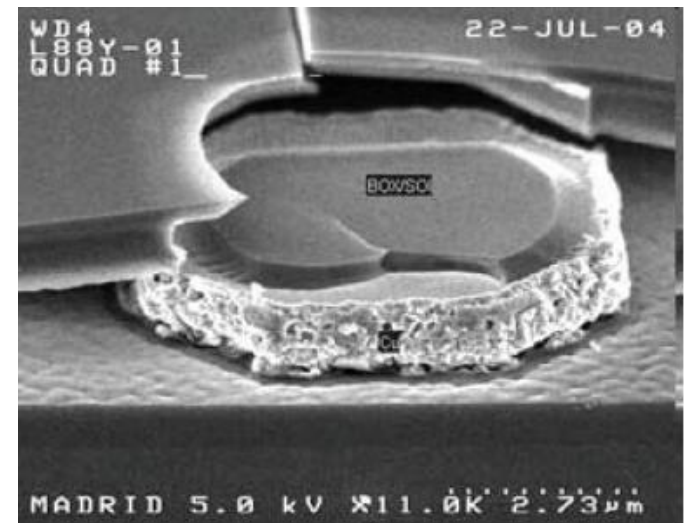
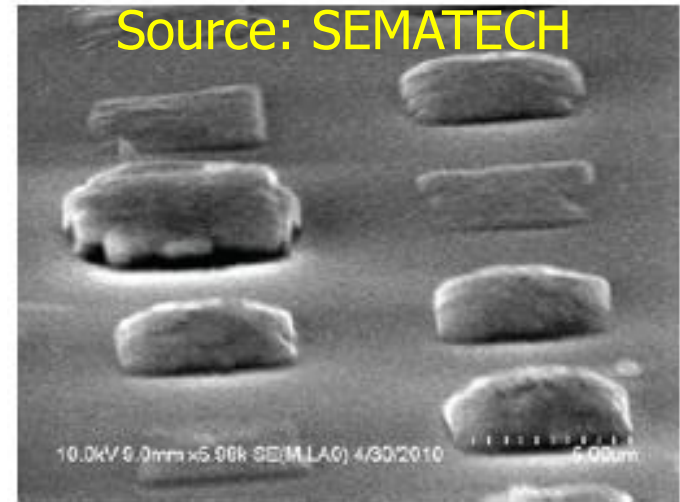
Void

Compressive Hydrostatic Stress in Cu TSV during Annealing

Cu TSV Protrusions:

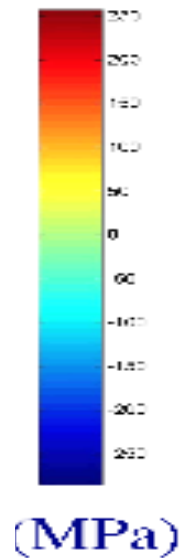
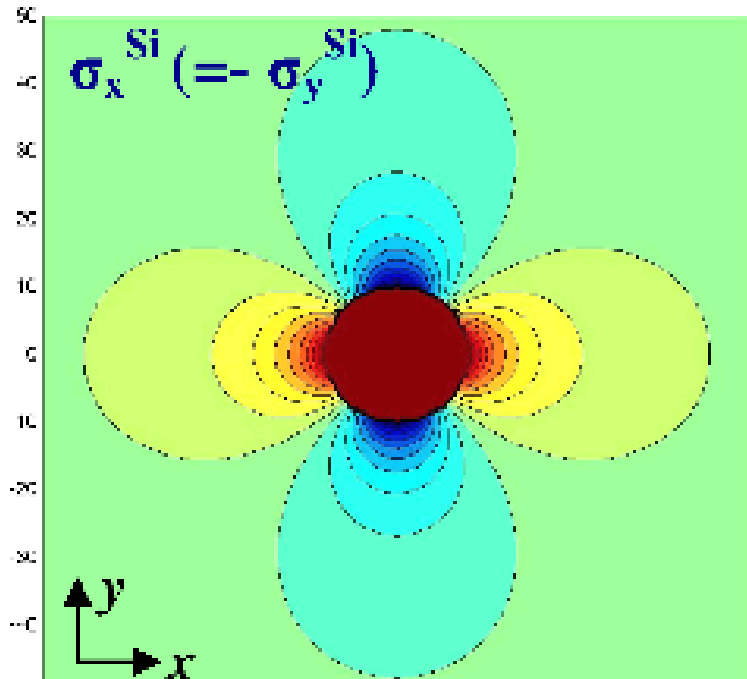
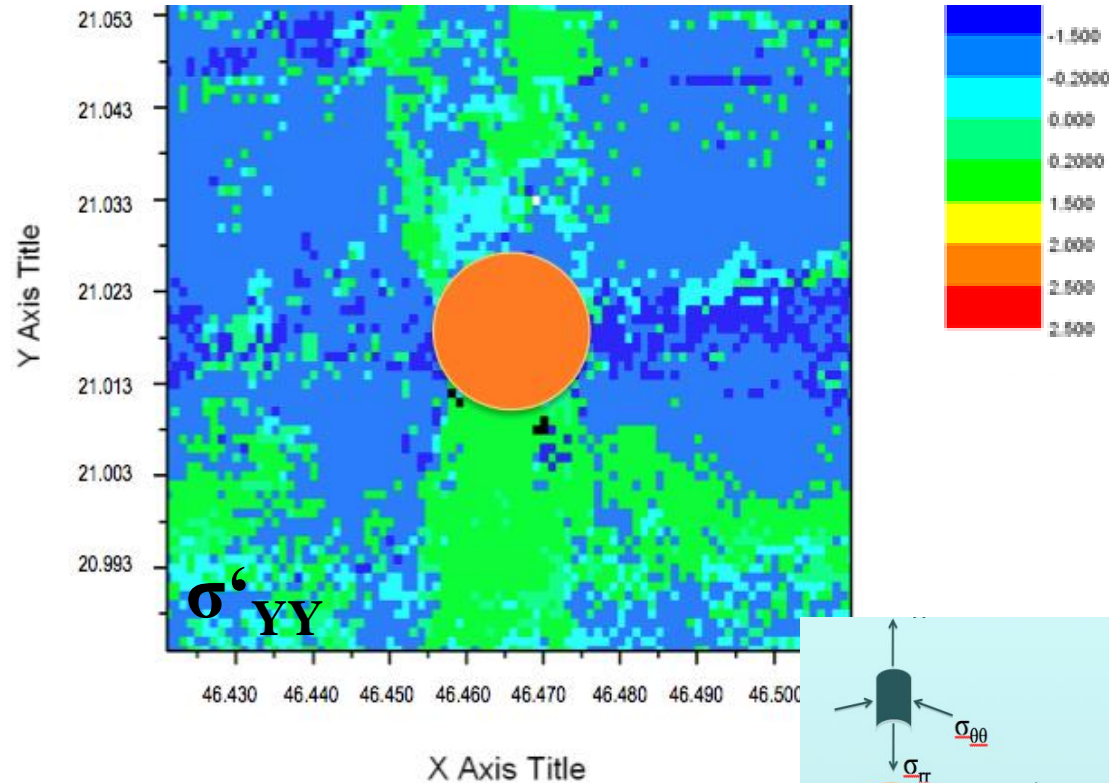
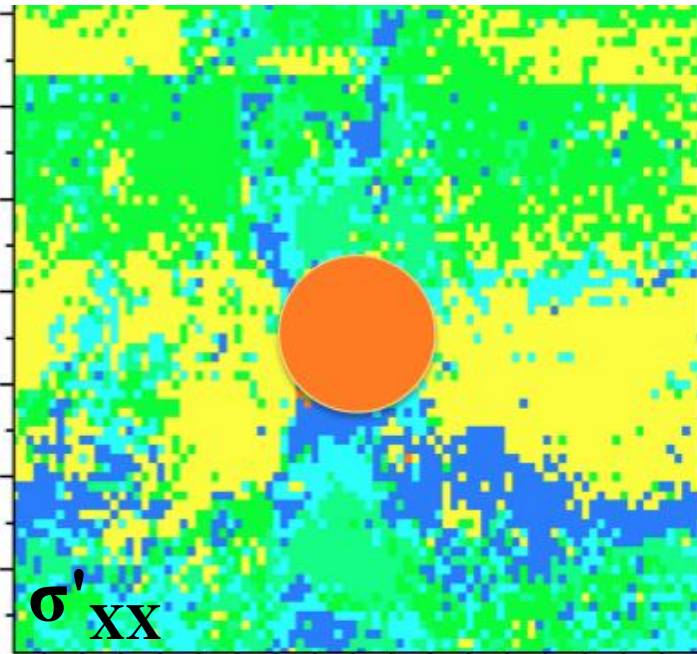
- Popping out, bulging out during high-temp processing steps
- Cracking/flaking of dielectrics over Cu TSV and open vias to above metallization lines

→ Integration issues as well as serious reliability concerns!



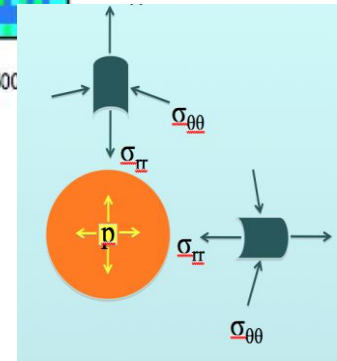
Copper expansion can fracture the oxide layer above. (Source: Tezzaron)

Si Stress State in TSV – *SK Hynix* (Post Annealed)



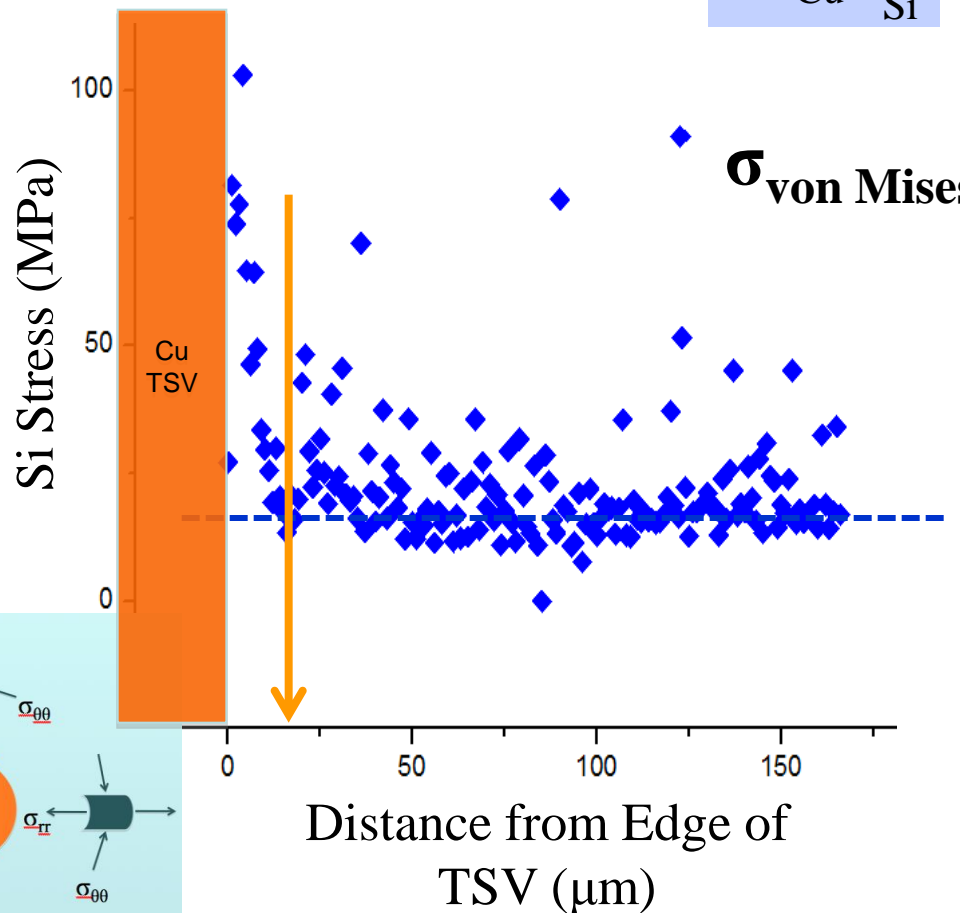
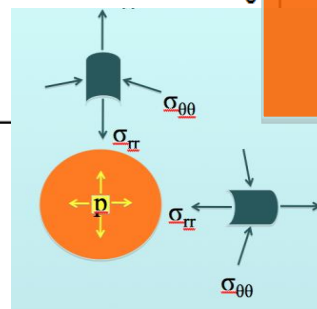
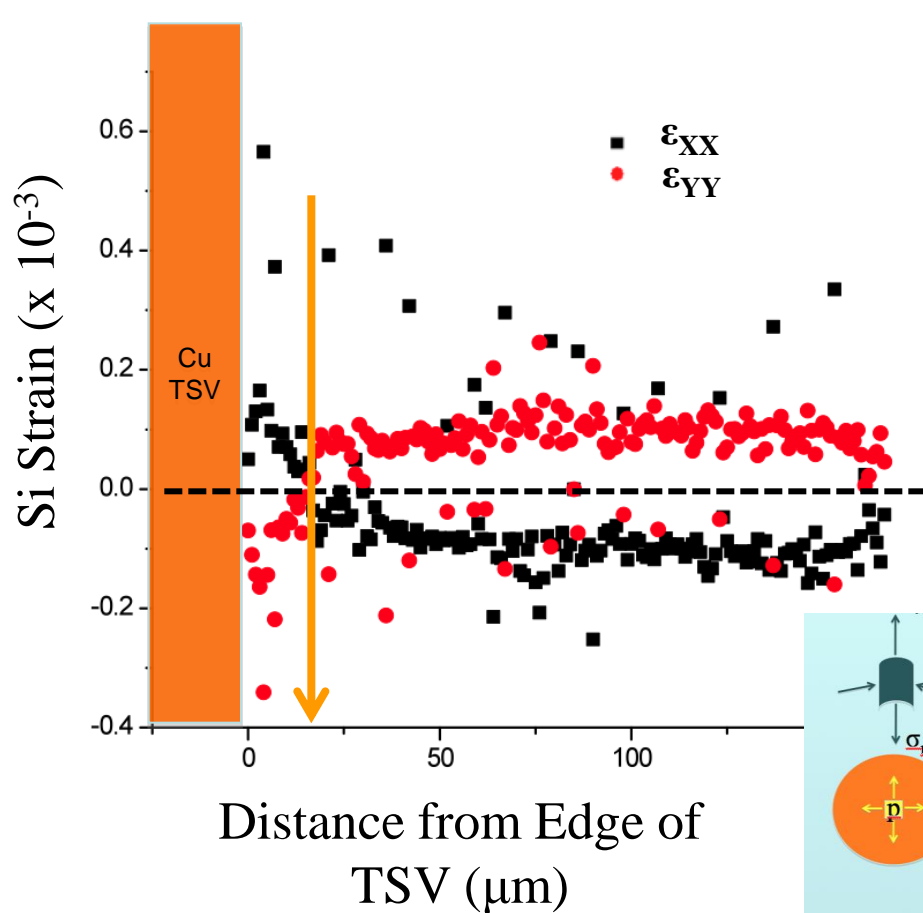
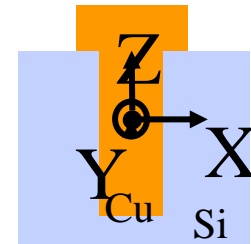
$$\sigma_{xx} = -\sigma_{yy} = -\frac{R^2 B \Delta \alpha \Delta T (x^2 - y^2)}{2(x^2 + y^2)^2}$$

Lu et al., AIP, 2009;
TSV diam. = 20 μm
Stress Map = 100 μm x 100 μm



Si Strain Profile from Edge of TSV

- SK Hynix (Post Annealed)



Si Keep-Away Zone:

SK Hynix: 17 μm

→ Reduce as-received Cu TSV high tensile stress!!

❖ As-received



233.8 MPa

❖ at 200°C

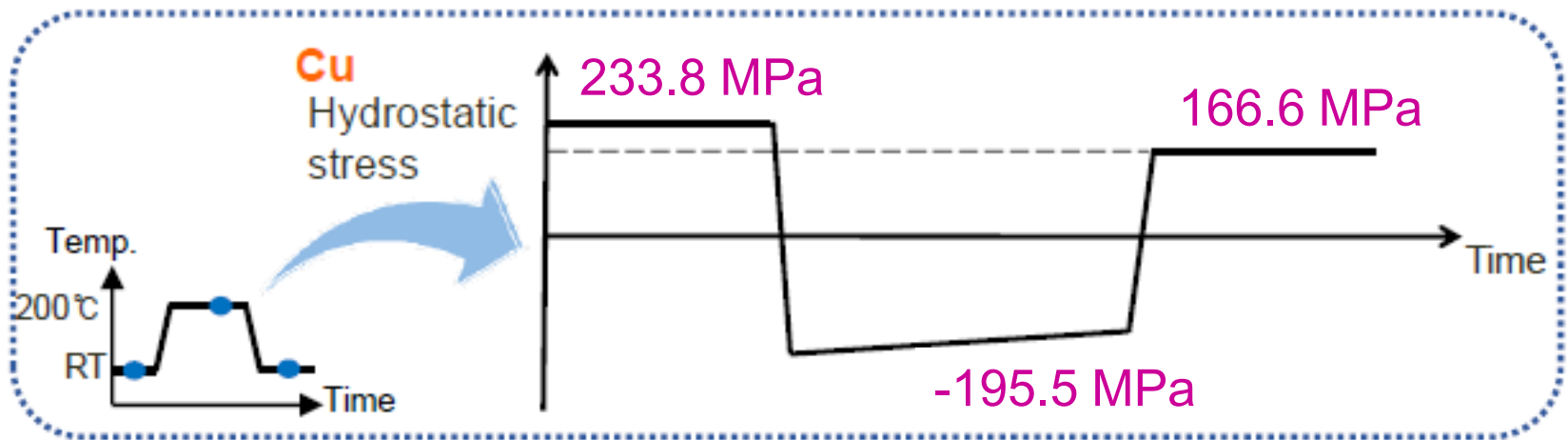


-195.5 MPa

❖ After annealing



166.6 MPa



Electroplating process? Thermal treatment?
Reduce Cu RT grain growth?

Summary

- Synchrotron X-ray submicron diffraction (white + monochromatic beam) has proven to be a powerful tool to measure stress states in TSV in situ and while the Cu via is still buried under Silicon
- Cu stress state is mostly in tensile and considerable shear stresses at the post-annealed state:
 - Comparison SK Hynix vs. SEMATECH samples → RT grain growth leads to high tensile stress in the as-received state
 - How to reduce stress-induced reliability/integration → reduce Cu hydro stress in the as-received state
- Stress in Si surrounding Cu TSV was found to follow Cu hydrostatic stress: higher Cu hydrostatic stress → higher Si stress → larger “keep-away zone”
 - Si stress in array of TSV’s → important for design/layout
 - Stress scanning from the top would be valuable → to optimize layout!

Acknowledgements

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