Mechanical Stresses and Reliability Study of Cu Through-Silicon Via (TSV) Samples Fabricated by SK Hynix vs. SEMATECH using Synchrotron X-Ray Microdiffraction for 3-D Integration and Reliability

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Outline

• Background – Mechanical Stresses and Reliability/Performance Implications in 3-D Cu TSV Integration Schemes

• The Technique – Synchrotron X-Ray Submicron Diffraction (White and Monochromatic Beam)

• Experimental –
  – Mechanical Stresses in Cu TSV and Their Potential Impacts on 3-D Interconnect Reliability: SK Hynix vs. SEMATECH
  – Mechanical Stresses in Silicon Surrounding TSV and Their Potential Impacts on 3-D Interconnect Performance as well as Reliability: SK Hynix vs. SEMATECH

• Conclusions & Future Work
Impact to Reliability and Performance of Device

- **Si stress**
  - Keep-away zone
  - Device must be kept away from the zone in which mobility is changed.
  - Si cracking

- **Cu stress**
  - Debonding, TSV cracking
  - TSV Pop-up, Bulging-up → Integration Issues

- Thermal stress of TSV → Si stress and Cu stress.
- Si stress (residual stress) → degradation of device performance.
- Cu stress (thermal stress) → mechanical failure of Cu TSV.

*Source: SEMATECH*
Stress of Si: μ-Raman spectroscopy

Okoro, et al., IRPS, 2010

- TSV-induced stress extends about 10 µm in Si
- 50 MPa tensile stress in Si after cycling

Lee, et al., TSV 3D Packaging Technology Workshop, 2010

- 40 MPa tensile stress in Si was developed near Cu TSV after cycling.

Diameter 5 µm, pitch 10 µm, depth 24 µm
Stress of Cu: Laboratory XRD

Lack of micron resolution

- + 225 MPa at 200 °C.
- -100 MPa at 25 °C.

Diameter 70 µm, pitch 140 µm, depth 460 µm
**Synchrotron X-Ray Sub-micron Diffraction**

X-ray source: ALS Synchrotron, Berkeley Lab (Beamline 12.3.2)

Beam size: 0.5x0.5 μm

Deviatoric strain tensor: Small shifts in spot relative positions \(\rightarrow\) Crystal deformation at constant volume \(\approx 1 \times 10^{-4}\) accuracy
Laue pattern and energy scanning analysis

Total strain = dilatational + deviatoric

\[ \varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon'_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon'_{33} \end{pmatrix} \]
Experimental

- Sample
  - **Hynix**: 20 µm TSV diameter, 90 µm pitch, 90 µm height
  - **SEMATECH**: 5.5 µm TSV diameter, 80 µm pitch, 50 µm height

- Condition of measurement
  - Measurement of stress for: Si, Cu TSV
  - Thermal treatment:
    - *in situ* at 200 °C (**SK Hynix**)
    - *ex situ* post-annealed (200 °C for 1 hour) sample (**SK Hynix**)
    - *ex situ* post-annealed (350 °C for 30 mins) - **SEMATECH**
Cu Stress State in TSV – *SK Hynix* - Post Annealed Sample (measure at RT)

Only deviatoric components of stress

\[ \varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon'_{12} & \varepsilon'_{13} \\ \varepsilon'_{21} & \varepsilon'_{22} & \varepsilon'_{23} \\ \varepsilon'_{31} & \varepsilon'_{32} & \varepsilon'_{33} \end{pmatrix} \]
Cu Hydrostatic Stress State in TSV – SK Hynix
- Post Annealed Sample (measure at RT)

Hydrostatic stress = +166.6 MPa

- Hydro + deviatoric

One area

All area scan
Stress Evolution in Cu TSV – SK Hynix

Cu hydrostatic stress

- As-received: 233.8 MPa
- at 200°C: -195.5 MPa
- After annealing: 166.6 MPa
High Tensile in As-Received $\rightarrow$ Cu RT Grain Growth

- Hardness change by annealing

- Elastic modulus

- Decreasing hardness $\rightarrow$ Cu stress toward more tensile stress after annealing and R. T. aging.

Microstructure change of Cu during annealing leads to tensile stress – SK Hynix

As received

200°C 1hr annealing

Grain growth

Crack

Void
**Compressive** Hydrostatic Stress in Cu TSV during Annealing

Cu TSV Protrusions:

- Popping out, bulging out during high-temp processing steps
- Cracking/flaking of dielectrics over Cu TSV and open vias to above metallization lines

→ Integration issues as well as serious reliability concerns!

Source: SEMATECH

Copper expansion can fracture the oxide layer above. (Source: Tezzaron)
Si Stress State in TSV – *SK Hynix* (Post Annealed)

Lu et al., AIP, 2009;
TSV diam. = 20 μm
Stress Map = 100 μm x 100 μm
Si Strain Profile from Edge of TSV
- SK Hynix (Post Annealed)

**Si Keep-Away Zone:**

*SK Hynix:* 17 μm
→ Reduce as-received Cu TSV high tensile stress!!

As-received: 233.8 MPa

at 200°C: -195.5 MPa

After anealing: 166.6 MPa

Electroplating process? Thermal treatment? Reduce Cu RT grain growth?
Summary

- Synchrotron X-ray submicron diffraction (white + monochromatic beam) has proven to be a powerful tool to measure stress states in TSV \textit{in situ} and while the Cu via is still \textit{buried under Silicon}

- \textbf{Cu stress state} is mostly in tensile and considerable shear stresses at the post-annealed state:
  - Comparison SK Hynix vs. SEMATECH samples $\rightarrow$ RT grain growth leads to high tensile stress in the as-received state
  - How to reduce stress-induced reliability/integration $\rightarrow$ reduce Cu hydro stress in the as-received state

- \textbf{Stress in Si surrounding Cu TSV} was found to follow Cu hydrostatic stress: higher Cu hydrostatic stress $\rightarrow$ higher Si stress $\rightarrow$ larger “keep-away zone”
  - Si stress in array of TSV’s $\rightarrow$ important for design/layout
  - Stress scanning from the top would be valuable $\rightarrow$ to optimize layout!
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