FDSOI Metal Gate Transistors for Ultra Low Power Subthreshold Operation

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Outline

• Motivation

• FDSOI for Subthreshold Optimized Transistors

• Metal Gate Electrode Workfunction Tuning

• Transistor Results

• Initial Circuit Results

• Summary
• Motivation

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• Summary
Conventional vs. Low Power Microelectronics

- Unattended ground sensors
- Embedded medical devices
- Space based sensors

Optimized FDSOI ultralow power devices can realize an energy savings of 93% compared to bulk silicon.
Bulk Silicon Subthreshold Transistors

Commercial 65nm Low Power Bulk Silicon

Switching Speed*
\[ t_s = (R_t + R_m)(C_t + C_m) \]
Conventional \( t_s \approx 11 \text{ ps} \)
Subthreshold \( t_s \approx 2,750 \text{ ps} \)

Switching Energy*
\[ E_s = (C_t + C_m)V^2 \]
Conventional \( E_s \approx 2.59 \text{ fJ} \)
Subthreshold \( E_s \approx 0.23 \text{ fJ} \)

*calculated for a 1µm-wide transistor driving 1µm metal line

Subthreshold operation at \( V_{dd} = 0.3 \text{ V} \) provides an 11x decrease in switching energy, but at a 250x decrease in switching speed
• Motivation

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Subthreshold Operation Tradeoffs

**Advantages**
- Most efficient way to reduce power
- Highest $g_m$ for given drain current
- Not mobility limited
- Equal NMOS and PMOS $I_{on}/\mu$m

**Disadvantages**
- Slow switching speed
- $I_{on}$ very sensitive to $V_t$
- Device matching more difficult
- Need higher voltage I/O transistor

*Subthreshold-operation is a viable option for energy-starved applications*
- Unattended ground sensors
- Embedded medical devices
- Space based sensors
FDSOI Advantage for Low Power

Silicon-On-Insulator Provides:
- Up to 90% lower junction capacitance
- Near ideal subthreshold swing
- Reduced device cross-talk
- Lower junction leakage
- Increased radiation hardness
- Reduced short channel effects

Fully depleted SOI allows higher performance at lower switching energy for subthreshold operation
0.3 V Operation

Can we take a typical low power device and just turn down the operating voltage to 0.3 V?

*Not with optimal performance. For conventional (SOI) transistors:*

1. Subthreshold swing will be higher than necessary

2. $V_t$ variation will be high due to:
   - SOI thickness variation
   - Random dopant fluctuations

3. Capacitance will be higher than necessary

4. NMOS on PMOS $I_{on}$ will be wildly mismatched
The improved ULP transistor will have four key components:
1. FDSOI, 2. Undoped Channel, 3. Mid-Gap Gate, 4. Underlap S/D
SOI for Ultralow Power (ULP)

Compared to Bulk Silicon

FDSOI exhibits 2.5x improvement in $I_{on}/I_{off}$ ratio at 0.3 V
SOI for Ultralow Power (ULP)

Compared to Bulk Silicon

**Advantages**
- 90% lower junction capacitance
- Near-ideal subthreshold swing
- Full dielectric isolation of transistor
- No substrate reverse bias effects
- Reduced short channel effects
- Reduced source-to-drain leakage

**Disadvantages**
- Higher cost
- Silicon thickness control
- Floating body effects
  
  Can be minimized through transistor engineering
Partially vs. Fully Depleted SOI

Depletion depth: \[ T_{\text{dep}} = \sqrt{\frac{4\varepsilon\Phi_f}{qN_{ch}}} \]

\[ \rightarrow \text{For highly doped channel (10}^{18} / \text{cm}^3), T_{\text{dep}} = 32 \text{ nm} \]
\[ \rightarrow \text{For lightly doped channel (10}^{15} / \text{cm}^3), T_{\text{dep}} = 1,012 \text{ nm} \]

Compared to PDSOI, FDSOI:
1. Is more difficult to fabricate due to thin silicon
2. Has higher series resistance
3. Is more susceptible to charge in the buried oxide
4. Has higher \( g_m \)
5. Has reduced floating body effects
6. More-ideal subthreshold swing

- For high performance devices, the tradeoffs may favor PDSOI
- For ULP devices, the tradeoffs favor FDSOI
Substrate Biasing

Threshold voltage of N and P transistors initially mismatched

Experimental data

SOI transistor design enables use of substrate biasing to match NMOS and PMOS transistors in subthreshold operation

Well matched with +3V on substrate
Ring Oscillator Substrate Biasing

Experimental data

Minimum stage delay occurs when N and P $I_{on}$ are matched

97 stage ring oscillator
$L_g = 150 \text{ nm}$
$V_{dd} = 0.3 \text{ V}$
## FDSOI, PDSOI, and Bulk Comparison

<table>
<thead>
<tr>
<th>Transistor Type</th>
<th>Bulk</th>
<th>PDSOI</th>
<th>FDSOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Approximate Substrate Cost (300mm)</td>
<td>$180</td>
<td>$500</td>
<td>$500</td>
</tr>
<tr>
<td>Active Silicon Thickness (nm)</td>
<td>&gt;1000</td>
<td>~100</td>
<td>&lt;40</td>
</tr>
<tr>
<td>Subthreshold Swing (mV/dec)</td>
<td>&gt;120</td>
<td>80-120</td>
<td>65-80</td>
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<tr>
<td>Junction Capacitance</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Diode Leakage</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
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<tr>
<td>$V_t$ Sensitivity to Si Thickness</td>
<td>None</td>
<td>Medium</td>
<td>High</td>
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<tr>
<td>Extreme Environment Performance, (&lt;4K or &gt;300°C)</td>
<td>Poor</td>
<td>Good</td>
<td>Good</td>
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<tr>
<td>Series Resistance</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
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<td>$V_t$ Sensitivity to BOX Charge</td>
<td>None</td>
<td>Low</td>
<td>High</td>
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<tr>
<td>Transconductance</td>
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<td>Medium</td>
<td>High</td>
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<tr>
<td>Kink Effect</td>
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<td>High</td>
<td>Medium</td>
</tr>
</tbody>
</table>

*Not important for subthreshold ULP*
Subthreshold optimized FDSOI

1. Wide spacer & no extensions
2. Undoped channel
   ⇒ Reduced capacitance
   ⇒ Improved $V_t$ control
   ⇒ No extension has small impact to $I_{on}$ due to low $V_{ds}$ and low barrier
   ⇒ Requires mid-gap gate electrode

Simulation data

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Switching Time (ps)</th>
<th>Switching Energy (fJ)</th>
</tr>
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<tr>
<td>1.2V Bulk Si</td>
<td>11</td>
<td>2.59</td>
</tr>
<tr>
<td>0.3V Bulk Si</td>
<td>2750</td>
<td>0.23</td>
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<tr>
<td>0.3V sub$V_t$ FDSOI</td>
<td>176</td>
<td>0.07</td>
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</table>

Subthreshold-optimized FDSOI can provide a 50x reduction in energy-delay product compared to Bulk Si
• Motivation

• FDSOI for Subthreshold Optimized Transistors

• **Metal Gate Electrode Workfunction Tuning**

• Transistor Results

• Initial Circuit Results

• Summary
Channel Doping

\[ V_t = \Phi_{ms} + 2\Phi_f - \frac{1}{C_{ox}} \left( Q_{it} + q\int_0^t \rho(x)dx - qN_{ch}t_{soi} \right) \]

- Metal to silicon workfunction difference
- Fermi potential
- Gate dielectric charge
- Channel doping

[Excludes short channel effects]

Low channel doping reduces \( V_t \) variation, critical for subthreshold operation.

Threshold voltage no longer varies with SOI film thickness for very low channel doping.
After evaluation of several options (e.g., TaN, NiSi), TiN was selected as metal gate material for ultra-low power transistors.
Effect of TiN Deposition Conditions

N$_2$/Ar flow ratio during reactive sputter deposition of TiN allows adjustment of workfunction between 4.30 and 4.55 eV

Workfunction target ~ 4.65 eV
Sub-atmospheric $N_2$ anneal increases workfunction and should improve reliability of TiN metal gate transistors.

Quantum-corrected model fit from NCSU

Increasing Workfunction

Lower $D_{it}$

Effect of TiN Post-Deposition Anneal

Capacitance (pF) vs. Voltage (V)

- No anneal
- $N_2$ anneal
Effect of TiN Thickness

Reducing TiN thickness: 1) increases workfunction, 2) should reduce $V_t$ variation

→ May be due to reduced gate dielectric damage or lower stress

7nm TiN
$\sigma = 0.012 \text{ eV}$

20nm TiN
$\sigma = 0.023 \text{ eV}$
Workfunction Tuning

Workfunction can be adjusted by varying N₂ gas flow and substrate temperature during reactive PVD.

<table>
<thead>
<tr>
<th>Deposition Temp.</th>
<th>Ar flow</th>
<th>N₂ flow</th>
<th>Anneal</th>
<th>Œm (eV)</th>
<th>3 sigma</th>
<th>EOT (nm)</th>
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<td>110</td>
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<td>4.30</td>
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<tr>
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<td>0.07</td>
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<tr>
<td>Polysilicon</td>
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<td></td>
<td></td>
<td>4.65</td>
<td></td>
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</tbody>
</table>

C-V curves fit using quantum corrected model from NCSU¹

Workfunction (Φₘ) tunable from 4.20 to 4.65eV (more on HfO₂)

Target = 4.65eV

EOT reduced by 4-5Å with TiN gate (no poly depletion)

¹ N. Yang et al., IEEE Trans Elect. Dev. 46 (7) p. 1464, 1999
FDSOI ULP Gate Stack

- 400nm PR
- 100nm ARC
- 200nm Poly Si
- 20nm TiN
- 40nm Si
- 400nm Buried Oxide
- Bulk Si

CD = 150nm

4 nm SiO$_2$ or HfO$_2$

ULP SRAM Bit Cell

Active Si

PR/ARC

TiN

Poly

BOX
FDSOI ULP Gate Stack

Little TiO$_2$ mixing observed

Polysilicon (200nm)
- Furnace, SiH$_4$, 800$^\circ$C

TiN (20nm)
- Reactive PVD, Ar/N$_2$
- 626$^\circ$C N$_2$ anneal for workfunction tuning
- Columnar grain structure

SiO$_2$ Gate dielectric (4nm)
- Dry furnace oxidation

Active Silicon (40nm)
- Thinned SOITEC Unibond
- Light p-type doping
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Subthreshold Optimized Transistors

Experimental TiN Metal Gate Transistors

Subthreshold operation performance metrics:

1. Tight $V_t$ distribution
2. N/P $I_{on}$ ratio near 1:1
3. Low subthreshold swing
4. Low $I_{off}$
5. Correct workfunction tuning
6. Low capacitance

$L=180\text{nm}, W=8\mu\text{m}$

$I_{ds} (\text{A/\mu m})$

$V_{dd} = 0.05 \text{ V}$
$V_{dd} = 0.3 \text{ V}$

$I_{off} = 4 \text{ pA/\mu m}$

TiN Gate
SOI
Subthreshold Swing

- $S$ is near-ideal at long gate lengths
- $S$ increases as $L_g$ decreases due to short channel effects
- Should improve by using thinner SOI
NMOS and PMOS On-Current

Equal $I_{\text{on}}$ allows equal NMOS and PMOS transistor sizing and equal N and P device capacitance

100x change in P/N ratio results from only 70 mV change in $V_t$

$V_t$ control is critical
Threshold Voltage Control

- Reduces $V_t$ sensitivity to silicon thickness
- No Random Dopant Fluctuations
- Reduces channel length sensitivity to S/D anneal variations

$V_t$ variation improves from 18 mV to 8 mV (3$\sigma$)

With channel and extension implants

No channel or extension implants

$V_{dd} = 0.3$ V
$L_g = 180$ nm

**Ids (A/µm)**

$-2.0$ $-1.5$ $-1.0$ $-0.5$ $0.0$

$10^{-12}$ $10^{-10}$ $10^{-8}$ $10^{-6}$ $10^{-4}$
Reduced Capacitance

• S/D underlap and wider spacers reduce capacitance by 70%
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• **Initial Circuit Results**

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Circuit Verification Run

- 3 Level metal
- 150 nm design rules

Novel ultra low power circuits from MIT-LL and 3 university partners

Wafer Map of Functional Multiplier Circuits
~ 2,000 transistors

71% yield on best wafer
97 Stage Ring Oscillator (Lg=150nm)

- 29x decrease in Energy-Delay product over commercial bulk silicon
- Measured switching energy = 0.099 fJ/op.
  → Simulation predicted 0.070 fJ/op.
- Stage delay is significantly higher than simulation

TSMC 180nm CMOS
501 stage ring oscillator
Deen et al, JVSTA 2006

Functional down to 100mV

0.099fJ at 0.3V
Energy Harvesting Ring Oscillator

Diode-connected Ring Oscillator powered by microscope light

- Potential for Ultra Low Power circuits requiring no battery
Ultra Low Power Multiproject Run

- Currently in fabrication at MIT-LL Microelectronics Lab
- Enthusiastic response from design community
- Over 30 participating institutions
- Die area oversubscribed by 50%
As gate length shrinks, subthreshold swing and DIBL degrade significantly

Future Scaling

To scale $L_g$ to 40nm, ultra-thin SOI is required.

Below 40nm, non-planar SOI designs may be necessary for improved channel control.


Silicon

Fin

Gate

Bottom Gate

Source

Drain

Silicon

Gate

Silicon Fin

BOX

Roy, Int. Conf. VLSI Des., 2006

SOI Thickness
- 15nm
- 10nm
- 7nm
- 5nm

Gate Length (nm)

-DIBL (mV/V)

$S$ (mV)
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Summary

• FDSOI offers significant advantages for ultra low power operation
  - Lower capacitance
  - Improved subthreshold swing
  - Up to 50x reduction in energy-delay product

• Workfunction engineered TiN Metal Gate developed
  - Allows systematic adjustment of $V_t$

• Subthreshold Optimized Transistors fabricated
  - 70% decrease in $C_{gd}$
  - 55% reduction in across wafer $V_t$ variation
  - NMOS / PMOS $I_{on}$ ratio near 1
  - 65-70 mV/decade subthreshold swing (for $L_g > 200$nm)

• 30+ Participant Multiproject Run in fabrication
  - Prior simple circuit test run demonstrated functional circuits

• Looking for collaborators interested in ultra-low-power process technology
  - Next Multiproject Run (2011) will be at 90nm design rules
  - Enabled by considerable new investment in MIT-LL Microelectronics Lab, including ASML 193nm lithography