FDSOI Metal Gate Transistors for Ultra Low Power Subthreshold Operation

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Outline

- Motivation
- FDSOI for Subthreshold Optimized Transistors
- Metal Gate Electrode Workfunction Tuning
- Transistor Results
- Initial Circuit Results
- Summary

- **Motivation**
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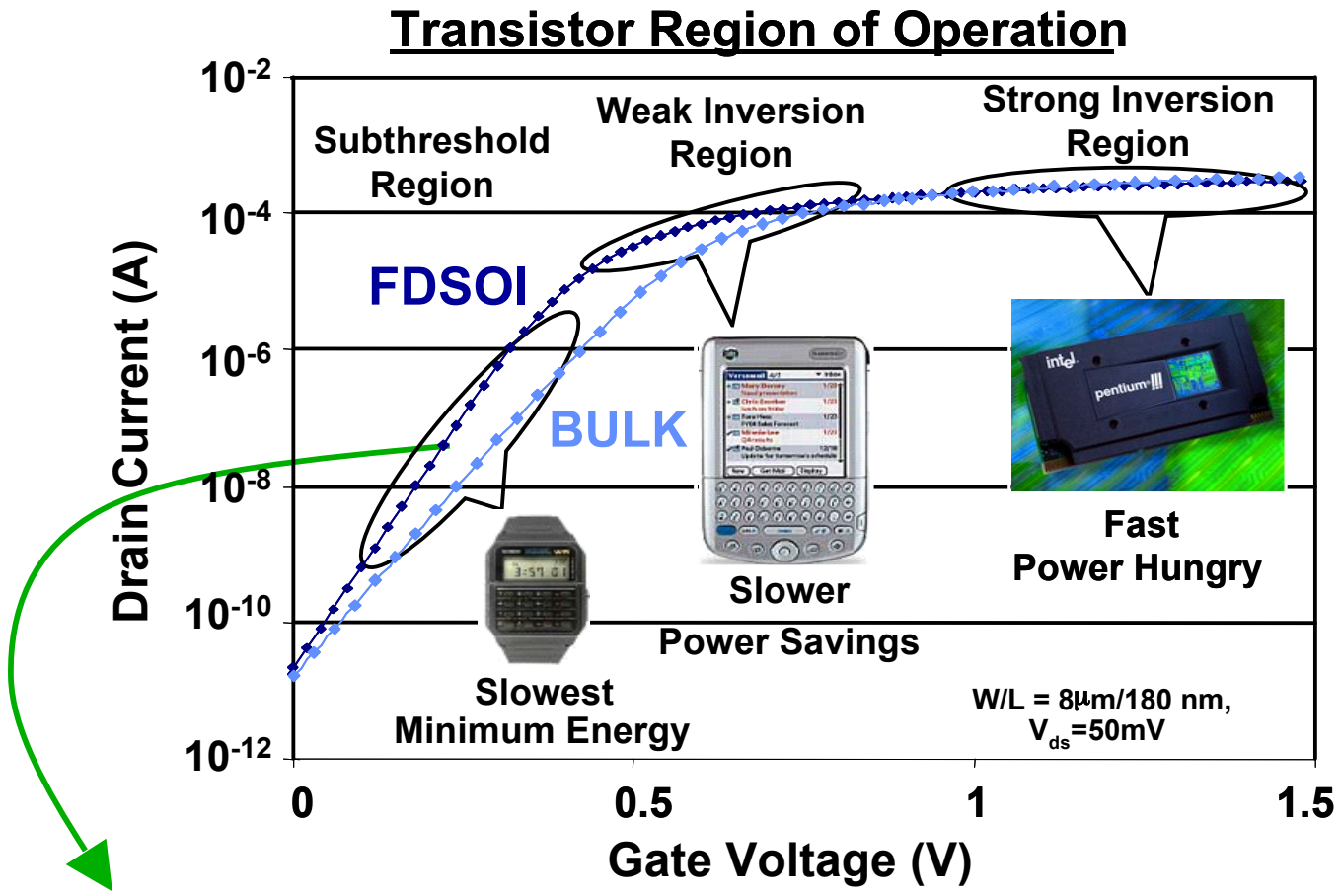
Conventional vs. Low Power Microelectronics

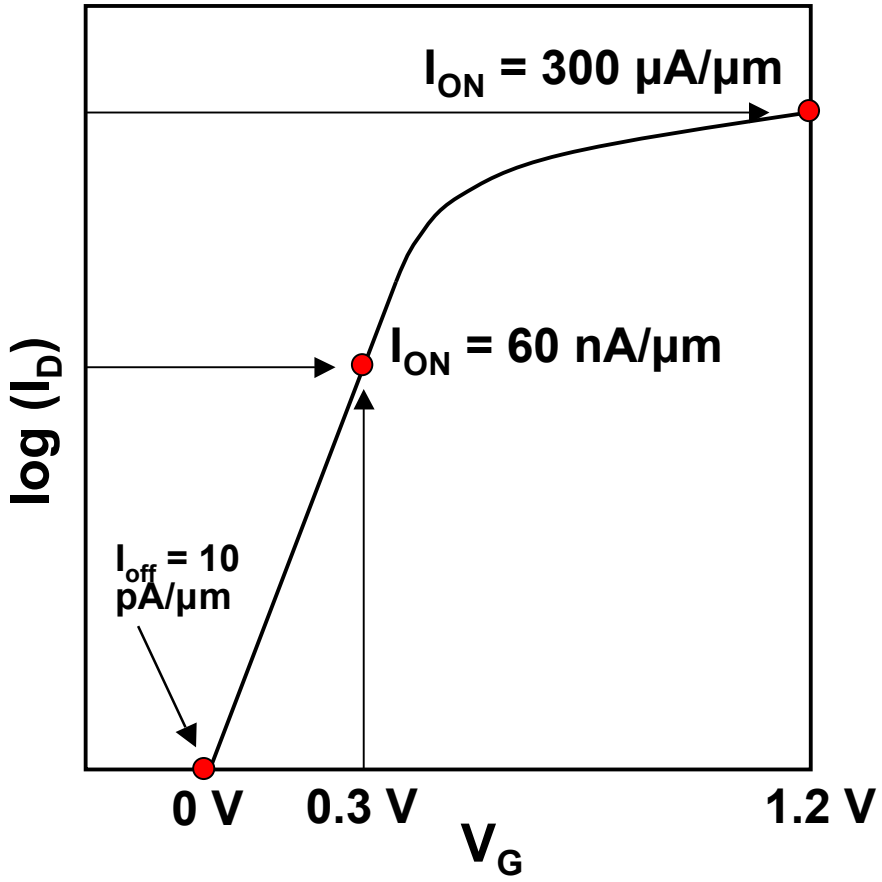


- Unattended ground sensors
- Embedded medical devices
- Space based sensors

Optimized FDSOI ultralow power devices can realize an energy savings of 93% compared to bulk silicon

Bulk Silicon Subthreshold Transistors

Commercial 65nm Low Power Bulk Silicon



Transistor

Metal Interconnect

Switching Speed*

$t_s = (R_t+R_m)(C_t+C_m)$

Conventional $t_s \approx 11$ ps

Subthreshold $t_s \approx 2{,}750$ ps

Switching Energy*

$E_s = (C_t+C_m)V^2$

Conventional $E_s \approx 2.59$ fJ

Subthreshold $E_s \approx 0.23$ fJ

*calculated for a 1µm-wide transistor driving 1µm metal line

Subthreshold operation at V_{dd} = 0.3 V provides an 11x decrease in switching energy, but at a 250x decrease in switching speed

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Subthreshold Operation Tradeoffs

Advantages

Most efficient way to reduce power
Highest g_m for given drain current
Not mobility limited
Equal NMOS and PMOS I_{on}/μm

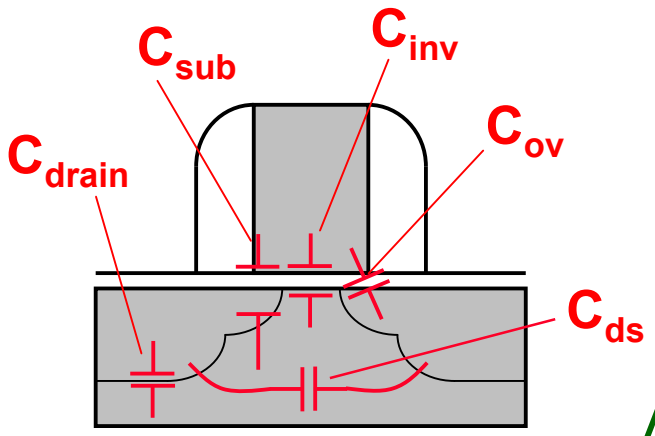
Disadvantages

Slow switching speed
I_{on} very sensitive to V_t
Device matching more difficult
Need higher voltage I/O transistor

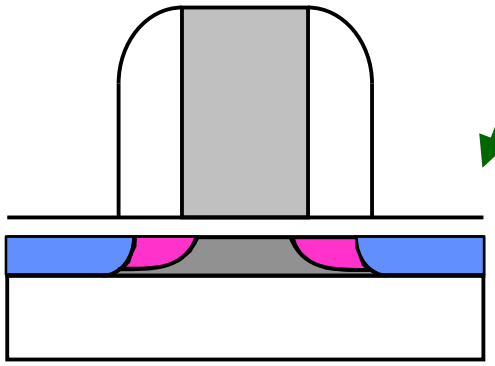
Subthreshold-operation is a viable option for energy-starved applications

- Unattended ground sensors
- Embedded medical devices
- Space based sensors

FDSOI Advantage for Low Power



Bulk Silicon



Standard FDSOI

Silicon-On-Insulator Provides:

- **Up to 90% lower junction capacitance**
- **Near ideal subthreshold swing**
- Reduced device cross-talk
- Lower junction leakage
- Increased radiation hardness
- Reduced short channel effects

Fully depleted SOI allows higher performance at lower switching energy for subthreshold operation

0.3 V Operation

Can we take a typical low power device and just turn down the operating voltage to 0.3 V?

Not with optimal performance. For conventional (SOI) transistors:

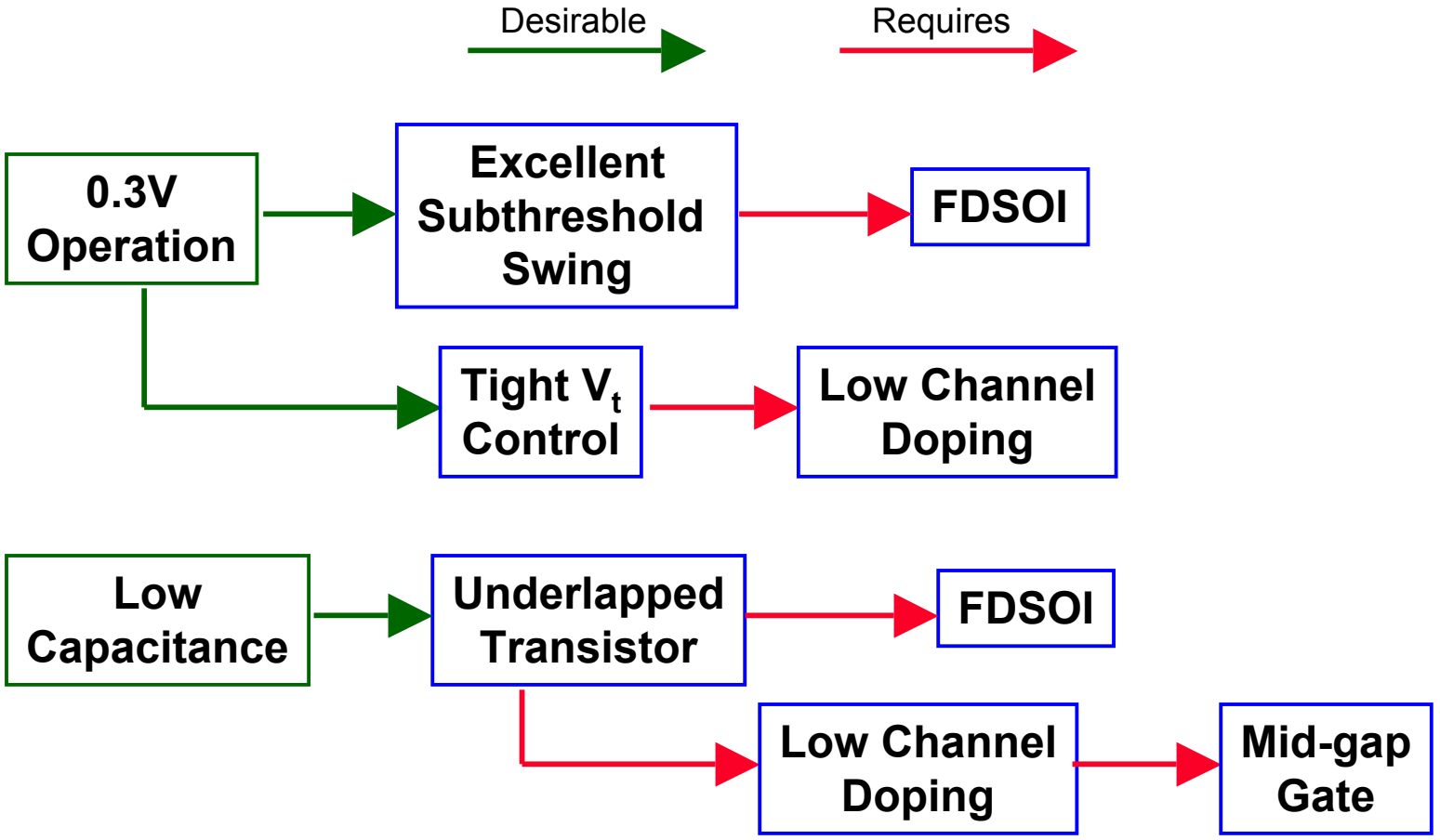
1. **Subthreshold swing will be higher than necessary**

2. **V_t variation will be high due to:**
   - SOI thickness variation
   - Random dopant fluctuations

3. **Capacitance will be higher than necessary**

4. **NMOS on PMOS I_{on} will be wildly mismatched**

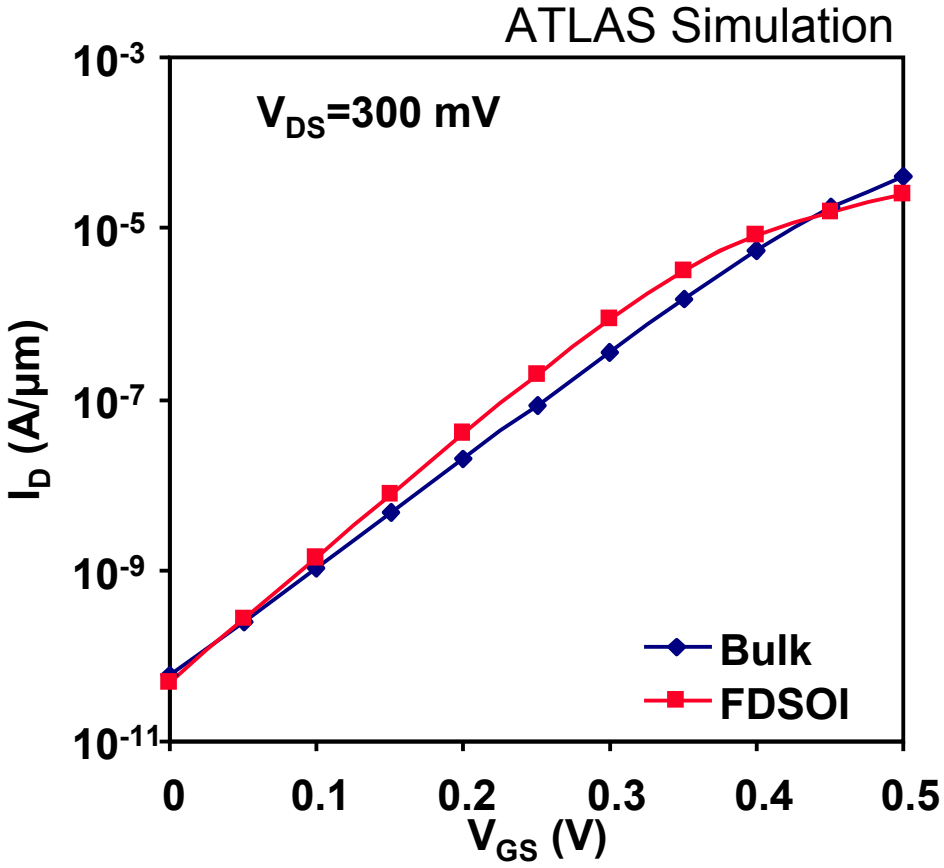
Ultralow Power (ULP) Transistor Engineering



The improved ULP transistor will have four key components:
1. FDSOI, 2. Undoped Channel, 3. Mid-Gap Gate, 4. Underlap S/D

SOI for Ultralow Power (ULP)

Compared to Bulk Silicon



FDSOI exhibits 2.5x improvement in I_{on}/I_{off} ratio at 0.3 V

SOI for Ultralow Power (ULP)

Compared to Bulk Silicon

Advantages

90% lower junction capacitance
Near-ideal subthreshold swing
Full dielectric isolation of transistor
No substrate reverse bias effects
Reduced short channel effects
Reduced source-to-drain leakage

Disadvantages

Higher cost
Silicon thickness control
Floating body effects

Can be minimized through transistor engineering

Partially vs. Fully Depleted SOI

Depletion depth: $$T_{dep} = \sqrt{\frac{4\varepsilon\Phi_f}{qN_{ch}}}$$

→ For highly doped channel (10^{18} / cm^3), T_{dep} = 32 nm
→ For lightly doped channel (10^{15} / cm^3), T_{dep} = 1,012 nm

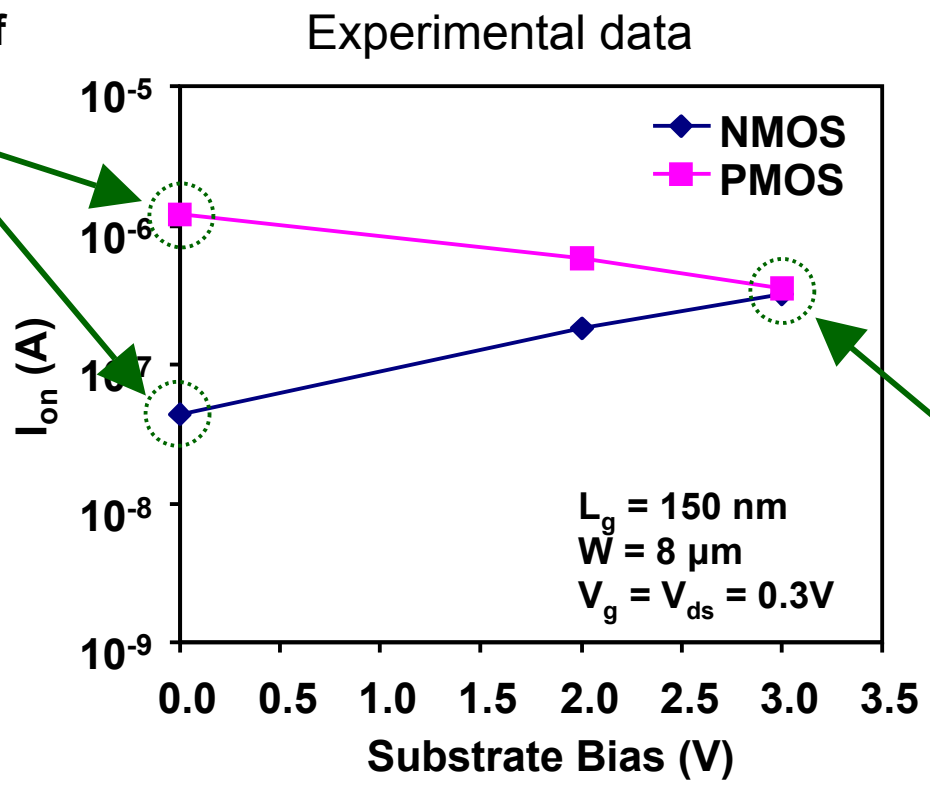
Compared to PDSOI, FDSOI:

1. Is more difficult to fabricate due to thin silicon
2. Has higher series resistance
3. Is more susceptible to charge in the buried oxide
4. Has higher g_m
5. Has reduced floating body effects
6. More-ideal subthreshold swing

- For high performance devices, the tradeoffs may favor PDSOI
- For ULP devices, the tradeoffs favor FDSOI

Substrate Biasing

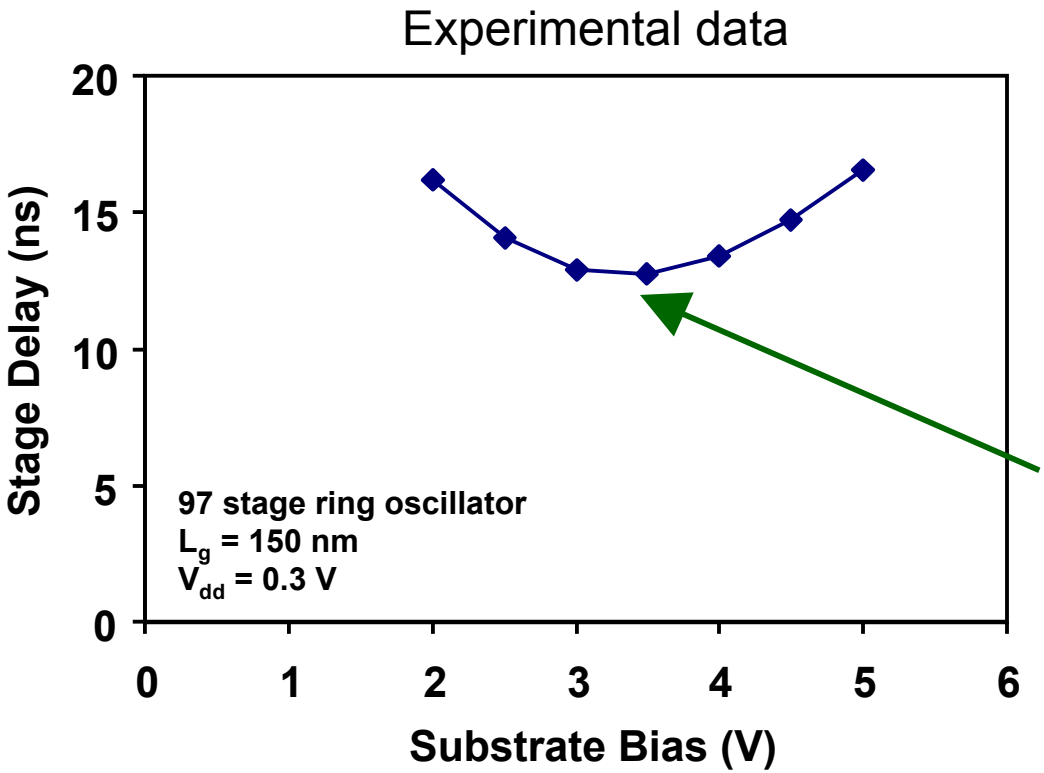
Threshold voltage of N and P transistors initially mismatched



Well matched with +3V on substrate

SOI transistor design enables use of substrate biasing to match NMOS and PMOS transistors in subthreshold operation

Ring Oscillator Substrate Biasing



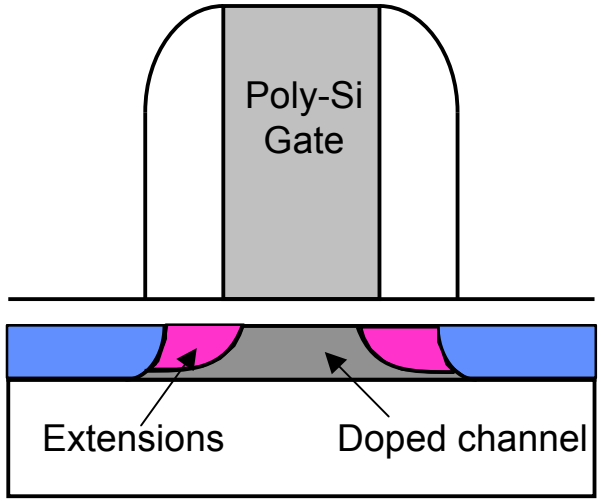
Minimum stage delay occurs when N and P I_{on} are matched

FDSOI, PDSOI, and Bulk Comparison

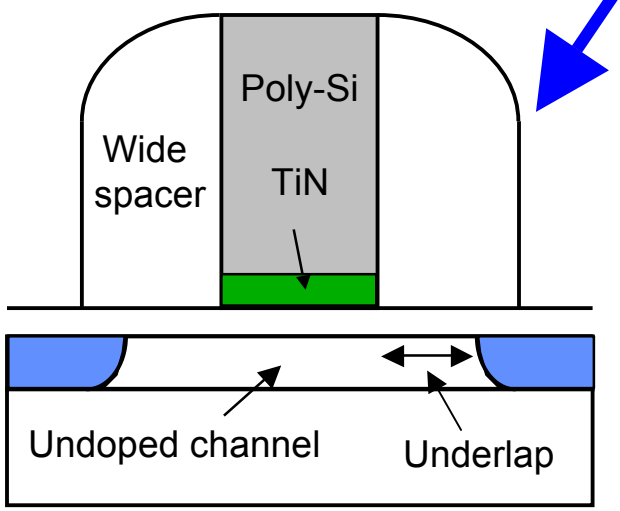
Transistor Type	Bulk	PDSOI	FDSOI
Approximate Substrate Cost (300mm)	$180	$500	$500
Active Silicon Thickness (nm)	>1000	~100	<40
Subthreshold Swing (mV/dec)	>120	80-120	65-80
Junction Capacitance	High	Low	Low
Diode Leakage	High	Low	Low
V_t Sensitivity to Si Thickness	None	Medium	High
Extreme Environment Performance, (<4K or >300°C)	Poor	Good	Good
Series Resistance	Low	Medium	High
V_t Sensitivity to BOX Charge	None	Low	High
Transconductance	High	Medium	High
Kink Effect	None	High	Medium

Not important for subthreshold ULP

Subthreshold optimized FDSOI



Standard FDSOI



Subthreshold FDSOI

1. Wide spacer & no extensions

2. Undoped channel

⇒ Reduced capacitance

⇒ Improved V_t control

⇒ No extension has small impact to I_{on} due to low V_{ds} and low barrier

⇒ Requires mid-gap gate electrode

Simulation data	Switching Time (ps)	Switching Energy (fJ)
1.2V Bulk Si	11	2.59
0.3V Bulk Si	2750	0.23
0.3V subV$_t$ FDSOI	**176**	**0.07**

Subthreshold-optimized FDSOI can provide a 50x reduction in energy-delay product compared to Bulk Si

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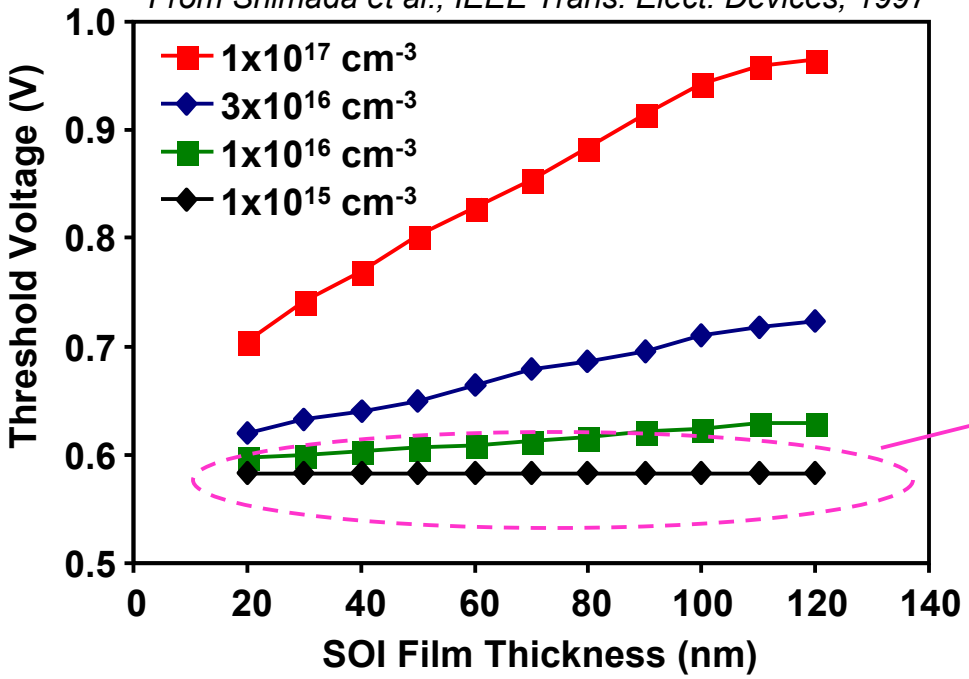
Channel Doping

$$V_t = \Phi_{ms} + 2\Phi_f - \frac{1}{C_{ox}}\left(Q_{it} + q\int_o^t \rho(x)dx - qN_{ch}t_{soi}\right)$$

- Φ_{ms}: Metal to silicon workfuction difference
- $2\Phi_f$: Fermi potential
- $Q_{it} + q\int_o^t \rho(x)dx$: Gate dielectric charge
- $qN_{ch}t_{soi}$: Channel doping

[Excludes short channel effects]

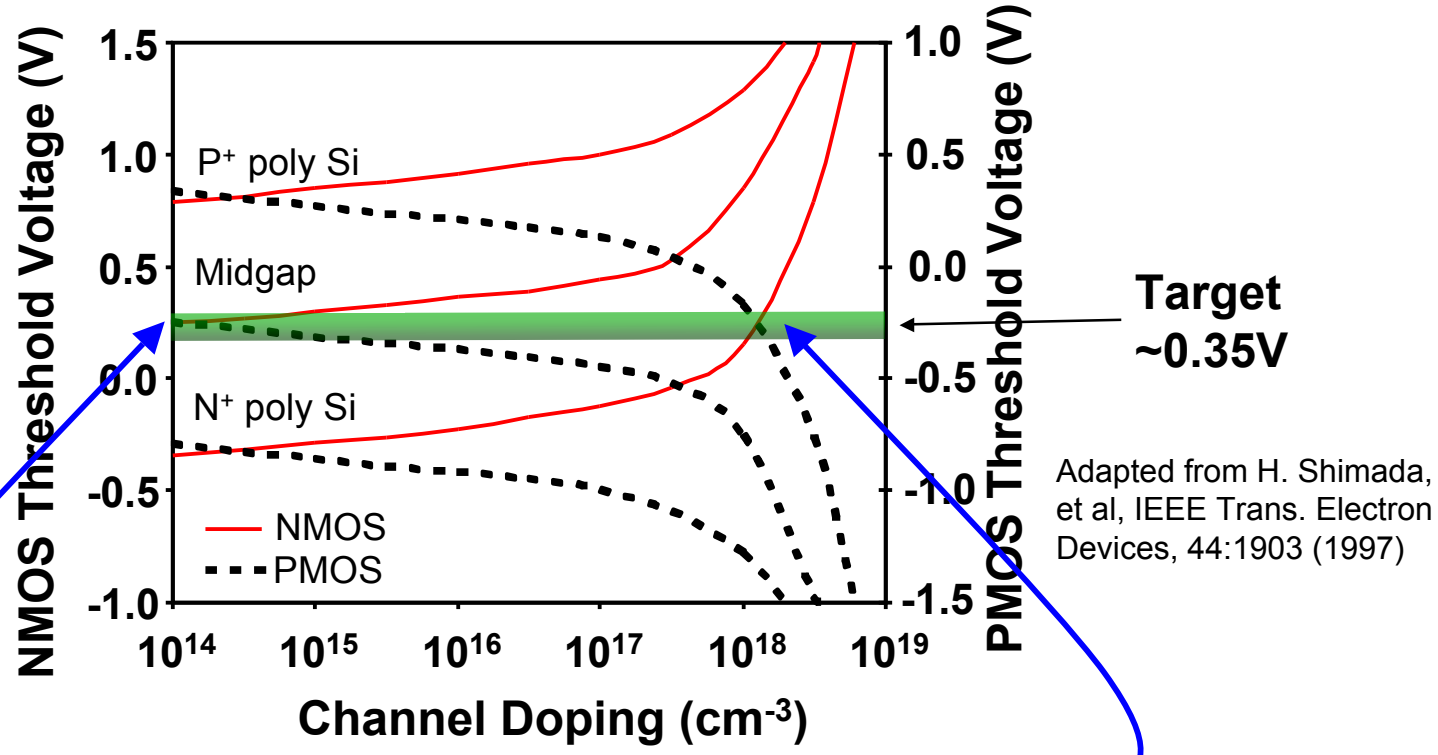
From Shimada et al., IEEE Trans. Elect. Devices, 1997



Low channel doping reduces V_t variation, critical for subthreshold operation

Threshold voltage no longer varies with SOI film thickness for very low channel doping

Threshold Voltage Tuning



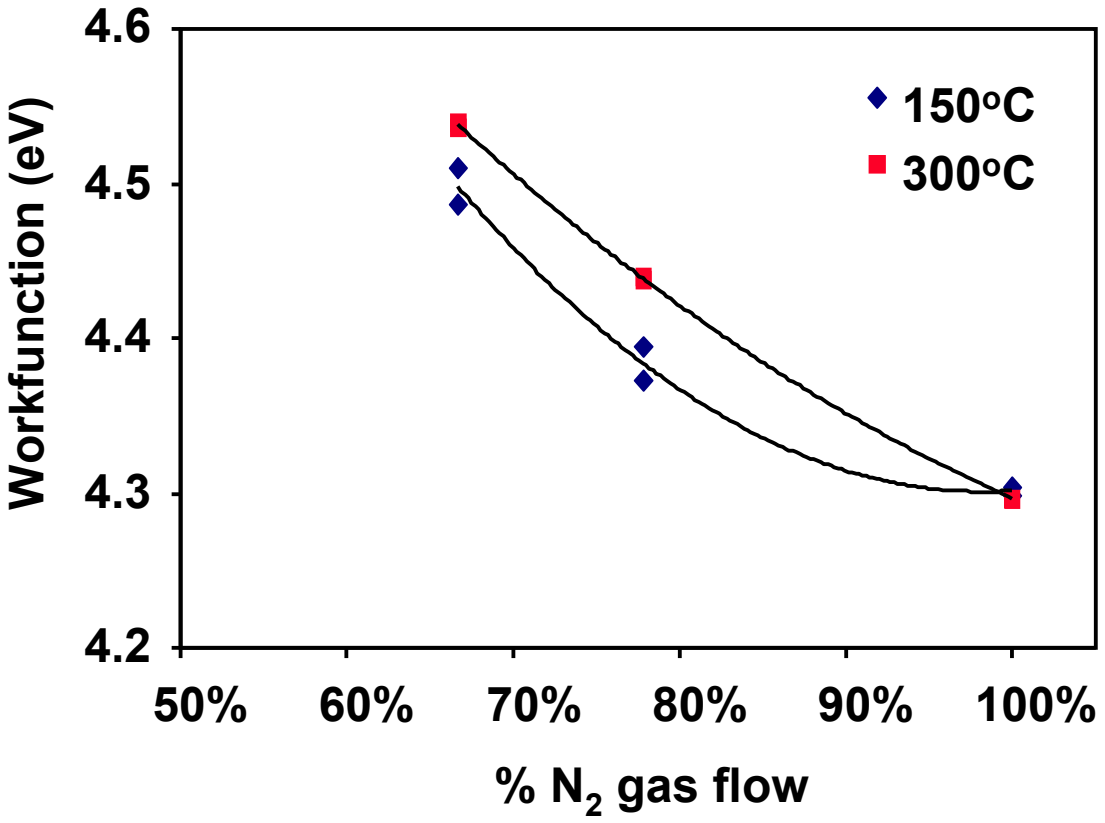
Adapted from H. Shimada, et al, IEEE Trans. Electron Devices, 44:1903 (1997)

- Undoped channel and mid-gap gate electrodes (subthreshold-optimized)
- Highly doped channel and band-edge gate electrodes (high performance)

After evaluation of several options (e.g., TaN, NiSi), TiN was selected as metal gate material for ultra-low power transistors

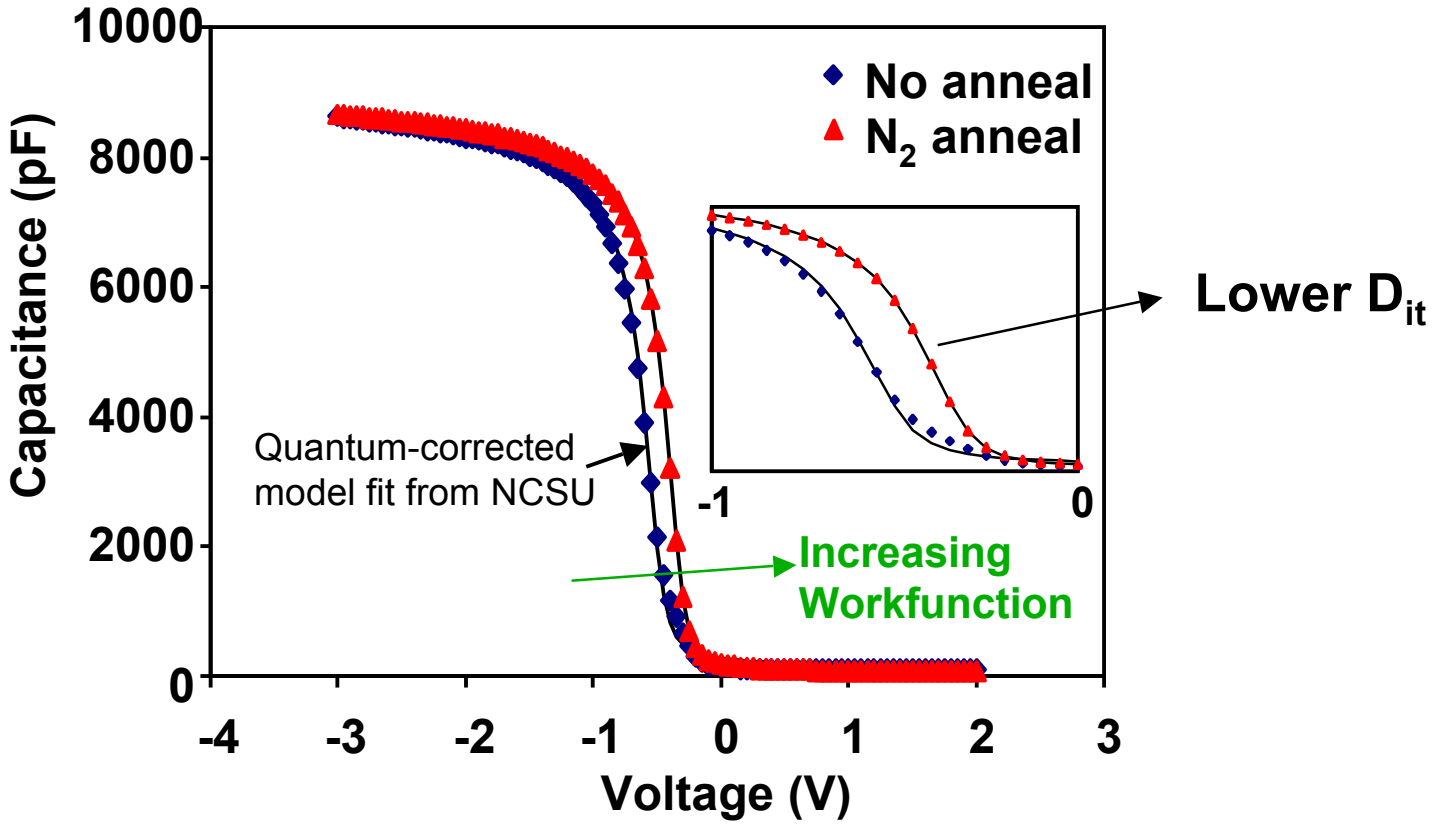
Effect of TiN Deposition Conditions

Workfunction target ~ 4.65 eV



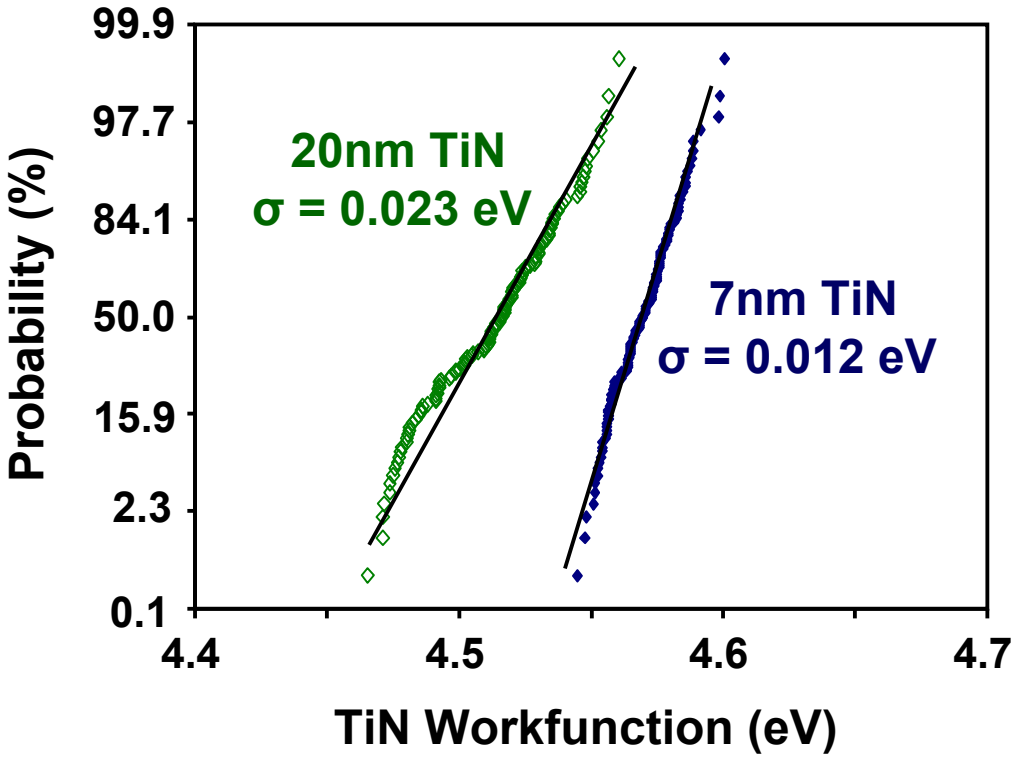
N_2/Ar flow ratio during reactive sputter deposition of TiN allows adjustment of workfunction between 4.30 and 4.55 eV

Effect of TiN Post-Deposition Anneal



Sub-atmospheric N_2 anneal increases workfunction and should improve reliability of TiN metal gate transistors

Effect of TiN Thickness



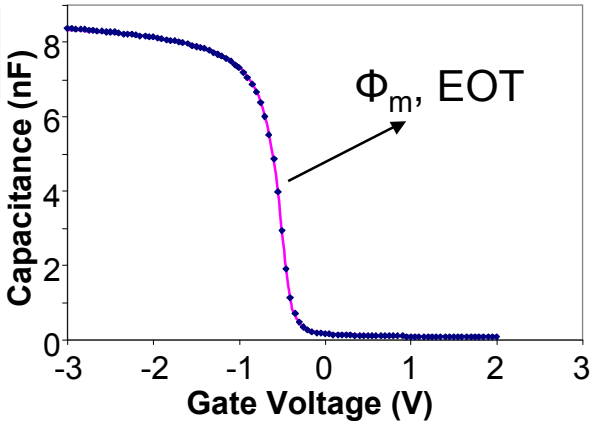
Reducing TiN thickness: 1) increases workfunction,
2) should reduce V_t variation

→ May be due to reduced gate dielectric damage or lower stress

Workfunction Tuning

Workfunction can be adjusted by varying N_2 gas flow and substrate temperature during reactive PVD

Deposition Temp.	Ar flow	N2 flow	Anneal	Öm (eV)	3 sigma	EOT (nm)	3 sigma
150	0	110	No	4.30	0.06	4.27	0.07
150	0	110	No	4.30	0.07	4.22	0.06
150	20	70	No	4.39	0.11	4.30	0.09
150	20	70	No	4.37	0.08	4.29	0.05
150	30	60	No	4.49	0.05	4.33	0.06
150	30	60	No	4.51	0.07	4.31	0.06
300	0	110	No	4.30	0.05	4.24	0.04
300	20	70	No	4.44	0.10	4.30	0.24
300	20	70	No	4.44	0.06	4.29	0.04
300	30	60	No	4.54	0.02	4.35	0.04
300	30	60	No	4.54	0.02	4.35	0.04
300	36	74	No	4.45	0.04	4.23	0.08
300	36	74	No	4.45	0.05	4.18	0.07
300	36	74	No	4.46	0.04	4.24	0.04
300	36	74	No	4.47	0.04	4.20	0.05
300	**36**	**74**	**626C**	**4.65**	**0.04**	**4.19**	**0.08**
300	36	74	626C	4.58	0.08	4.24	0.07
300	36	74	626C	4.58	0.07	4.17	0.07
300	36	74	626C	4.62	0.05	4.22	0.07
Polysilicon						**4.65**	



C-V curves fit using quantum corrected model from NCSU[1]

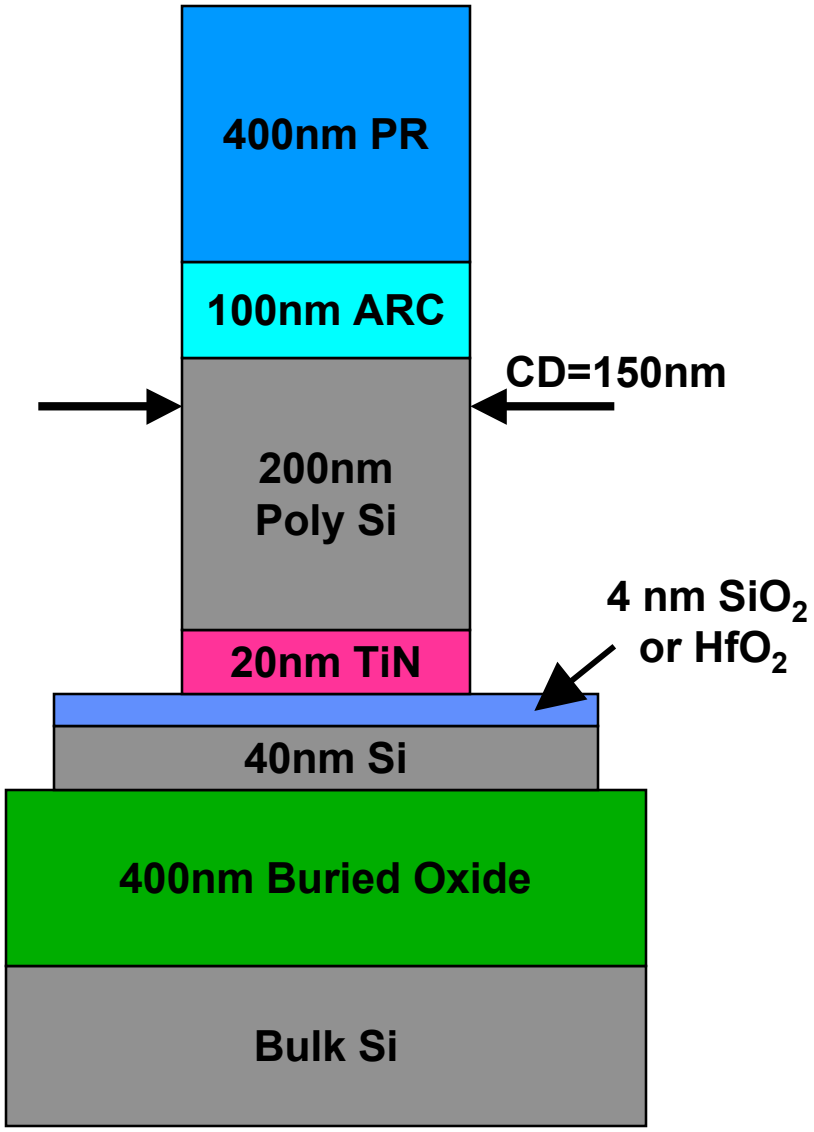
Workfunction (Φ_m) tunable from 4.20 to 4.65eV (more on HfO_2)

Target = 4.65eV

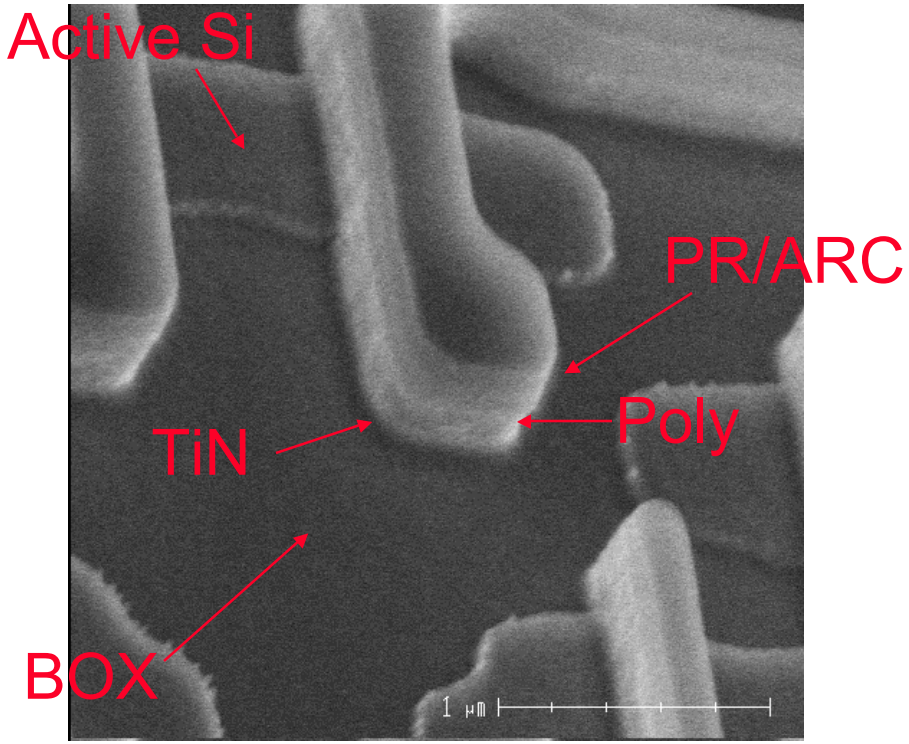
EOT reduced by 4-5Å with TiN gate (no poly depletion)

1. N. Yang et al., IEEE Trans Elect. Dev. 46 (7) p. 1464, 1999

FDSOI ULP Gate Stack

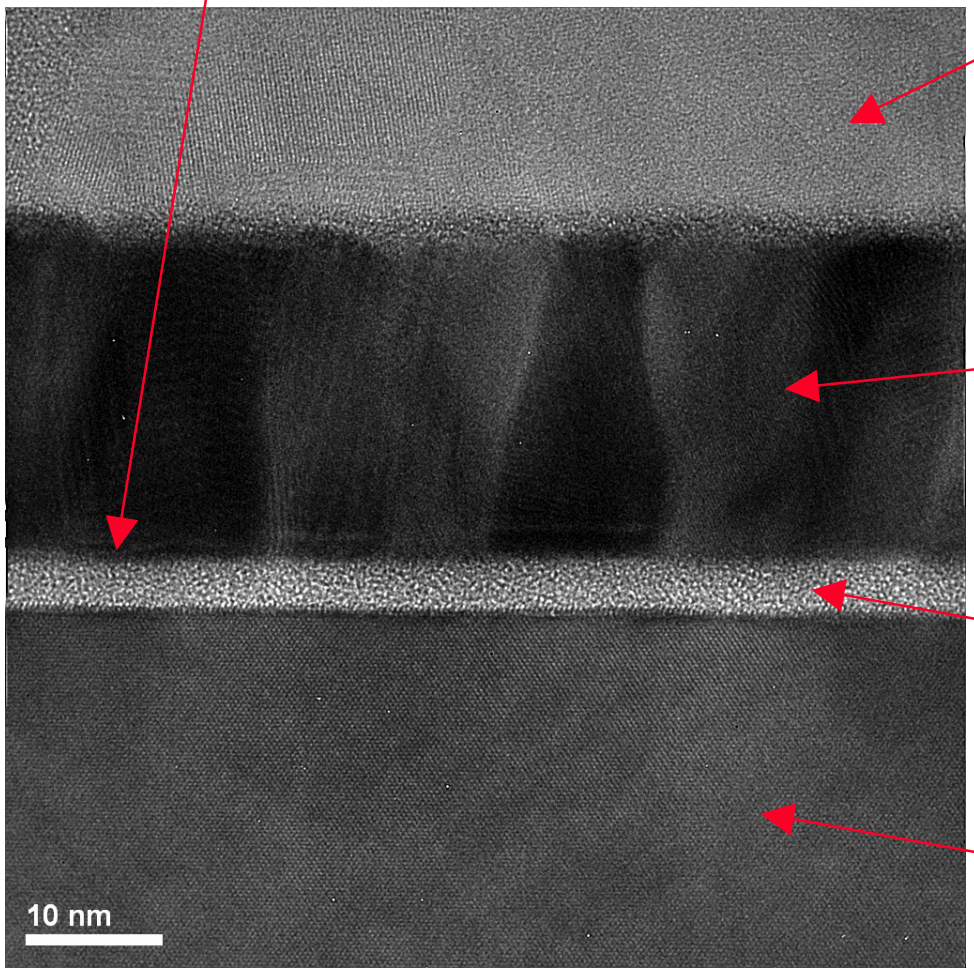


ULP SRAM Bit Cell



FDSOI ULP Gate Stack

Little TiO_2 mixing observed



Polysilicon (200nm)
- Furnace, SiH_4, 800°C

TiN (20nm)
- Reactive PVD, Ar/N_2
- 626°C N_2 anneal for workfunction tuning
- Columnar grain structure

SiO_2 Gate dielectric (4nm)
- Dry furnace oxidation

Active Silicon (40nm)
- Thinned SOITEC Unibond
- Light p-type doping

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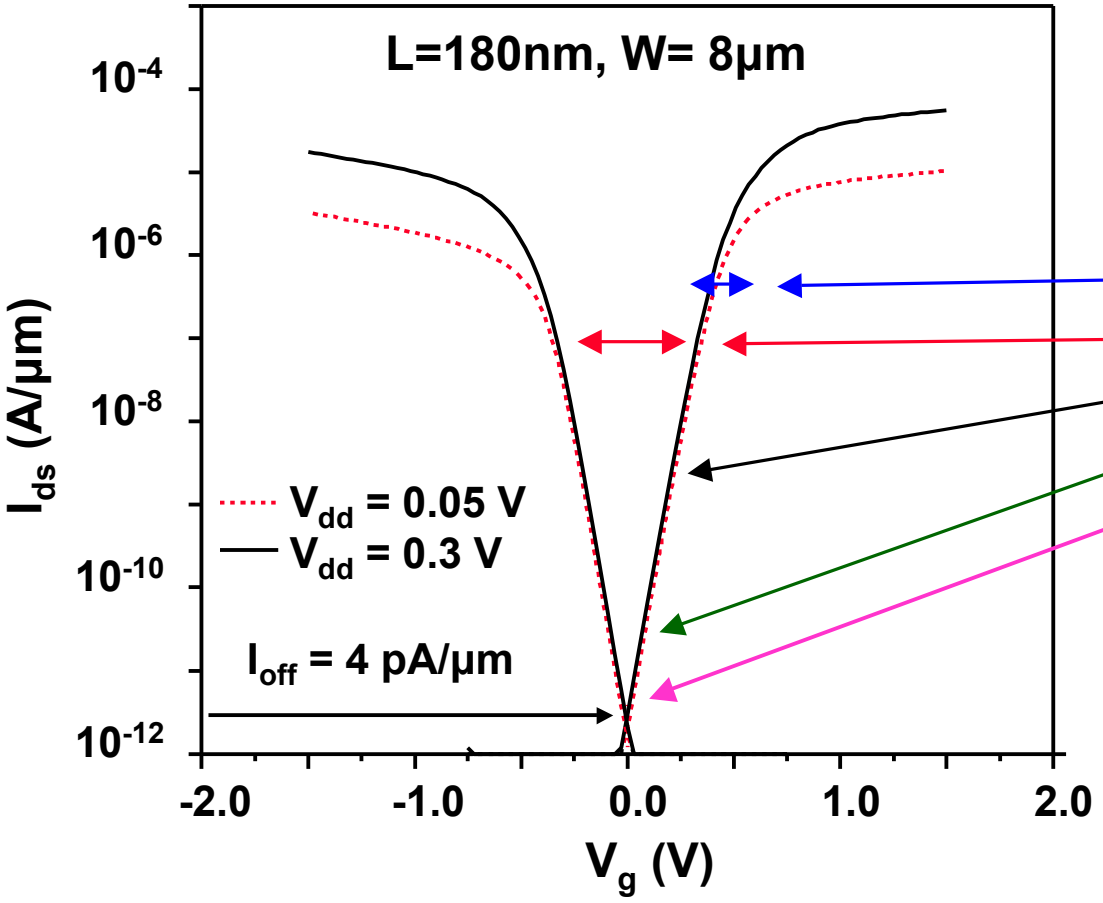
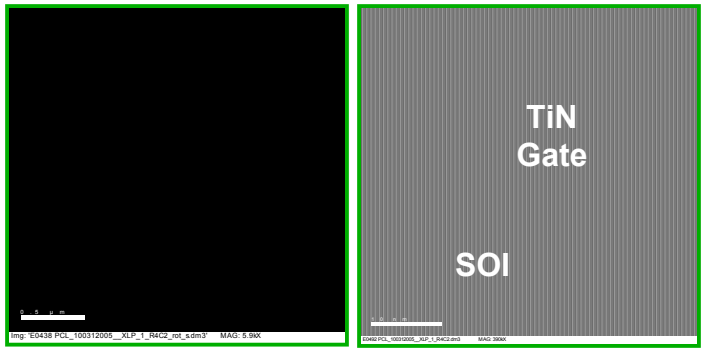
Subthreshold Optimized Transistors

Experimental TiN Metal Gate Transistors

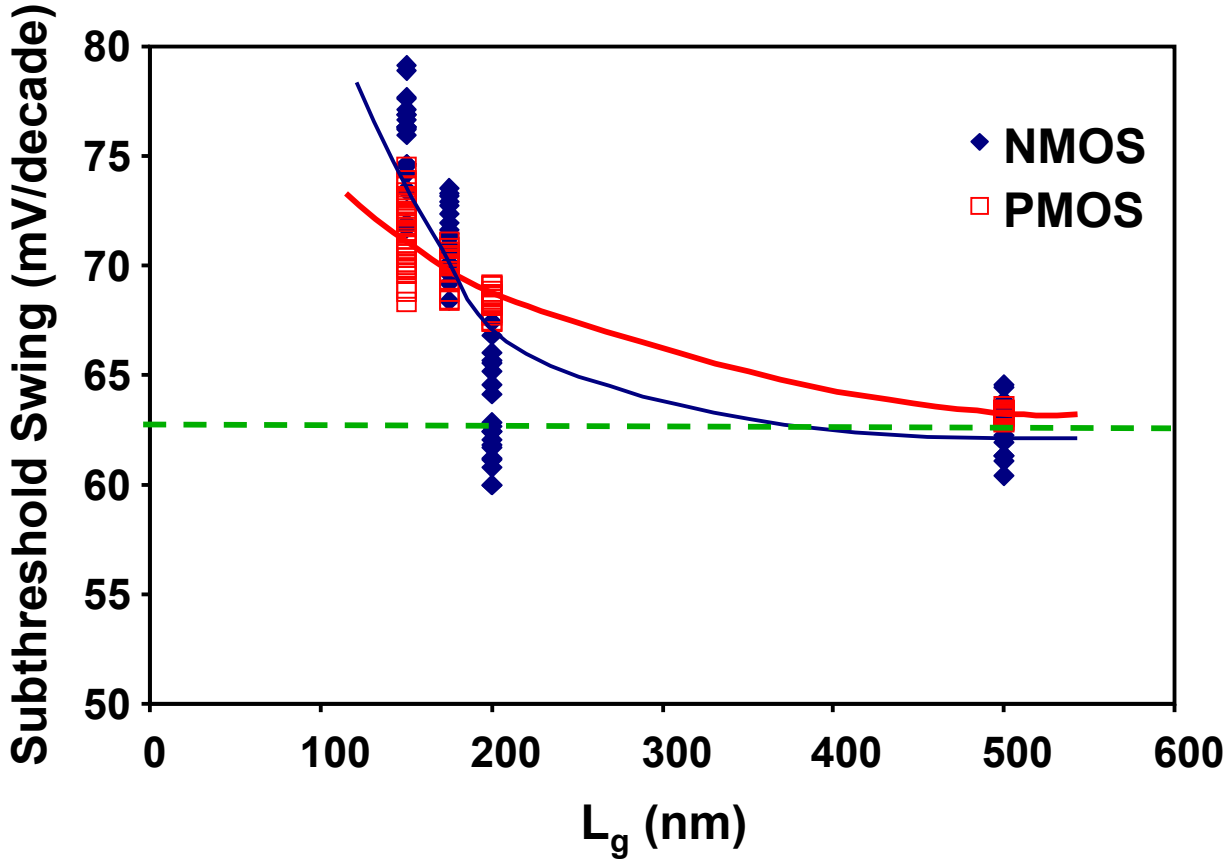


Subthreshold operation performance metrics:

1. Tight V_t distribution
2. N/P I_{on} ratio near 1:1
3. Low subthreshold swing
4. Low I_{off}
5. Correct workfunction tuning
6. Low capacitance

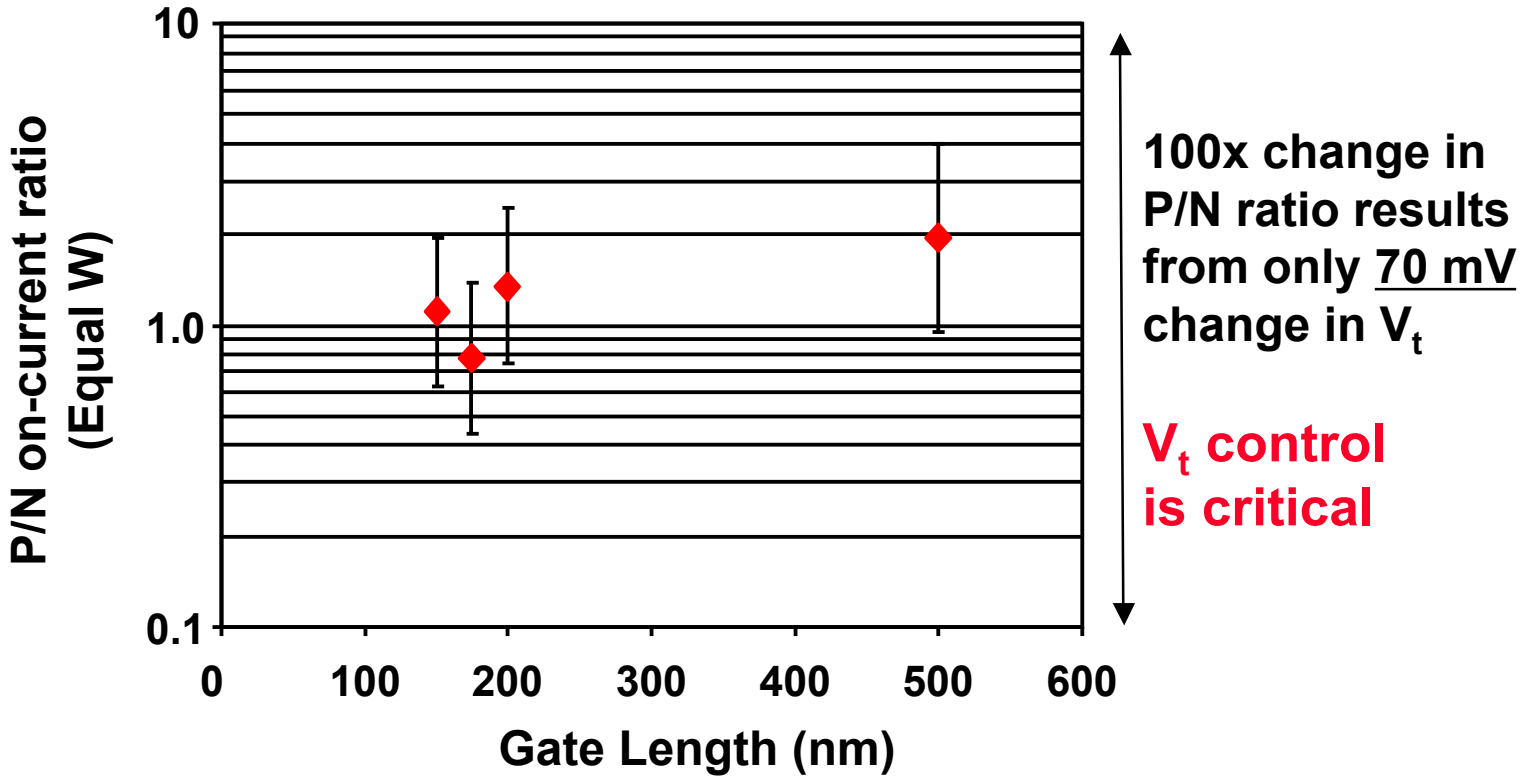


Subthreshold Swing



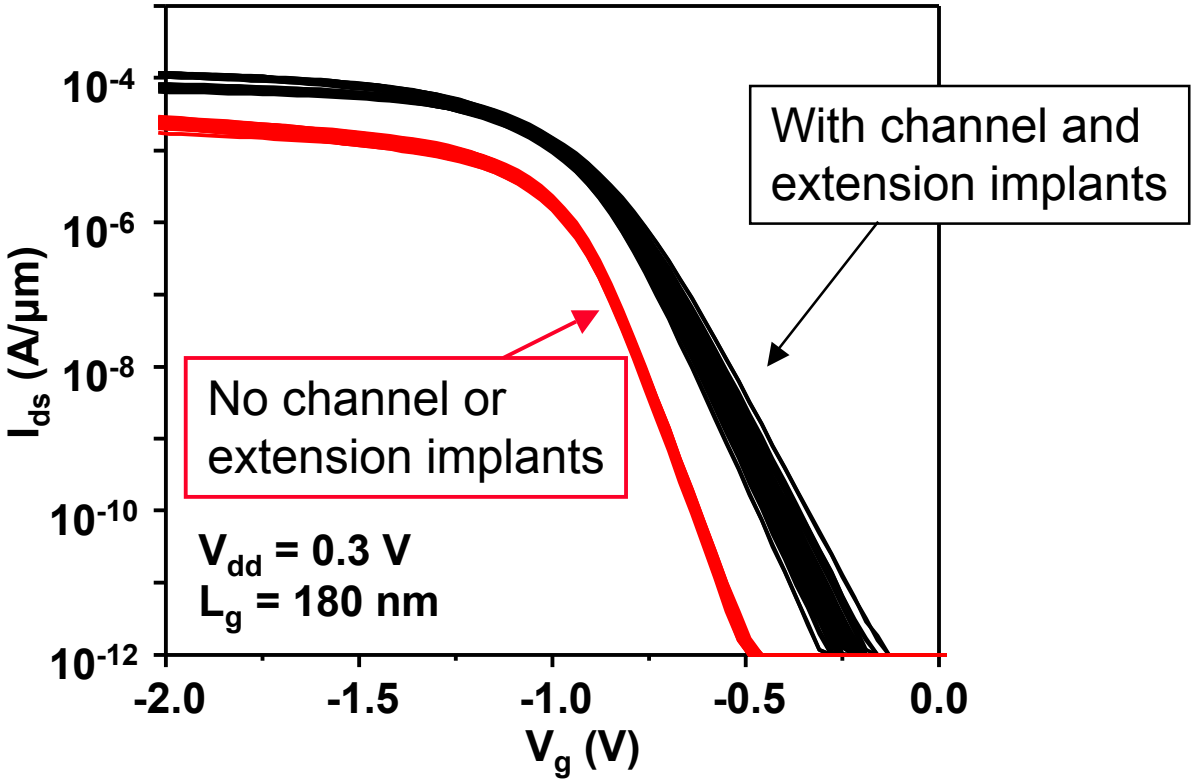
- S is near-ideal at long gate lengths
- S increases as L_g decreases due to short channel effects
- Should improve by using thinner SOI

NMOS and PMOS On-Current



Equal I_{on} allows equal NMOS and PMOS transistor sizing and equal N and P device capacitance

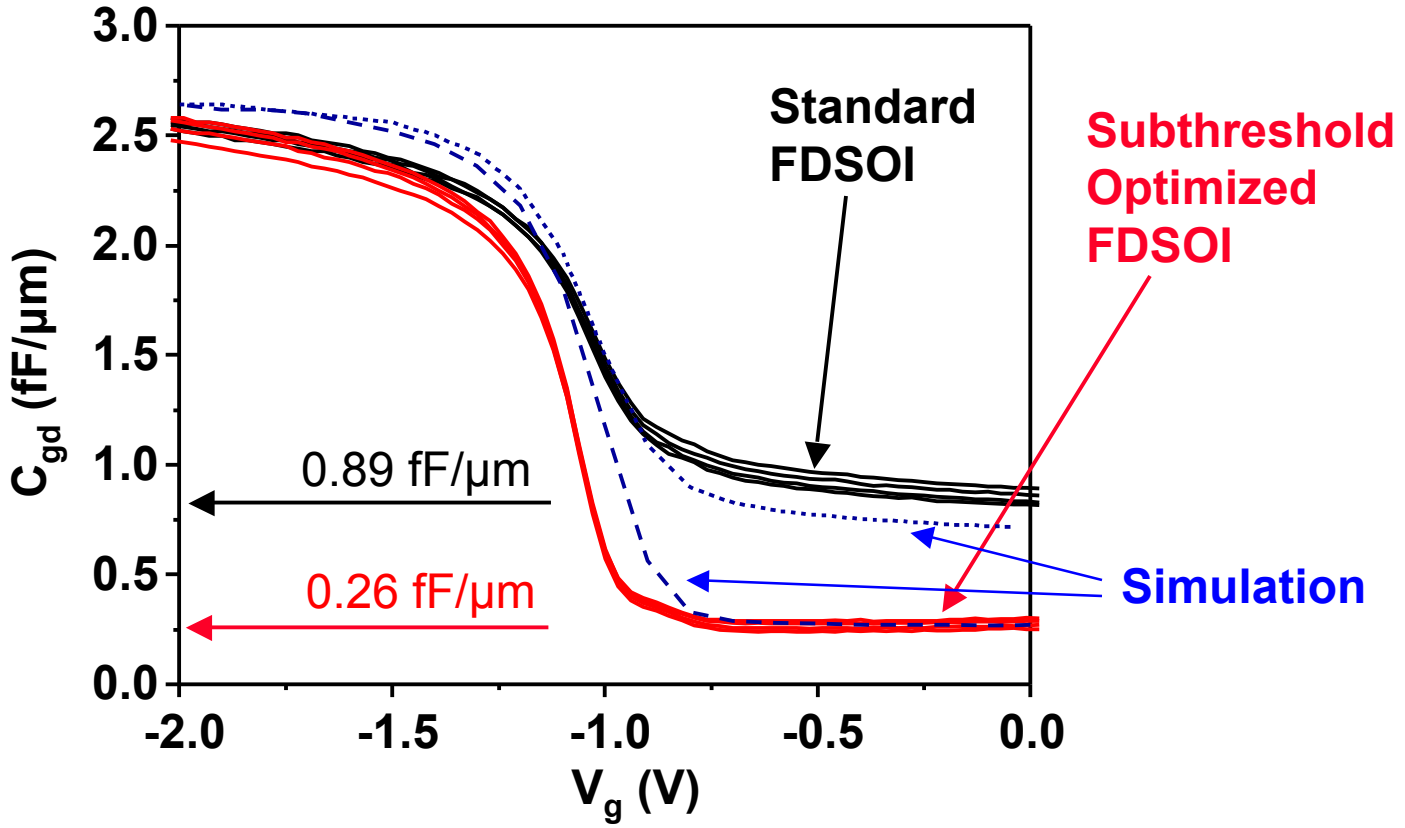
Threshold Voltage Control



- Reduces V_t sensitivity to silicon thickness
- No Random Dopant Fluctuations
- Reduces channel length sensitivity to S/D anneal variations

V_t variation improves from 18 mV to 8 mV (3σ)

Reduced Capacitance



- S/D underlap and wider spacers reduce capacitance by 70%

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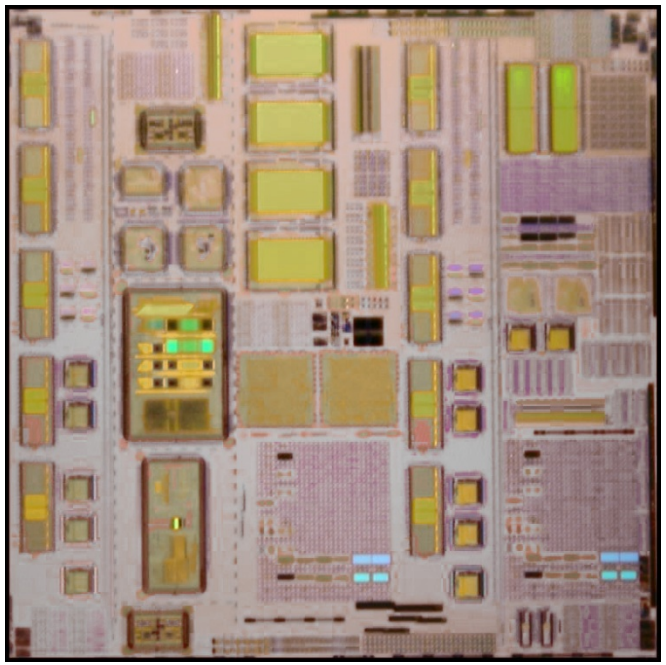
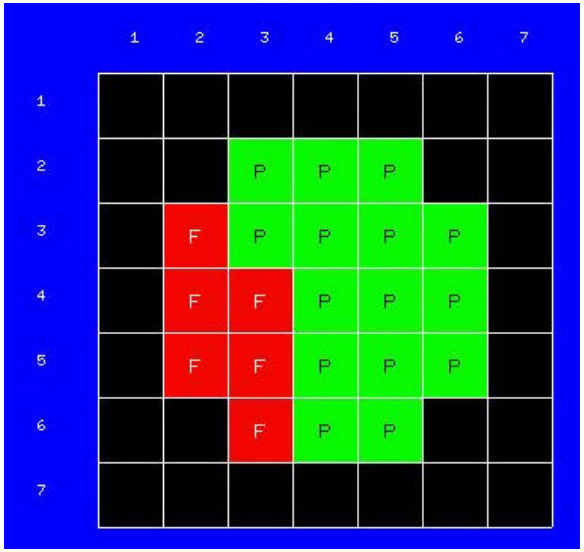
Circuit Verification Run



- 3 Level metal
- 150 nm design rules

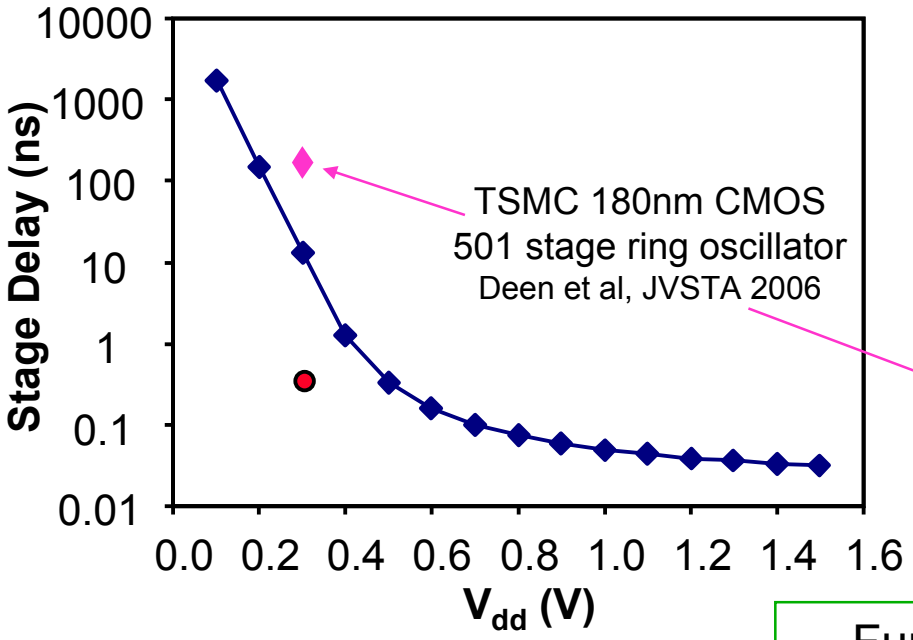
Wafer Map of Functional Multiplier Circuits ~ 2,000 transistors

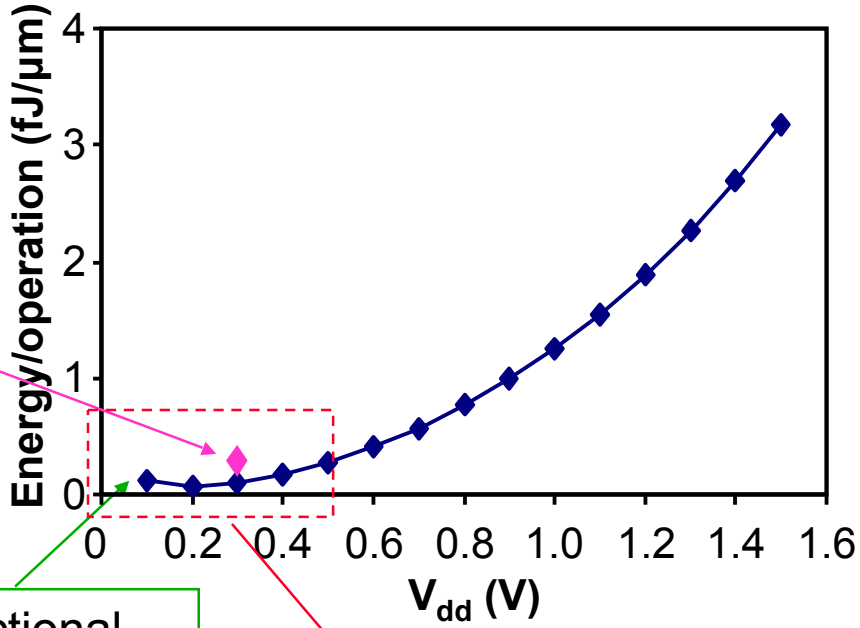


71% yield on best wafer

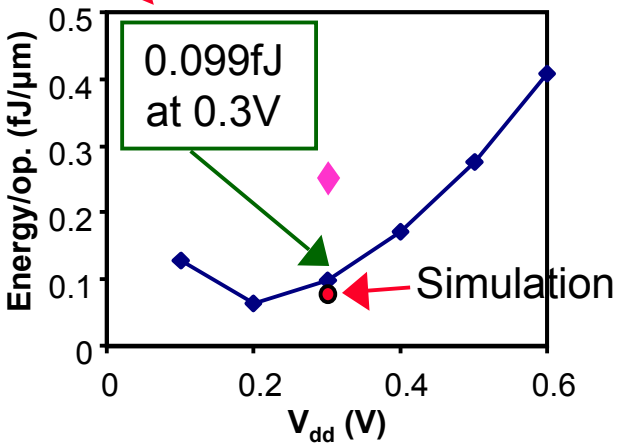
Novel ultra low power circuits from MIT-LL and 3 university partners

97 Stage Ring Oscillator (L_g=150nm)



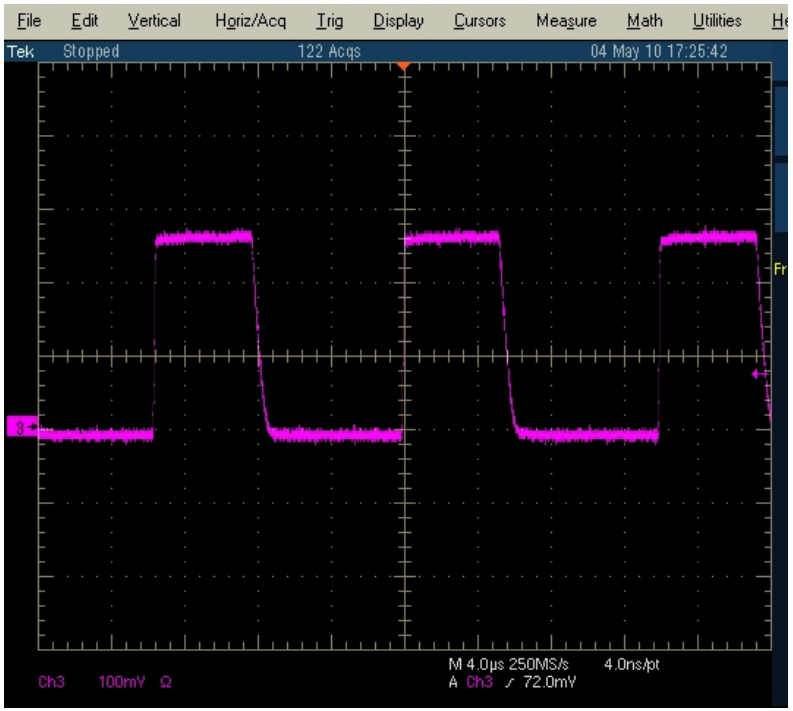


Functional down to 100mV

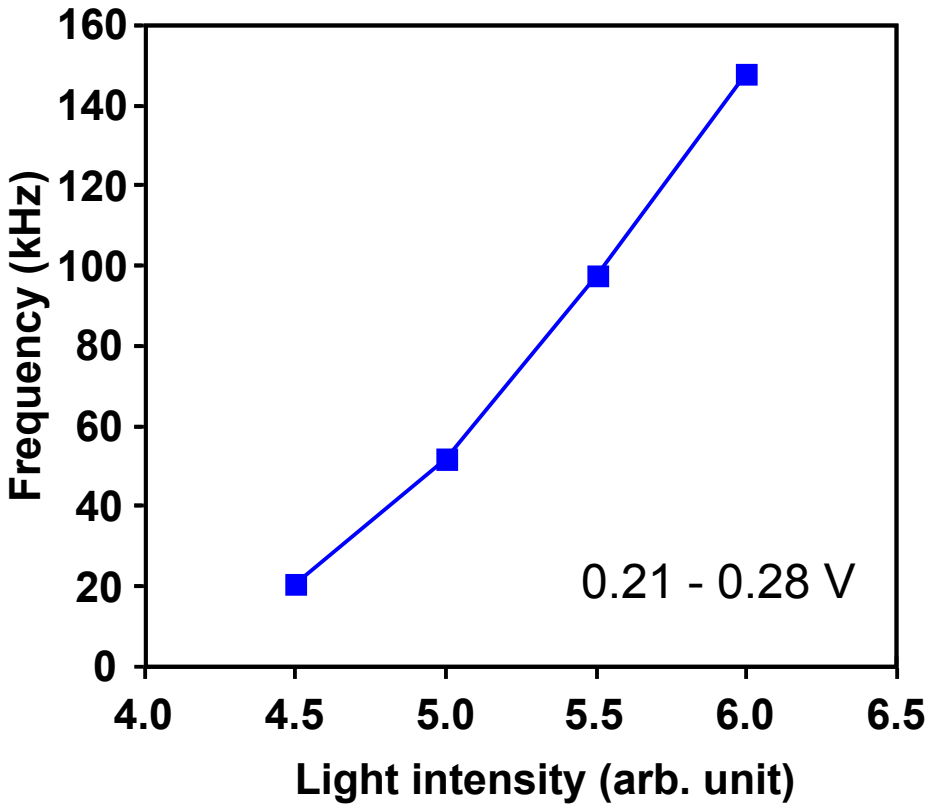


- 29x decrease in Energy-Delay product over commercial bulk silicon
- Measured switching energy = 0.099 fJ/op.
  → Simulation predicted 0.070 fJ/op.
- Stage delay is significantly higher than simulation

Energy Harvesting Ring Oscillator



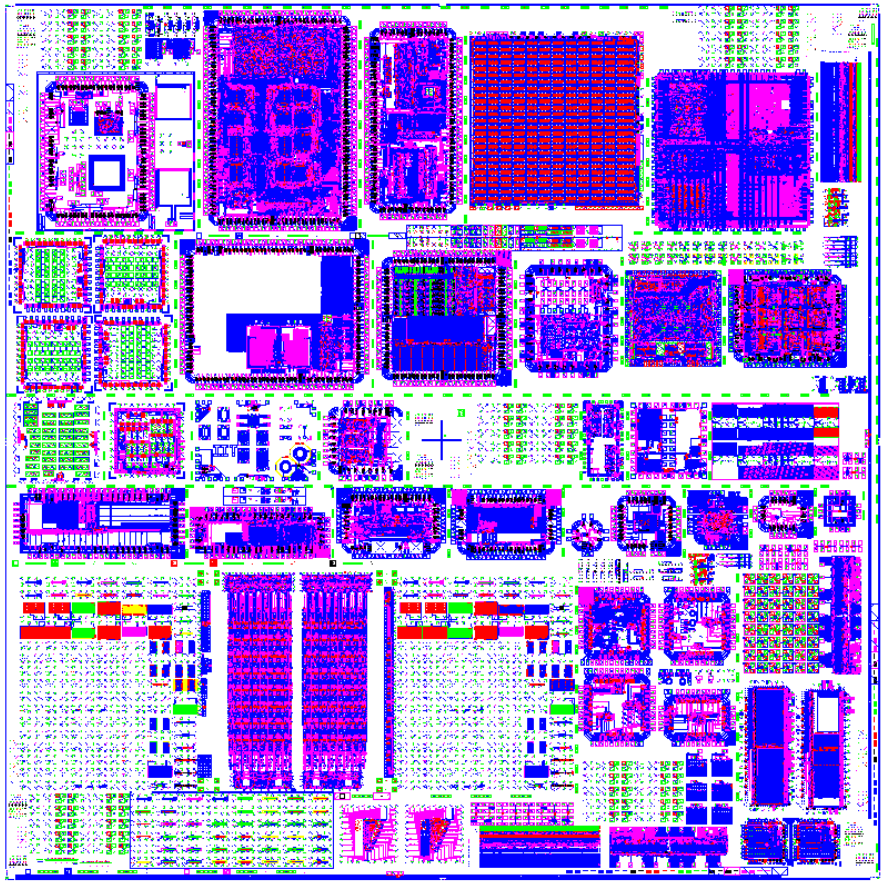
Diode-connected Ring Oscillator powered by microscope light



- Potential for Ultra Low Power circuits requiring no battery

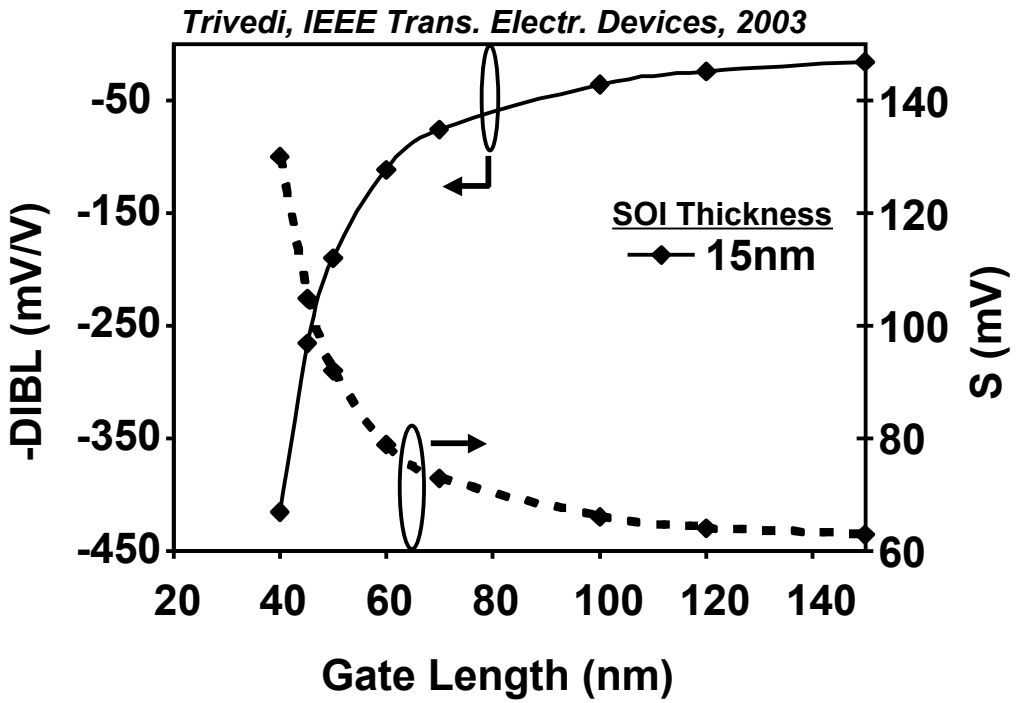
Ultra Low Power Multiproject Run

- Currently in fabrication at MIT-LL Microelectronics Lab



- Enthusiastic response from design community
- Over 30 participating institutions
- Die area oversubscribed by 50%

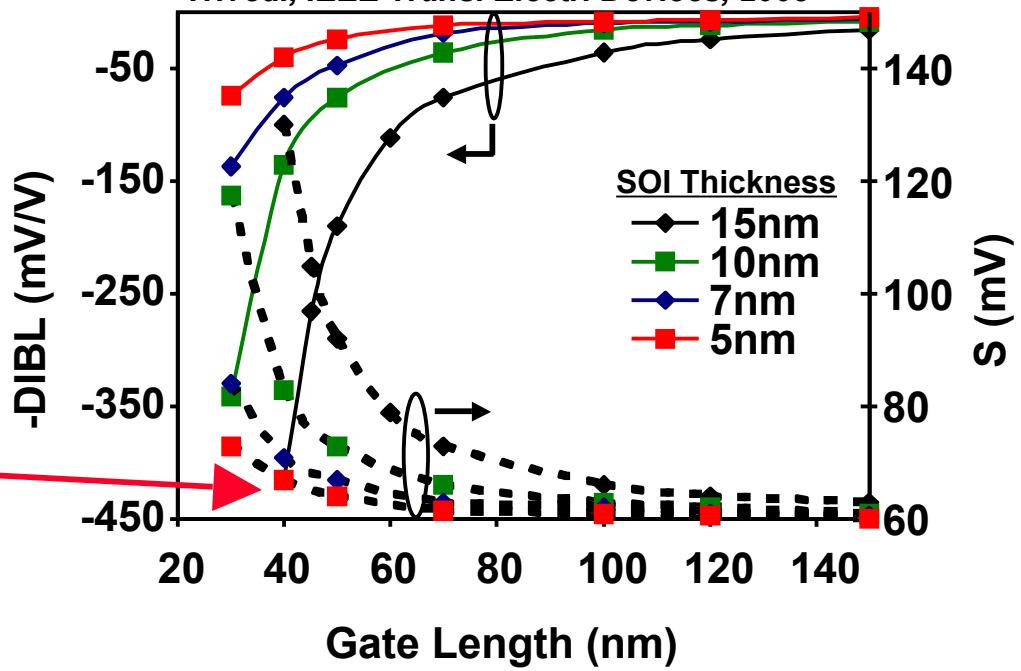
Future Scaling



As gate length shrinks, subthreshold swing and DIBL degrade significantly

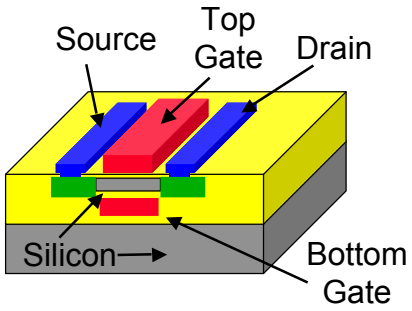
Future Scaling

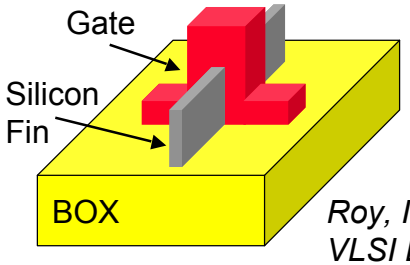
Trivedi, IEEE Trans. Electr. Devices, 2003



To scale L_g to 40nm, ultra-thin SOI is required

Below 40nm, non-planar SOI designs may be necessary for improved channel control





Roy, Int. Conf. VLSI Des., 2006

- Motivation
- FDSOI for Subthreshold Optimized Transistors
- Metal Gate Electrode Workfunction Tuning
- Transistor Results
- Initial Circuit Results
- **Summary**

Summary

- **FDSOI offers significant advantages for ultra low power operation**
  - Lower capacitance
  - Improved subthreshold swing
  - Up to 50x reduction in energy-delay product

- **Workfunction engineered TiN Metal Gate developed**
  - Allows systematic adjustment of V_t

- **Subthreshold Optimized Transistors fabricated**
  - 70% decrease in C_{gd}
  - 55% reduction in across wafer V_t variation
  - NMOS / PMOS I_{on} ratio near 1
  - 65-70 mV/decade subthreshold swing (for L_g >200nm)

- **30+ Participant Multiproject Run in fabrication**
  - Prior simple circuit test run demonstrated functional circuits

- **Looking for collaborators interested in ultra-low-power process technology**
  - Next Multiproject Run (2011) will be at 90nm design rules
  - Enabled by considerable new investment in MIT-LL Microelectronics Lab, including ASML 193nm lithography