Process Technology Explosion: New Frontiers at Intersections of Semiconductor and Related Technologies

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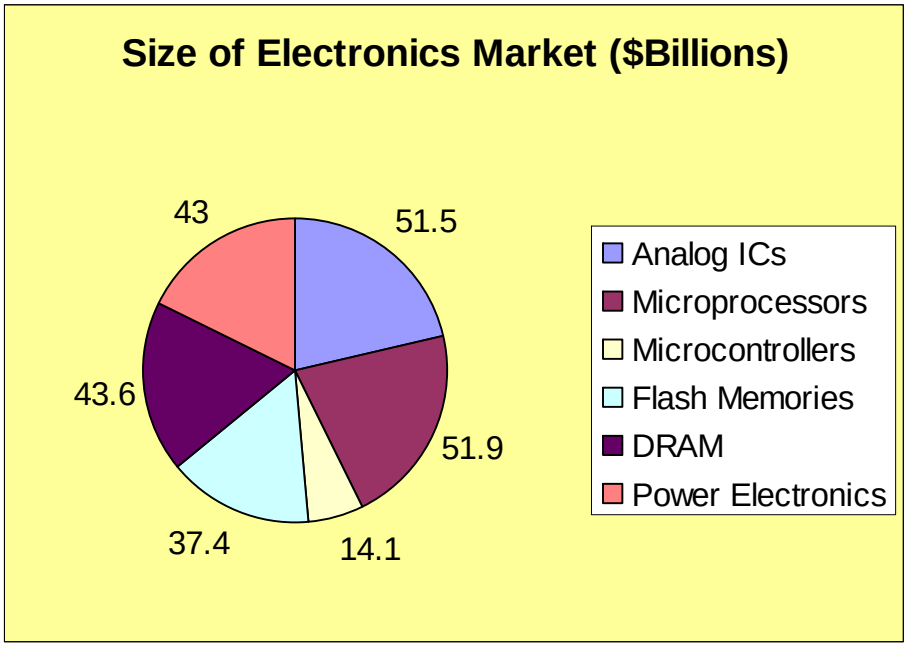
Texas Instruments

Outline of Talk

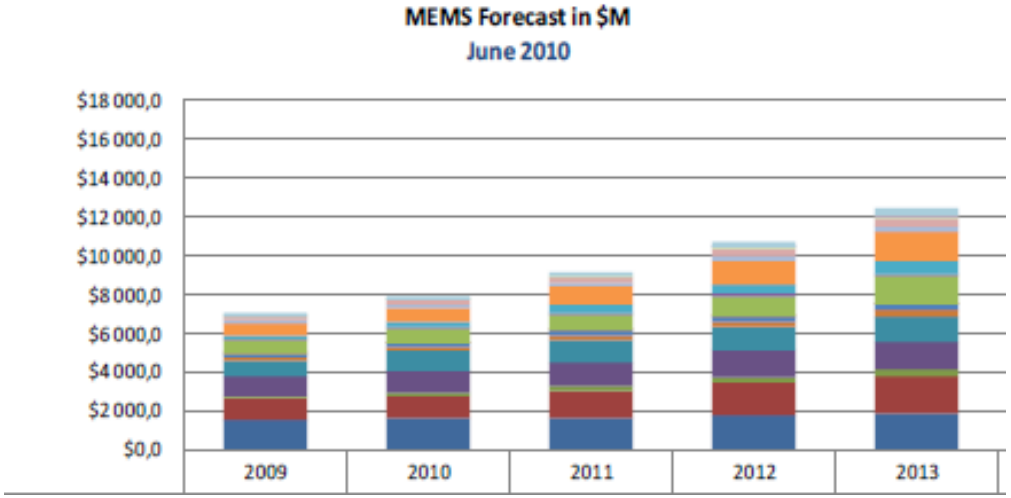
- Introduction
  - Semiconductor industry trends – no longer just Moore's Law
  - Process technology explosion in different segments
  - Significant opportunities exist at intersections of these segments and markets demand
- 3DIC/TSV Examples
  - MEMS Etch -> TSV Etch
  - Damascene Electroplating -> TSV Electroplating
- How to successfully assess other process technology alternatives?
- Conclusions

Electronic, MEMS markets

- Large markets exist and continue to expand for key market segments
- MEMS is emerging rapidly as a key market segment



[Source: Palacios, ESSDERC 2010]

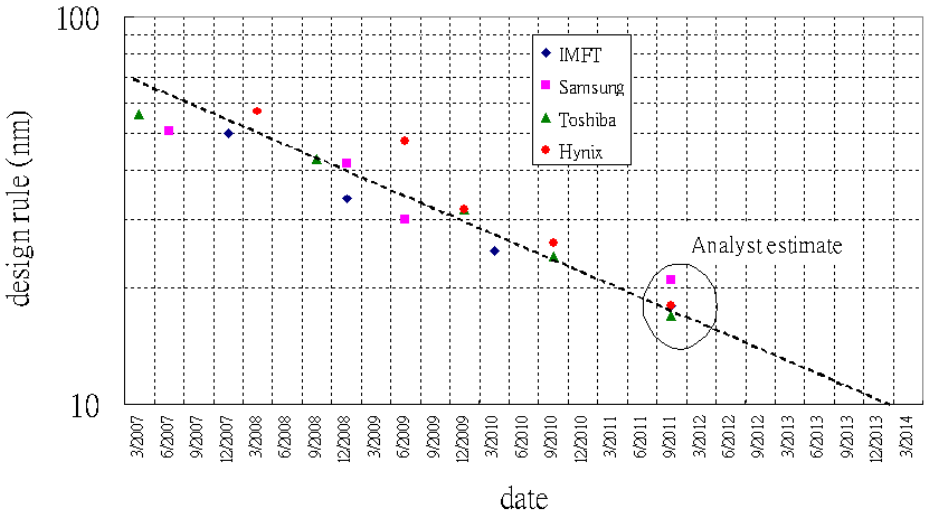


[Source: YoleDeveloppement, MEMS/Micromachine 2010]

Semiconductor industry trends CMOS/Memory

- Moore's Law scaling is running out of steam, while "more than Moore" is becoming new value proposition

NAND CD scaling



[Source: EE Times, 2010]

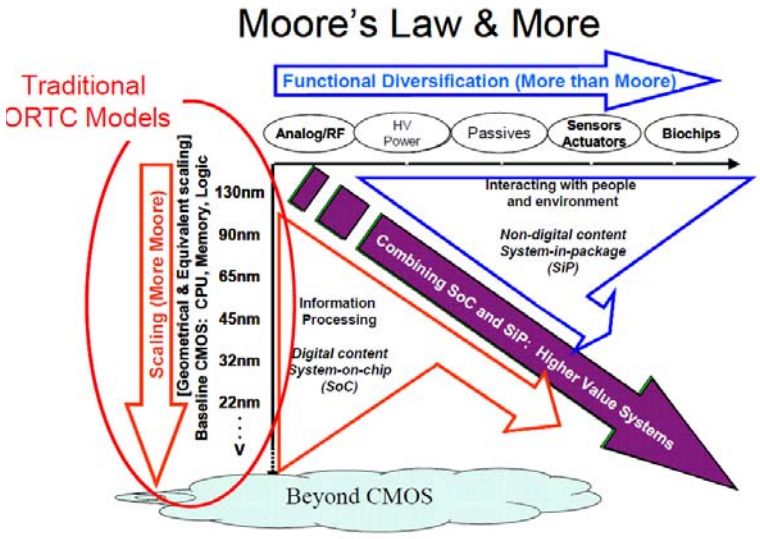
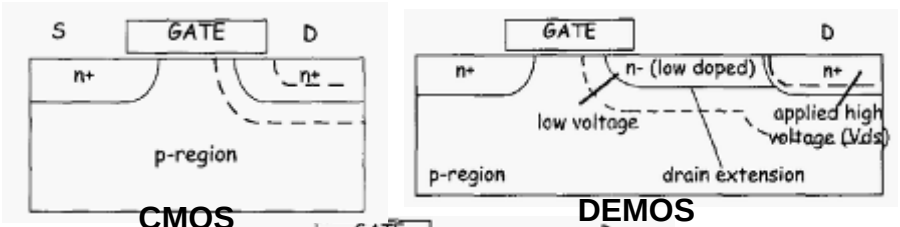


Figure 4 Moore's Law and More

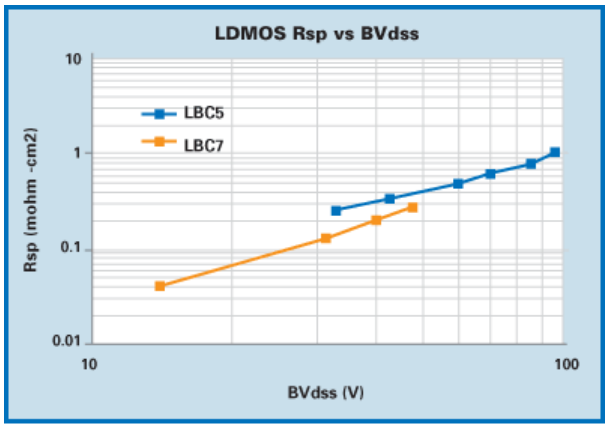
[Source: 2009 ITRS Roadmap]

Semiconductor industry trends
Power

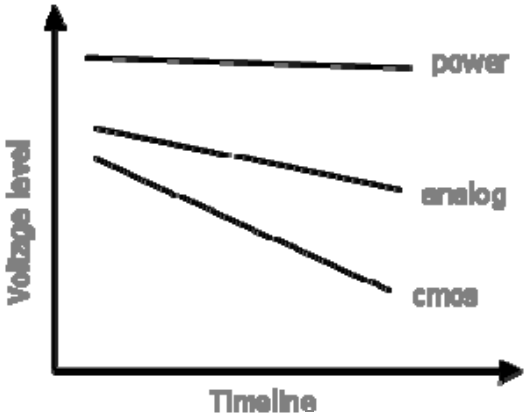
- Optimizing power performance, adding flexibility (multiple operating voltages), lowering cost, x,y scaling more challenging

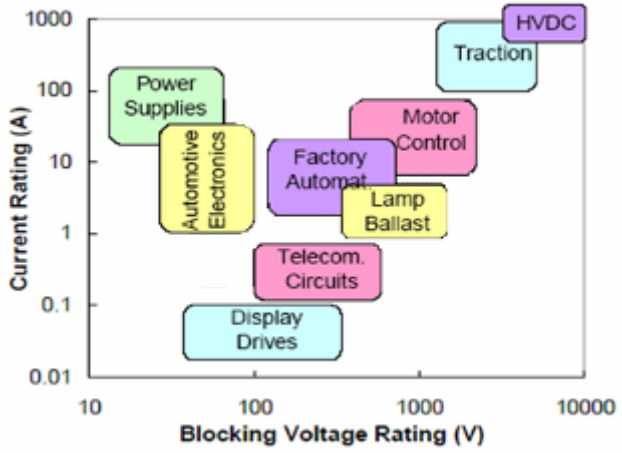


[Source: Hower et al., IEEE IRPS 2005]



[Source: TI Website]

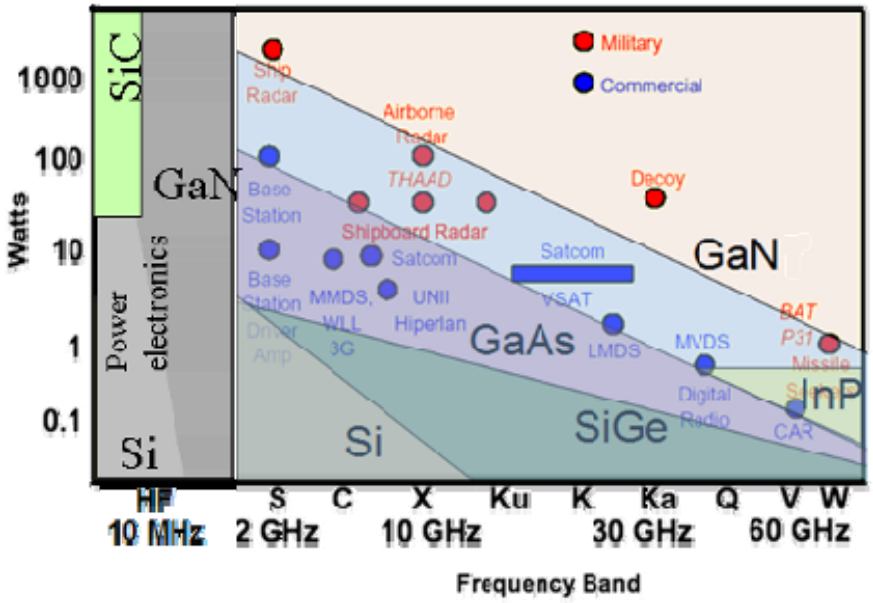




[Source: Palacios, ESSDERC 2010]

Semiconductor industry trends Power/RF

- III-V semiconductors, GaN increasing in usage
- RF CMOS FETs increasing competition with BiCMOS SiGe HBT in low GHz frequency



[Source: Palacios, ESSDERC 2010]

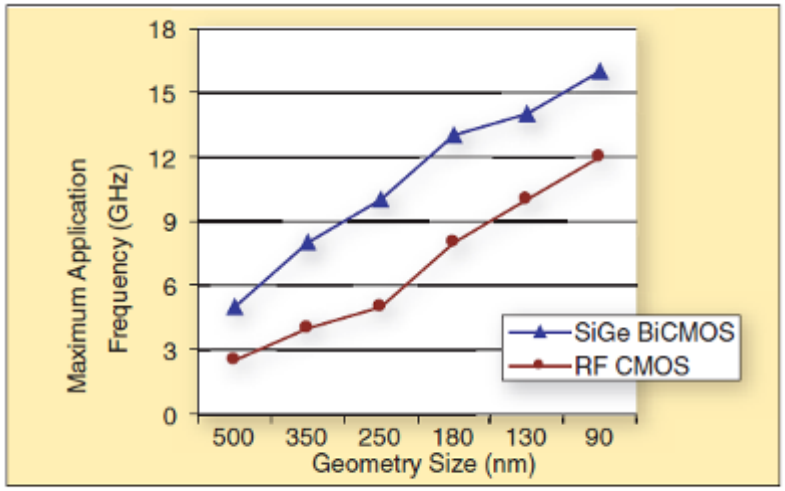


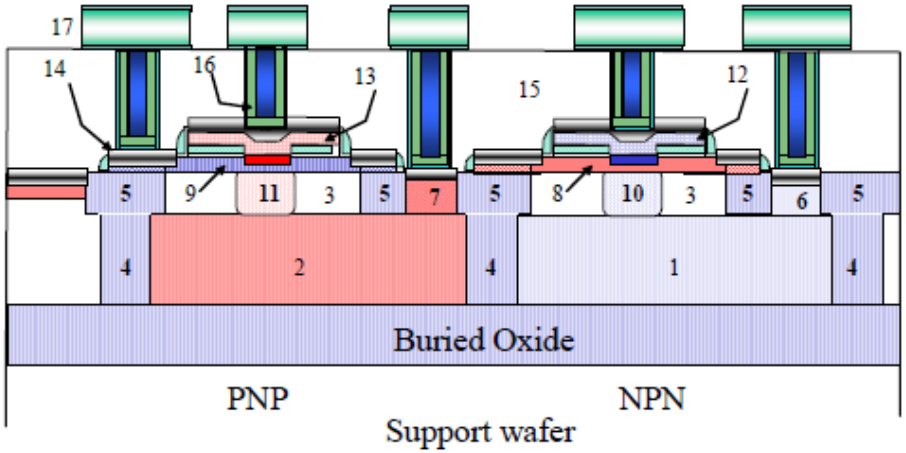
Figure 1. Maximum application frequency for CMOS and SiGe BiCMOS by transistor size (fT/8).

[Source: Pawlikiewicz et al. RF Design 2006]

Semiconductor industry trends
High Speed/High Precision Analog

- Improving performance, adding flexibility, lowering cost, precision materials, complex device integration

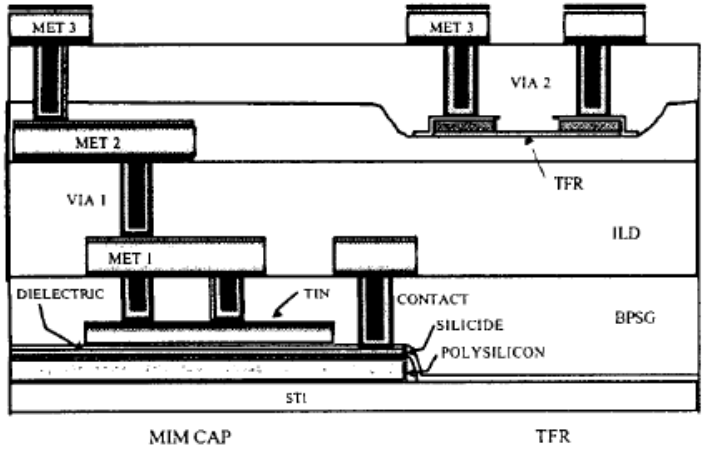
High Speed High Precision BiCMOS



1: N-buried layer; 2: P-buried layer; 3: Collector epitaxy 4: Deep trench; 5: STI; 6: NPN sinker; 7: PNP sinker; 8: NPN base; 9: PNP base; 10: NPN SIC; 11: PNP SIC; 12: NEMIT POLY; 13: PEMIT POLY; 14: $CoSi_2$; 15: BPSG; 16: Contact; 17: 1st metal (2nd-4th metal not shown).

Fig.1: Schematic of NPN and PNP transistors

[Source: B. El-Kareh, et al., ECS 2004]



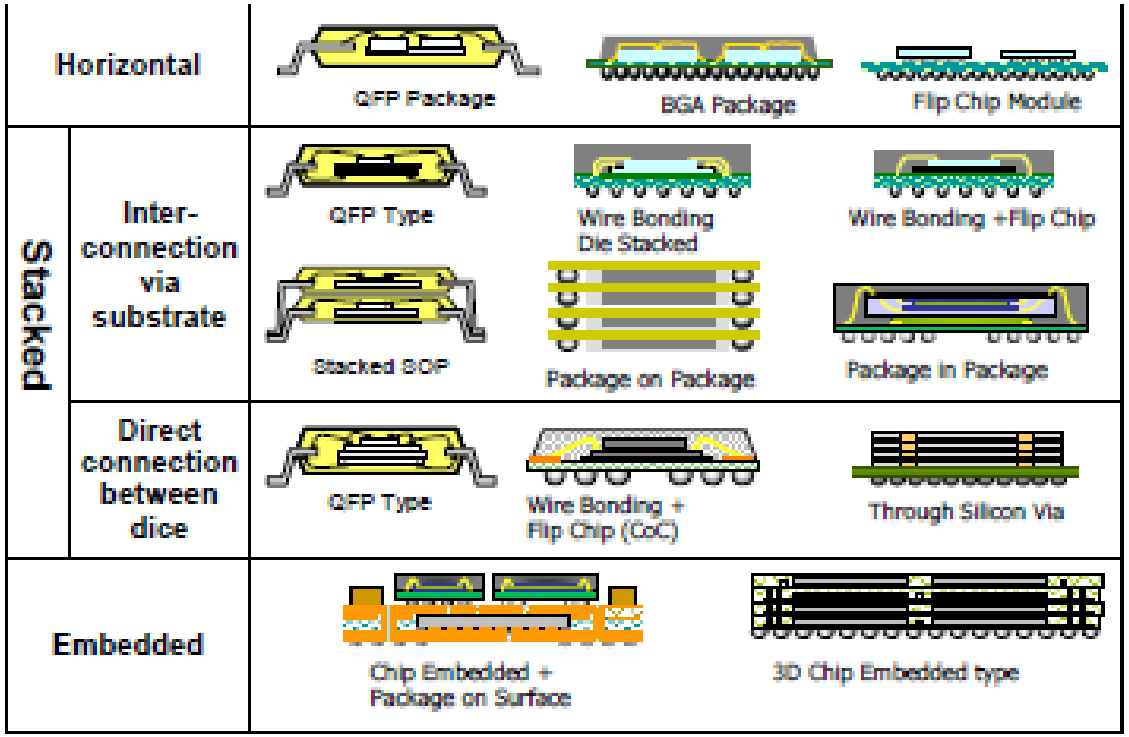
Precision Caps and Resistors

[Source: B. El-Kareh, et al., IEEE BCTM 2003]

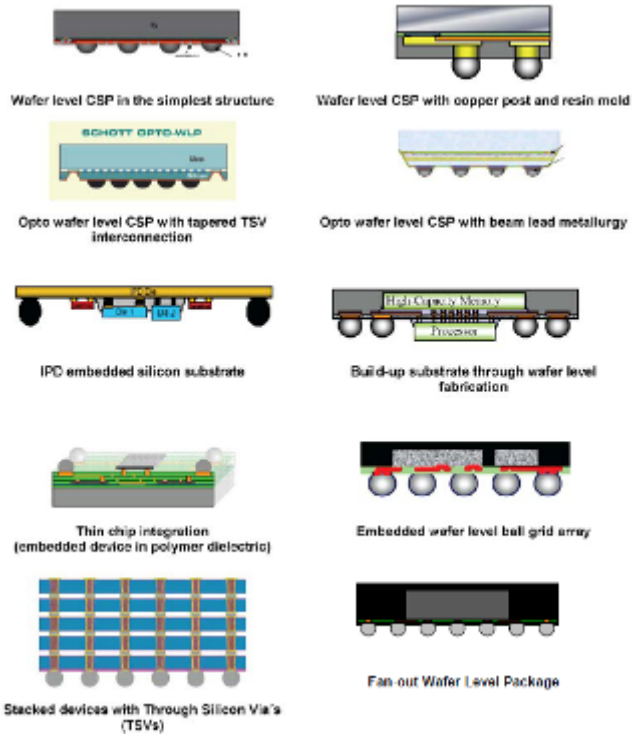
Semiconductor industry trends
Package development

- Package – POP, PIP, SIP, passive components in package, smaller sizes, WLP. Many advances in wirebond and package types.

SIP, POP, PIP, Embedded



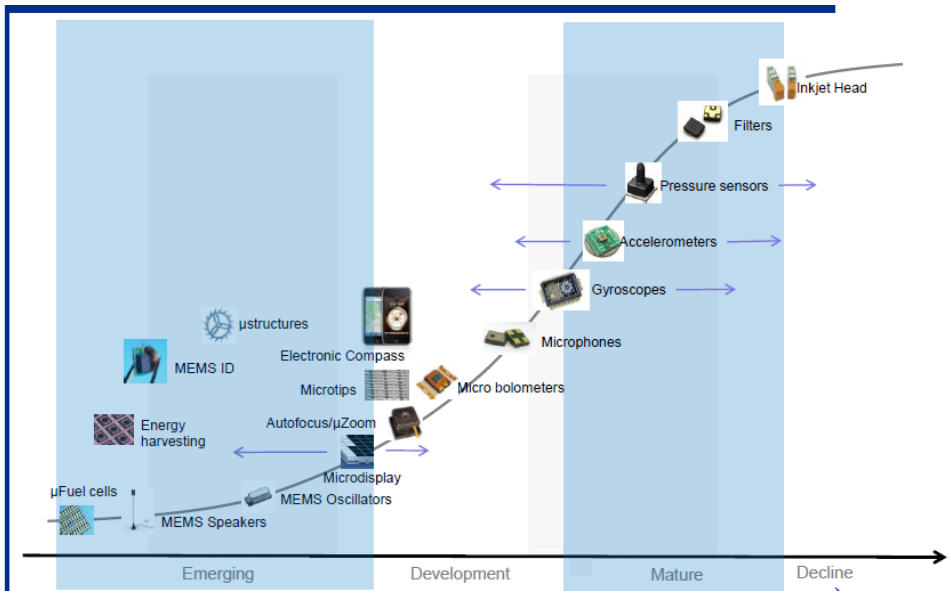
WLP



[Source: 2009 ITRS Roadmap]

Semiconductor industry trends
MEMS

- Increased usage in consumer electronics segment (thanks Apple!)
- 3D MEMS starting to arrive



Simplification of manufacturing is still an objective

- The MEMS law "One product, one process, one package" is still there
- MEMS packaging is more and more an "added value step" with 3D MEMS being more widely adopted
- Software development is now an important competence in MEMS companies in order to sell functions and not devices

8'' manufacturing infrastructure is needed for companies targeting consumer electronics

- The MEMS manufacturers not involved in consumer electronics are facing a very strong risk to lose competitiveness

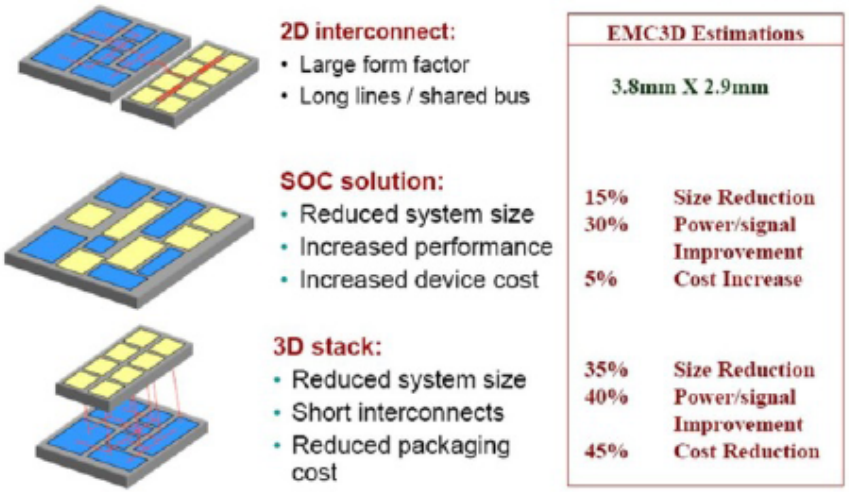
Competition is increasing on consumer electronics applications:

- STM is now proposing accelerometers, gyroscopes, microphones and digital compass
- Invensense is searching in its IPO large extra funding to compete on motion sensing applications

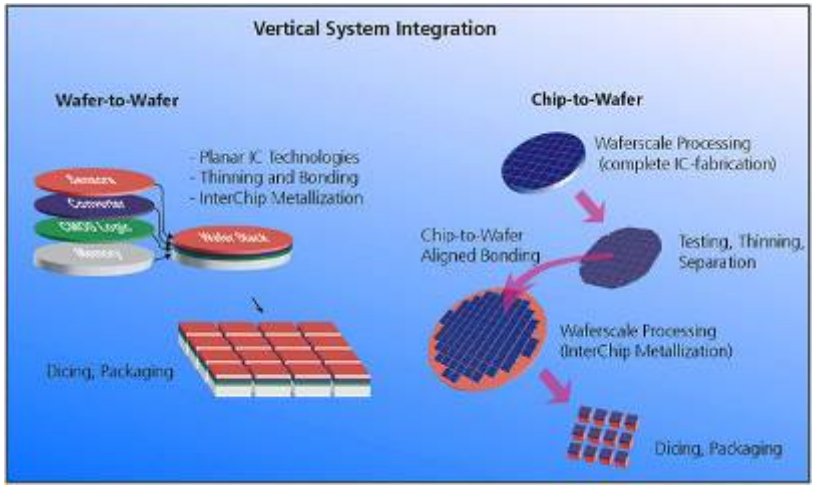
[Source: YoleDeveloppement, MEMS/Micromachine 2010]

Semiconductor industry trends
3DIC/TSV

- 3DIC/TSV, More than Moore – die stacking, increased bandwidth, lower inductance, ultimately heterogeneous integration is goal



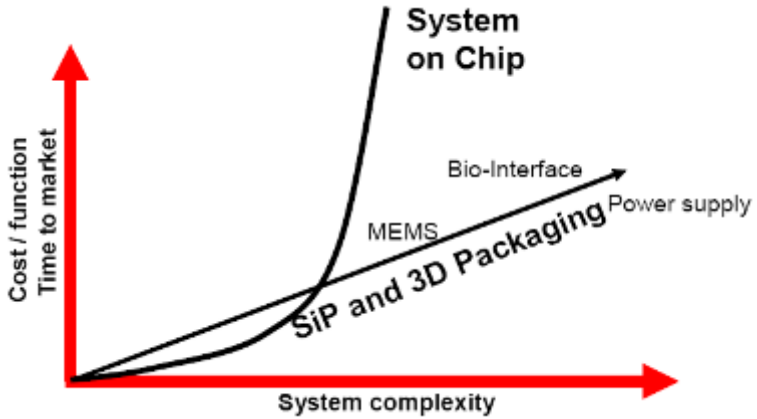
[Source: 2009 ITRS Roadmap]



[Source: E-Cubes website]

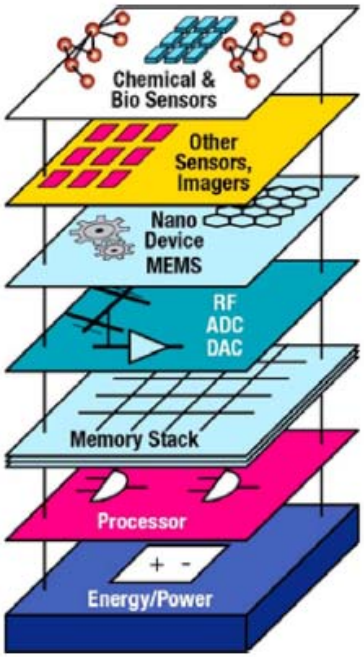
Semiconductor industry trends 3DIC/TSV

- Drive to Heterogeneous integration



SoC and SiP Comparison for Cost per Function and Time to Market vs. Complexity

[Source: 2009 ITRS Roadmap]

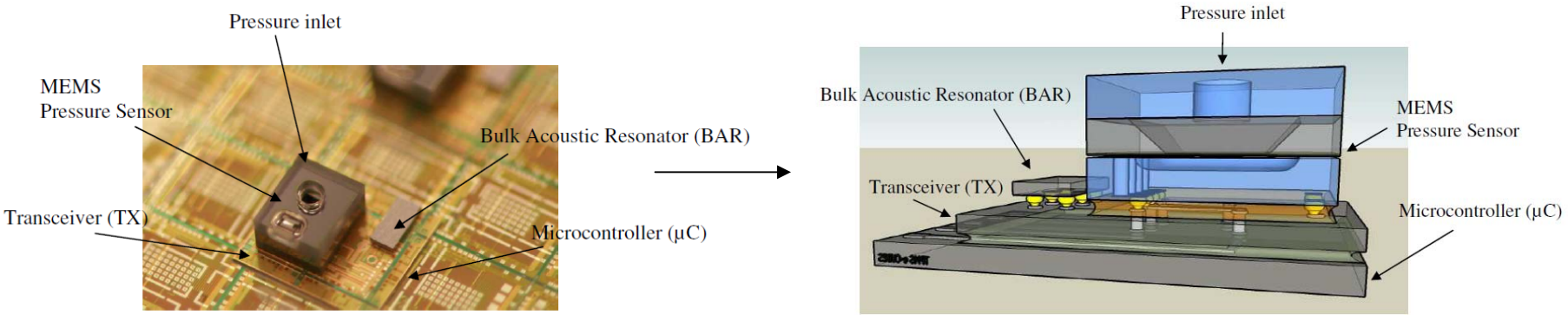


[Source: J.Q. Lu - 2009 IEEE Proceedings]

Semiconductor industry trends
3DIC/TSV

- 3D and MEMS a little more challenging, but significant work is being done

E-cubes project for fully integrated Tire pressure monitoring system



[Source: M. Taklo et al., MRS 2009]

Miniaturization

Process Technology Explosion across segments

CMOS/Memory
- Advanced lithography (immersion, double patterning, RET, tri-layer resist)
- SiGe epi
- USJ (anneal, …)
- Low-k materials
- HAR trenches
- High-k ALD

Packaging
- Backgrind developments
- BUMP/RDL
- Pick-and-place
- Mold materials development
- Bonding technology (solder/IMC)
- Embedded components integration

MEMS
- Thick Photoresists
- KOH etch
- HF vapor
- LIGA
- Front-to-back printing
- Wafer-to-wafer bonding
- Bosch etching
- Piezoelectric materials and processing
- Micro-fluidics

Analog/RF
- Precision Passives
- Deep Trench
- Thick metal routing
- VHE implants, high temperature furnace
- Epitaxy/SOI
- III-V materials

3DIC
- Deep Si etch
- Laser drilling
- Wafer carriers
  - Bond/Debonding
- Large feature/HAR plating
- Front-to-back printing
- Large feature insulation
- Fusion bonding

Others
- LED technologies
- Solar technologies
- Thin film battery
- Ferromagnetics on chip
- Ferroelectrics on chip
- Optics on chip
- Liquid flow thru pipes
- Many more…

It is great to be a process/integration engineer in the year 2010

Texas Instruments

Process Technology Explosion across segments

- Markets are driving more integrated solutions that are smaller, higher performing, and cheaper….
- Innovation = Differentiation, significant opportunities exist at intersections of these technologies
- But need to choose wisely and realize new challenges arise when we start to hybridize these technologies (examples from 3DIC/TSV to follow)

3DIC/TSV Case example

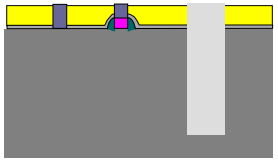
- Why 3DIC/TSV?
  - Higher bandwidth (CMOS/MEMORY stacking)
  - Lower inductance (RF)
  - Smaller form factor, improved package soln (CMOS image sensors, others to follow)
  - Heterogeneous integration…well, eventually
- Why is it taking so long?
  - CMOS Image Sensors in MFG, but others applications are taking longer
  - Packaging alternatives abound
  - Cost is too high
    - Still need to work on high volume manufacturing improvements
  - Performance improvements not needed yet

TSV Integration approaches

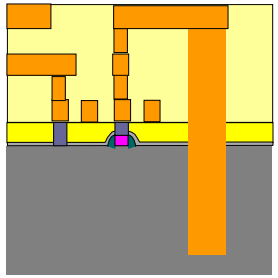
TSV Creation in FAB

1. Via-First Pre-PMD (poly)

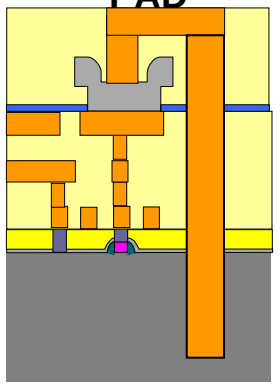
2. Via-First Post PMD (W or Cu)



3. Via-First M1 to TLM

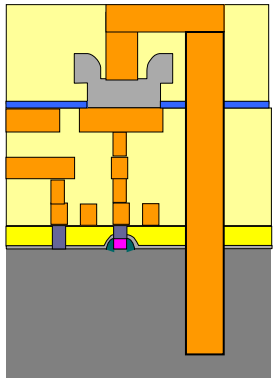


4. Via-First Post PAD

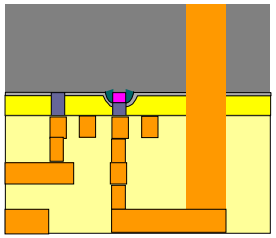


TSV Creation in BUMP or A/T

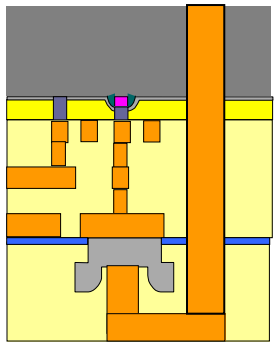
5. Via-First Post PAD



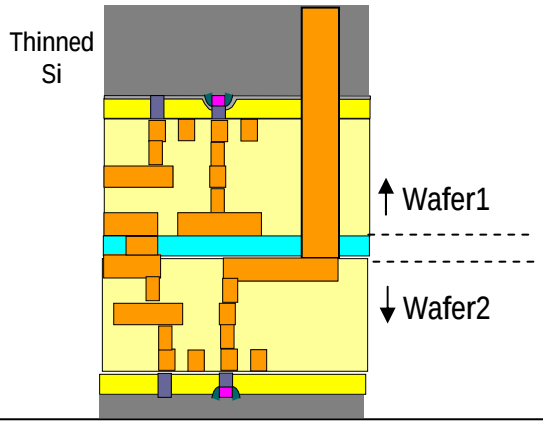
6. Via-last - to M1 to TLM



7. Via-last – Post PAD



8. Via-last – after W2W Bonding

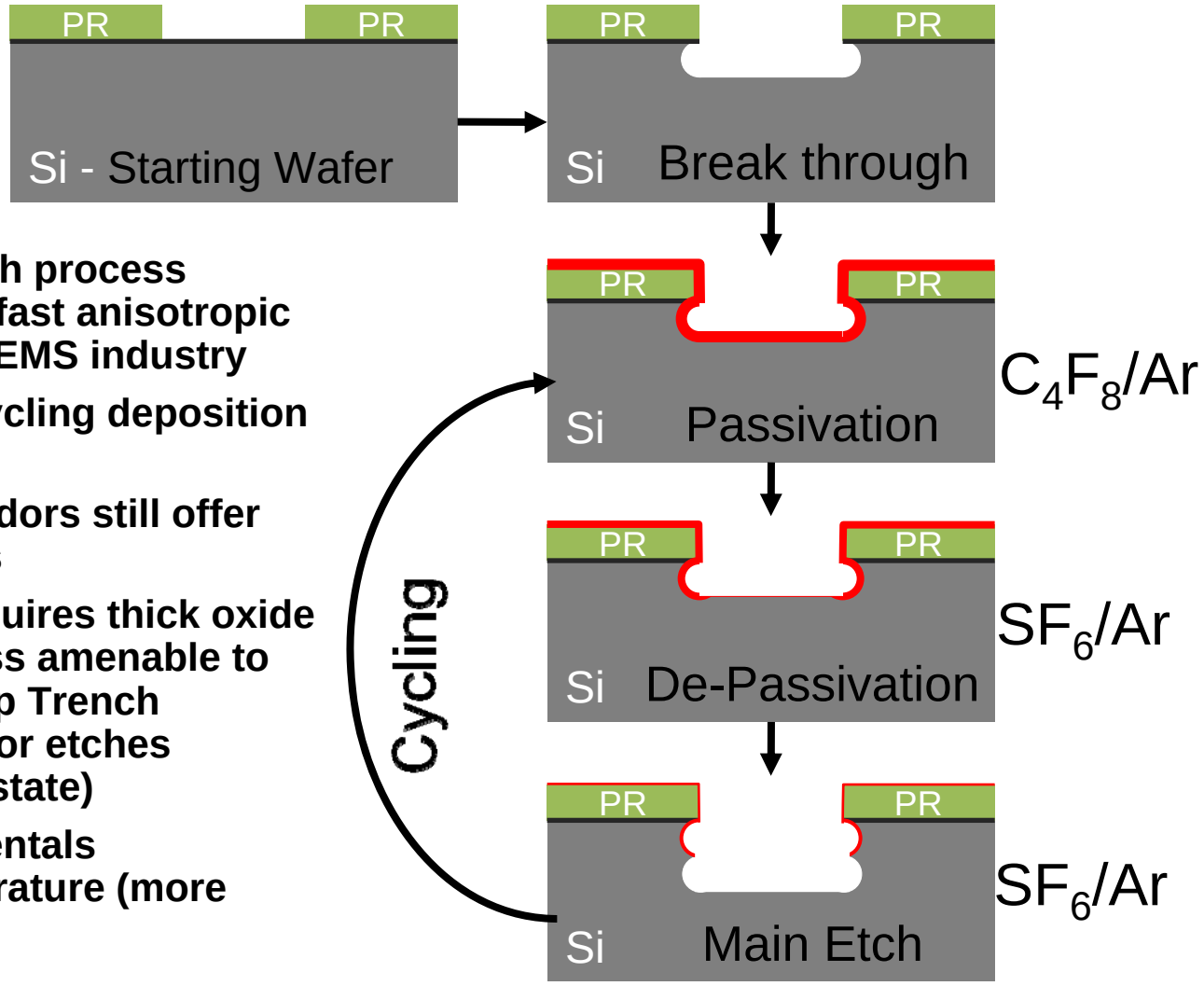


Process Translation to TSV 3D – Significant Technical Challenges

- MEMS Bosch Etch -> TSV Bosch Etch
  - More attention to feature level detail for TSV etch
  - Still needs throughput improvements for High Volume Implementation
- Electroplating CMOS Vias -> Electroplating TSVs
  - Significant challenges for bottom up void-free plating, reliability concerns
  - Significant challenges from copper “pumping” issue (huge volume of copper exposed to high temperatures, 400C)
  - Still needs throughput improvements for High Volume Implementation
- CMOS Cu CMP -> TSV Thick Copper CMP
  - 5-10 um of Copper to polish, but need minimal erosion for small features in adjacent regions containing much smaller vias (typically 10-100 times smaller)
- Backgrind thinning -> BG thinning and TSV tip exposure
  - BG tapes don’t translate well, so generally carriers are in use -> requires temporary bonding and debonding (immature technology)
  - Significant challenges with TSV tip exposure
  - Chipping at edge of wafer is still an issue

Bosch Etch Process

- **Cyclic deposition/etch process developed to enable fast anisotropic bulk Si etching for MEMS industry**
- **Etch controlled by cycling deposition and etch processes**
- **Many equipment vendors still offer Bosch etch solutions**
- **Steady state etch requires thick oxide HM and is slower, less amenable to TSV Integration (Deep Trench isolation and capacitor etches typically use steady state)**
- **Very limited fundamentals understanding in literature (more later)**



Deep Si Etch (Bosch Etch) – MEMS vs. TSV

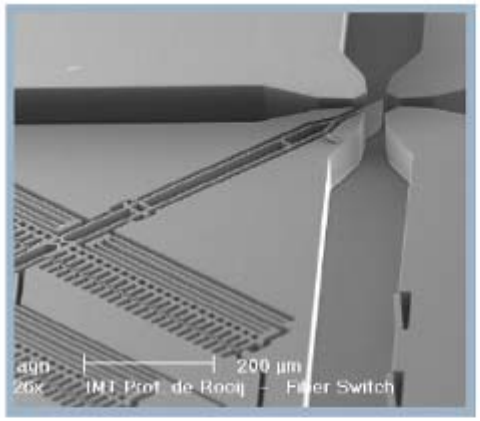
MEMS

- Typical etch stop on Resist or SOI
- Feature size variation on wafer
- High % open area >10%
- Depth often entire thickness of wafer (400-700um)
- No feature fill
- Retrograde profiles (larger CD at bottom than top)
- Profile control less relevant
- Sidewall roughness, mask undercut not that important
- Tilt common due to across wafer variation in sheath thickness
- Contamination, particle control not a strong consideration

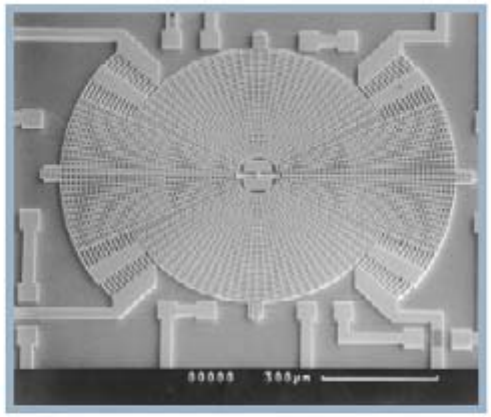
TSV needs (Via first)

- No etch stop, good etch depth control
- Single feature size
- Low open area
- Depths 50-200um
- Features need filled, PVD Barrier/Seed preferable
- Slightly tapered profile preferable
- No bowing, consistent profile
- Smooth sidewalls and no mask undercut allowed
- No tilt allowed, feature profiles need to be consistent
- Mobile ion contaminants and particle controls high

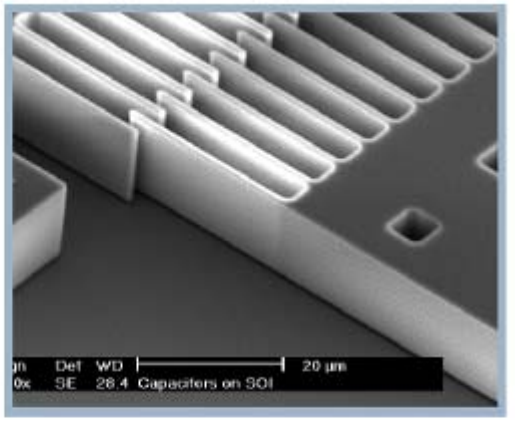
MEMS Etched features (examples)



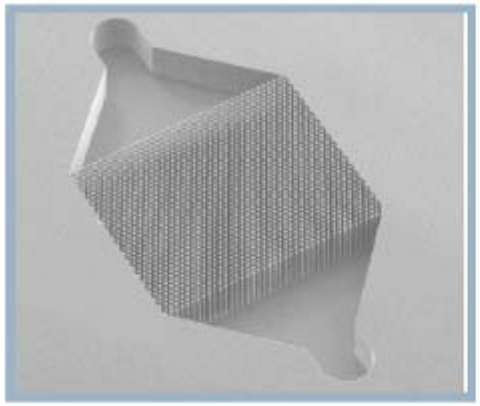
Optical MEMS and Displays



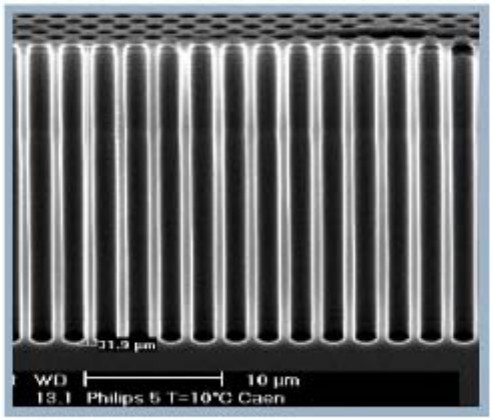
Inertial MEMS and P Sensors



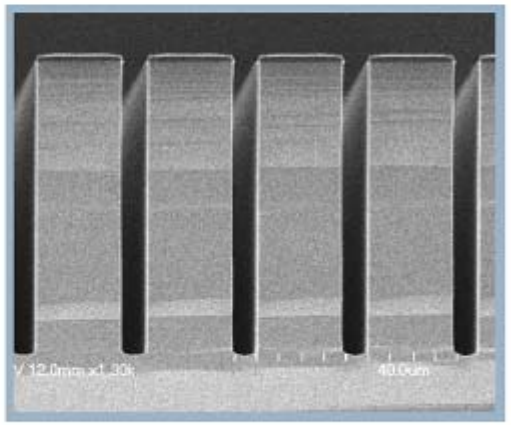
RF MEMS



Micro-fluidics and Ink Jet



Integrated Passives

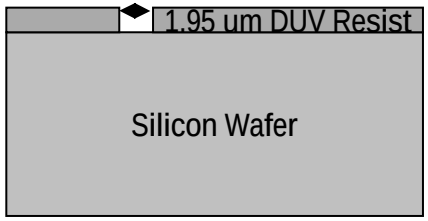


Power device Isolation

[Source: S. Lassig, STS, Suss Roadshow 2008]

Complexities with Deep Si etching

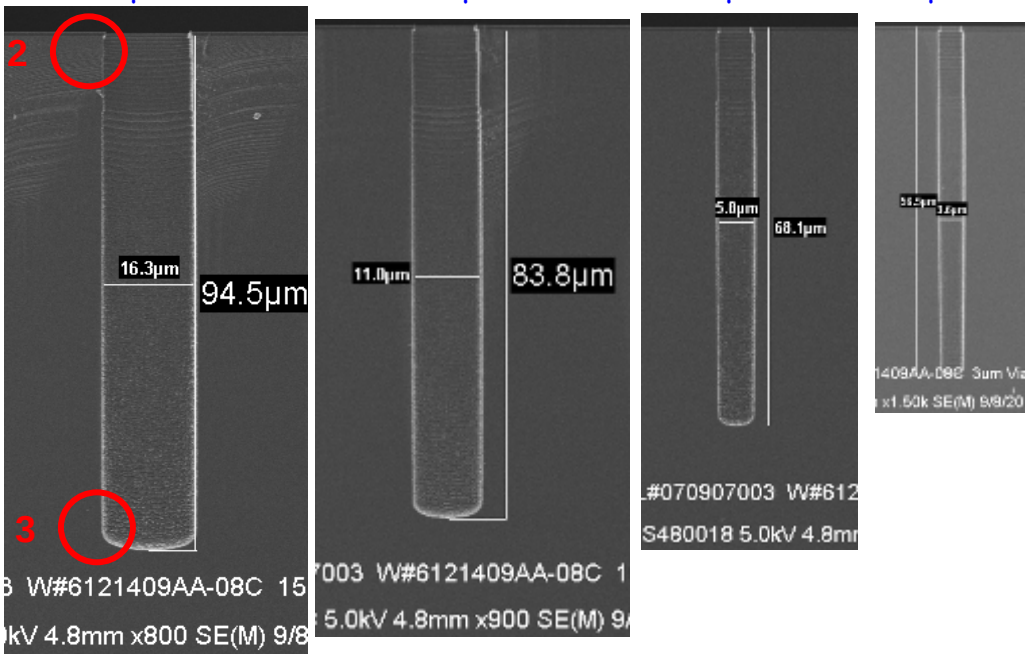
Pre-etch



Post-etch

1) Aspect ratio dependence is strong

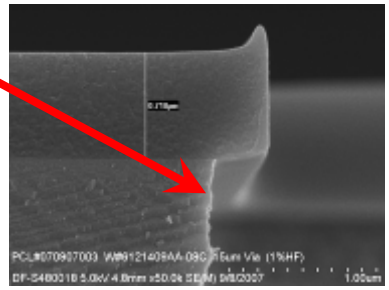
15µm 10µm 5µm 3µm CD



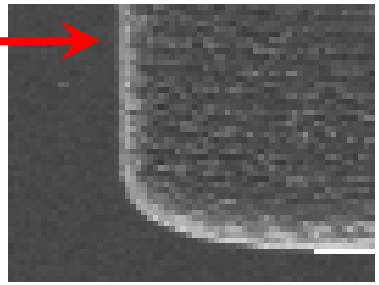
94.5µm 83.8µm 68.1µm 56.5µm Depth

2) Etch Time is very long!

3) Mask undercut



4) Sidewall Roughness



TSV Modeling– Etch rate deceleration vs. depth

- **Model the etch rate vs. time given the initial etch rate and the feature size**
- **Molecular transport regime model shows transmission decreases as a function of aspect ratio depending on geometry (Berman, 1965)**
  - **Assumes no sticking or consumption at walls**
  - **Assumes molecules come off wall surface with cosine distribution**
  - **Assumes walls are perfectly vertical**
- **Conservation of gas flux model (reaction/diffusion) is used to determine the instantaneous etch rate at varying depths given transmission coefficient (Coburn, Winters 1989)**

$$\frac{R(z/d)}{R(0)} \propto \frac{\upsilon_b}{\upsilon_t} = \frac{K}{K + S - KS}$$

K = transmiss ion coefficien t

S = reaction probabilit y

- **Evolution of depth can be determine by integration**

$$z = \int_0^t R(0)\frac{K(z)}{K(z) + S - KS}\,dt$$

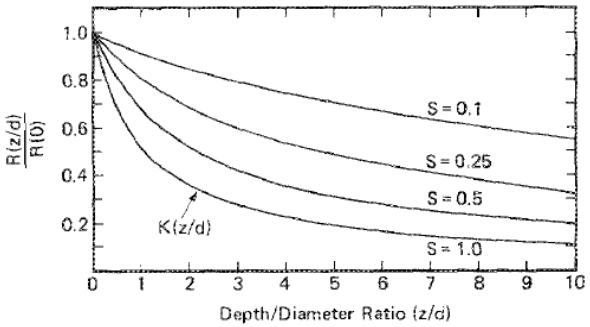
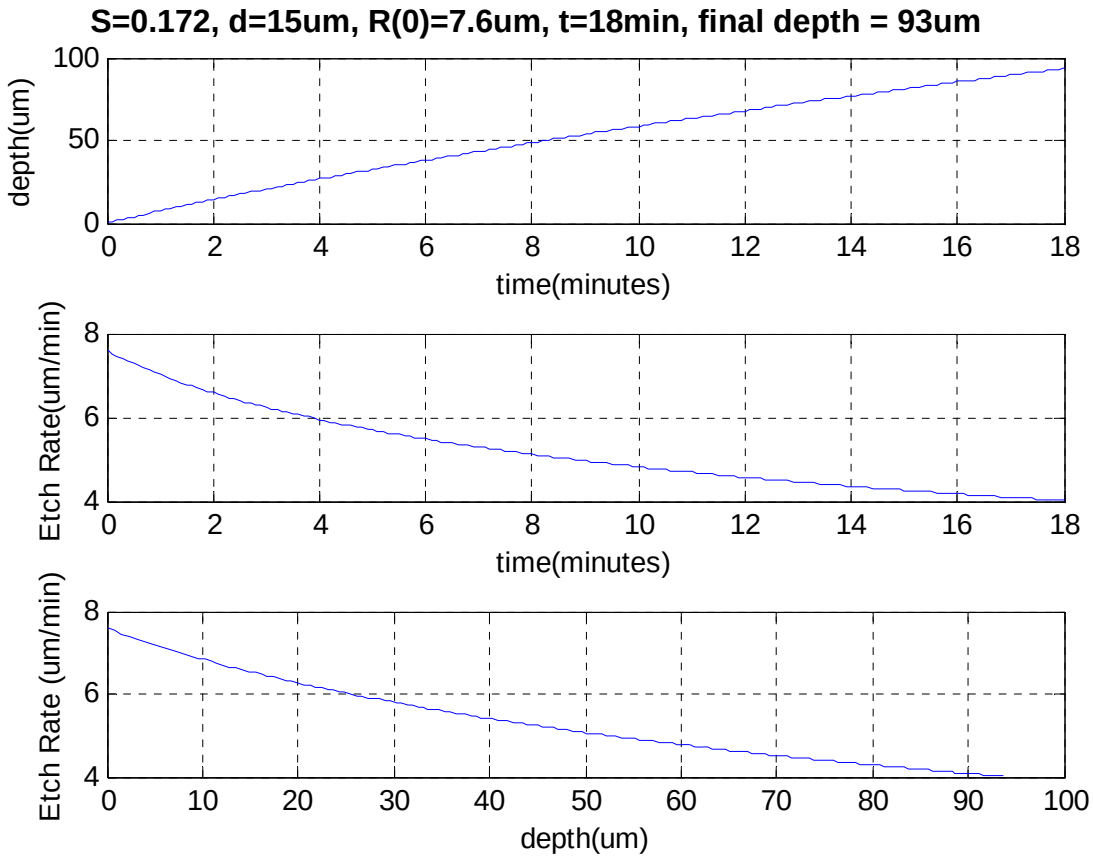


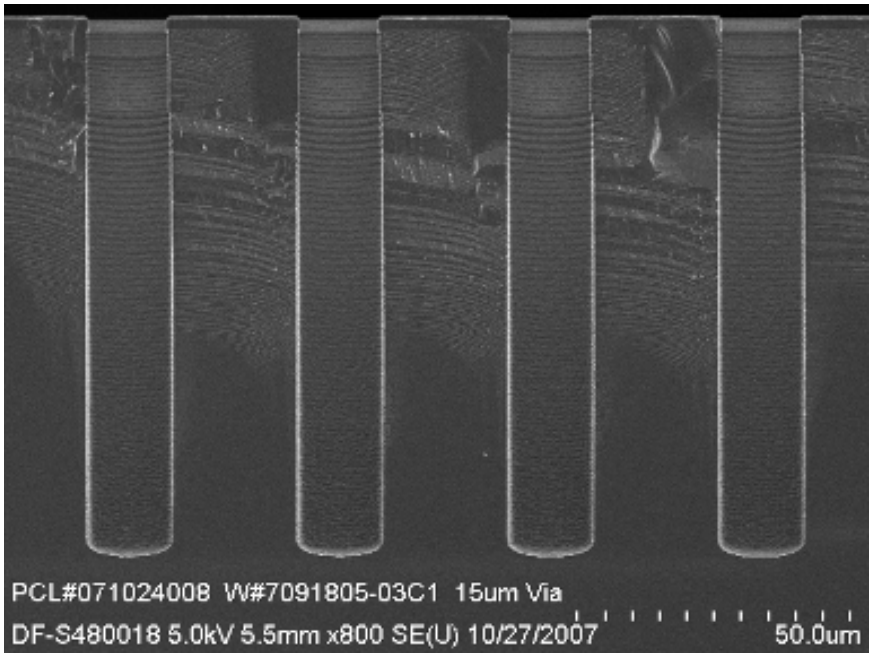
FIG. 2. Effect of the feature conductance on the instantaneous etch rate as a function of the feature aspect ratio for circular holes. The parameter S is the reaction probability of the etching species with the bottom surface of the feature. It has been assumed that the etching species are scattered diffusely from the sidewall and do not react with it.

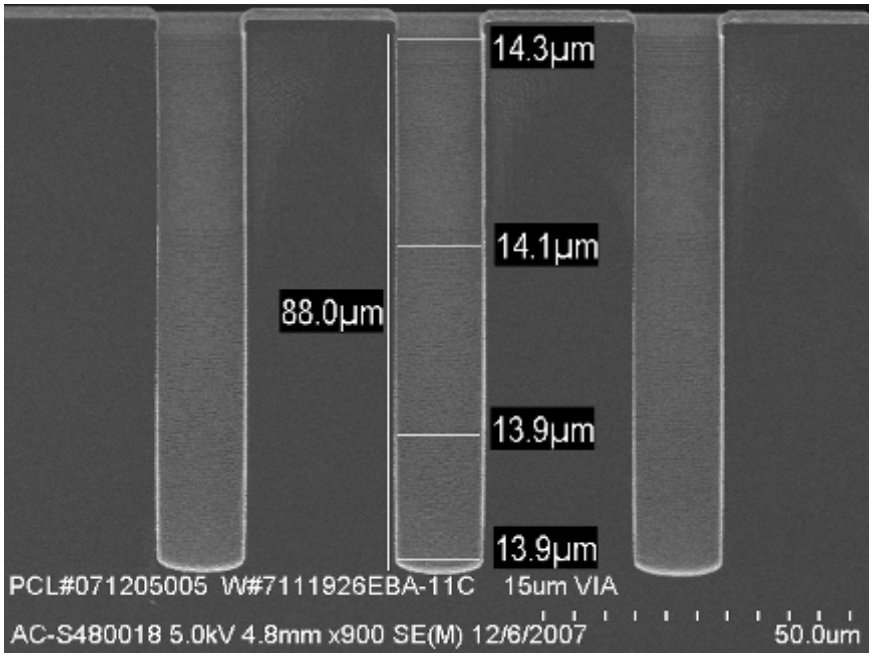
TSV Etch Depth Modeling



Fitted S=0.172 is low, so assumption of no sticking is reasonable. This model predicts the aspect ratio dependent etch characteristics reasonably well.

Poor etch profile = poor PVD coverage for Copper Barrier/Seed





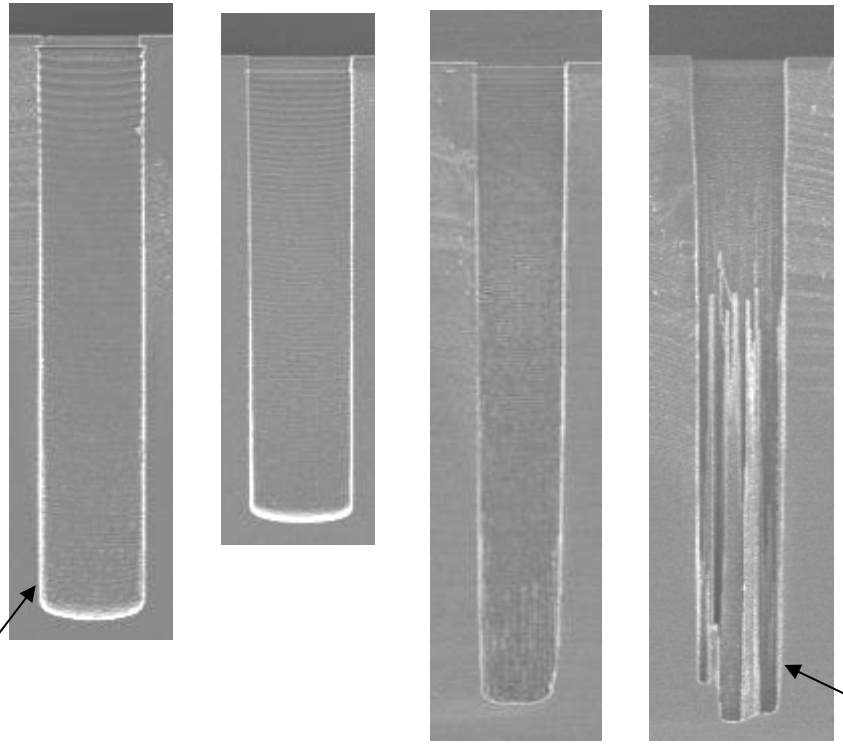
Improvements to profile needed for continuous barrier coverage:

- More tapered profile
- Reduced scallops
- Less HM undercut

Profile control thru etch/deposition steps

More etch, less deposition by recipe

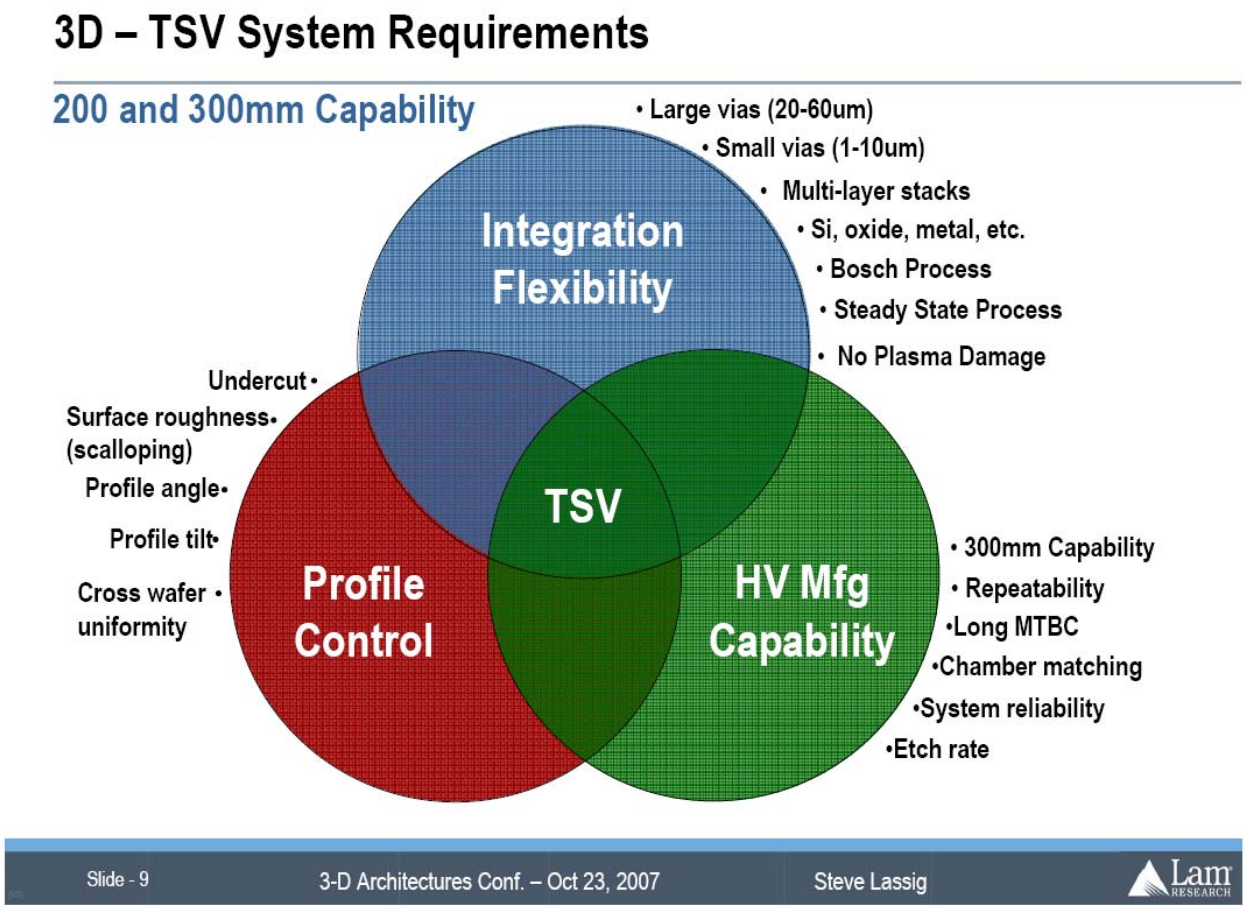
Less scalloping vs. etch depth result of higher dep/etch at bottom of feature



Scallops appear to improve as depth increases

Black Si and slower etch rate

Equipment Vendors Understand the Issues



TSV vs. STI etch comparison for manufacturability

TSV

20um CD, 100um depth

- Etch Rate = 5um/min
- Throughput <3pph
- Depreciation CoO >= $10
  - New Tool cost of $1M
- Chemicals CoO = high

STI, 130nm node

170nm CD, 5200A depth

- Etch Rate = 2800A/min
- Throughput > 15 wph
- Depreciation CoO <= $1
  - Used tool cost of ~$500k
- Chemicals CoO = low

Shown as example only: True CoO can vary widely depending on process and assumptions.

High volume manufacturing demands significant improvements to throughput to enable wider adoption of TSV -> Cost as well as footprint in fab are still issues! Also, need to find ways to improve chemicals usage from CoO and environmental standpoint.

TSV Etch throughput improvement options

- Scale down size of TSV - evolutionary
- Faster MFC switching between etch/dep steps (less time in depassivation)
- Faster etch rate at time=0 (higher decomposition)
- Faster etch rate in hole -> enhanced neutral flux to bottom of hole (alternative chemistries?)
- Batch or mini-batch reactors –> no offerings at this time

TSV Copper Electroplating

CMOS Via/Trench

- CD<=0.5um
- Depth = <=0.5um
- AR<=3
- CuSO4 + Low Acid VMS, Cu>=30g/L
- Short diffusion times for copper, additives
- Typically DC only plating
- Bottom up fill
- Small overburden
- >100% overplating
- Throughput >=30wph
- Low Cost of Ownership

TSV (Via First)

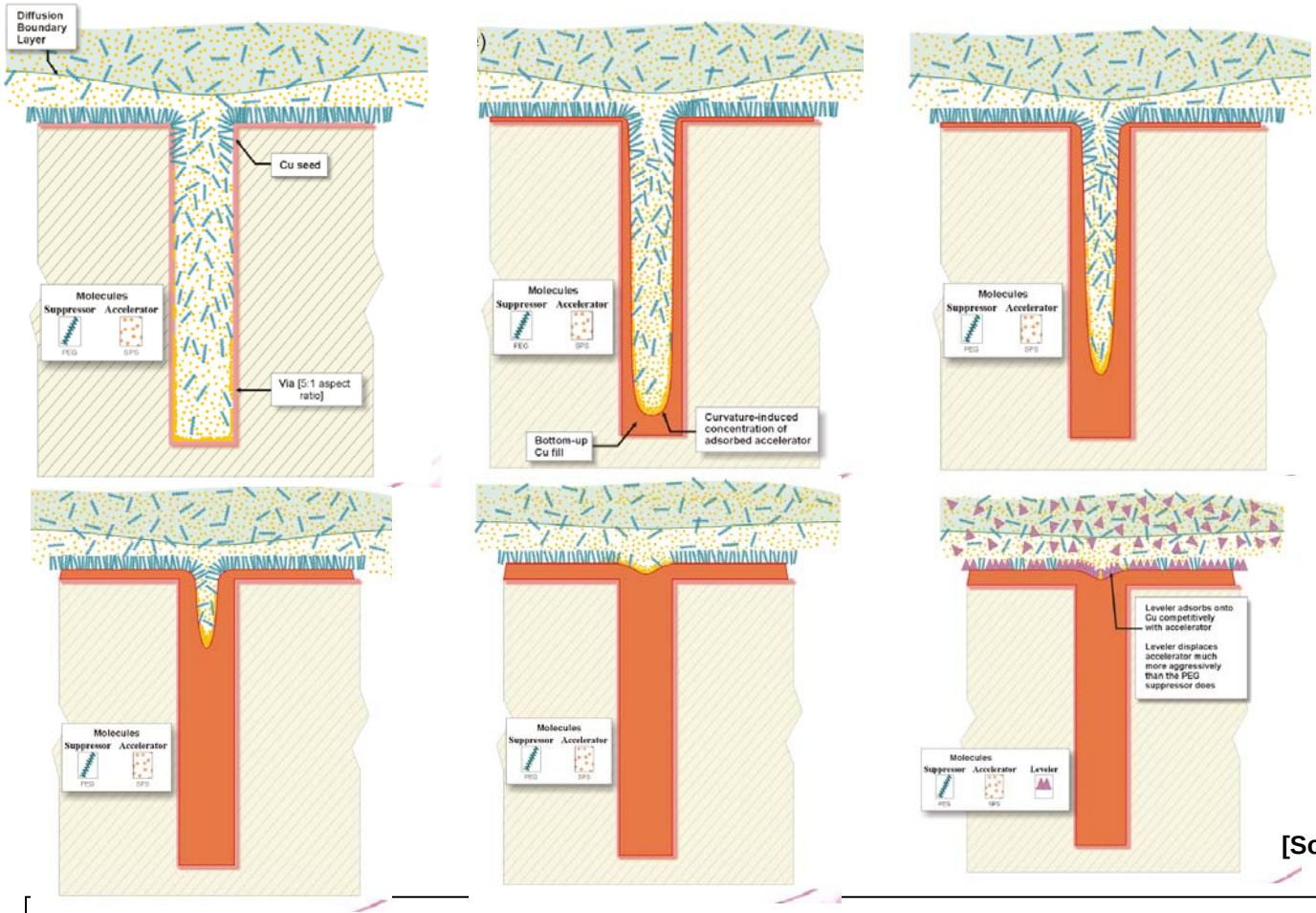
- CD = 2-50um
- Depth = 20-200um
- AR >= 3
- CuSO4 or CuMSA + Intermediate Acid VMS, Cu>=50g/L or higher desired
- Long diffusion times for Copper, additives
- DC + Reverse Pulse Plating
- Conformal + bottom up fill
- Overburden >=5um typical
- Less overplating to improve thruput, reduce overburden
- Throughput <= 1wph is common
- Cost of Ownership very high

TSV Electroplating Technical Challenges

- Initial challenges revolved around bottom up fill to create void free vias and reasonable throughput process
- Later challenges revolved around integration challenges such as Copper “Pumping” during subsequent high temperature processing
- Throughputs have improved, but are still too low for high volume manufacturing

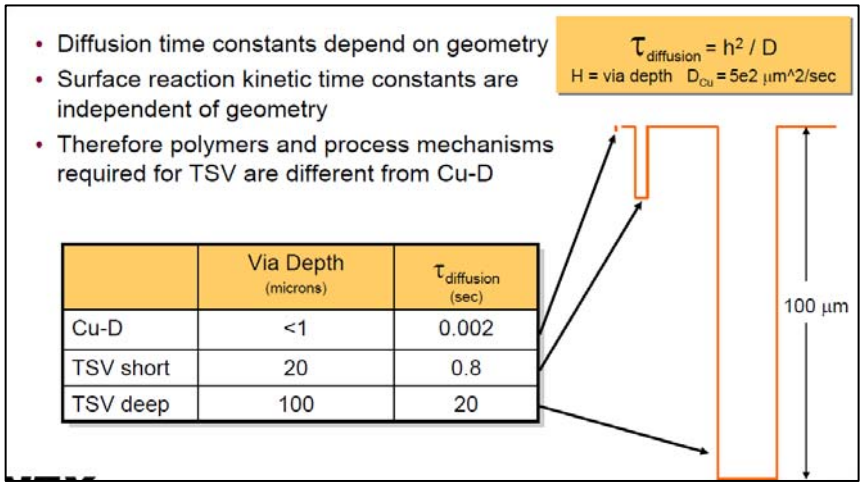
Electroplating of TSV – Same basic formula as Cu damascene plating, but…

- Fast diffusing Accelerator to enable bottom-up fill
- Slow diffusing Suppressor to prevent plating on field
- Leveler displacement of accelerator to reduce mounds



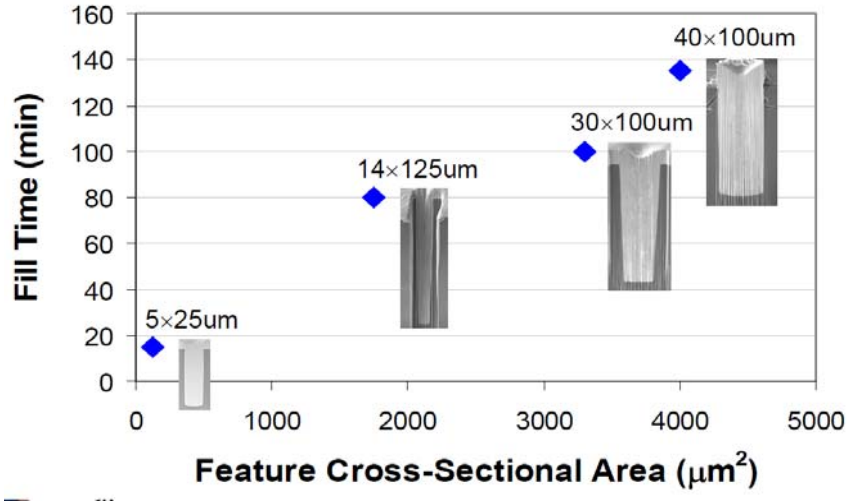
[Source: Keigler, Semicon West 2008]

Electroplating of TSV – Much longer diffusion length scales and much larger volume = low thruput!



	Via Depth (microns)	$\tau_{diffusion}$ (sec)
Cu-D	<1	0.002
TSV short	20	0.8
TSV deep	100	20

[Source: Keigler, Semicon West 2008]



[Source: Ritzdorf, EMC3D Europe 2007]

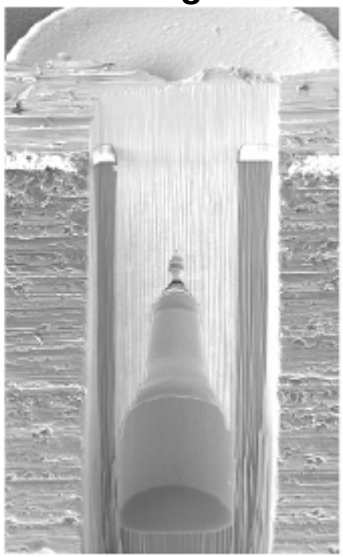
- Longer diffusion lengths combined with greater volumes leads to much lower thruputs for TSVs as compared with Damascene features
- High copper concentration helps improve

Copper Electroplating – Void Free fill

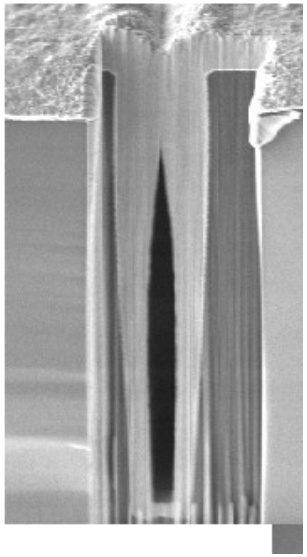
Conditions for Void Free Fill:

- Continuous Copper Seed
- Wetting of Copper solution
- Bottom-up fill capable chemistry
- Waveform control

Wetting Issue

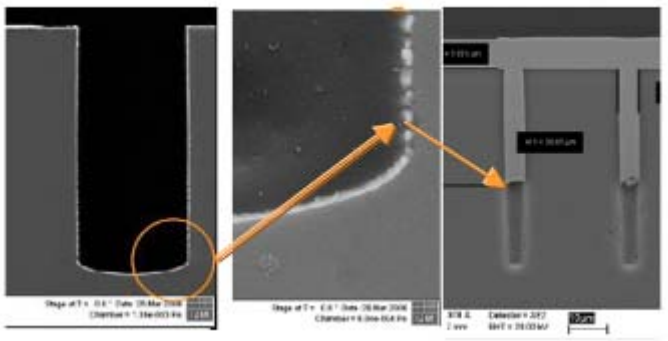


No bottom-up fill



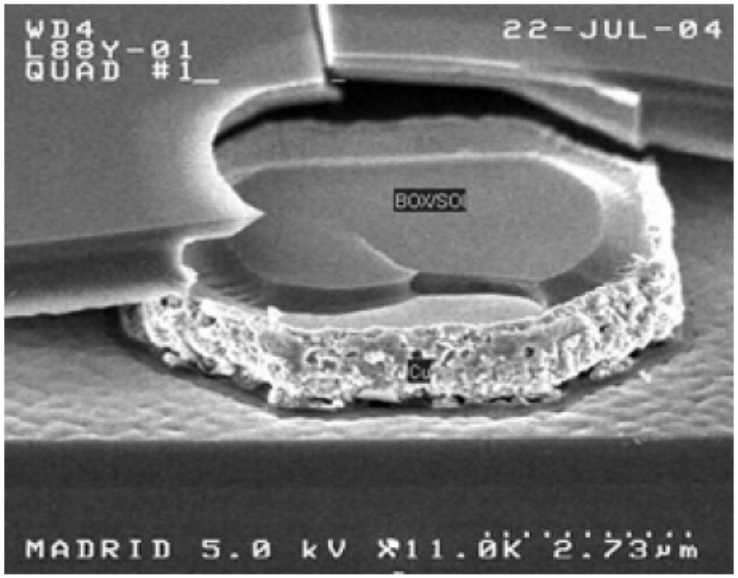
[Source: T. Ritzdorf, EMC3D Europe 2007]

Discontinuous Seed

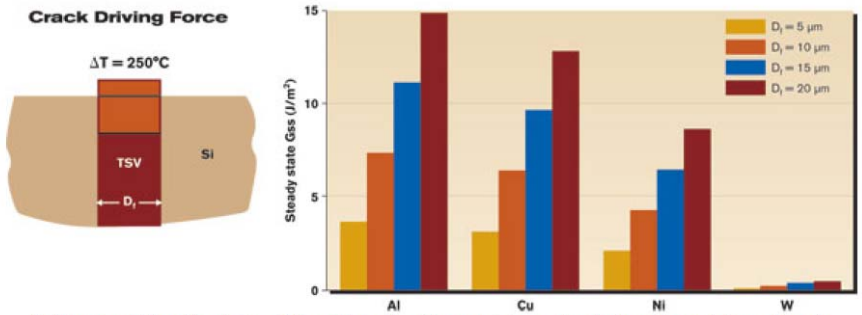


[Source: A. Uhlig, Sematech Workshop 9/2008]

TSV Electroplating – Copper “Pumping”



[Source: Tezzaron (as cited in P. Garrou, Semiconductor Intl. 2010)]



2. Tungsten TSV, with a better CTE match to the silicon matrix, creates far less thermal stress than do aluminum, copper or nickel. (Source: University of Texas)

[Source: Ho (as cited in P. Garrou, Semiconductor Intl. 2010)]

- What? Plastic deformation of Copper TSV leading to pump up effect during high temperature post-TSV processing
- IMEC disclosed solution (SI 3/10): proper anneal to stabilize Cu during high temperature processing
- Paul Ho (Univ. of Texas) group has studied thermal stresses in TSVs and has proposed mechanisms for delamination and subsequent “pumping” of copper and suggests improvements with lower CTE mismatch materials like W or Ni.
- IBM reported reliability issues that led it to move from Cu to W for its first production process.

How to assess process technology options and successfully implement?

- Identify device roadmap need that may be effectively met by alternative process technology
- Carefully consider and plan for technical challenges associated with crossing over process technologies up front to determine timeline/cost of development
- Compare costs/performance of alternatives (cost is king!)
  - For example, MEMS, 3DIC, passives integration to chip -> competition is often between packaging solution and wafer-based solutions
    - Which provides better performance?
    - Which provides lowest cost?
    - Cost tradeoffs for wafer level solutions are favorable for smaller die size ($300/wafer cost adder = ~$.01/die for 1mmx1mm, ~$1 for 10mmx10mm, not taking into account yield loss)
- Note: Implementation of new process technologies is easier/faster in modular way
  - For example, building TSVs as bolt-on to existing technology is faster/easier/cheaper than requiring a new technology that incorporates TSVs

Conclusions

- Process technologies have exploded across the various segments of consumer electronics
- Market demands are pushing further integration and intersection of these segments
- TSV/3DIC has exemplified new technical challenges that arise when applying “mature” process technologies in new/different ways…in addition to challenges of cost/manufacturability
- Many more opportunities exist, but need to evaluate carefully for need, cost, and difficulty to implement