Comprehensive Characterization of B⁺ Implanted Silicon after Rapid Thermal Annealing

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Outline

- Objectives: Visualization of Invisible Si Material Properties
 - Surface
 - Interface
 - Bulk
 - Defects
 - Charge Distribution
 - Stress/Strain
 - Band Bending
- Experiment:
 - Implanted Wafers
 - ¹¹B⁺ 1keV 1x10¹⁵ atoms/cm²
 - RTA System (Hot Wall System)
 - Resistively heated single wafer rapid thermal furnace (SRTF)
 - Annealing Conditions
 - Temperature: 850°C~1050°C
 - Time 30s~180s (Residence time in SRTF)
 - 1s~150s (Equivalent soak time in lamp-based RTP)
 - Atmosphere: 1 atm, N_2
 - Multiwavelength Room Temp. Photoluminescence (RTPL)
- Results and Discussions
- Prospects





Band Structure of Semiconductors



Detailed Information Needed for Proper Interpretation





PL Mapping Examples (SiO₂/Si)

SiO₂/Si Interface Quality Monitoring





MPL-300: Multiwavelength Photoluminescence

Multiwavelength Photoluminescence Spectroscopy: The most direct way to measure band-gap energies, dopant activation, electrically active defects, plasma induced damage (PID), dielectrics/Si interface quality, metal contamination which affect minority carrier lifetime and electron mobility characteristics of the semiconductor.



Single Wafer Rapid Thermal Furnace (SRTF)

Hot Wall RTA Process Chamber



Wafer Temperature Profile





Boron Diffusion from Limited Source after RTA















Stress Induced Property Change

(a) As Received

Free Standing in Container



Tightly Closed Lid with Washer

(b) Stressed for 3 days



(c) RTPL Mapping & Line Scan Direction



Si Wafer Diameter: 50 mm Edge Exclusion: 3 mm Intervals: 500 µm in X and Y Directions Measurement Points: >6000 Points Excitation Wavelength: 830 nm Exposure Time: 500 ms/point



C O

Distance from Y-axis (mm)

RTPL Line Scan (51 Points)

Stress Induced Property Change

(a) As Received

Free Standing in Container



Tightly Closed Lid with Washer

(b) Stressed for 3 days



(c) RTPL Mapping & Line Scan Direction



Si Wafer Diameter: 50 mm Edge Exclusion: 3 mm Intervals: 500 µm in X and Y Directions Measurement Points: >6000 Points Excitation Wavelength: 830 nm Exposure Time: 500 ms/point



C O

Distance from Y-axis (mm)

RTPL Line Scan (51 Points)

Stress Induced Property Change









650nm/827nm PL Mapping Results





Slot 01: Reference Si Slot 02: DOP Vapor 7 Days Slot 03: DOP Vapor 7 Days Slot 04: DOP Vapor 14 Days Slot 05: DOP Vapor 14 Days Slot 05: DOP Liquid Slot 06: DOP Liquid Slot 08: XRR + XRF Slot 09: XPS Slot 10: WDXRF

650nm Excitation PL Area Mapping

Slot 08: XRR+XRF



10mm x 10mm in 100um intervals

Slot 09: XPS



Slot 01: Reference Si Slot 02: DOP Vapor 7 Days Slot 03: DOP Vapor 7 Days Slot 04: DOP Vapor 14 Days Slot 05: DOP Vapor 14 Days Slot 05: DOP Liquid Slot 07: DOP Liquid Slot 07: DOP Liquid Slot 08: XRR + XRF Slot 09: XPS Slot 10: WDXRF



PL Wafer Mapping Results





Photoluminescence (PL) vs. Surface Photovoltaic (SPV)







Rs and PL Spectra from Implanted Si after RTA



Brightness: Overall Ariel Intensity



Spectra: Intensity Distribution in Wavelength Domain



650nm Excitation PL, 500ms Exposure



785nm Excitation PL, 500ms Exposure





Multiwavelength PL Mapping Results after Non-contact Corona-based C-V and I-V Measurements







Multiwavelength PL Mapping Results after C-V and I-V Measurements



Multiwavelength PL Mapping Results after UV-Based Film Thickness Measurements









Properties of Native Oxide/Si Interface after Electrical Breakdown

(a) HVDC Arc 2000V DC, ~1000 ms

(b) Piezo Ignition Arc ~4000V Pulse, ~1 ms



