Atomic Level Material and Device Analysis for FinFET and Nanowire Design

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July 13, Junction Technologies User Group Meeting
How Many Atoms Are We Talking About?

- Number of atoms per transistor is reducing by ~30% per generation
- At that pace, transistor can be scaled for another couple of decades before approaching variability & leakage limits
Definition of “Ab initio” Modeling Approach

Ab initio

From Wikipedia, the free encyclopedia

For other uses, see Ab initio (disambiguation).

Ab initio (IPA: /æbrɪˈnɪʃə/ AB-ɪ-NISH-ee) is a Latin term meaning "from the beginning" and is derived from the Latin ab ("from") + initio, ablative singular of initium ("beginning").

Science and engineering

A calculation is said to be ab initio (or "from first principles") if it relies on basic and established laws of nature without additional assumptions or special models. For example, an ab initio calculation of the properties of liquid water might start with the properties of the constituent hydrogen and oxygen atoms and the laws of electrostatics and quantum mechanics. From these basics, the properties of isolated individual water molecules would be derived, followed by computations of the interactions of larger and larger groups of water molecules, until the bulk properties of water had been determined.
**Ab initio Analysis Approaches vs Structure Size**

- **PDEs & ODEs**
- **SPICE**
- **TCAD**
- **Atomistic**
- **Force Field**
- **Tight Binding**
- **LCAO**
- **Ab initio**
  - Plane-wave
  - Plane-wave with Hybrid Functional
  - Plane-wave with GW

### Practical maximum structure size
- **Logic block**
- **Transistor & small cell**
  - ~1,000,000 atoms
  - ~100,000 atoms
  - ~10,000 atoms
  - ~300 atoms
  - ~100 atoms
  - ~20 atoms

### Complexity
- **Modeling demand**
- **Circuit**
- **Whole transistor**
- **Piece of transistor**
- **Bulk**
- **Ref.**

### Realm of periodic structures
- **Structure size**

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Outline

Ab-initio analysis

Emerging memory: ReRAM, PCM, OTS, ...

TCAD

Manufacturing & Design

Process flow
Design rules
BSIM
Parasitic RC

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Design rules
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Parasitic RC

HKMG: Vt, band structure, ...
Ferroelectrics and NCFET
Carrier transport thru dielectrics
Dopant diffusion and activation
Dopant diffusion and activation in thin layers
Chemical reactions in Epi, ALD, ALE
Contact resistance: MIS, silicide, melt
Dopant diff. in bulk material
Extended defects
Interconnects: barriers, EM
Collapse of fins and pillars
NEGF: DFT, TB, K.P, EMA
Carrier transport thru dielectrics
Plasma etch damage in low-k & Si

Surface roughness
Channel material
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Ferroelectrics and NCFET

Dopant diffusion and activation
Dopant diffusion and activation in thin layers
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# Pattern Collapse Mechanisms

<table>
<thead>
<tr>
<th>Capillary forces at wet cleaning</th>
<th>Push-pull during STI densification</th>
<th>Thermal mismatch stress</th>
<th>Zipping effect during deposition</th>
</tr>
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</table>

- **Capillary forces at wet cleaning**
- **Push-pull during STI densification**
- **Thermal mismatch stress**
- **Zipping effect during deposition**
Pattern Bending Due to Zipping Effect

Layer deposition over a patterned structure
Pattern Bending Due to Zipping Effect

Let's zoom into the interesting part and look at it on atomistic scale.
Pattern Bending Due to Zipping Effect

Atomistic amorphous oxide

Full scale structure
Molecular Dynamics: Zipping of the $8^\circ$ Oxide Gap

Timeline: initial
Molecular Dynamics: Zipping of the $8^\circ$ Oxide Gap

Timeline: initial  intermediate
Molecular Dynamics: Zipping of the $8^\circ$ Oxide Gap

Timeline: initial  intermediate  final
Molecular Dynamics: Zipping of the 8° Oxide Gap

Interaction starts with Van der Waals bonds, and eventually switches to covalent bonds.
Molecular Dynamics: No Zipping of the 10° Oxide Gap

Timeline: initial  intermediate  final
Molecular Dynamics: No Zipping of the 10° Oxide Gap

Timeline: initial  

No zipping, just a few bonds at the bottom of the gap
Interaction of the Oxide Layers vs Gap Width

Potential Energy for SiO2 ‘walls’

Force between SiO2 ‘walls’
Interaction of the Oxide Layers vs Gap Width

Two attraction peaks at 3.4 Å and at 1.9 Å

Sweet spot at 0.8 Å

Repulsion below 0.8 Å
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Advanced Electron Transport

- Drift-Diffusion
- Full band Boltzmann
- Sub band Boltzmann
- Effective mass NEGF
- K.P. NEGF
- T.B. NEGF
- Ab initio

Requires calibration to advanced transport

Predictive power

Structure size & Modeling speed

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Ballistic ratio keeps improving with scaling.

And projected to improve towards 2nm design rules for FinFET or nano-slab.

One important side effect is that fundamental physics plays increasing role, and there’s less need for calibration.
• Ballistic ratio keeps improving with scaling
• And projected to improve towards 2nm design rules for FinFET or nano-slab
• One important side effect is that fundamental physics plays increasing role, and there’s less need for calibration
Quasi-Ballistic Electron Transport

- Ballistic ratio keeps improving with scaling
- And projected to improve towards 2nm design rules for FinFET or nano-slab
- One important side effect is that fundamental physics plays increasing role, and there’s less need for calibration
Modeling S/D Contact Resistance (G. Pourtois, IMEC)

• Fundamentals
  • Today: \(~1 \times 10^{21} \text{e}/\text{cm}^3 \rightarrow 2 \times 10^{-9} \ \Omega \cdot \text{cm}^2\)
  • Can we reach \(10^{-10} \ \Omega \cdot \text{cm}^2\)?
  • Is there a theoretical limit to it?

• A few practical difficulties:
  TiSi\(_x\) crystallites in a-TiSi alloy

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**Graph:**
- **Contact resistivity (\(\Omega \cdot \text{cm}^2\))**
- **Si:P-3E20**
- **No PAI**
- **PAI1**
- **RTP temperature (°C)**
  - A 3keV
  - B 600°C

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**Figure:**
- **TiSi\(_x\) crystallites in a-TiSi alloy**
- **EOR defects**
- **Defect-free bulk**

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**[1] Yang, JAP 98, 034302, 2005**

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**How do we model this?** → **Atomistic simulations**
How to Get Amorphous Material? (G. Pourtois, IMEC)

“melt & quench” process

Initial: crystal

Crystal TiSi

10% relaxed crystal

Melted TiSi

10% melt shrink

Quenching

Final: amorphous
The Si body should be at least 4 nm thick @ $1 \times 10^{20} \text{ } \text{ } |e|/\text{cm}^3$ To account for a proper depletion length
**Models (G. Pourtois, IMEC)**

- Probing different interface topologies

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**Avatar (movie 2009) resources:**
- 34 racks, each 4 chassis, 32 machines each
- 40,000 processors, 104 terabytes of memory
- 4 cores processors \(\rightarrow\) 160,000 cores
- Run time: \(\sim\) 3 hours, i.e. 480,000 core-hours

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**CPU Resources used for this project:**
- Total CPU usage so far: 453,120 core-hours
- Similar to Avatar movie
n-Si[100]|a-TiSi (G. Pourtois, IMEC)

Doping: n-1xe\textsuperscript{20} |e|/cm\textsuperscript{3}

Doping: n-3xe\textsuperscript{21} |e|/cm\textsuperscript{3}

- 10\textsuperscript{-10} \text{\Omega cm}^2 is possible with high doping and by matching metal/semi effective carrier masses
- Good agreement with Si data

What do we learn?

- 10\textsuperscript{-10} \text{\Omega cm}^2 is possible with high doping and by matching metal/semi effective carrier masses
- Good agreement with Si data

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Vt Eng: Material Modification

- Vt is modulated through trace element control in gate.
- Effectiveness increases for layers closer to HK.

S. Hung at IEDM 2017 short course
Hi-K Metal Gate: Vt Tuning, Traps, Variability

- One transistor contains millions of atoms, too much for atomistic models to handle
- So, we split it into several samples where we can apply atomistic analysis

届毕业生

Intel’s 22nm FinFETs, SEM by Chipworks @2013
Atomistic Analysis of the Multi-Layer Gate Stack

• HKMG:
  – Many layers of metals and dielectrics
  – Complicated bandstructure
  – Surface roughness
  – Tunneling
  – Traps

Goal: predict and engineer device behavior such as $V_t$ tuning, variability, traps, electron transport, leakage

HKMG: stack of thin layers
HKMG Modeling approach

• Molecular dynamics: empirical pseudopotentials or DFT
  – Melt-and-quench to obtain amorphous materials
  – Optimization of interface atomic configurations
  – Atomic positions are used as an input for electronic calculations

• Electronic calculations: DFT-NEGF
  – Band structure in the fin
  – Work function, barriers, local DOS across the stack
  – Tunneling through the stack
  – Extract essential properties for transistor scale analysis
Case study: W/aTiN/aHfO2/aSiO2/Si/aSiO2/aHfO2/aTiN/W
Atomistic Analysis of NCFET (Pawel Lenarczyk, ETH, Zurich)

non-polar: $P = 0$

polarized: $P = 0.22 \text{Cm}^{-2}$

Material behavior

<table>
<thead>
<tr>
<th>spontaneous polarization [cm$^{-2}$]</th>
<th>calculated</th>
<th>experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.25</td>
<td>0.22</td>
</tr>
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Device behavior

- $c/a=1$
- $c/a=1.05$
- $c/a=0.95$

60mV/dec
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Si Stacking Fault DFT Analysis (A. Pourghaderi, Samsung)

Type B

Type C

Green color for is for guiding the eyes only (not dangling bonds)
Si Stacking Fault DFT Analysis (A. Pourghaderi, Samsung)

Type C

Shape of wavefunctions

- Localized near the crossing point of stacking faults
- Bulk-like wavefunction (inside cond. band)

Green: pristine silicon bandstructure
Red: bandstructure of Si with crossing stacking fault

DFT calculation details
Quantumwise GGA-PBE exfunctional
SingleZeta basis function (minimal)
(in relaxation calculation) Force criterion: 0.05eV/A
Number of atoms in each structure:
Type B and type C: 2,808 (4 unitcell thick in z direction)
TAT: Relaxation within 3~5 days using 144 cpu cores

IDS (a.u) vs. VGS (V)
Type B results match the leakage level & floor in HW
Plasma Etch Damage Analysis: Fluorine Hitting Silicon

Timeline: initial

Bombarding Si by F⁺ ions
Plasma Etch Damage Analysis: Fluorine Hitting Silicon

Timeline: initial

Bombarding Si by F⁺ ions

Timeline: intermediate

Molecular dynamics analysis of accumulating damage
Plasma Etch Damage Analysis: Fluorine Hitting Silicon

Timeline: initial

Bombarding Si by F⁺ ions

Timeline: intermediate

Molecular dynamics analysis of accumulating damage

Timeline: final

Several nm of Si are damaged and contaminated
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Summary

• Increasing number of technology issues require understanding on atomic level to enable material engineering and transistor design

• Thin layers (below ~5nm) exhibit different properties than bulk material and can only be accurately analyzed by atomic methods

• We reviewed application of *ab initio* analysis tools to characterize some of the major technology issues