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Silicon to Software™

Atomic Level Material and Device Analysis for FinFET and Nanowire Design

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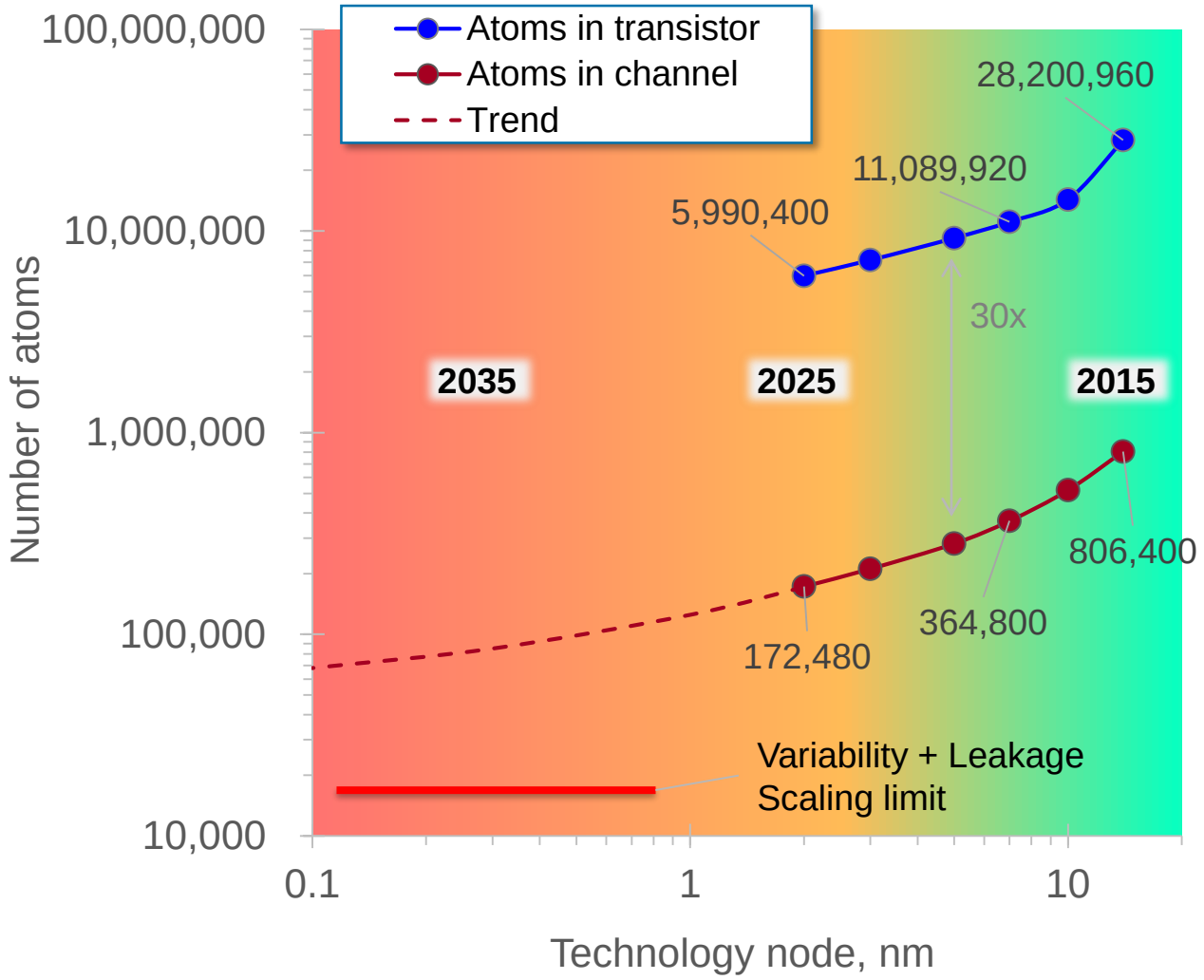
Munkang Choi, and Alexei Svizhenko

July 13, Junction Technologies User Group Meeting

How Many Atoms Are We Talking About?



- Number of atoms per transistor is reducing by ~30% per generation
- At that pace, transistor can be scaled for another couple of decades before approaching variability & leakage limits

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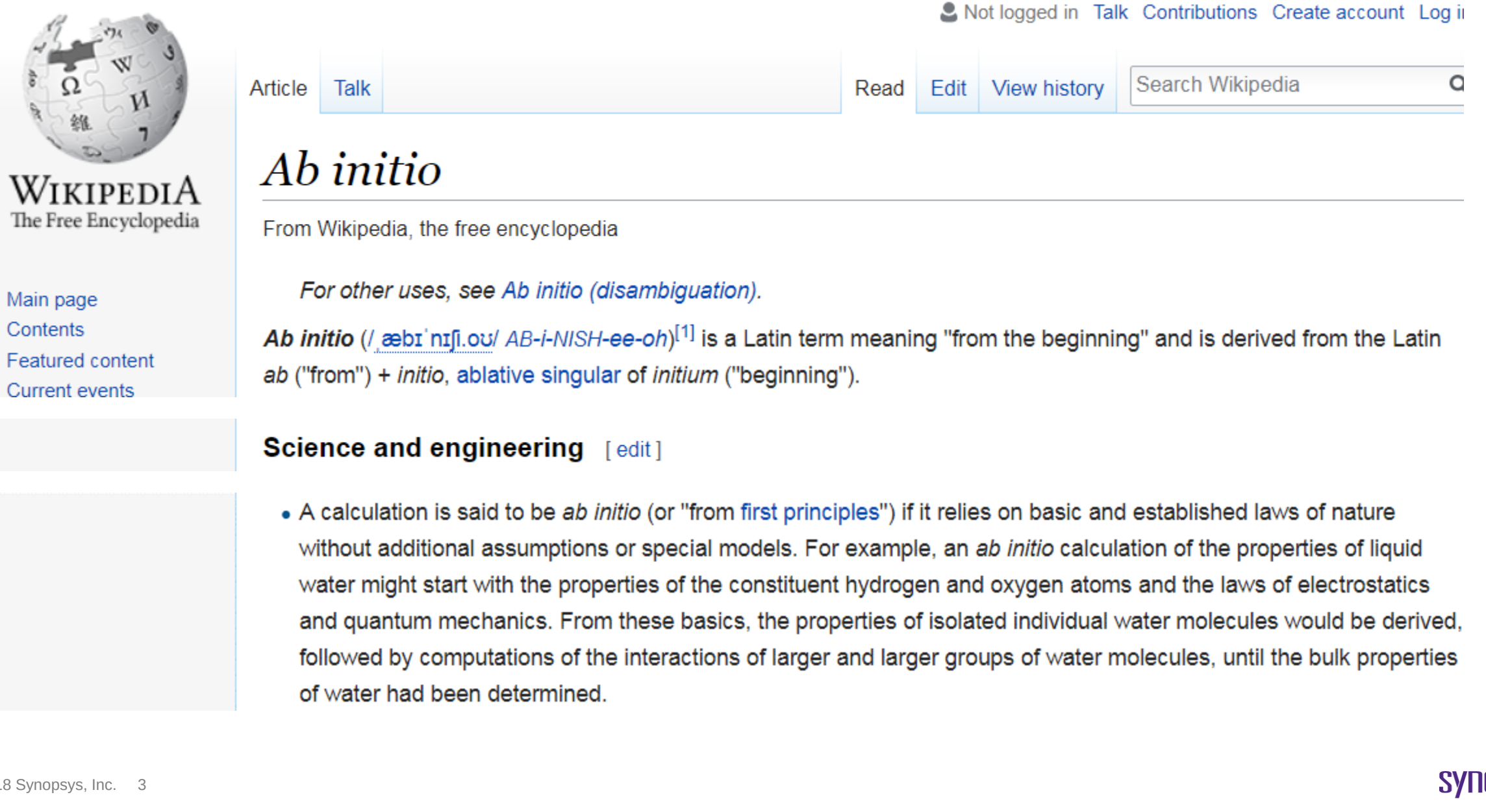
Definition of "*Ab initio*" Modeling Approach



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Ab initio

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For other uses, see Ab initio (disambiguation).

Ab initio (/ˌæbɪˈnɪʃi.oʊ/ *AB-i-NISH-ee-oh*)[1] is a Latin term meaning "from the beginning" and is derived from the Latin *ab* ("from") + *initio*, ablative singular of *initium* ("beginning").

Science and engineering [edit]

- A calculation is said to be *ab initio* (or "from first principles") if it relies on basic and established laws of nature without additional assumptions or special models. For example, an *ab initio* calculation of the properties of liquid water might start with the properties of the constituent hydrogen and oxygen atoms and the laws of electrostatics and quantum mechanics. From these basics, the properties of isolated individual water molecules would be derived, followed by computations of the interactions of larger and larger groups of water molecules, until the bulk properties of water had been determined.

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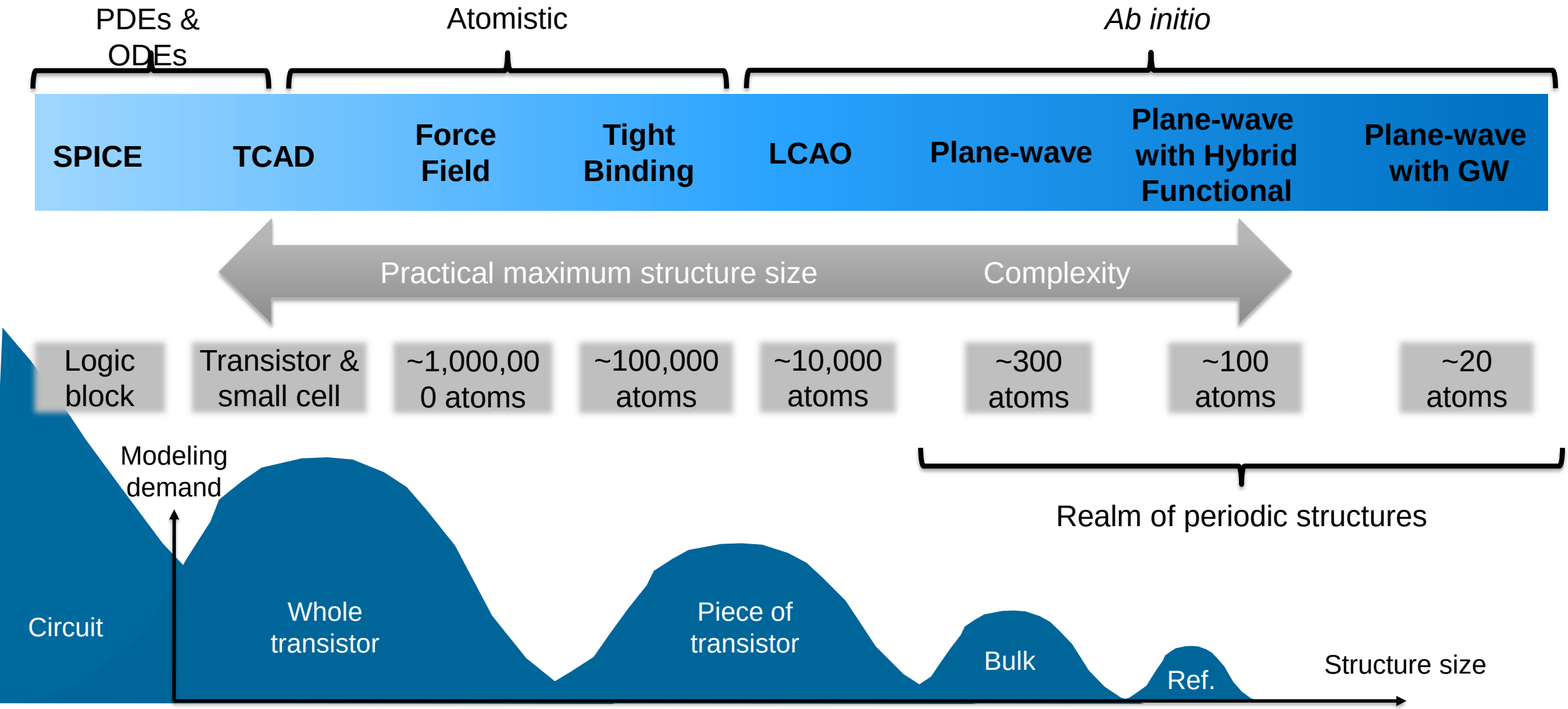
Ab initio Analysis Approaches vs Structure Size



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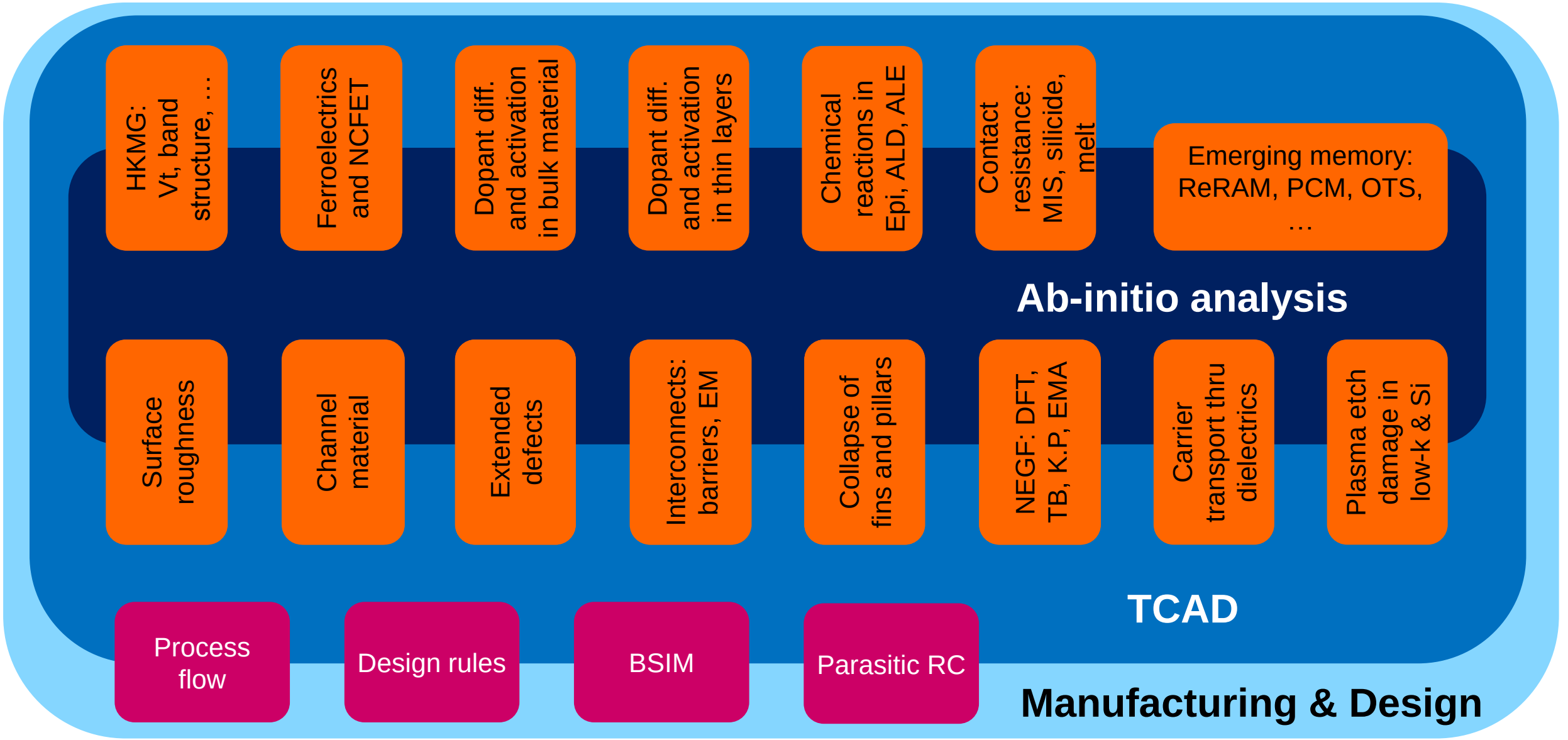
Outline



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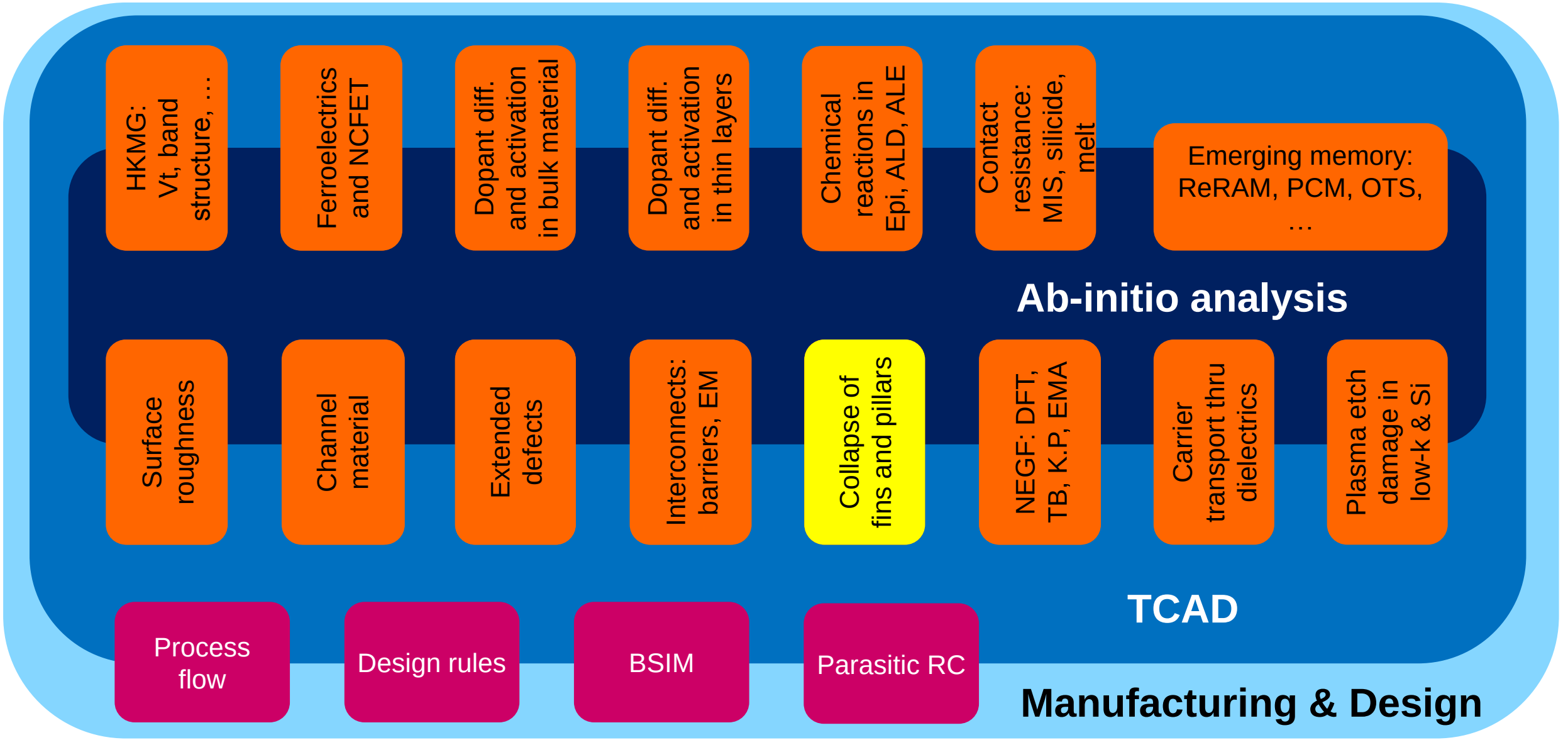

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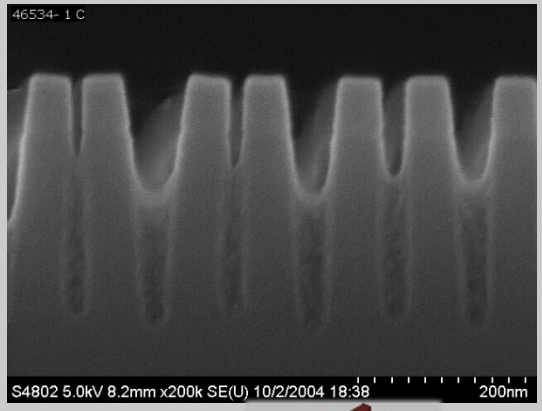
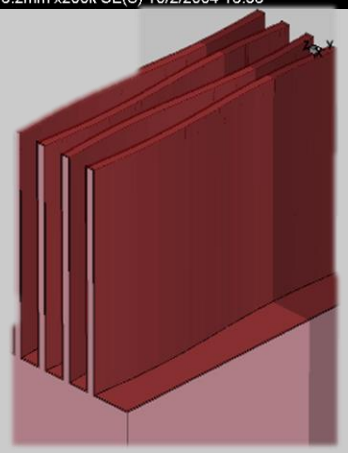
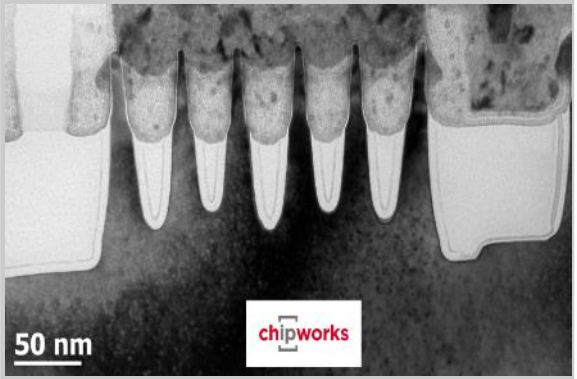
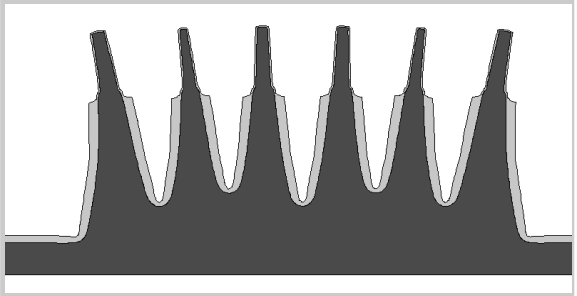
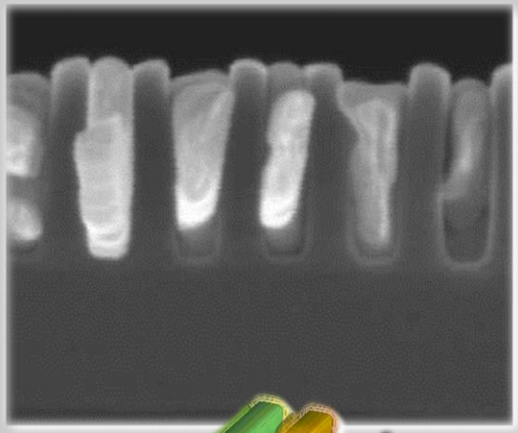
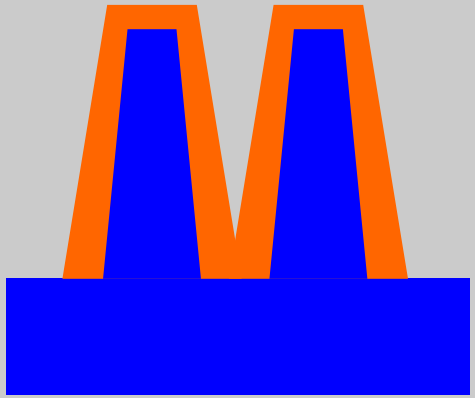
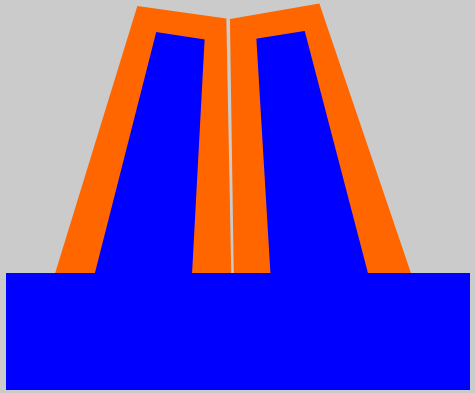
Pattern Collapse Mechanisms

Capillary forces at wet cleaning	Push-pull during STI densification	Thermal mismatch stress	Zipping effect during deposition
 	 	 	 

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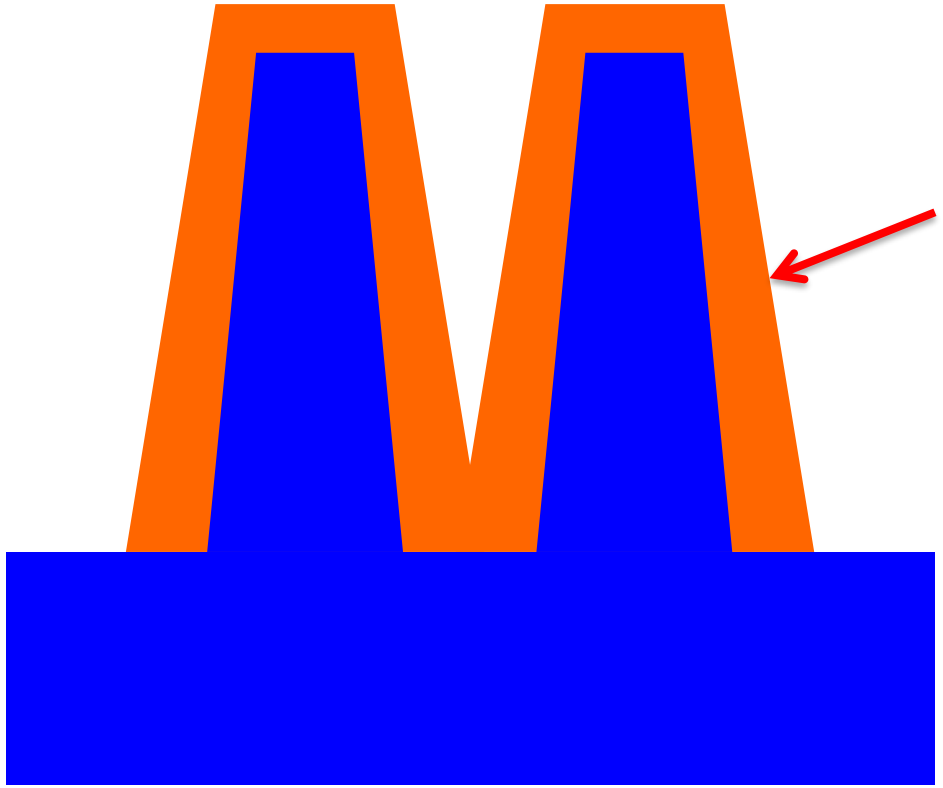
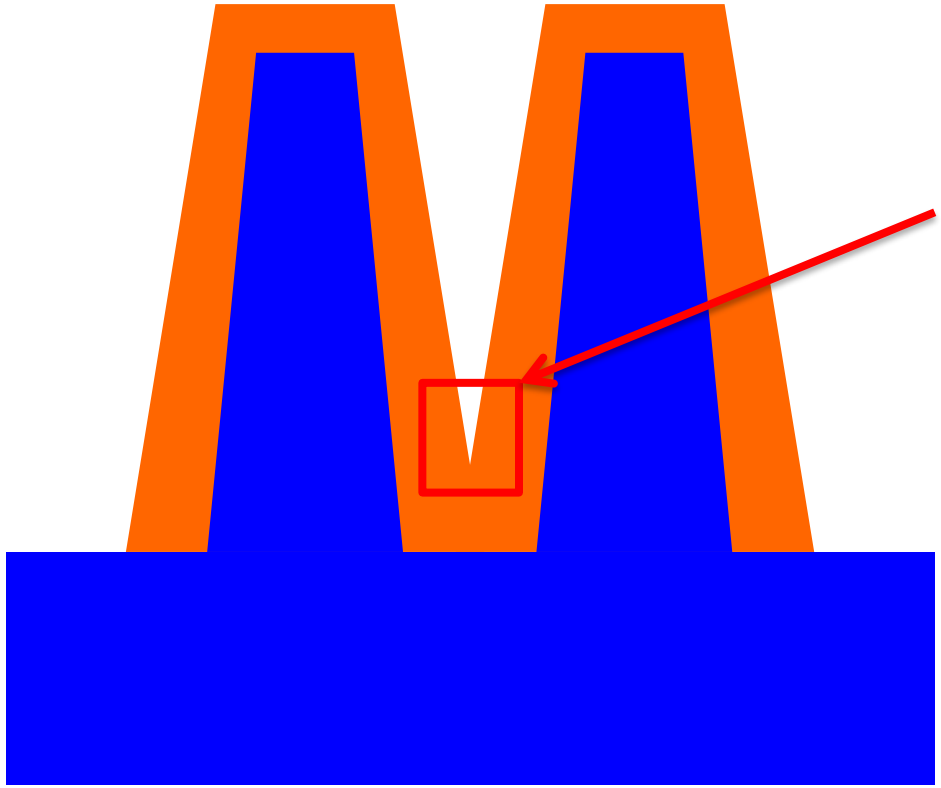
Pattern Bending Due to Zipping Effect



Layer deposition over a patterned structure

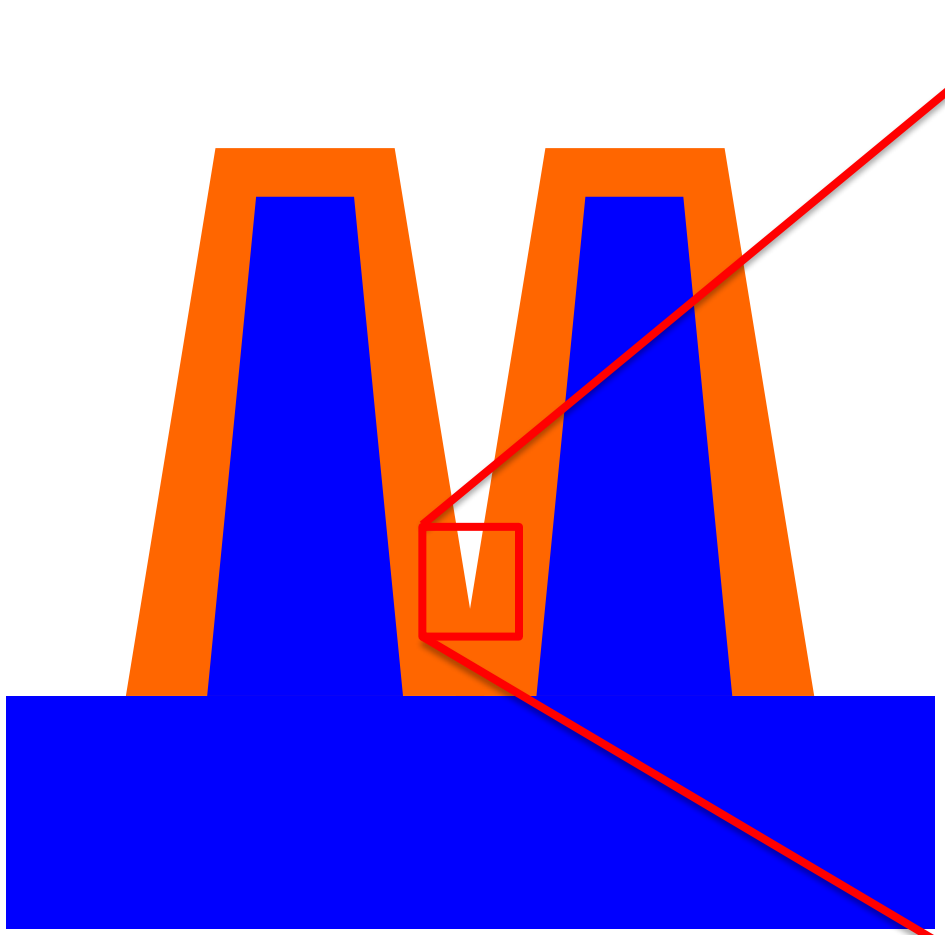
Pattern Bending Due to Zipping Effect



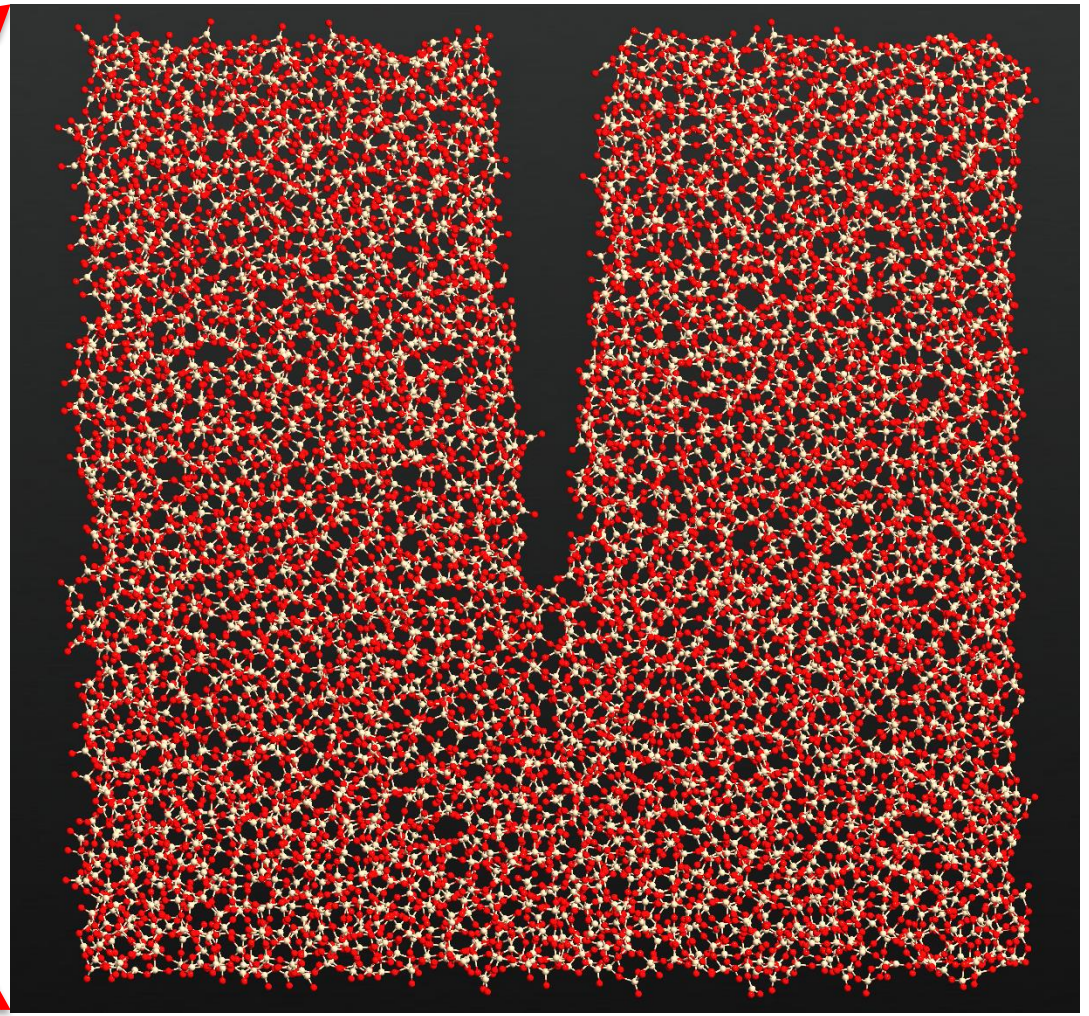
Let’s zoom into the interesting part and look at it on atomistic scale

Pattern Bending Due to Zipping Effect

Atomistic amorphous oxide



Full scale structure



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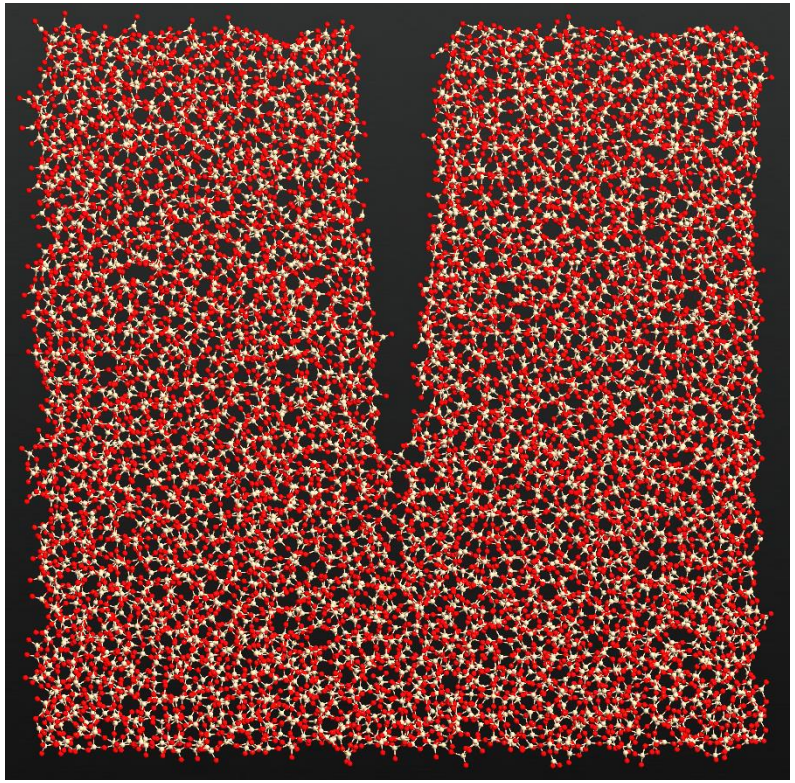
Molecular Dynamics: Zipping of the 8º Oxide Gap

Timeline: initial



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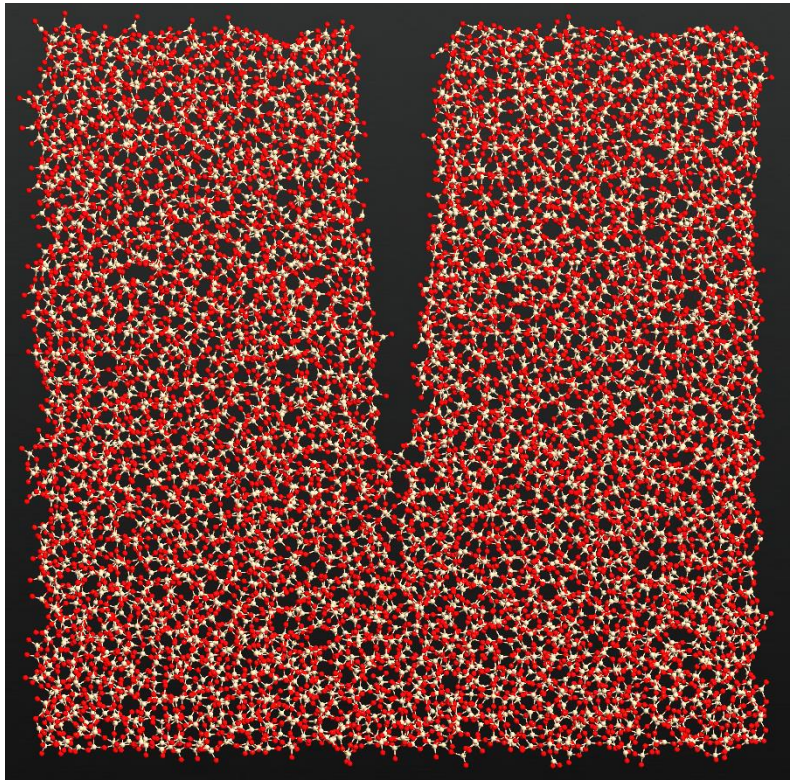
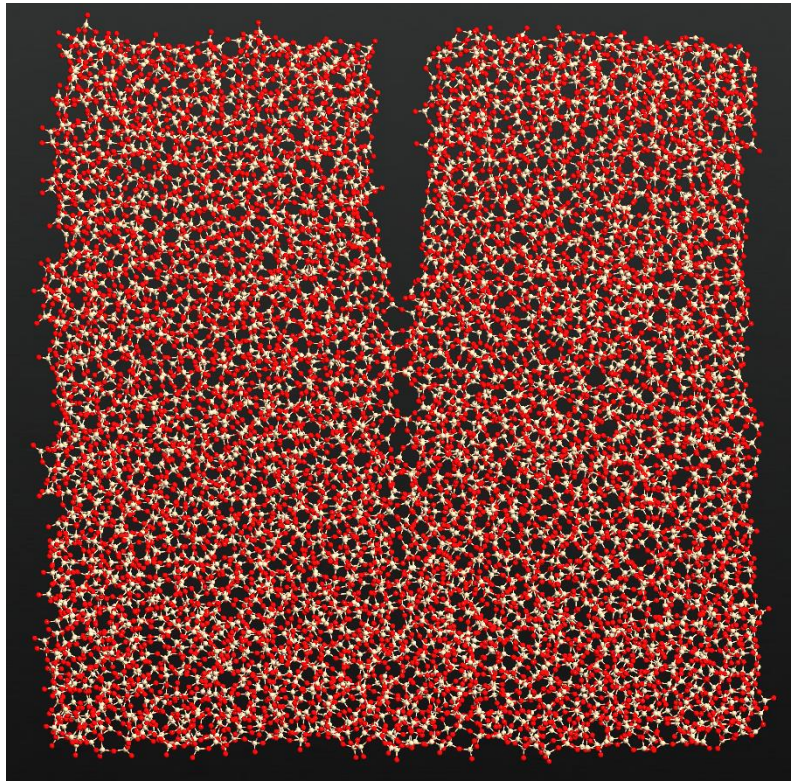
Molecular Dynamics: Zipping of the 8º Oxide Gap

Timeline: initial → intermediate





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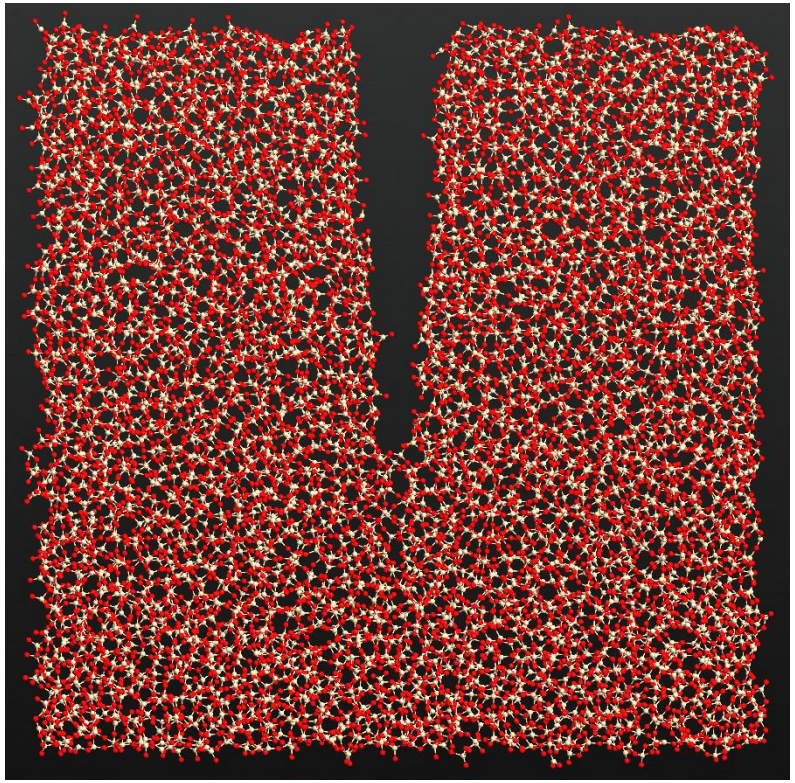
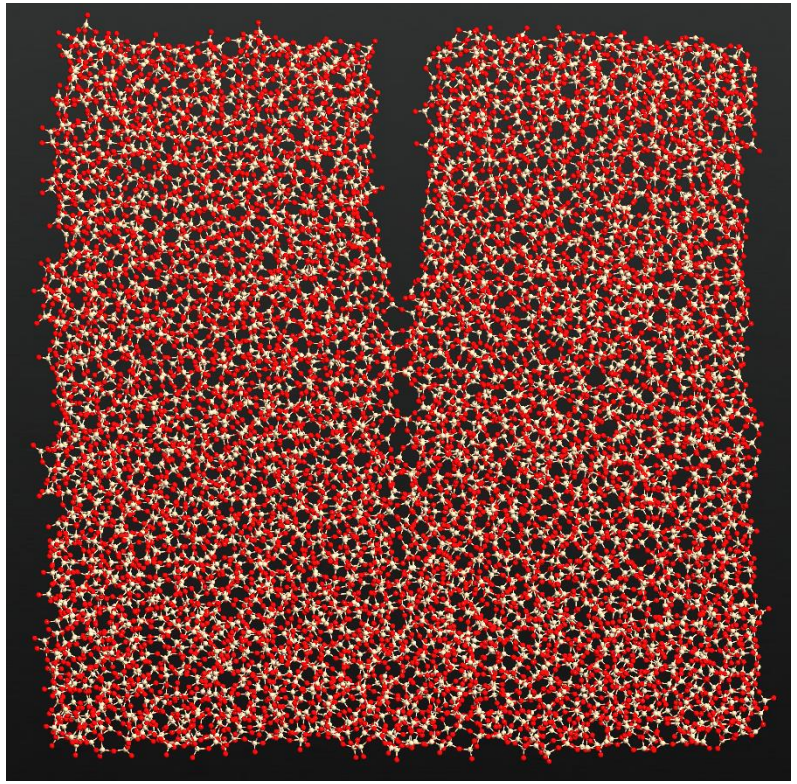
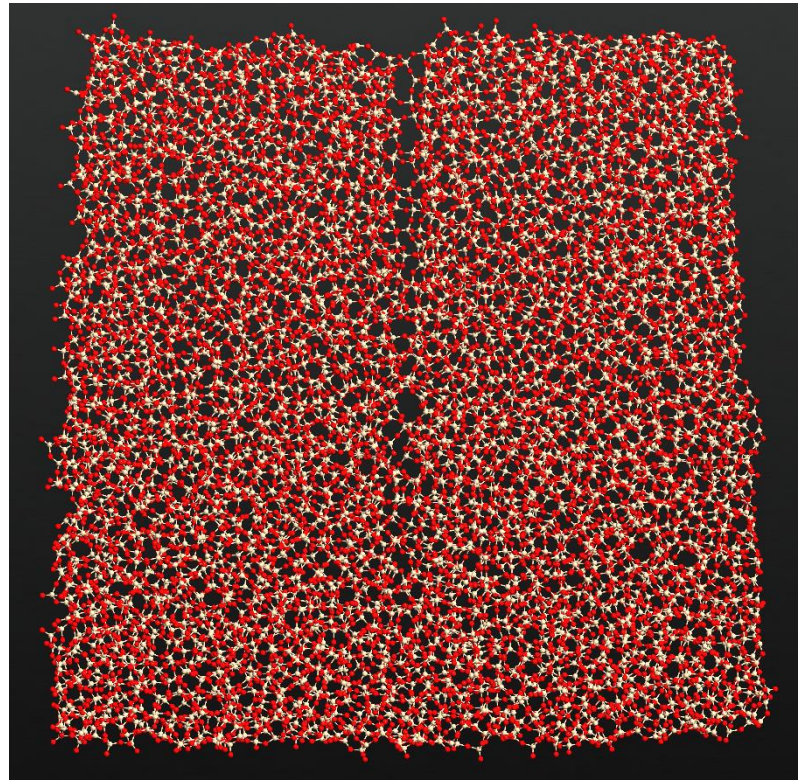
Molecular Dynamics: Zipping of the 8º Oxide Gap

Timeline: initial intermediate final







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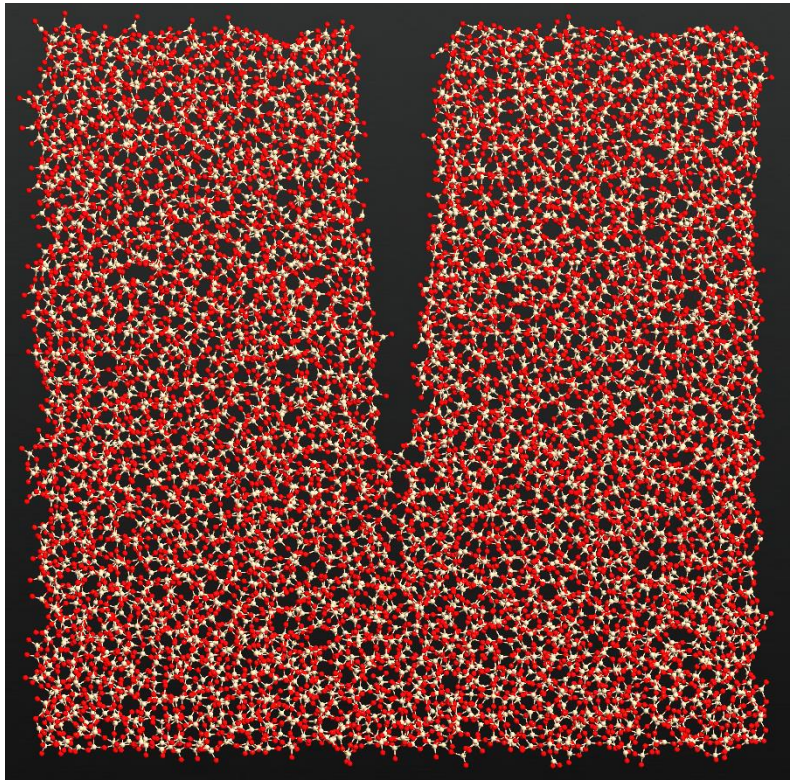
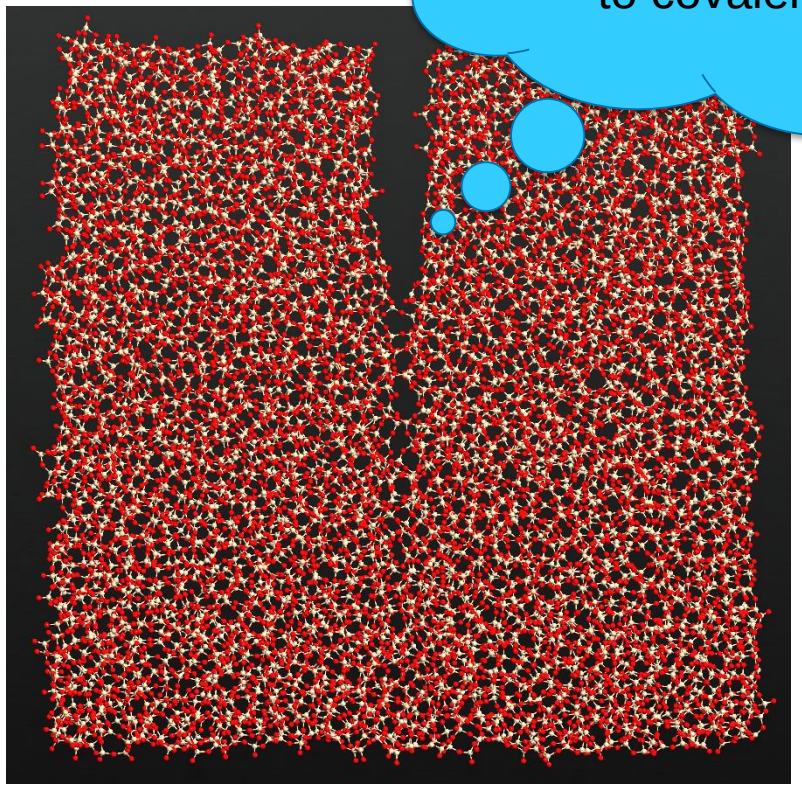
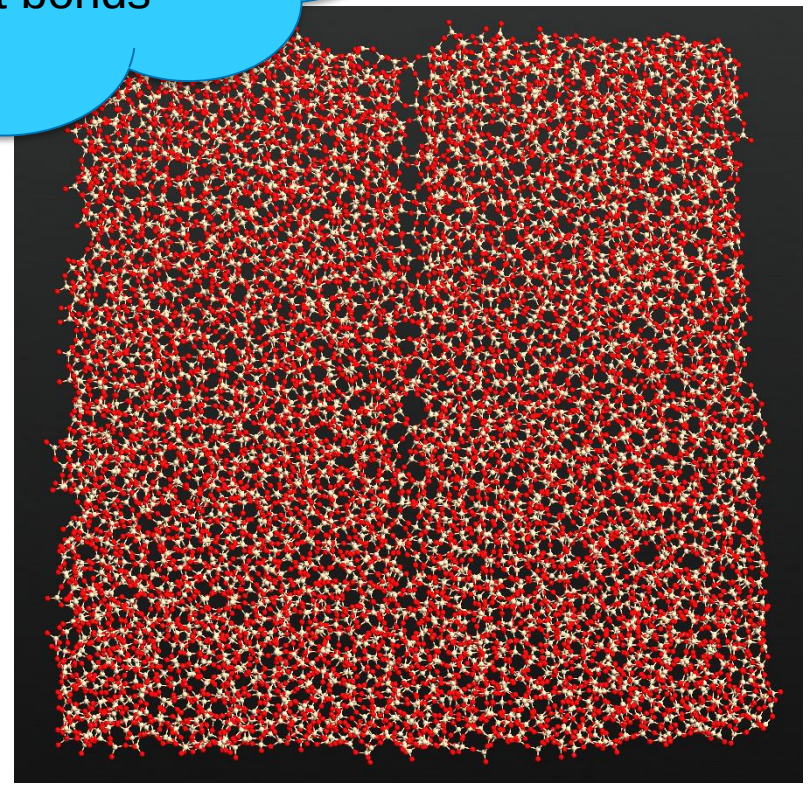
Molecular Dynamics: Zipping of the 8º Oxide Gap

Timeline: initial intermedi

Interaction starts with Van der Waals bonds, and eventually switches to covalent bonds







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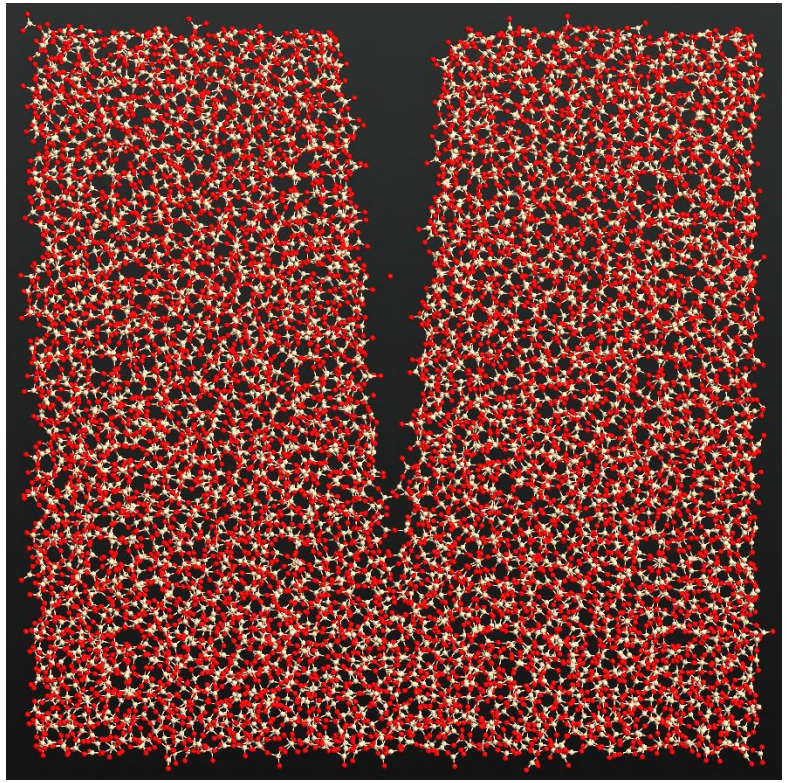
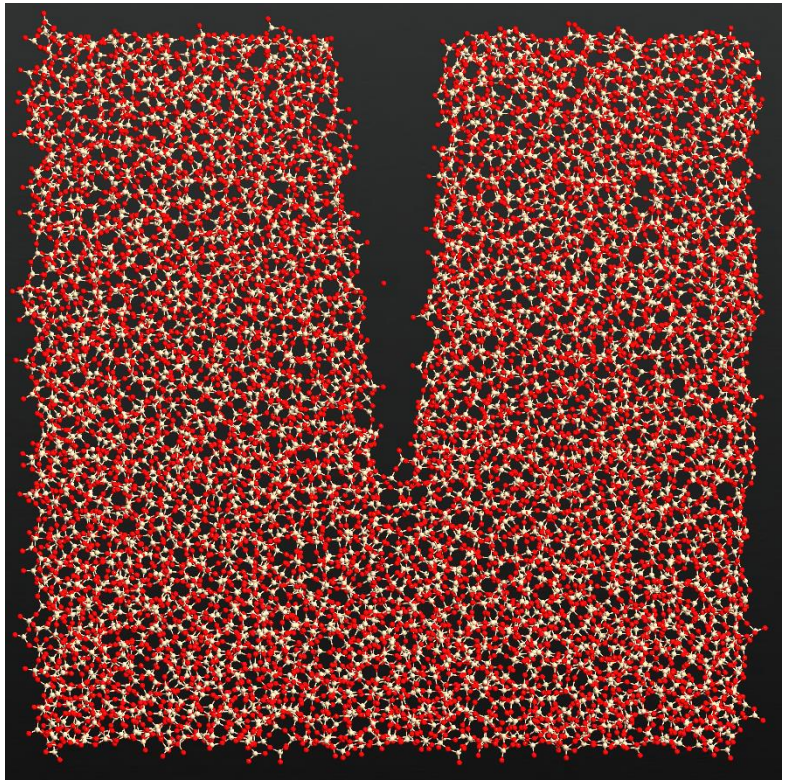
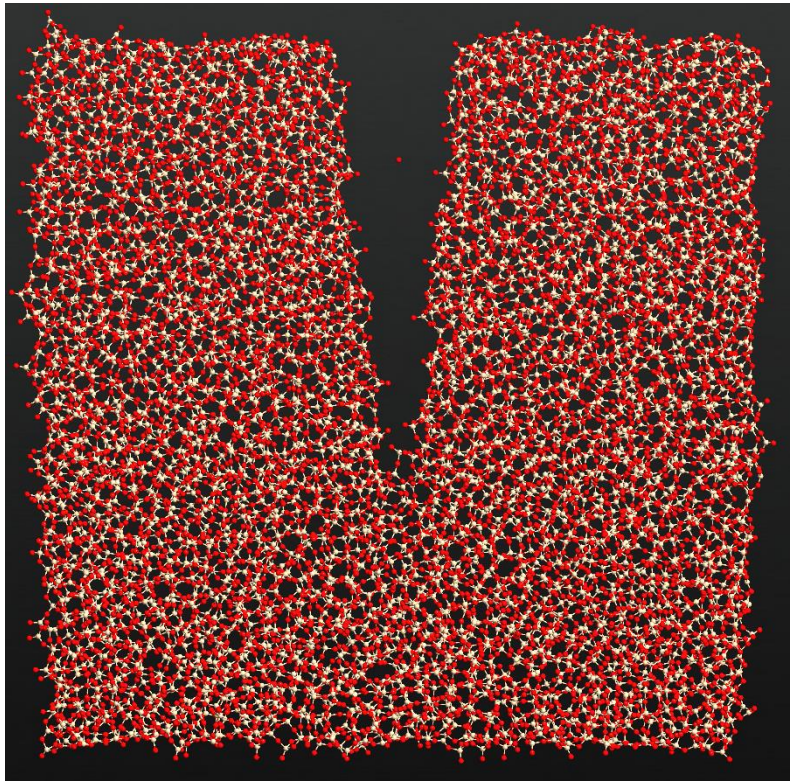
Molecular Dynamics: No Zipping of the 10º Oxide Gap

Timeline: initial intermediate final







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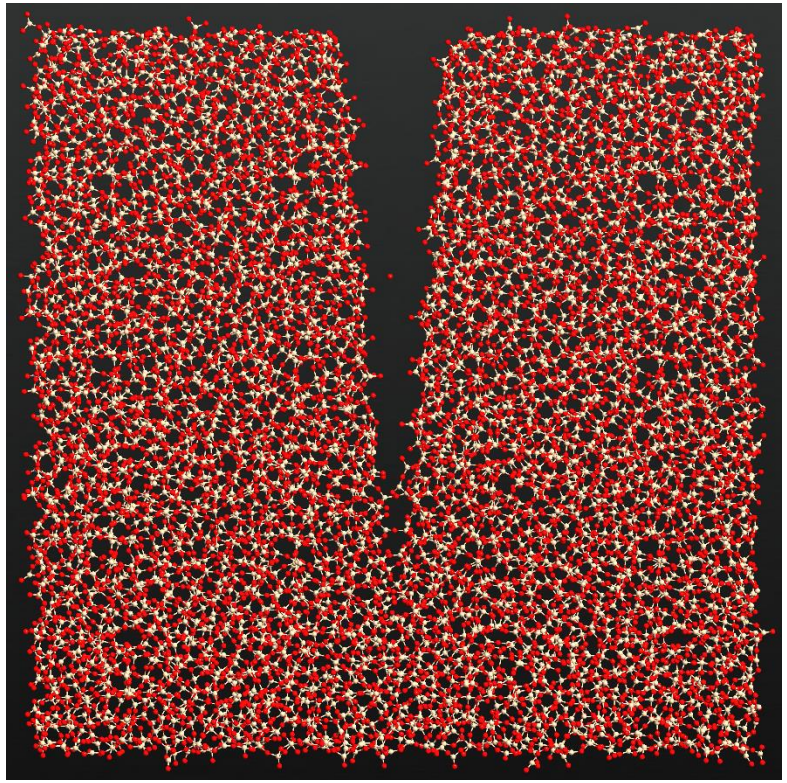
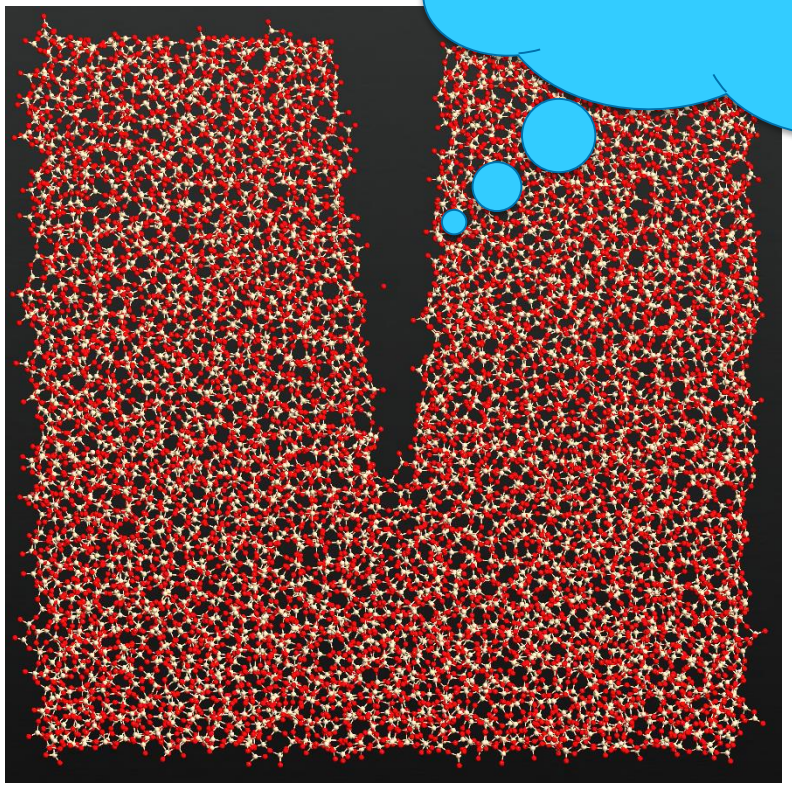
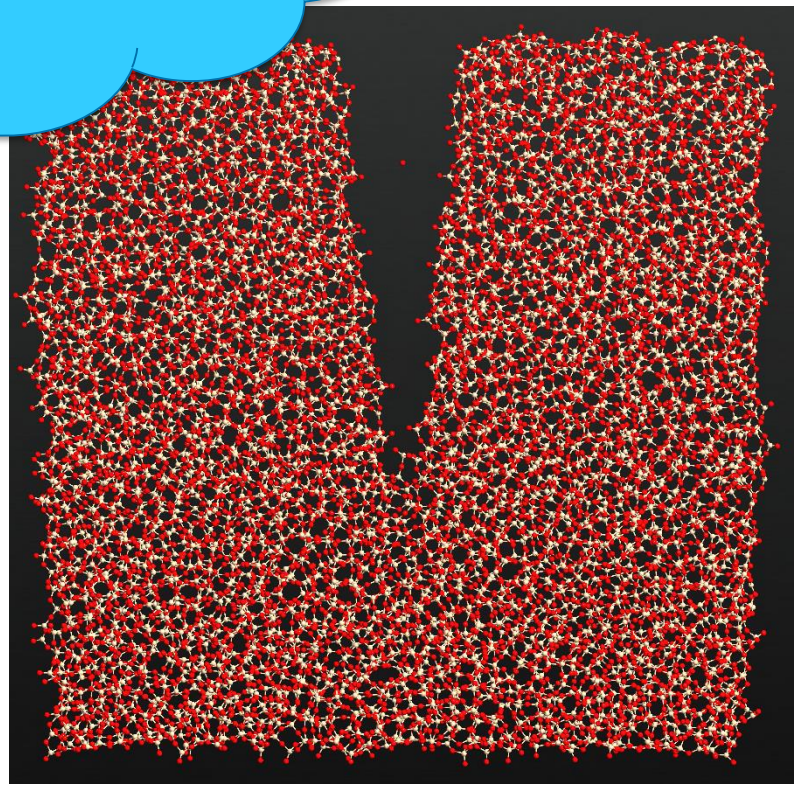
Molecular Dynamics: No Zipping of the 10º Oxide Gap

Timeline: initial intermedi

No zipping, just a few bonds at the bottom of the gap







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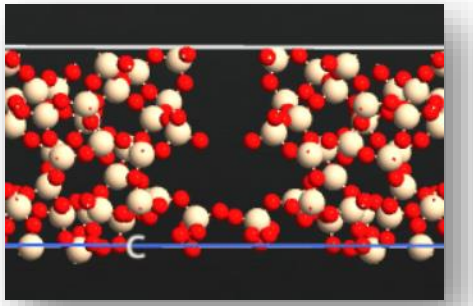
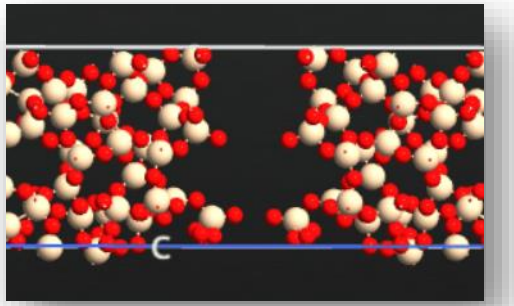
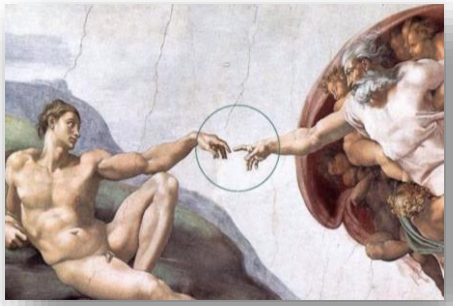
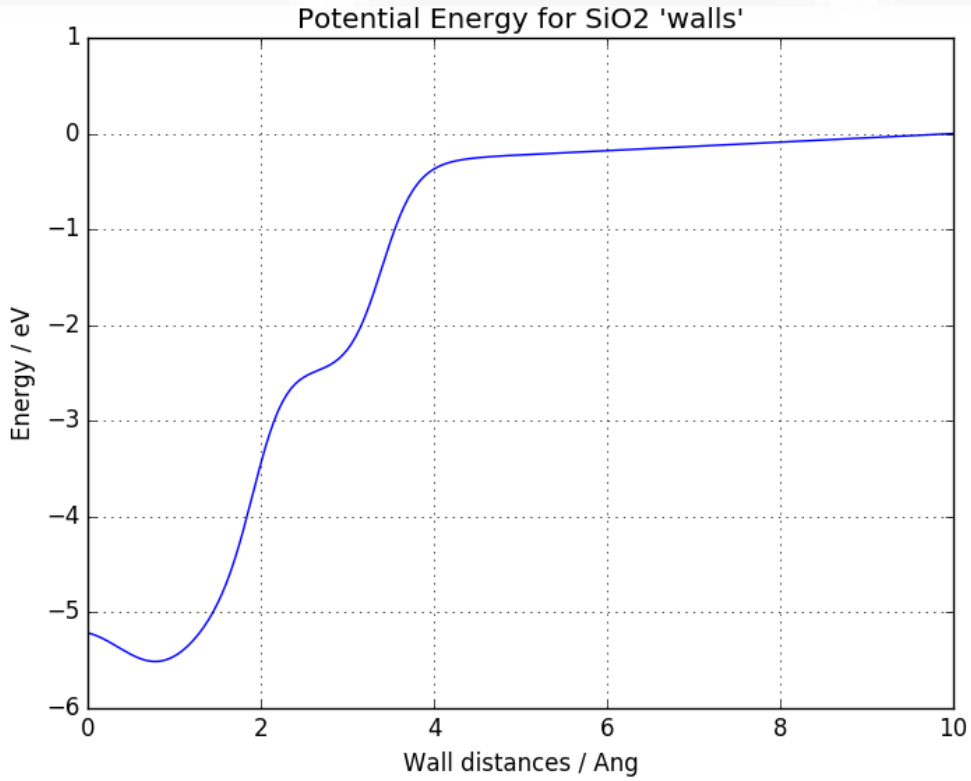
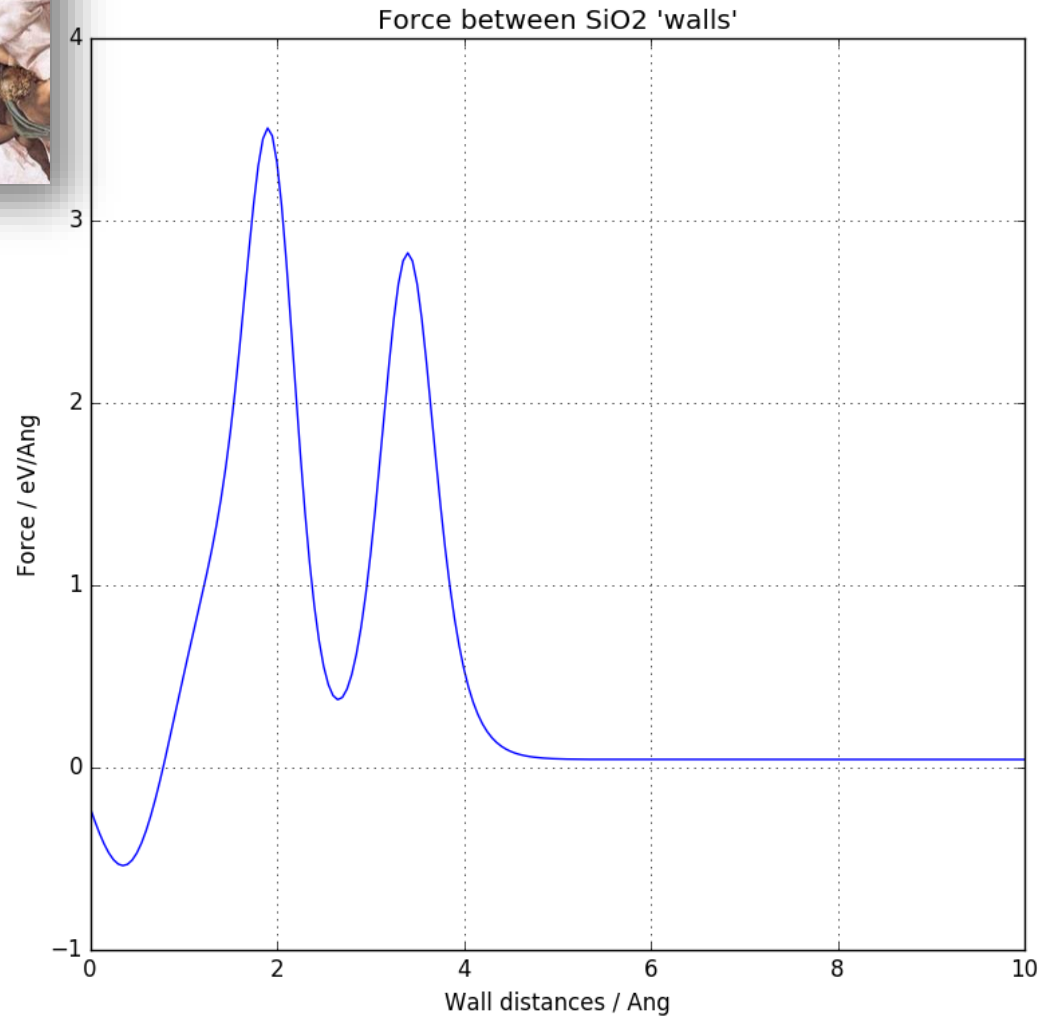
Interaction of the Oxide Layers vs Gap Width











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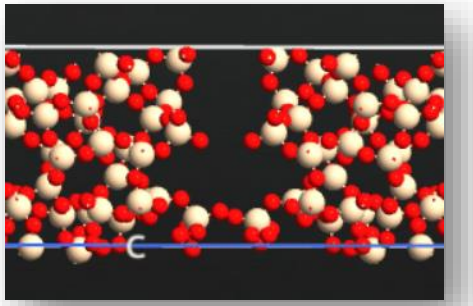
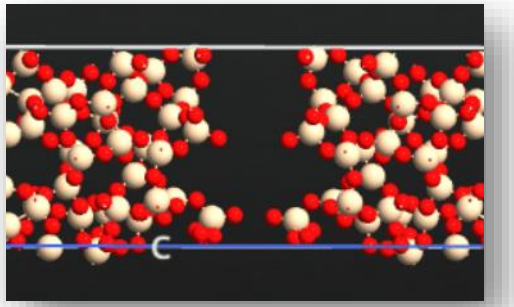
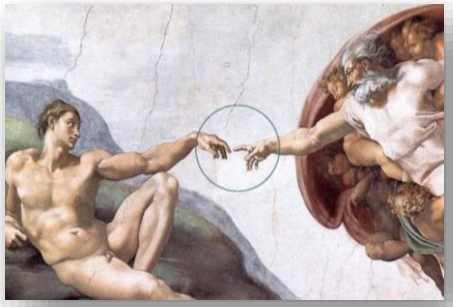
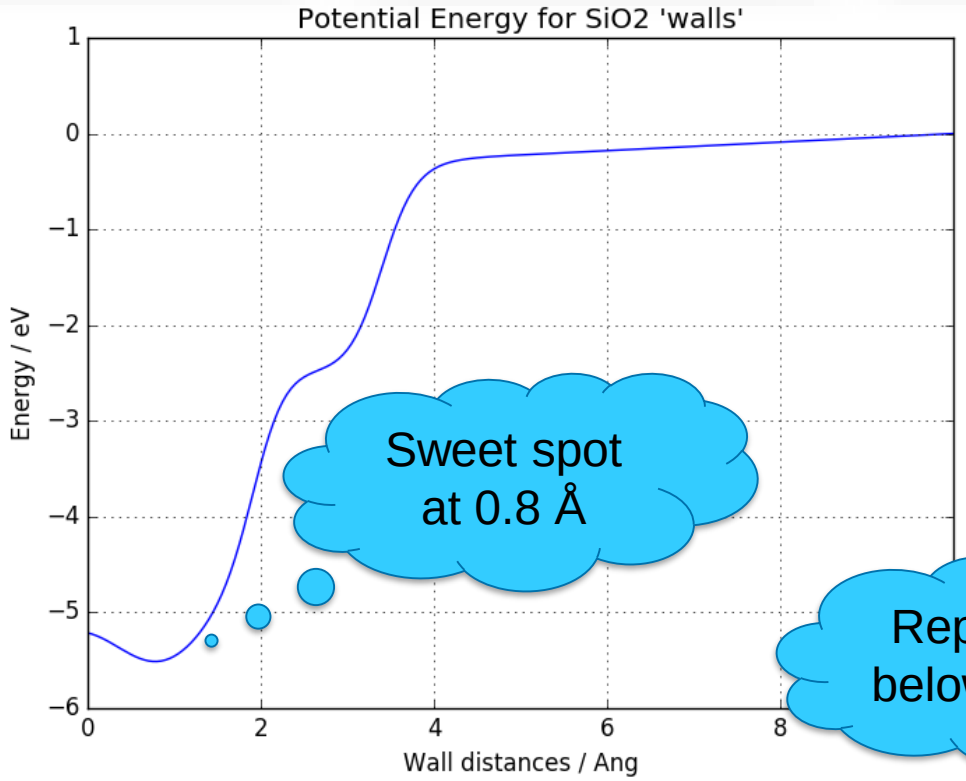
Interaction of the Oxide Layers vs Gap Width



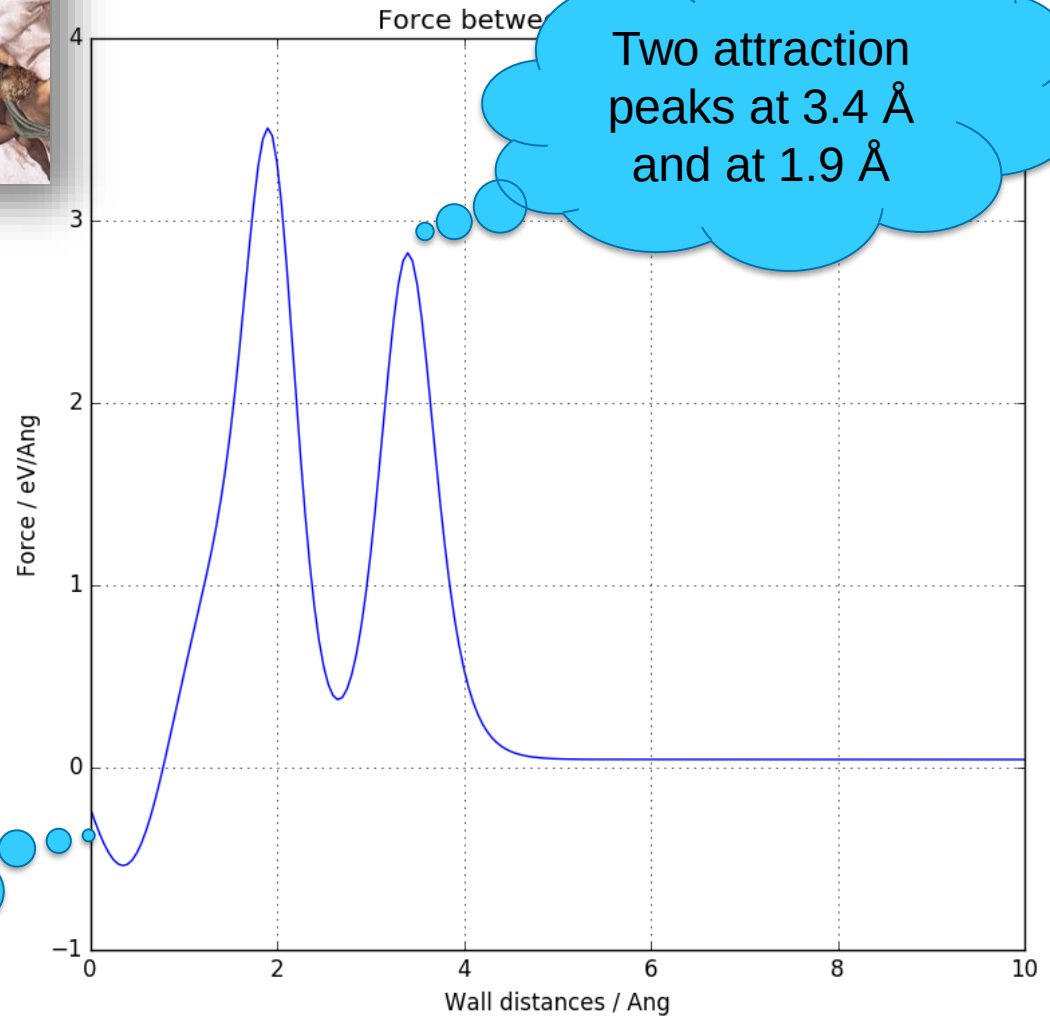






Sweet spot at 0.8 Å

Repulsion below 0.8 Å



Two attraction peaks at 3.4 Å and at 1.9 Å

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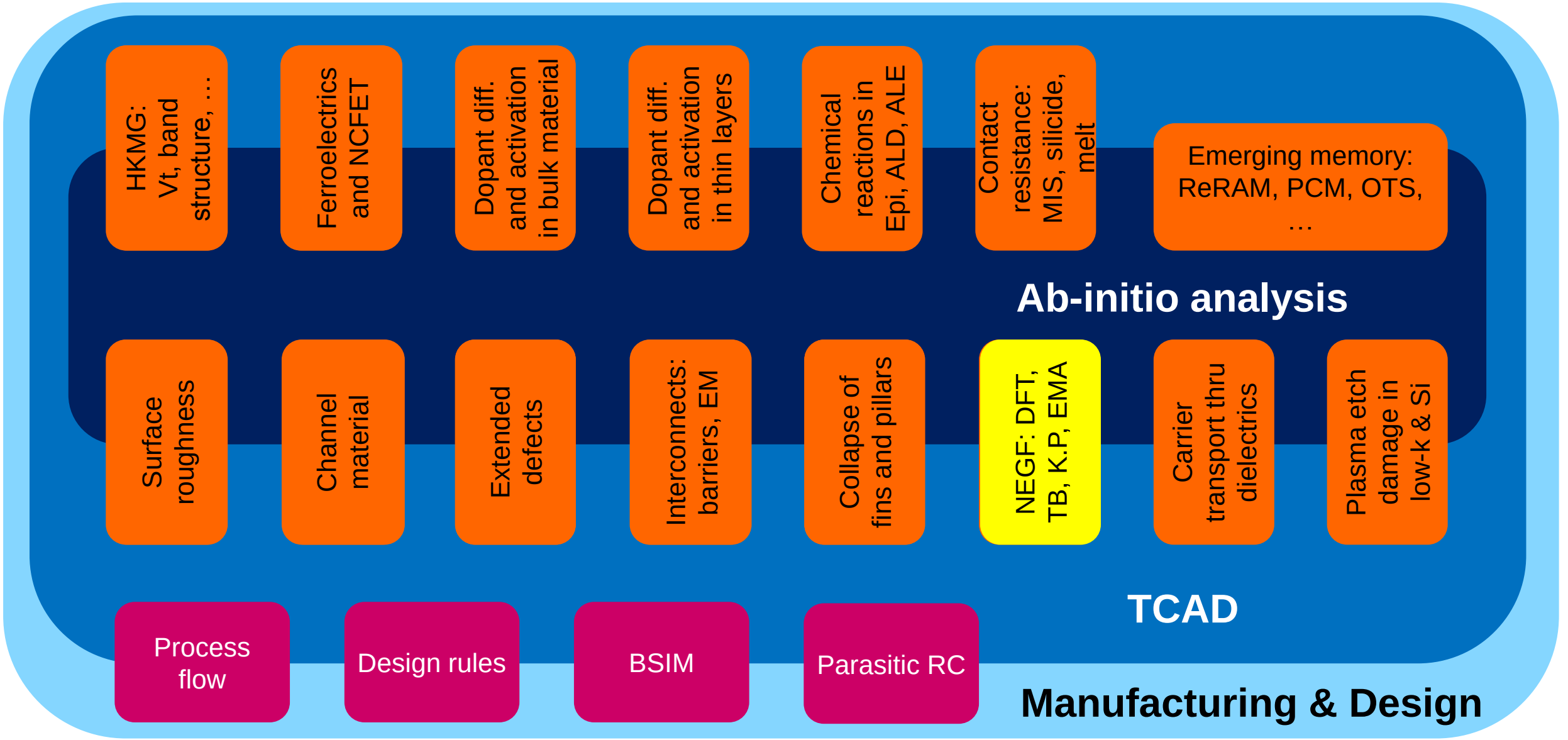
Outline



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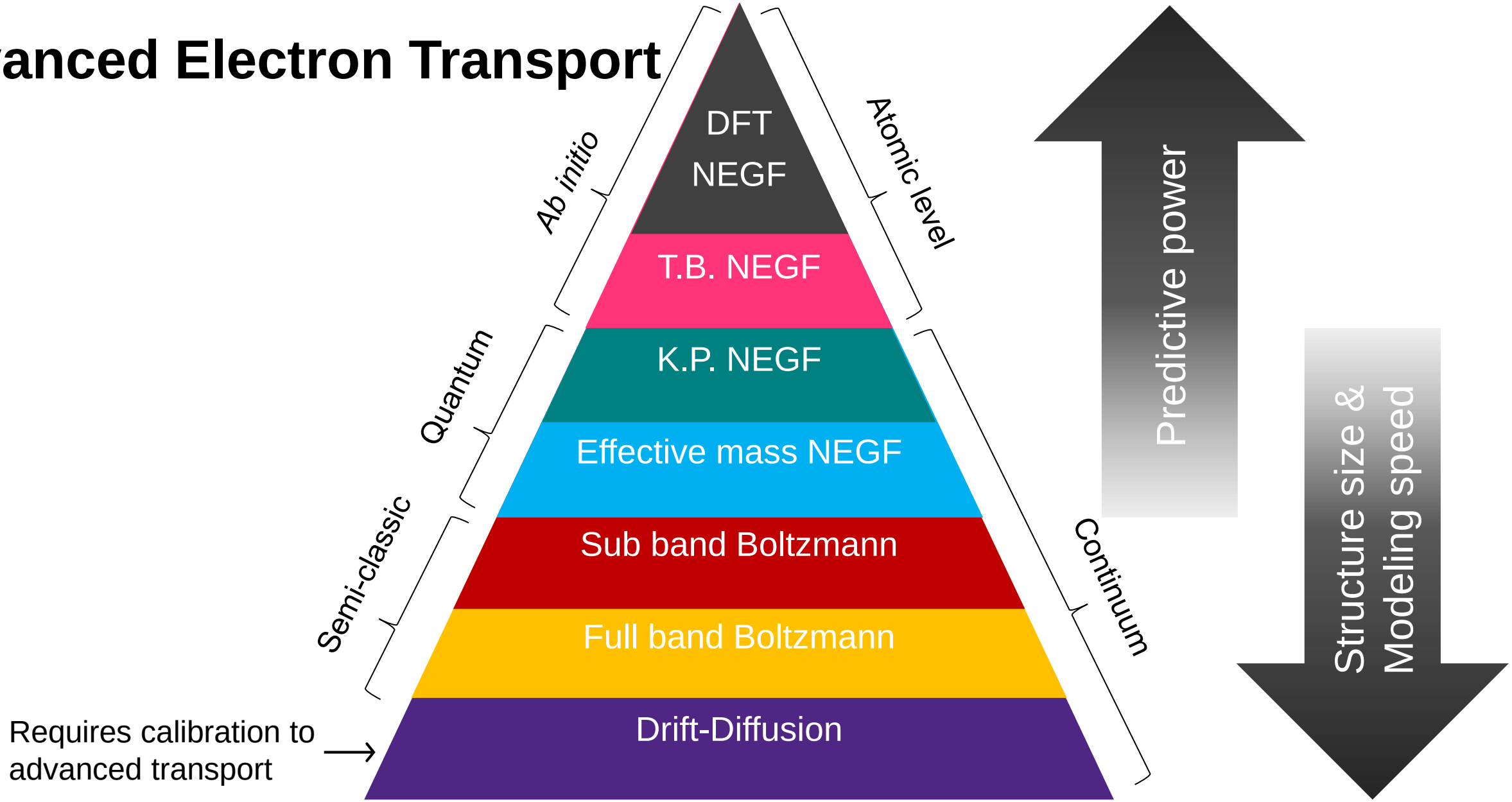
Advanced Electron Transport



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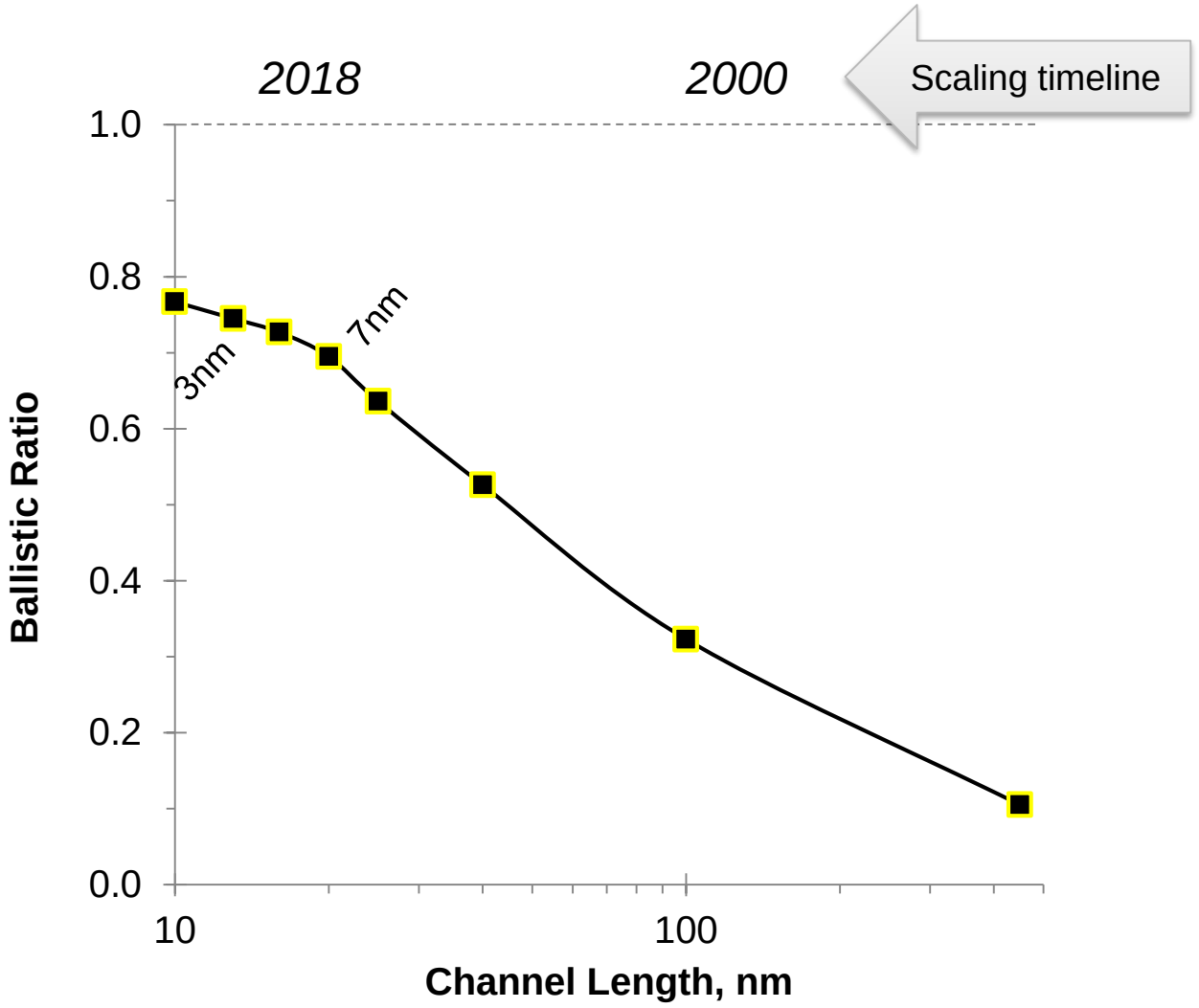
Quasi-Ballistic Electron Transport



- Ballistic ratio keeps improving with scaling
- And projected to improve towards 2nm design rules for FinFET or nano-slab
- One important side effect is that fundamental physics plays increasing role, and there's less need for calibration

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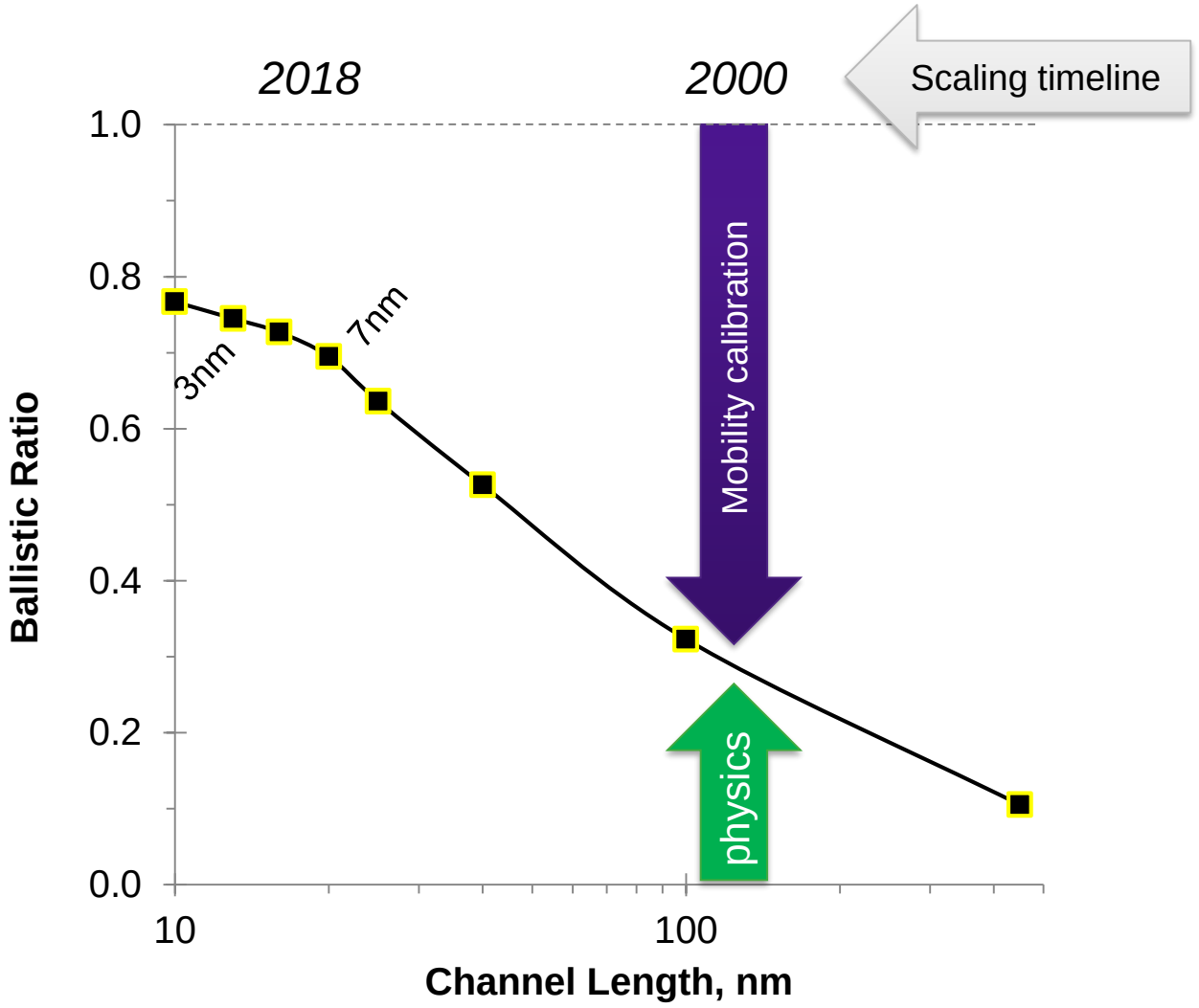
Quasi-Ballistic Electron Transport



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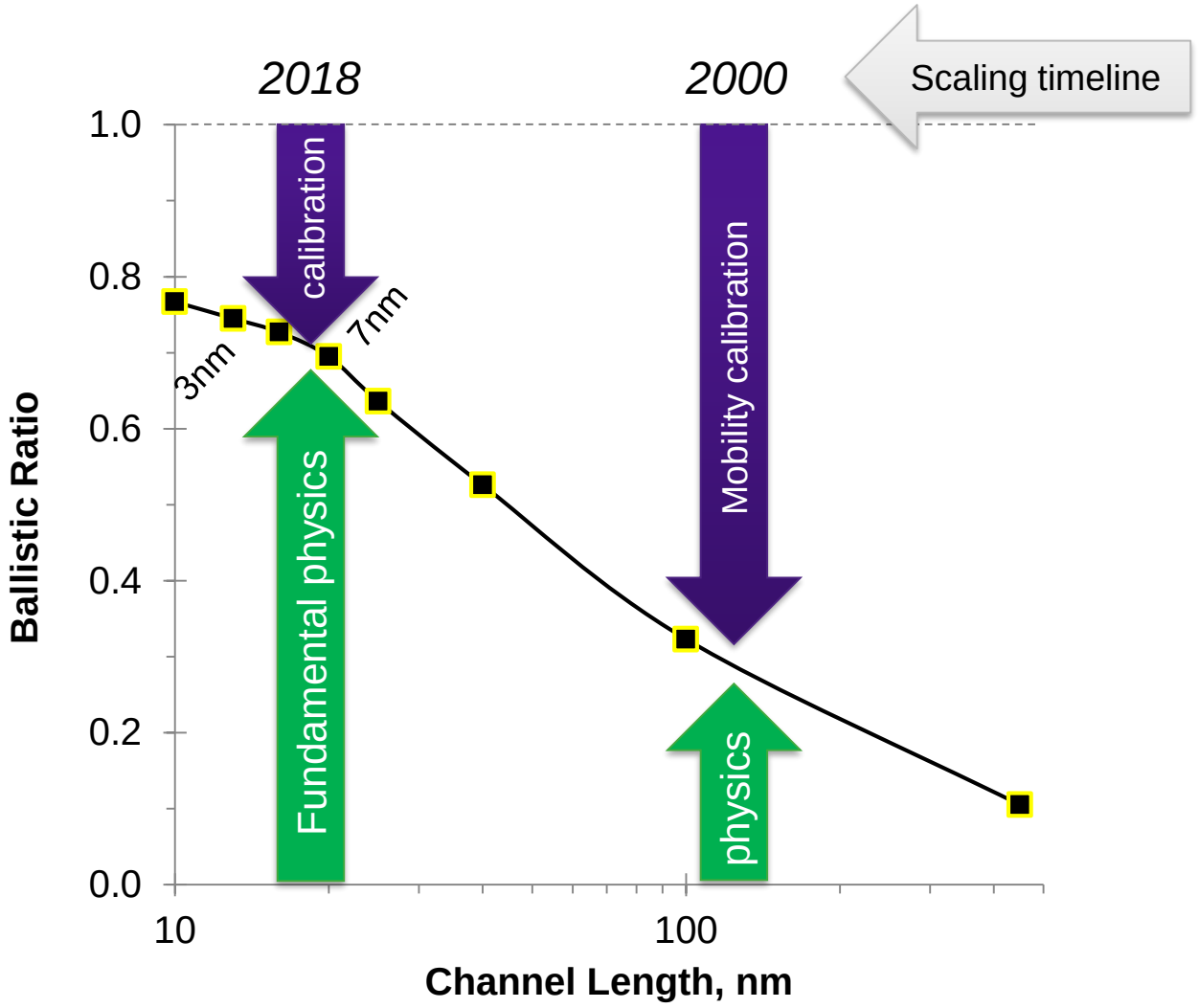

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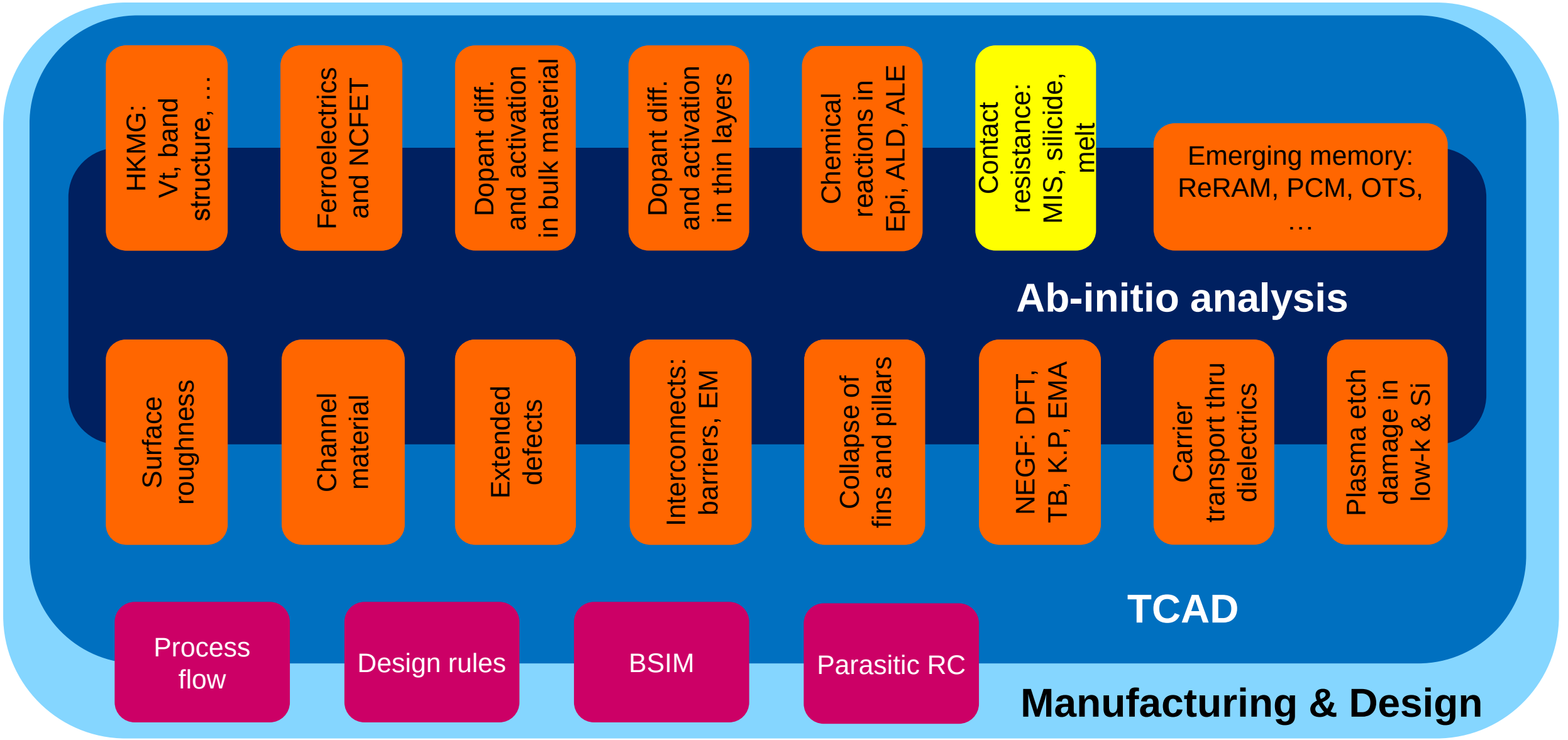

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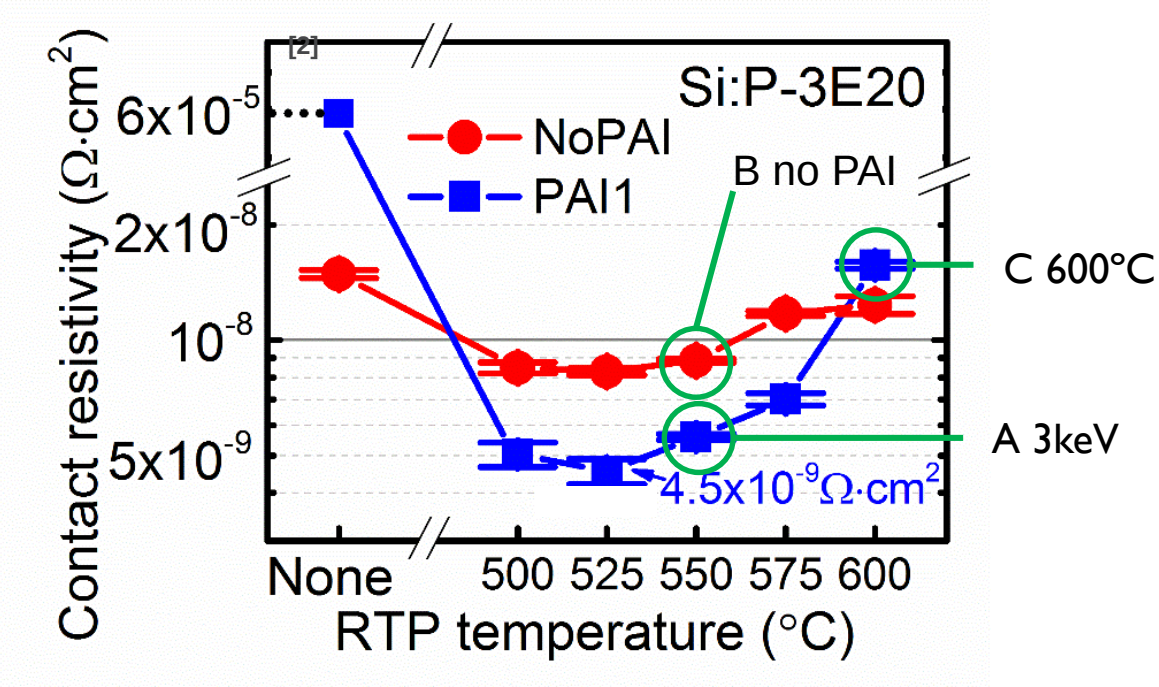
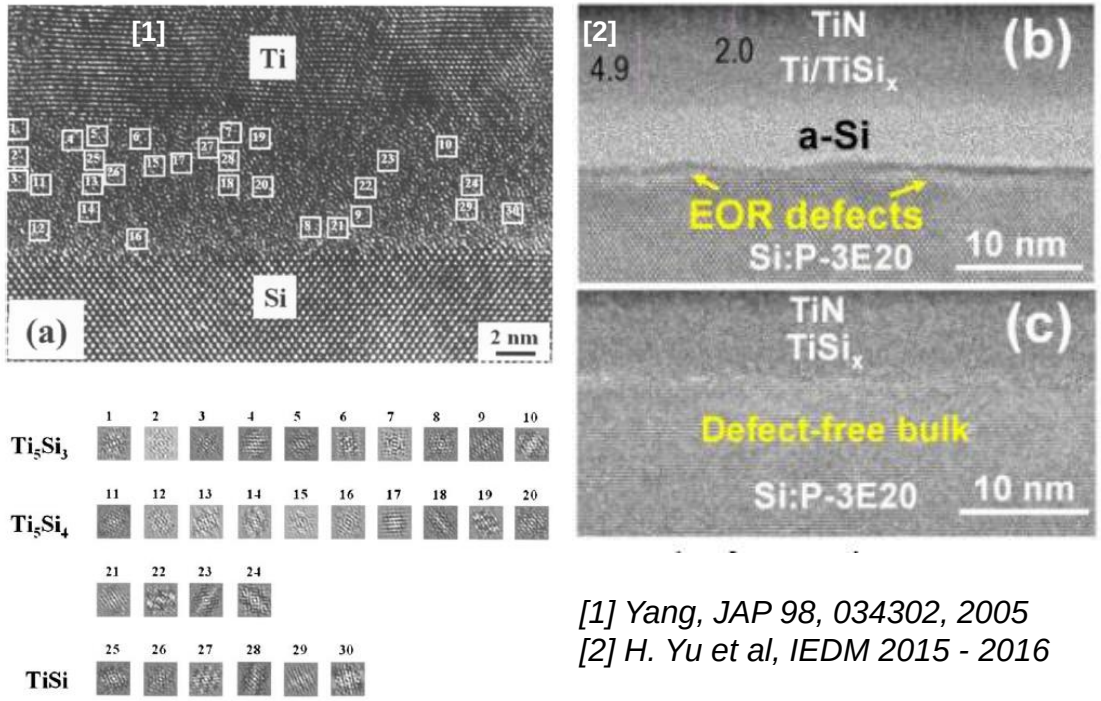
Modeling S/D Contact Resistance (G. Pourtois, IMEC)

- Fundamentals
  - Today: ~1e21|e|/cm^3 → 2x10^{-9} Ω·cm^2
  - Can we reach 10^{-10} Ω·cm^2 ?
  - Is there a theoretical limit to it?



A few practical difficulties:

TiSi$_x$ crystallites in a-TiSi alloy



[1] Yang, JAP 98, 034302, 2005
[2] H. Yu et al, IEDM 2015 - 2016

Amorphous & polycrystalline interfaces
How do we model this? → Atomistic simulations

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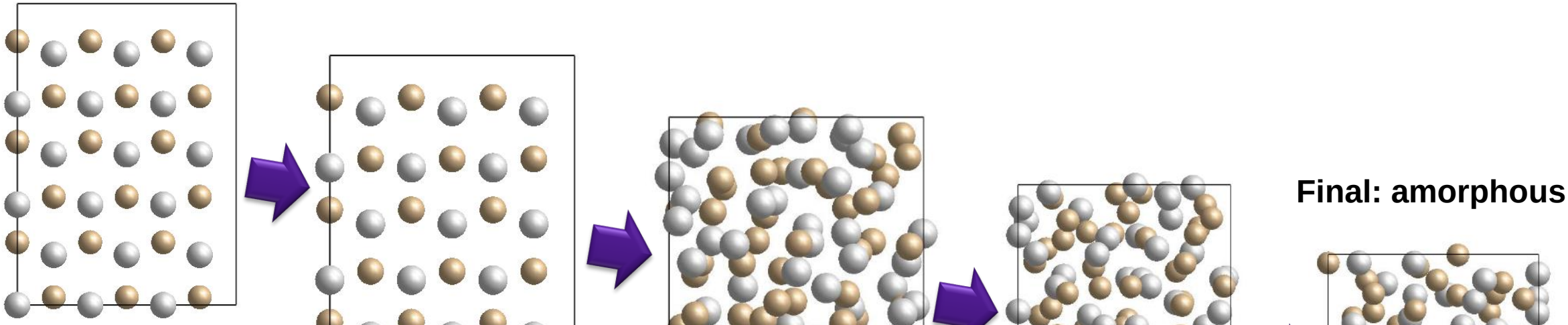
How to Get Amorphous Material? (G. Pourtois, IMEC)

"melt & quench" process

Initial: crystal



Crystal TiSi

10% relaxed crystal

Melted TiSi

10% melt shrink

Final: amorphous

Quenching

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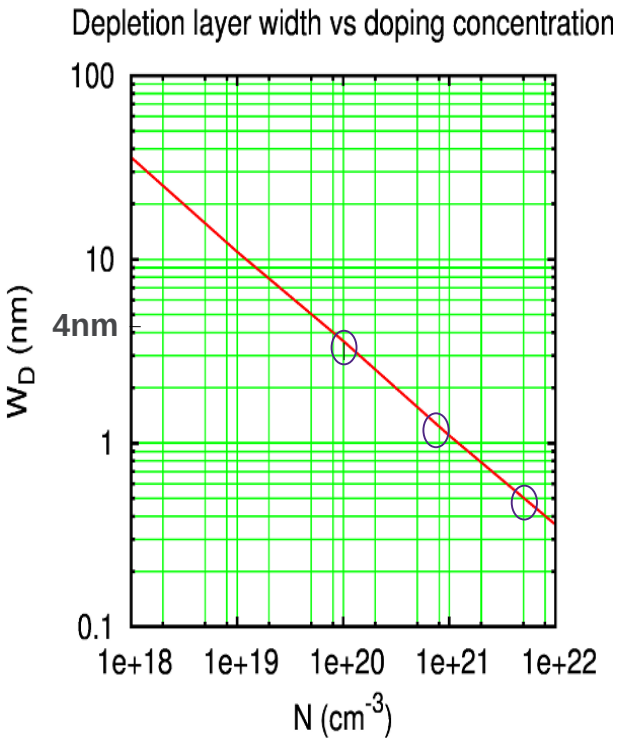
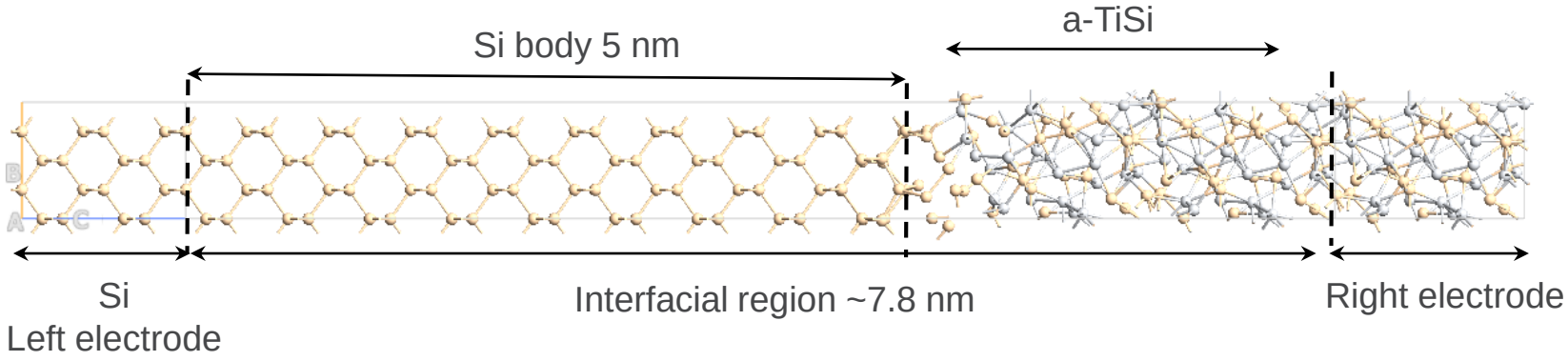
System Size & Interface Models (G. Pourtois, IMEC)



The Si body should be at least 4 nm thick @ $1 \cdot 10^{20}$ |e|/cm^3 To account for a proper depletion length



Methodology:

- DFT & NEGF: QuantumWise
- TB functional (c=1.08) → band gap Si: 1.18, Ge: 0.66 eV
- Lattice mismatch < 1% - tailored amorphous model
- Uniform doping
- 260 atoms model
- SZP basis

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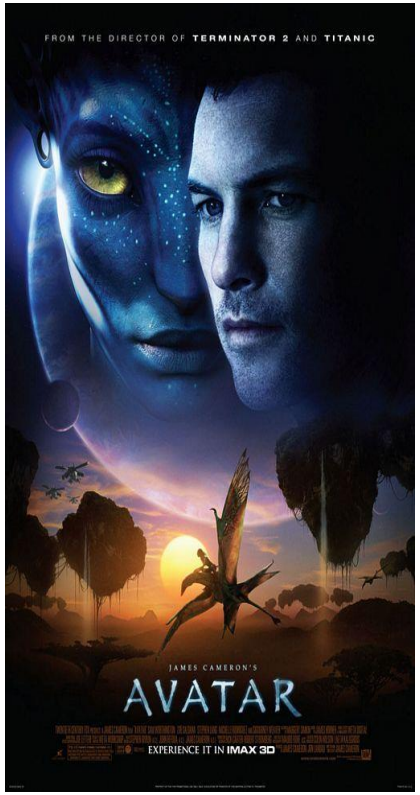
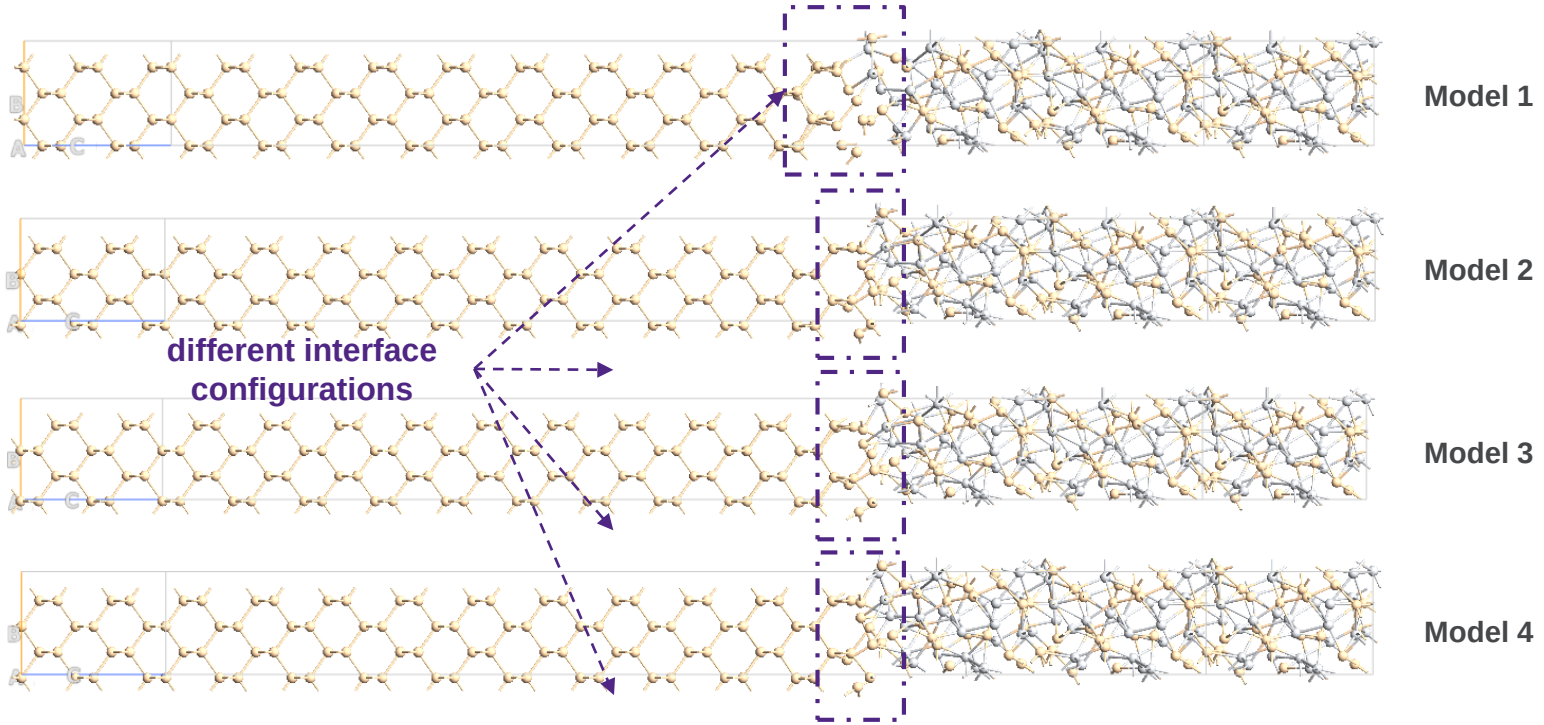


Models (G. Pourtois, IMEC)

Probing different interface topologies



Avatar (movie 2009) resources:

- 34 racks, each 4 chassis, 32 machines each
- 40,000 processors, 104 terabytes of memory
- 4 cores processors → 160,000 cores
- Run time: ~ 3 hours, i.e. 480,000 core-hours

CPU Resources used for this project:

- Total CPU usage so far: 453,120 core-hours
- Similar to Avatar movie

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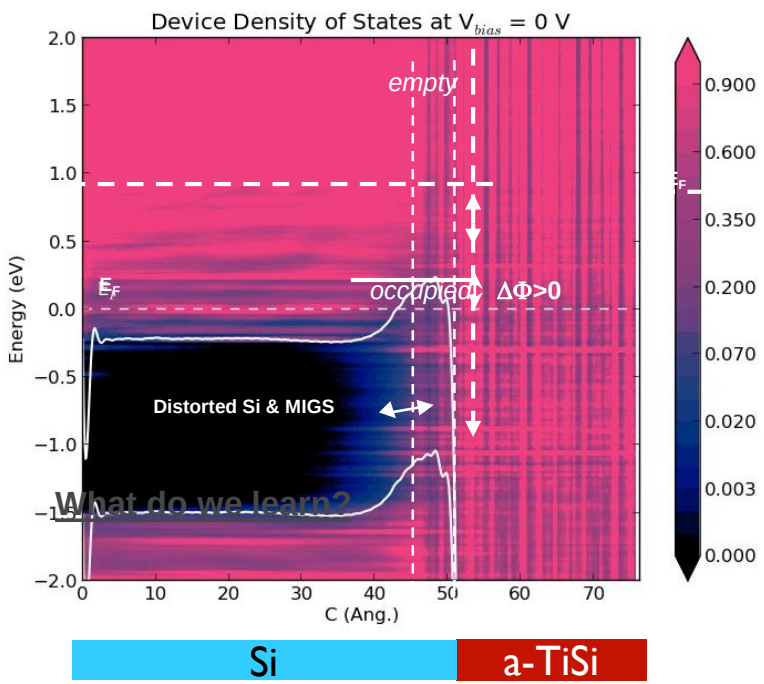
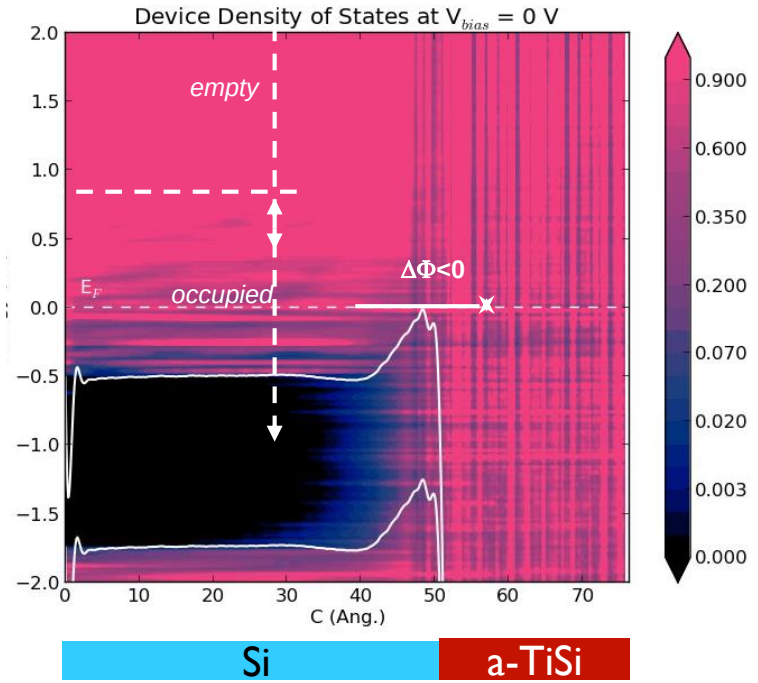
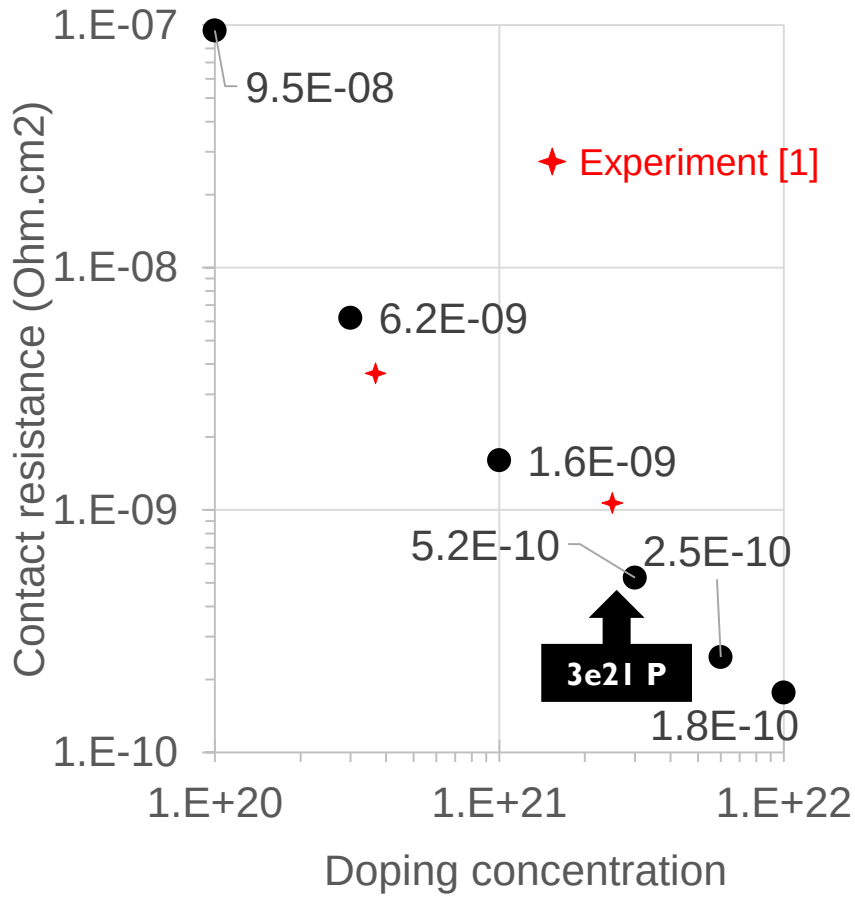
n-Si[100]|a-TiSi (G. Pourtois, IMEC)

Doping: n-1xe^{20} |e|/cm^3



Doping: n-3xe^{21} |e|/cm^3





- 10^{-10} Ω·cm^2 is possible with high doping and by matching metal/semi effective carrier masses
- **Good agreement with Si data**

[1] Yu et al, IEEE TEL Devices, Vol. 63 (12), 2016

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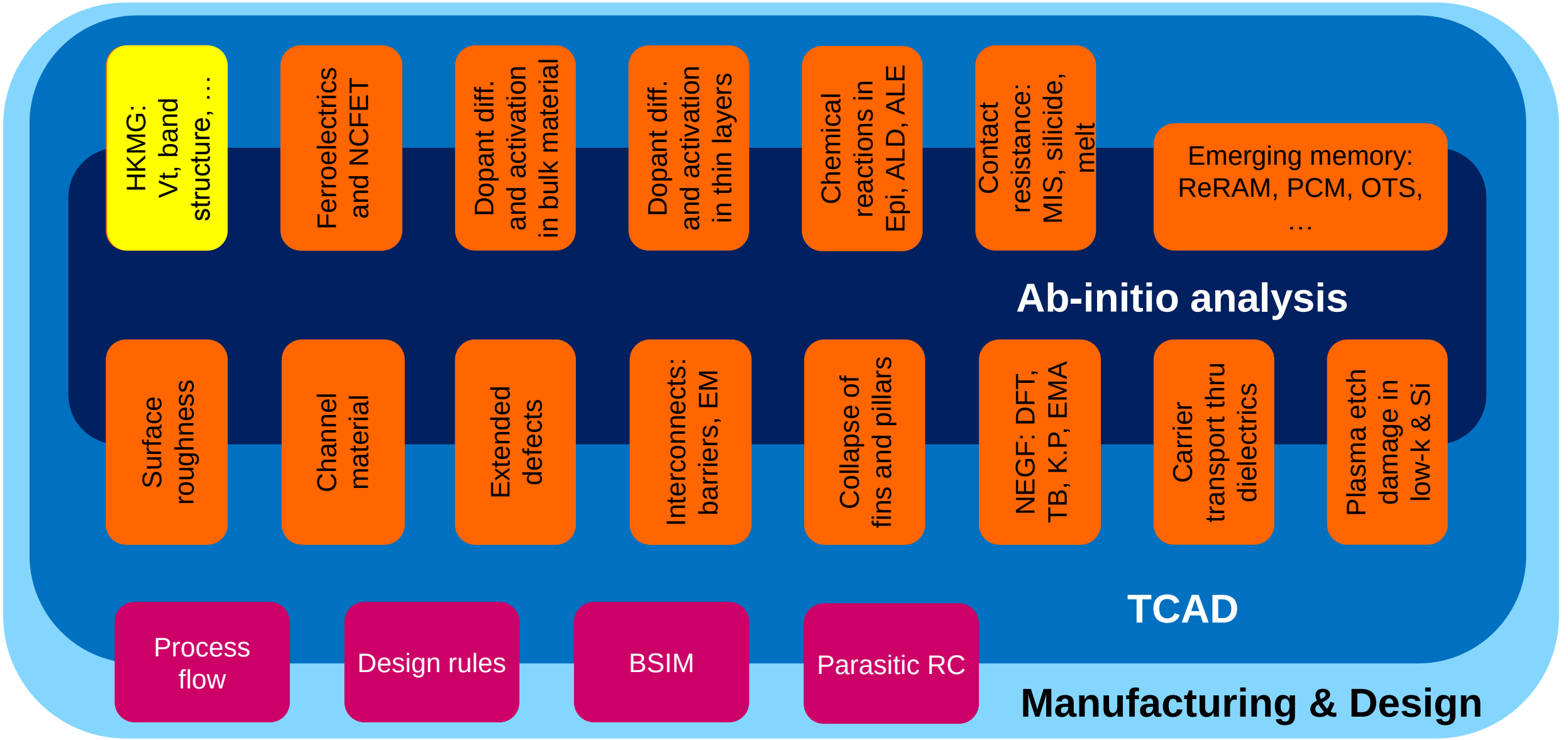
Outline



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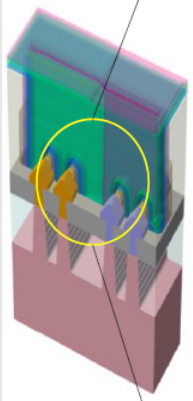
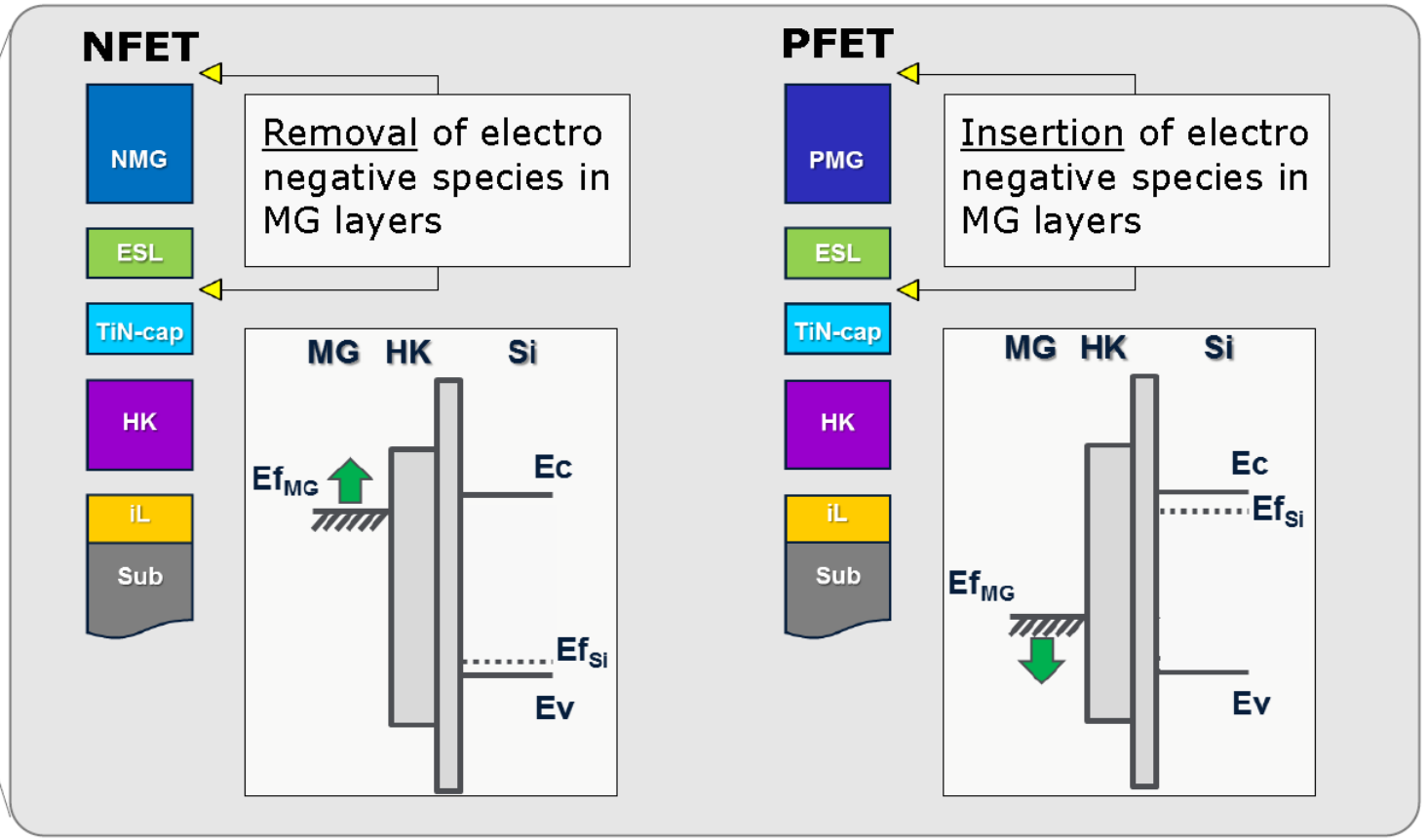
Vt Eng: Material Modification



FinFET Gate Stack



- **Vt is modulated through trace element control in gate.**
- **Effectiveness increases for layers closer to HK.**

S. Hung at IEDM 2017 short course

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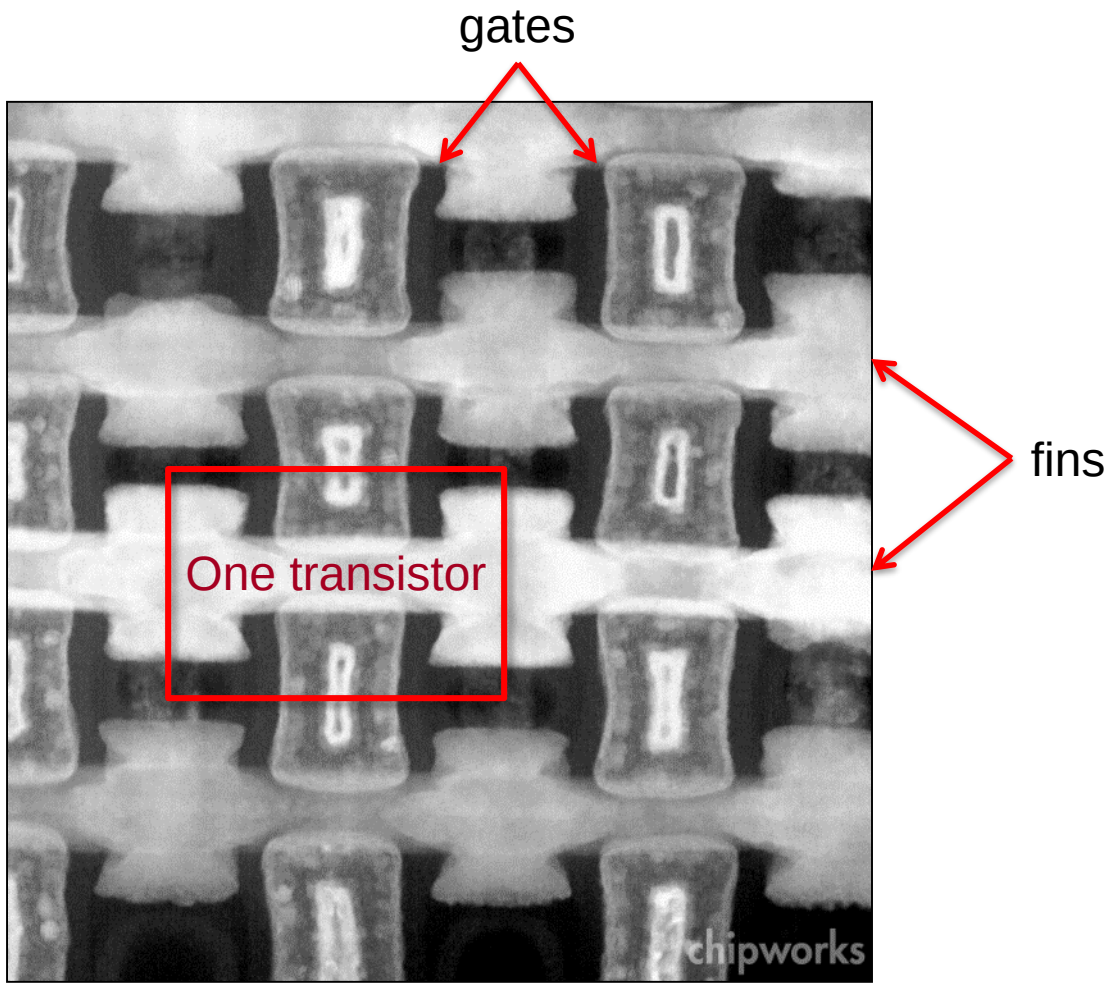
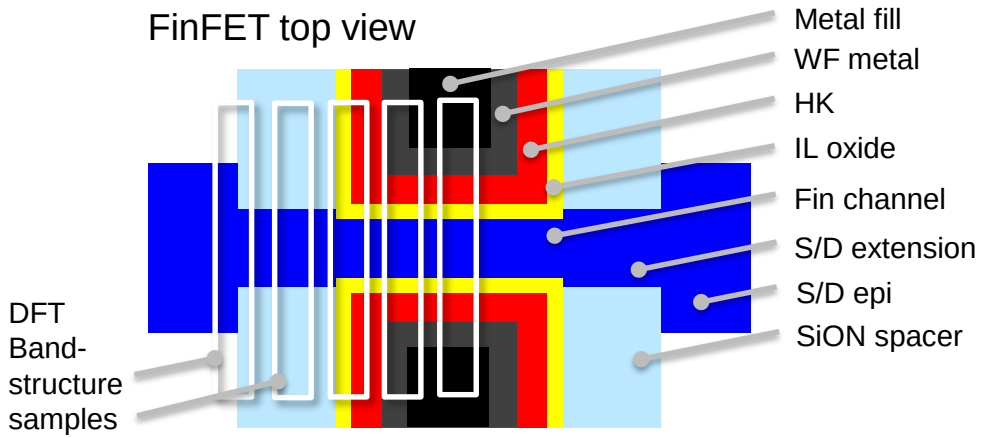
Hi-K Metal Gate: Vt Tuning, Traps, Variability



Intel's 22nm FinFETs, SEM by Chipworks @2013

- One transistor contains millions of atoms, too much for atomistic models to handle
- So, we split it into several samples where we can apply atomistic analysis



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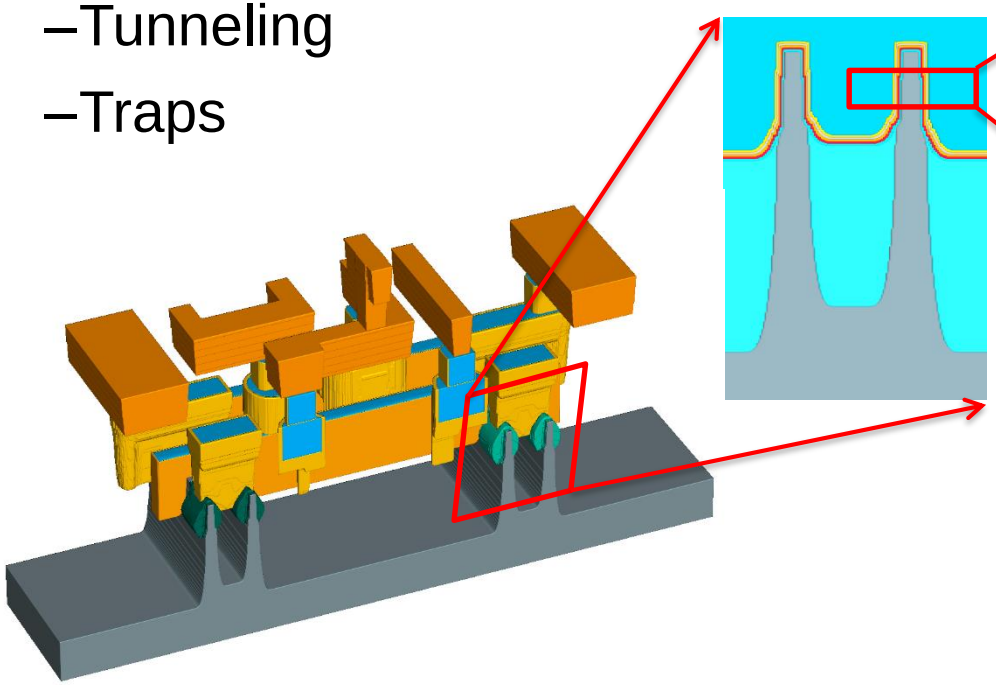
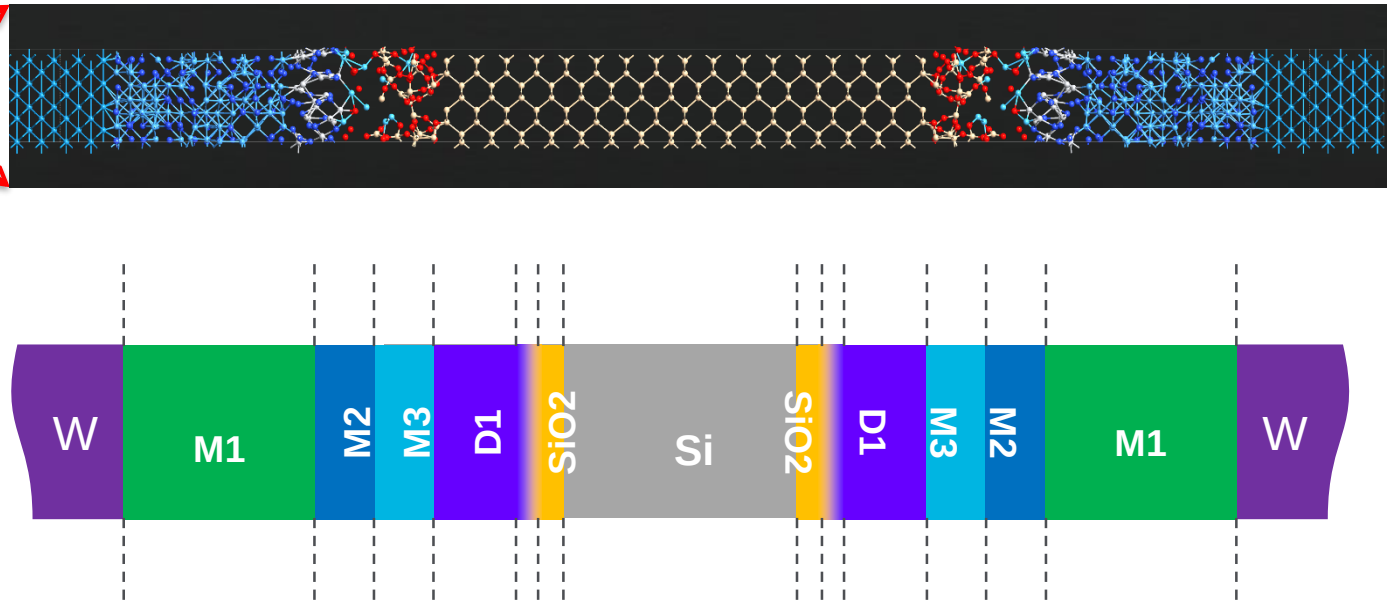
Atomistic Analysis of the Multi-Layer Gate Stack

- HKMG:
  - Many layers of metals and dielectrics
  - Complicated bandstructure
  - Surface roughness
  - Tunneling
  - Traps

Goal: predict and engineer device behavior such as Vt tuning, variability, traps, electron transport, leakage





HKMG: stack of thin layers

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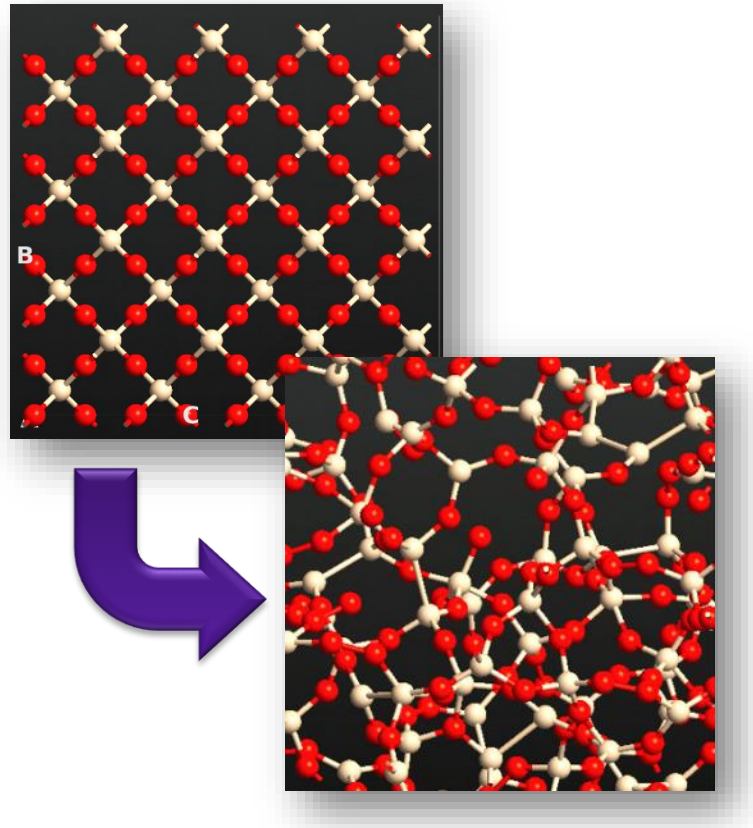
HKMG Modeling approach

- Molecular dynamics: empirical pseudopotentials or DFT
  - Melt-and-quench to obtain amorphous materials
  - Optimization of interface atomic configurations
  - Atomic positions are used as an input for electronic calculations

- Electronic calculations: DFT-NEGF
  - Band structure in the fin
  - Work function, barriers, local DOS across the stack
  - Tunneling through the stack
  - Extract essential properties for transistor scale analysis

Melting and quenching of SiO2



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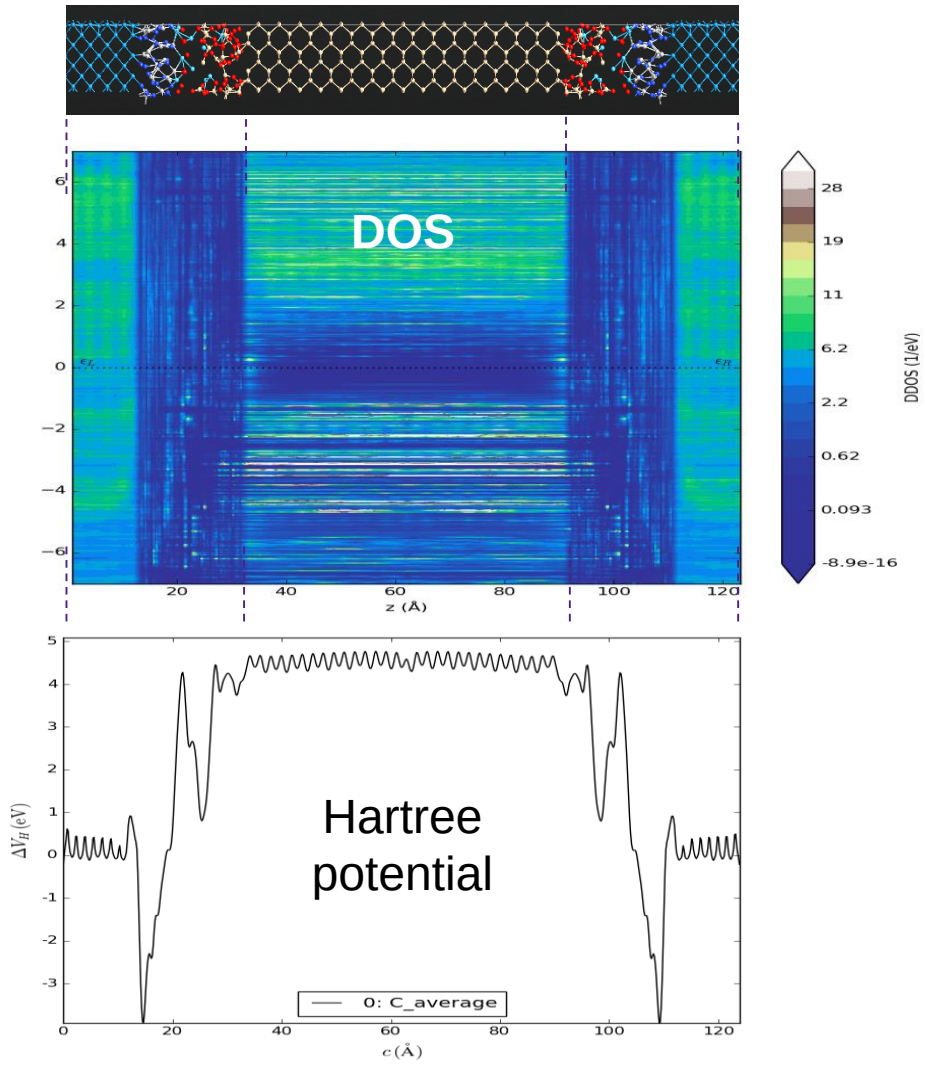
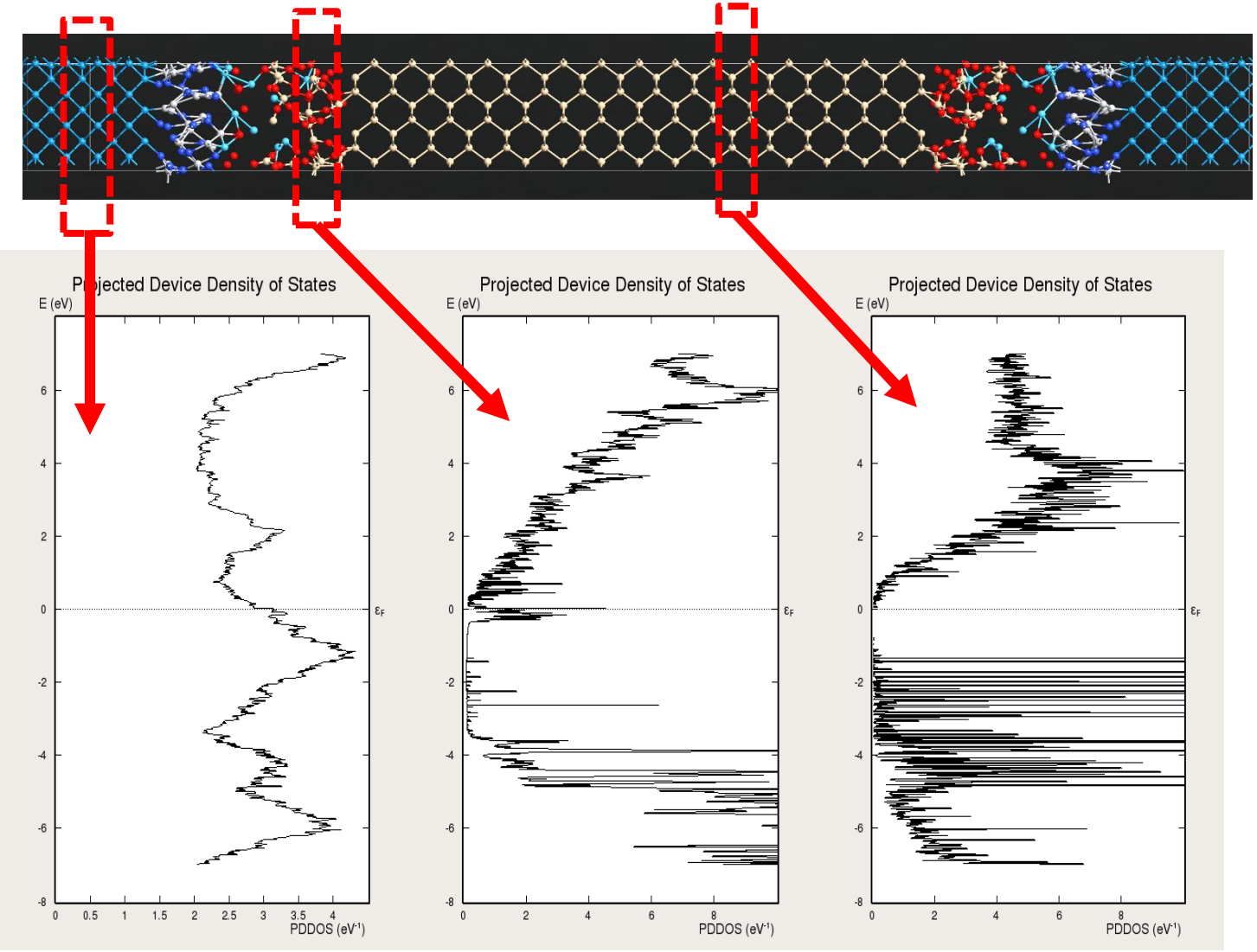
Case study: W/aTiN/aHfO2/aSiO2/Si/aSiO2/aHfO2/aTiN/W





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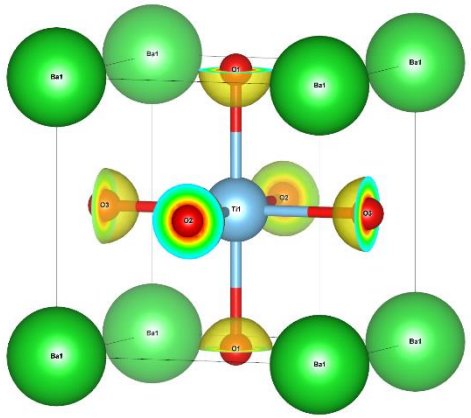
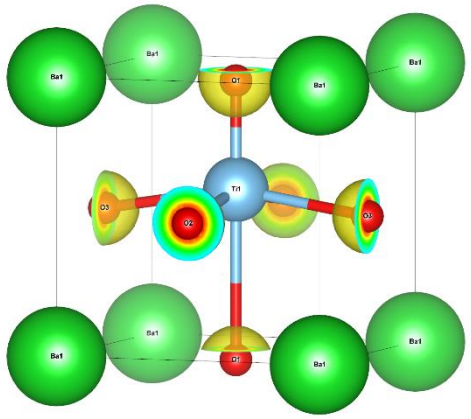
Atomistic Analysis of NCFET (Pawel Lenarczyk, ETH, Zurich)

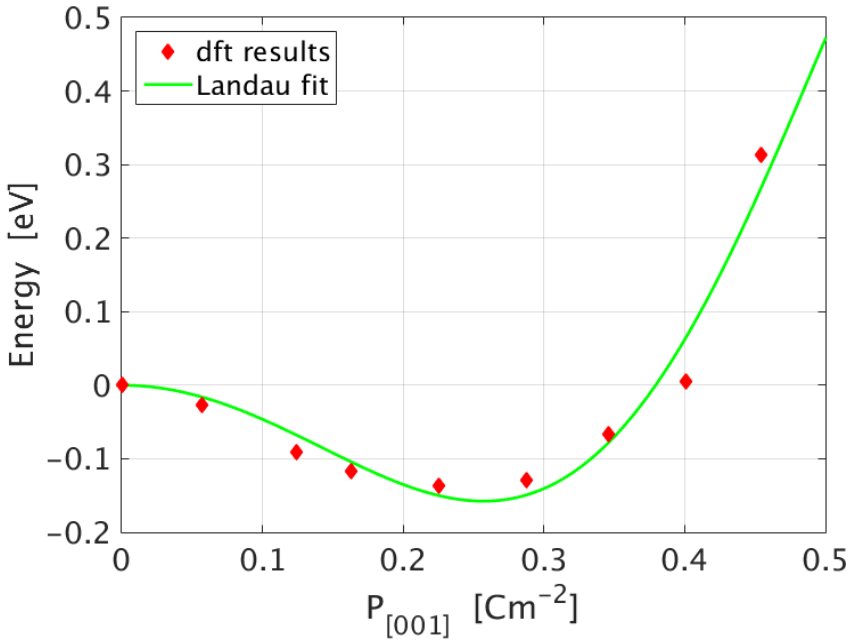
non-polar: $P = 0$



polarized: $P = 0.22\mathrm{Cm}^{-2}$

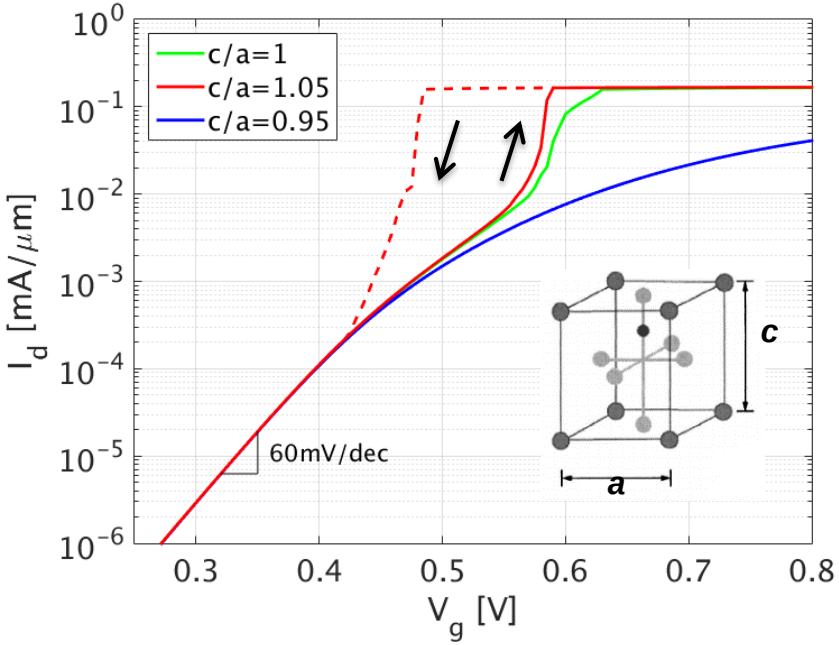


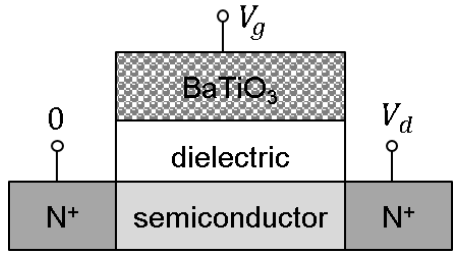
Material behavior



spontaneous polarization [cm^{-2}]	
calculated	0.25
experimental	0.22

Device behavior





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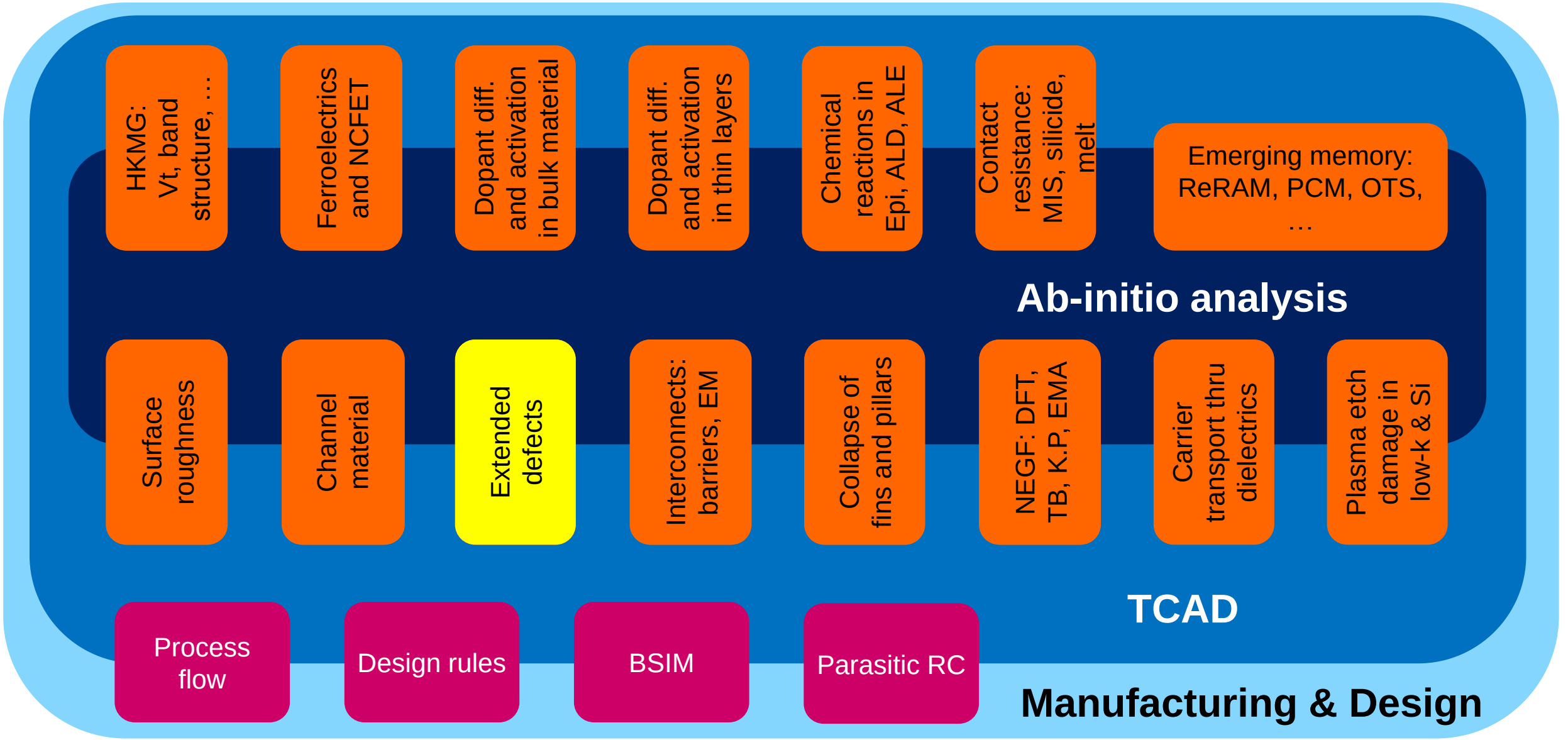
Outline



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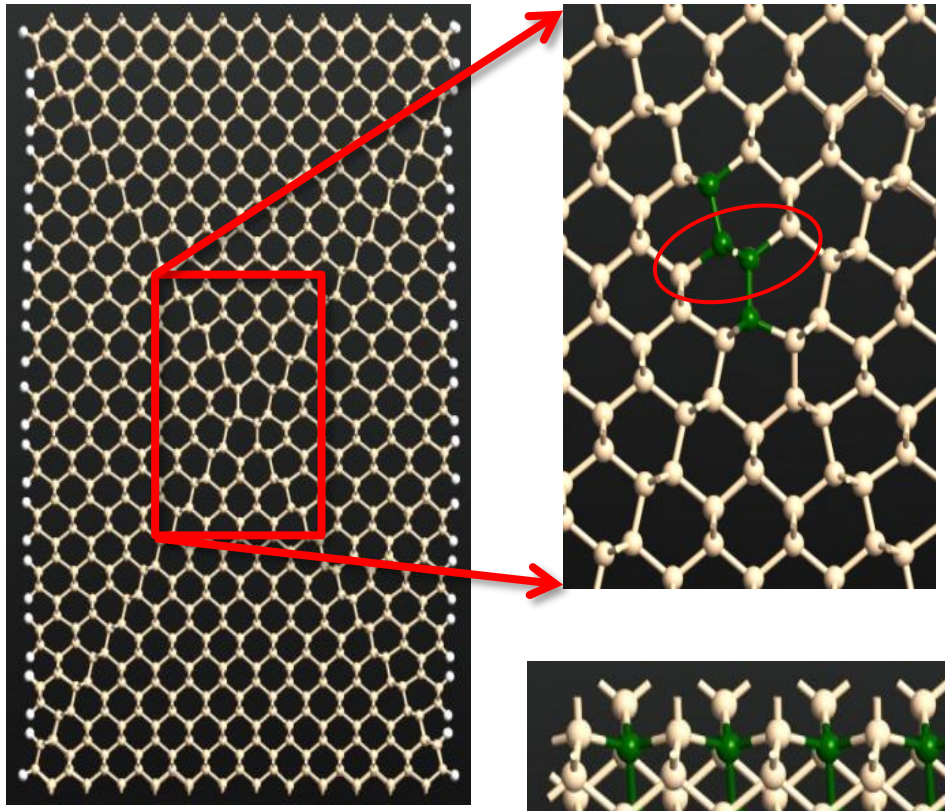
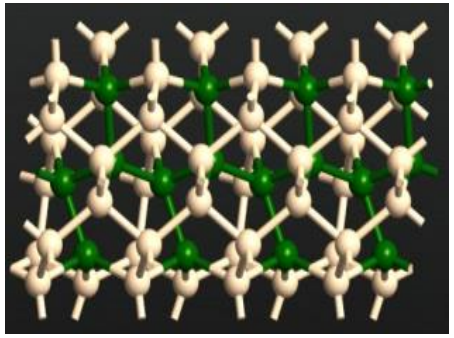
Si Stacking Fault DFT Analysis (A.Pourghaderi, Samsung)

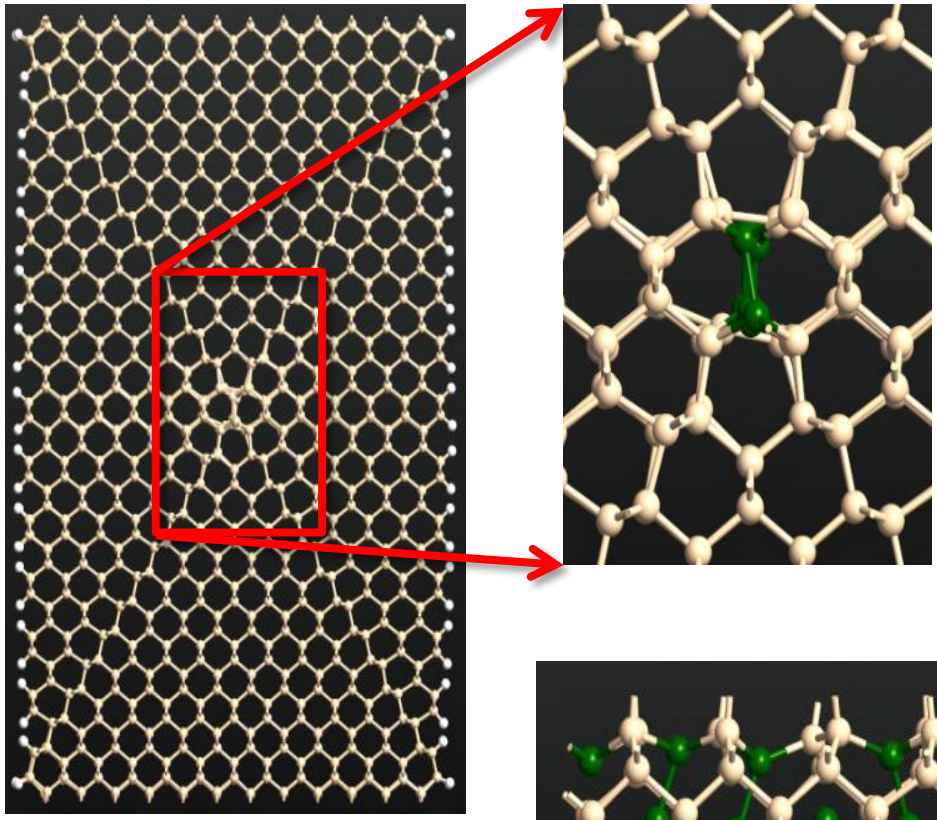
Type B



Side view



Type C



Side view

Green color for is for guiding the eyes only (not dangling bonds)

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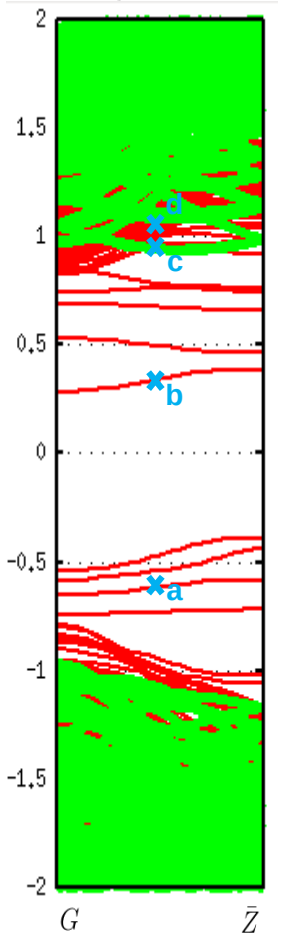
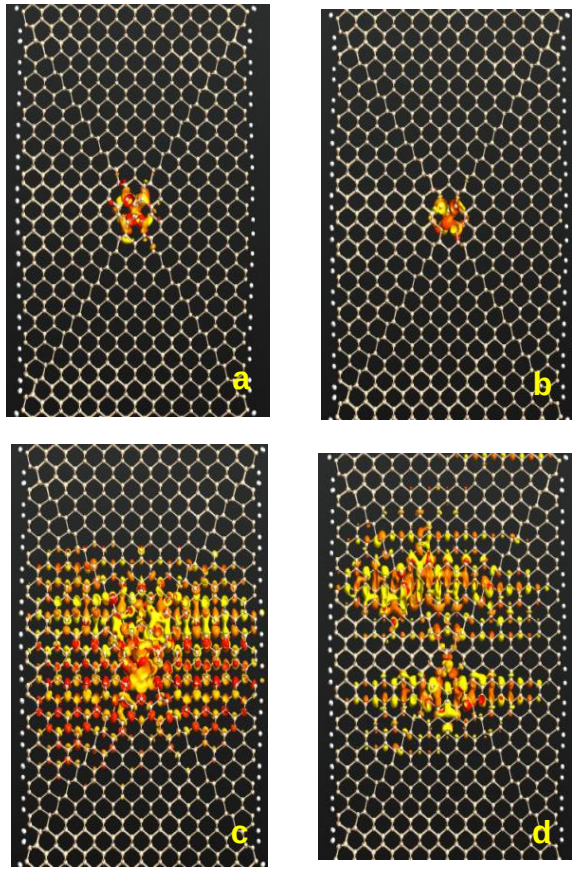
Si Stacking Fault DFT Analysis (A.Pourghaderi, Samsung)

Type C

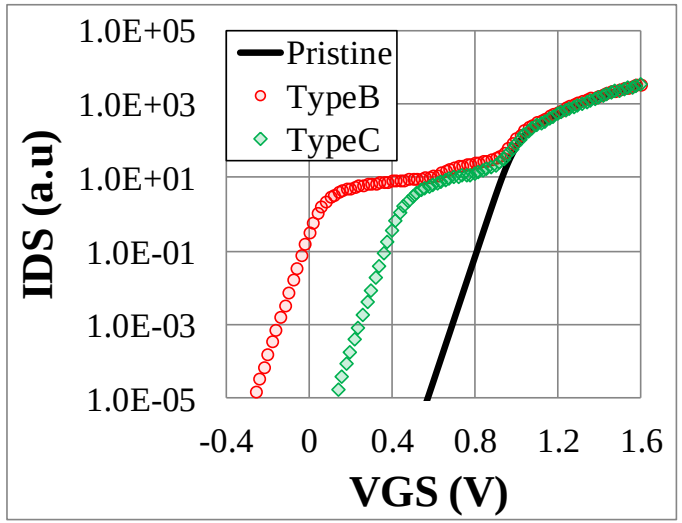


Shape of wavefunctions



Localized near the crossing point of stacking faults

Bulk-like wave-function (inside cond. band)



- TypeB results match the leakage level & floor in HW

DFT calculation details

Quantumwise GGA-PBE exfunctional
SingleZeta basis function (minimal)
(in relaxation calculation) Force criterion: 0.05eV/A
Number of atoms in each structure:
Type B and type C: 2,808 (4 unitcell thick in z direction)
TAT: Relaxation within 3~5 days using 144 cpu cores

Green: pristine silicon bandstructure
Red: bandstructure of Si with crossing stacking fault

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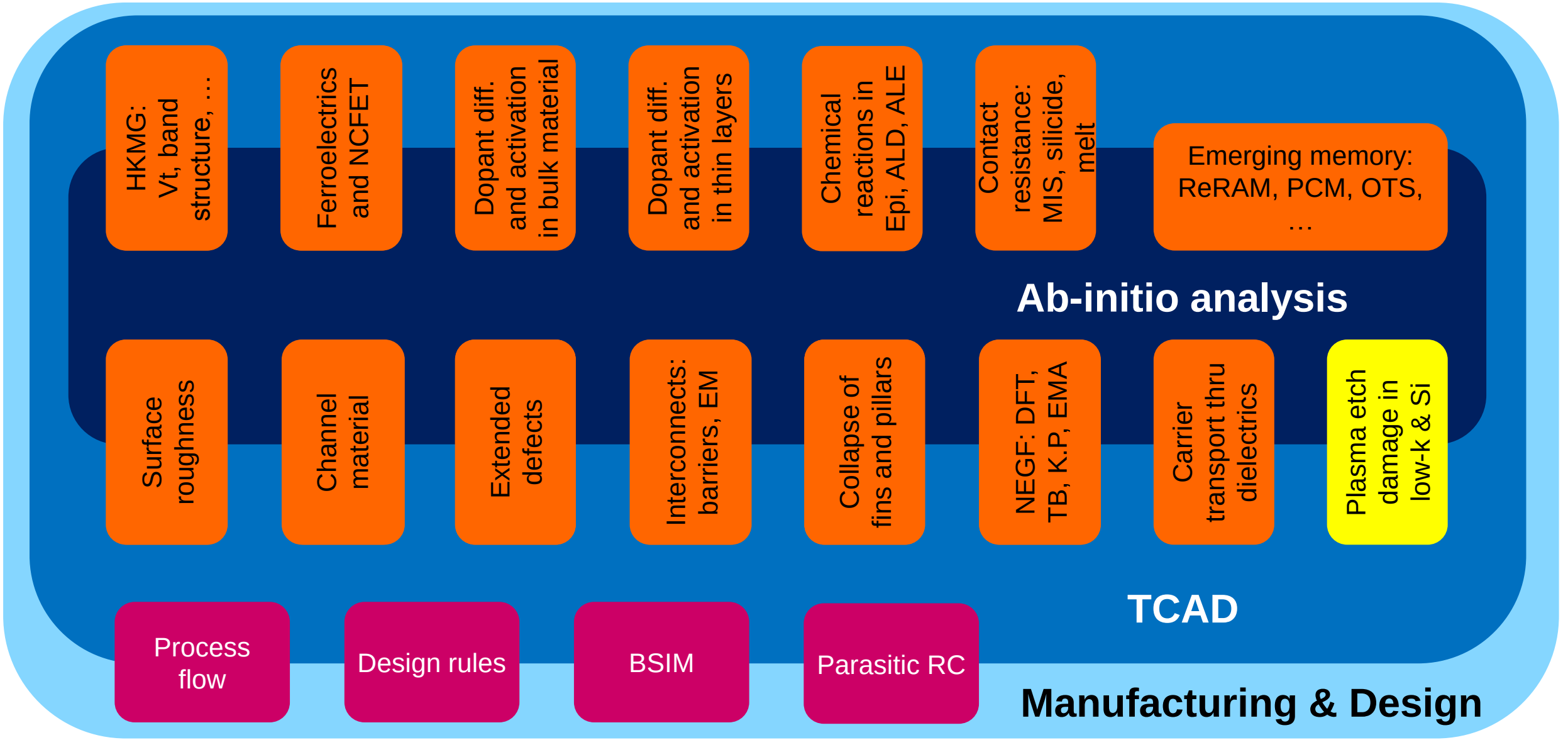
Outline



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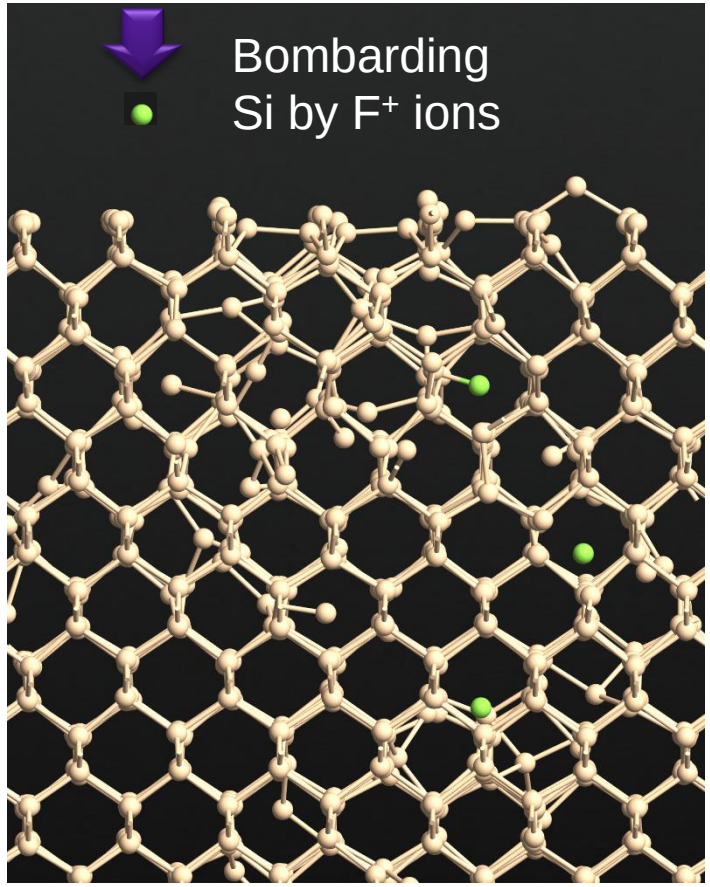
Plasma Etch Damage Analysis: Fluorine Hitting Silicon

Timeline: initial



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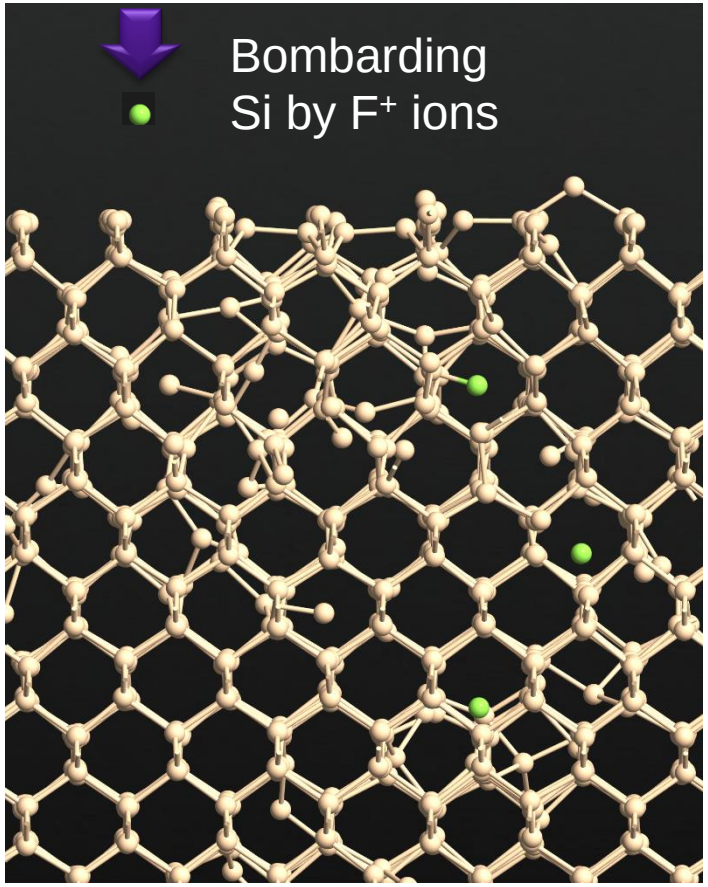
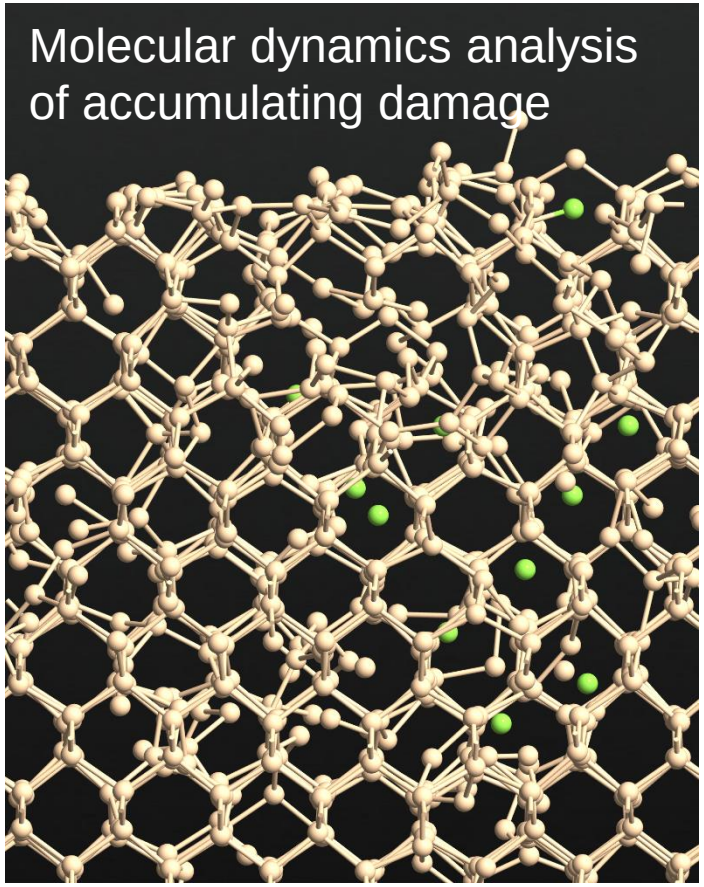
Plasma Etch Damage Analysis: Fluorine Hitting Silicon

Timeline: initial → intermediate





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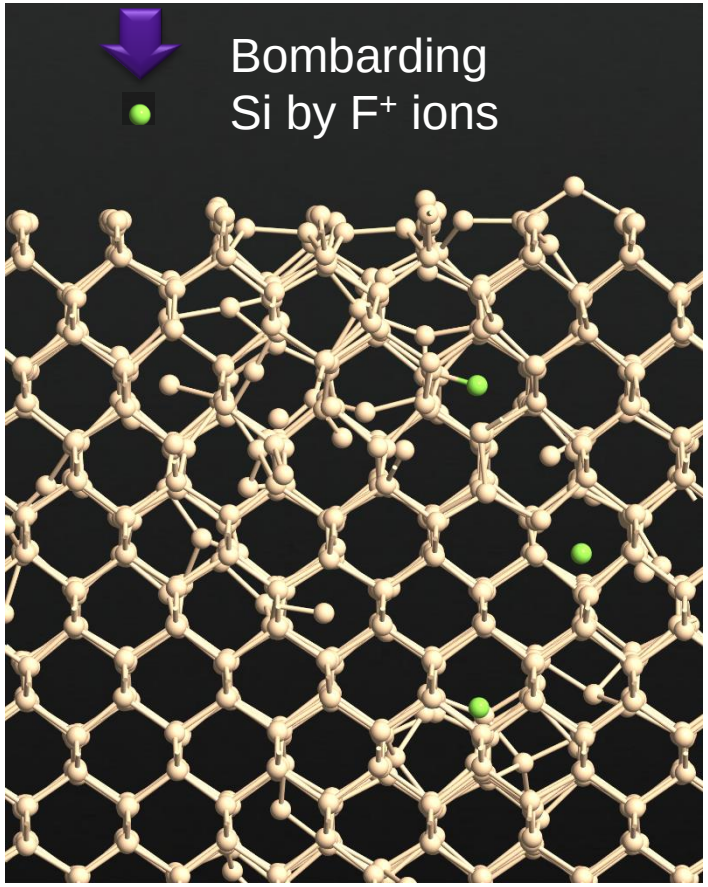
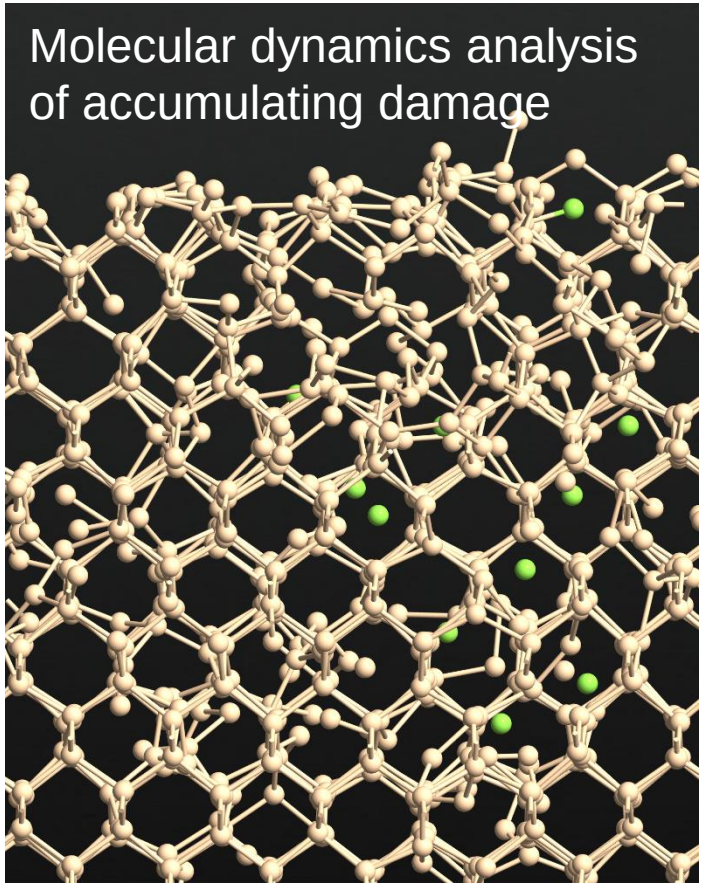
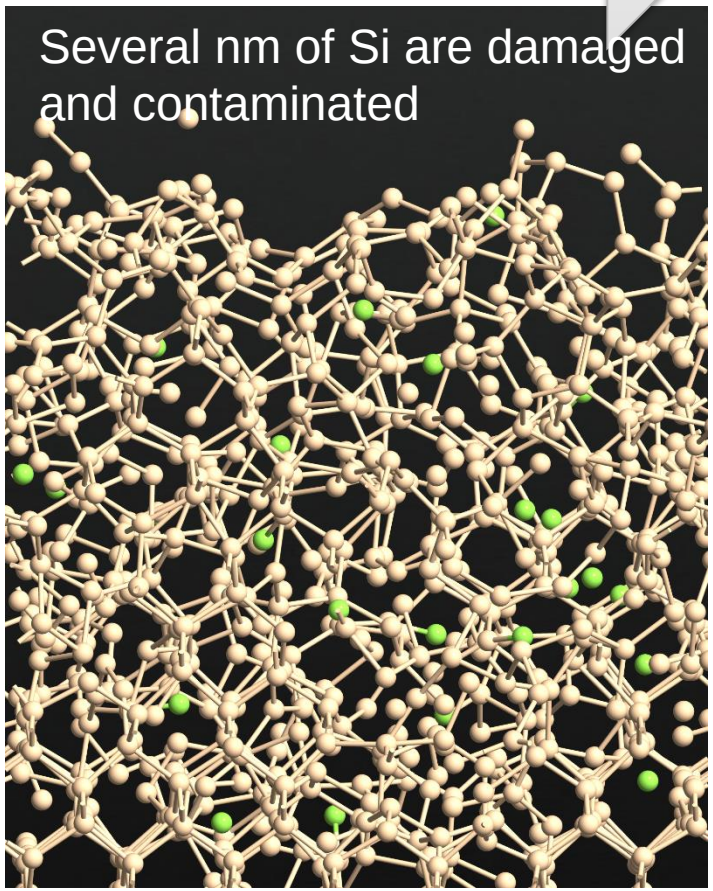
Plasma Etch Damage Analysis: Fluorine Hitting Silicon

Timeline: initial → intermediate → final







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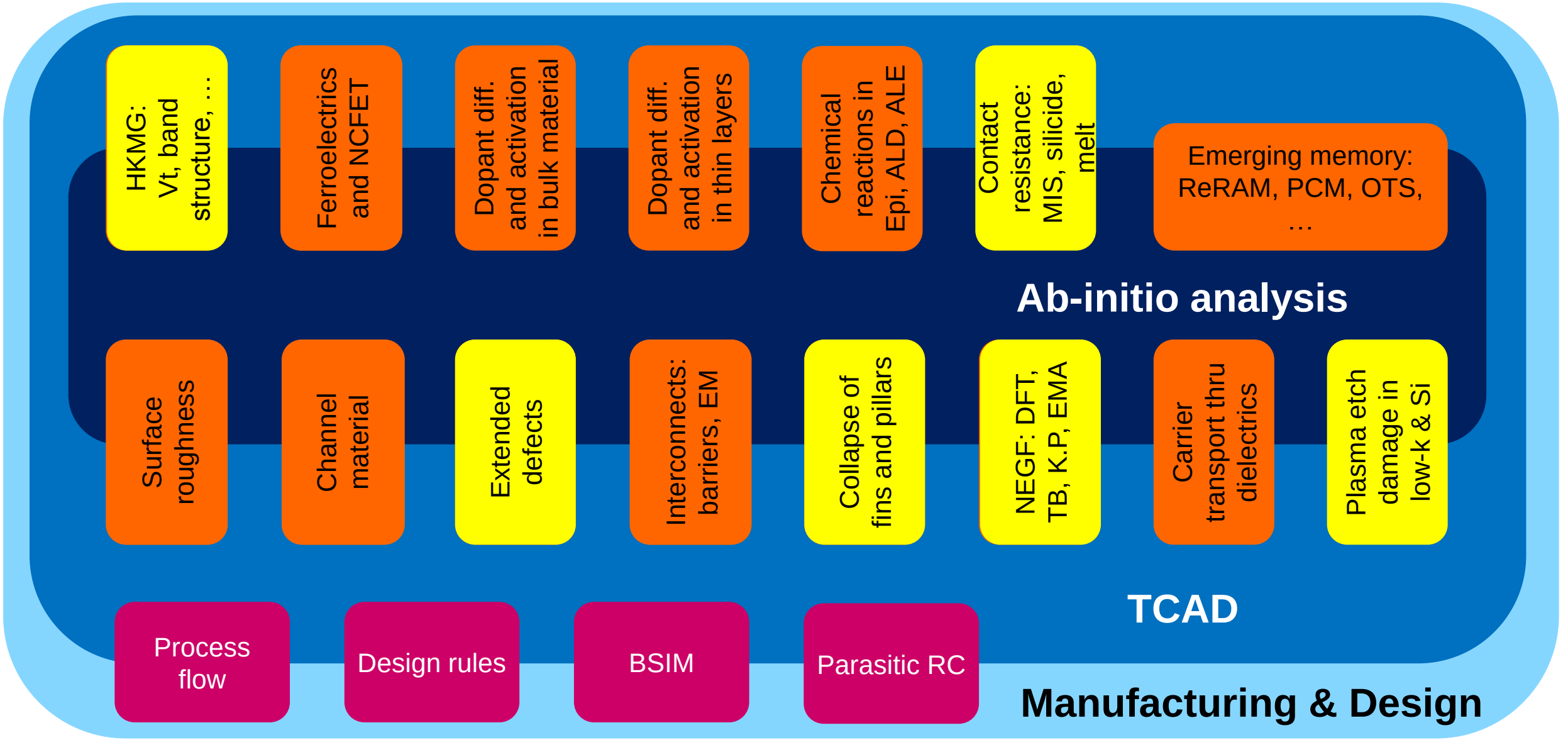
Outline



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Summary

- Increasing number of technology issues require understanding on atomic level to enable material engineering and transistor design
- Thin layers (below ~5nm) exhibit different properties than bulk material and can only be accurately analyzed by atomic methods
- We reviewed application of *ab initio* analysis tools to characterize some of the major technology issues