Dual Beam nSec Annealing for MOL & BEOL Applications

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Outline

• Dual beam nSec annealing technology
• Applications in MOL
• Applications in BEOL
Benefits for nSec Melt Annealing

Super Activation

- Super activation above solid solubility
- Ultra-shallow, box-like abrupt junction

Junction Profile
Conventional nSec Melt Annealing Challenges

- Non-uniform optical absorption
- Inhomogeneous thermal properties

- Severe pattern effect
- Very small or no process window
- Gate on oxide physical integrity also a concern

Pulsed Laser

Junction melt uniformity issue
Physical integrity issue

Poly/STI overheated & damaged
S/D and gate region is intact

Melt Depth (nm)

Isolated area
Dense area

Δ_ptn

0 5 10 15 20 25

Laser fluence
Dual Beam nSec Technology Advantages

- mSA provides low thermal budget & uniform heating
- nSec spike on top of MSA raises T to melt
- Pattern effect is significantly improved

![Diagram showing temperature vs time for conventional and LXA (w/ PH) processes](image)

**Reduction factor**

\[
\Delta T_{LXA} \approx \Delta T_{ns} = \left( \frac{T_{pk} - T_{PH}}{T_{pk} - T_{sub}} \right) \cdot \Delta T_{LTA}
\]

**Conventional nSec Anneal (no PH)**

- **nSec melt laser**
- **mSec non-melt preheat laser**

**LXA (w/ PH)**

- **nSec laser heating**
- **MSA preheat**

- **Reduction factor**
Optical Pattern Effects

Pre-heat reflectance

532nm reflectance

- 532 shows more optical pattern effects
- PH laser enables significant reduction of pattern effects
nSec Anneal for MOL Applications
MOL Application – Contact Rc Reduction

- Contact open
- Trench EPI (optional)
- I/I
- nSec LXA **meta-stable alloy formation**
- Preclean
- Metal liner/plug
- MSA

IBM Alliance record results:
- \( \rho_c < 1 \times 10^{-9} \ \Omega \cdot \text{cm}^2 \) achieved for N contact
- \( \rho_c < 2 \times 10^{-9} \ \Omega \cdot \text{cm}^2 \) achieved for P contact
mSec MSA Impact on \( V_t \)

- \( V_t \) is sensitive to MSA temperature
- Pattern effect further limits MSA process window
nSec LXA Impact on Vt

- nSec LXA has very low thermal budget
- 3~4X less impact on Vt than mSec anneals
nSec Anneal for BEOL Applications
Key Issue in the Industry – BEOL RC Delay

“BEOL performance/area/cost is the foremost issue for 10/7 nm node” – G. Yeap (VP, QCOM) IEDM 2013

- BEOL RC delay dominating
- Faster transistors don’t matter w/o fast BEOL
Control of BEOL Resistance Is Most CRITICAL

R increase is the root cause

Source: TSMC

- Industry is in urgent demand to control/mitigate Mx R increase
Root Causes for Cu R Skyrocketing

- Fine Cu grains → More grain boundaries → sharp R increase for narrow lines

Source: ITRS
Current Cu RC Delay Improvement Schemes

Current RC Control Solutions

• Enlarging Cu grain, as an effective R reduction method, has been OVERLOOKED before

No roadmap for Cu grain size
Process Flow

- Processed with 14nm BEOL process flow to 10+ Mx
Key Metrics for Evaluation

- Key Metrics include;
  - Cu line resistance
  - M1 capacitance
  - RC performance
  - Cu Grain Size
  - Impact on FEOL FETs
  - Reliability ($V_{BD}$, EM Lifetime)
Cu Line Resistance

- nSec enables 35% R reduction

R Lee et al, VLSI 2018
M1 Capacitance after nSec Anneal

- ULK capacitance increase 9% after nSec anneal
- Plans available to improve capacitance

*R. Lee et al, VLSI 2018*
nSec Anneal Impact on ULK

- $\kappa$ value increases $\sim 3\%$
- Young’s modulus improves $\sim 12\%$

R Lee et al, VLSI 2018
RC Improvement w/ nSec Anneal

- An impressive -15% RC improvement is achieved
Cu Grains after nSec Anneal

- 2.7X larger grains
- More bamboo like structures

R Lee et al, VLSI 2018
nSec Cu Anneal Impact on Devices

- +2% for NMOS
- +5% for PMOS

R Lee et al, VLSI 2018
M1-M1 Dielectric $V_{bd}$ after nSec Anneal

- 10% improvement, due to more interconnecting bonds

R Lee et al, VLSI 2018
EM Lifetime

- Comparable/better EM lifetime after anneal
# Summary

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Performance</th>
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</thead>
<tbody>
<tr>
<td>Line Resistance</td>
<td>+ 35%</td>
</tr>
<tr>
<td>Capacitance</td>
<td>- 9% (tunable)</td>
</tr>
<tr>
<td>RC Performance</td>
<td>+ 15%</td>
</tr>
<tr>
<td>Median Cu Grain Size</td>
<td>+ 2.7X</td>
</tr>
<tr>
<td>N/PMOS $I_{Dsat}$</td>
<td>+ 2%, +5%</td>
</tr>
<tr>
<td>M1-M1 Dielectric $V_{SD}$</td>
<td>+ 10%</td>
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<tr>
<td>V0-M1 EM Lifetime</td>
<td>+ 27%</td>
</tr>
<tr>
<td>V1-M1 EM Lifetime</td>
<td>+ 36%</td>
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