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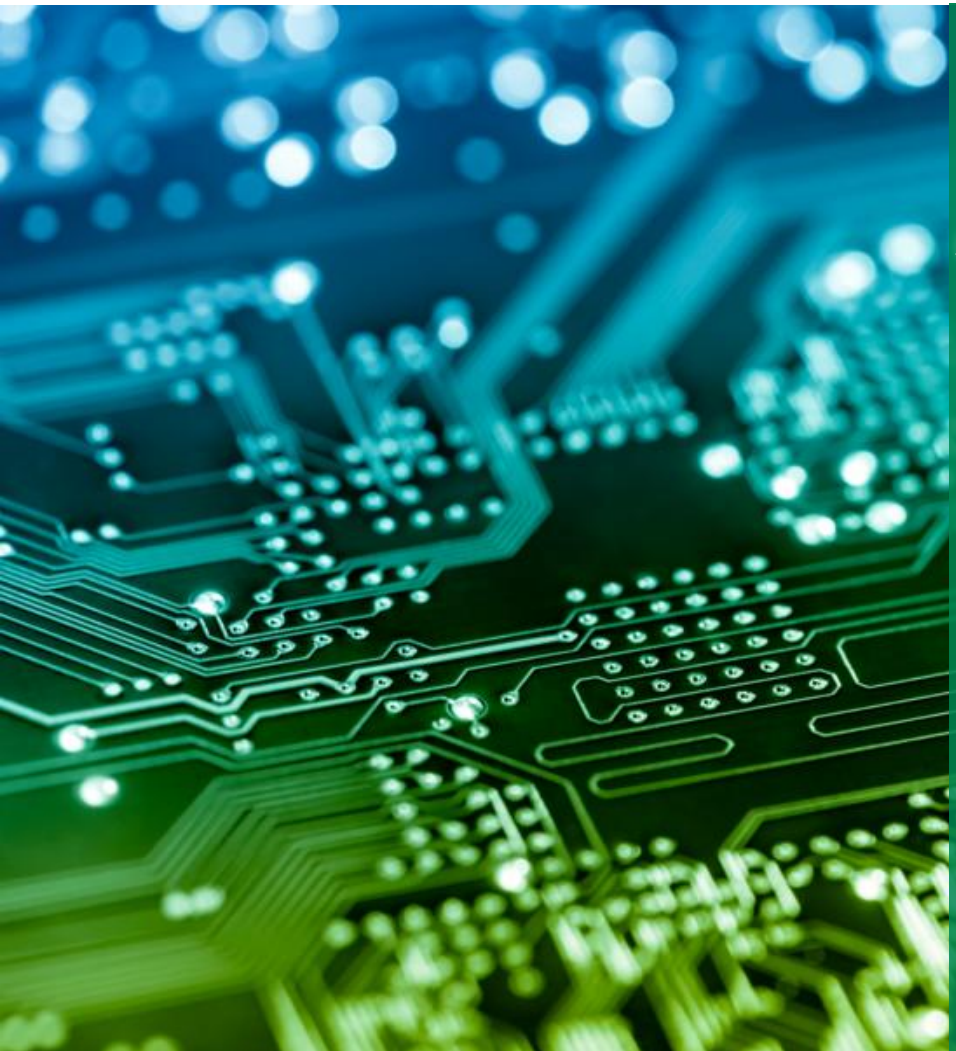

Dual Beam nSec Annealing for MOL & BEOL Applications

Shaoyin Chen

Chief Technical Scientist, LP

- Ultratech, Division of Veeco
- San Jose, CA, USA

- July 2018

Outline

- Dual beam nSec annealing technology
- Applications in MOL
- Applications in BEOL

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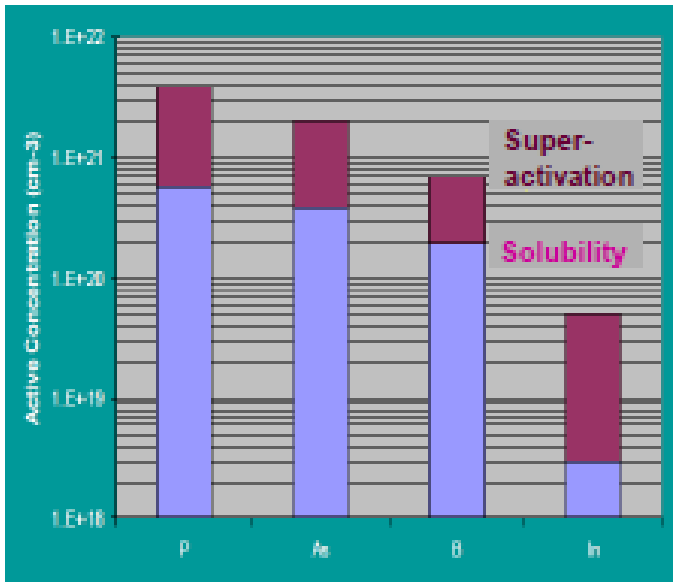
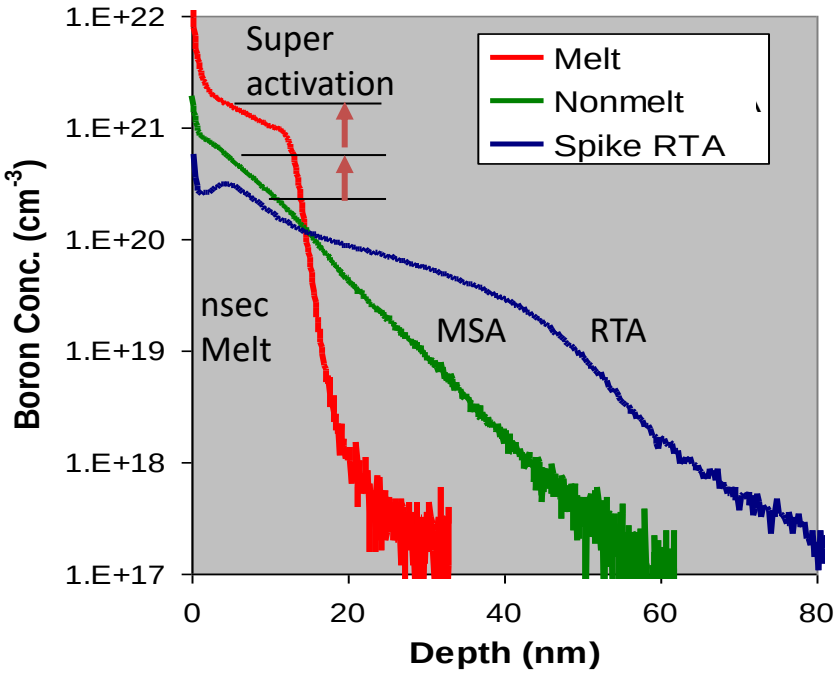
Benefits for nSec Melt Annealing

Super Activation



Junction Profile



- Super activation above solid solubility
- Ultra-shallow, box-like abrupt junction

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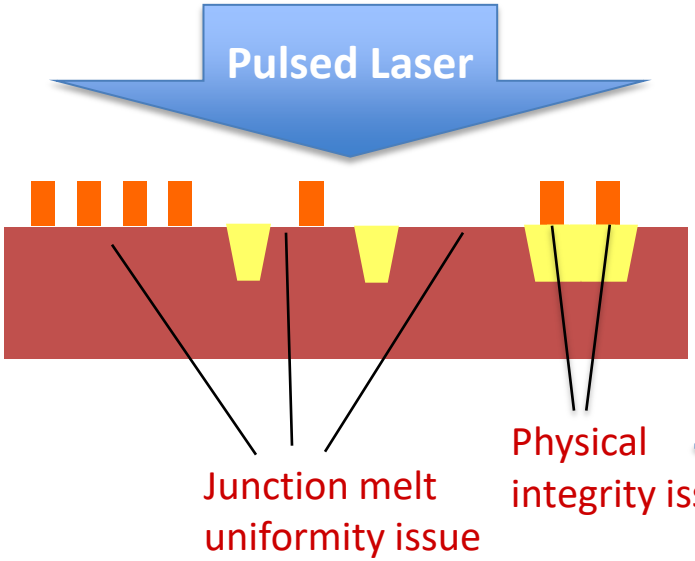
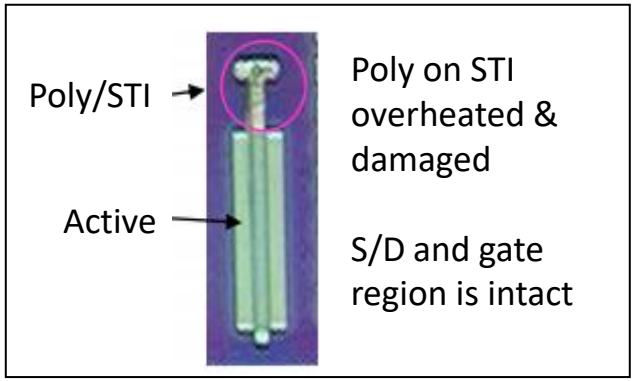
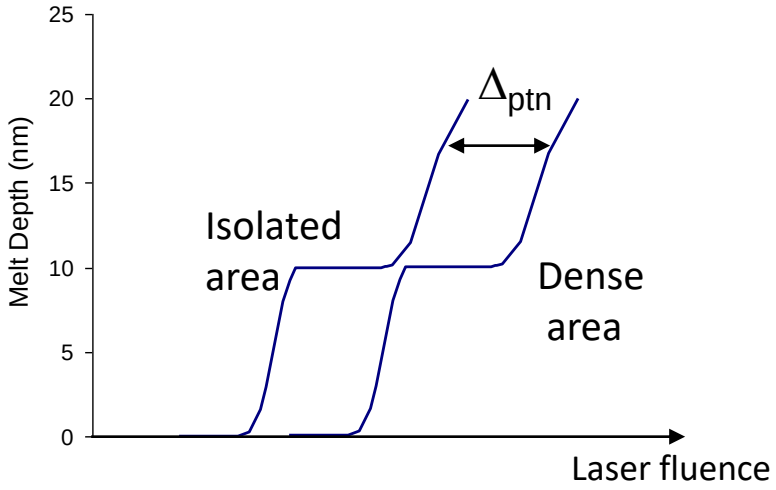
Conventional nSec Melt Annealing Challenges



- Non-uniform optical absorption
- Inhomogeneous thermal properties





- **Severe pattern effect**
- **Very small or no process window**
- **Gate on oxide physical integrity also a concern**

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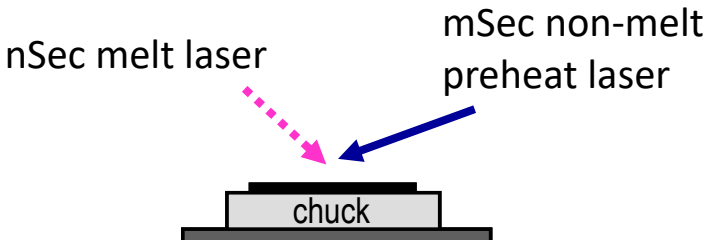
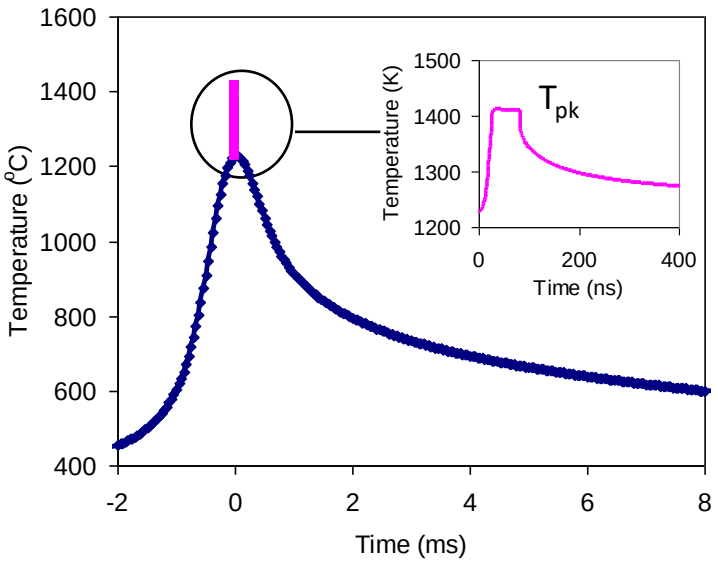
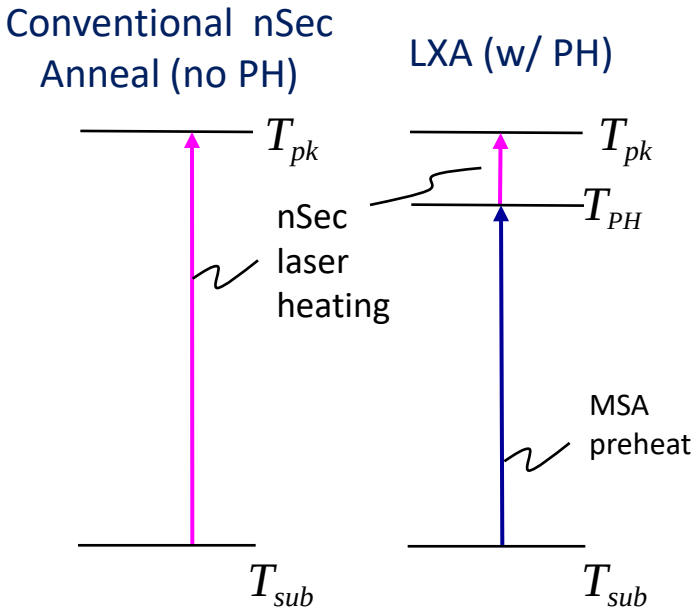
Dual Beam nSec Technology Advantages





Reduction factor

$$\Delta T_{LXA} \approx \Delta T_{ns} = \left(\frac{T_{pk} - T_{PH}}{T_{pk} - T_{sub}} \right) \cdot \Delta T_{LTA}$$



- mSA provides low thermal budget & uniform heating
- nSec spike on top of MSA raises T to melt
- Pattern effect is significantly improved

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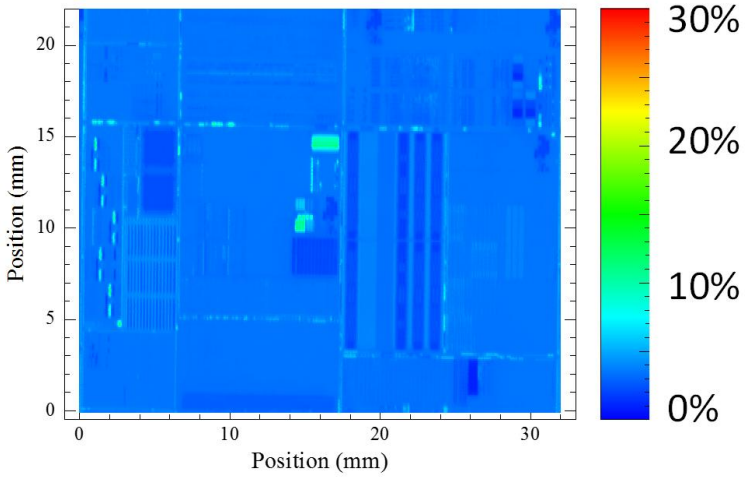
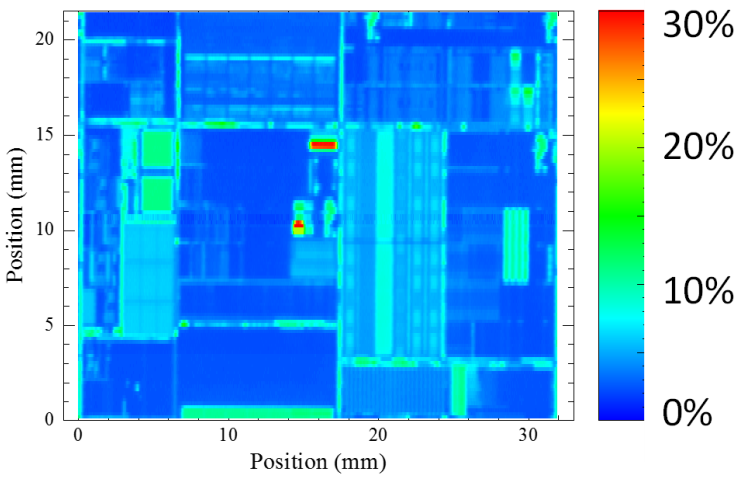
Optical Pattern Effects

Pre-heat reflectance



532nm reflectance



- 532 shows more optical pattern effects
- PH laser enables significant reduction of pattern effects

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nSec Anneal for MOL Applications

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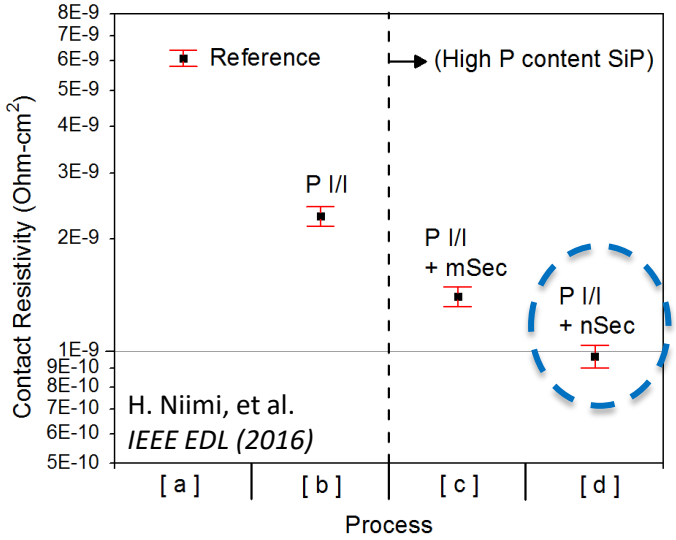
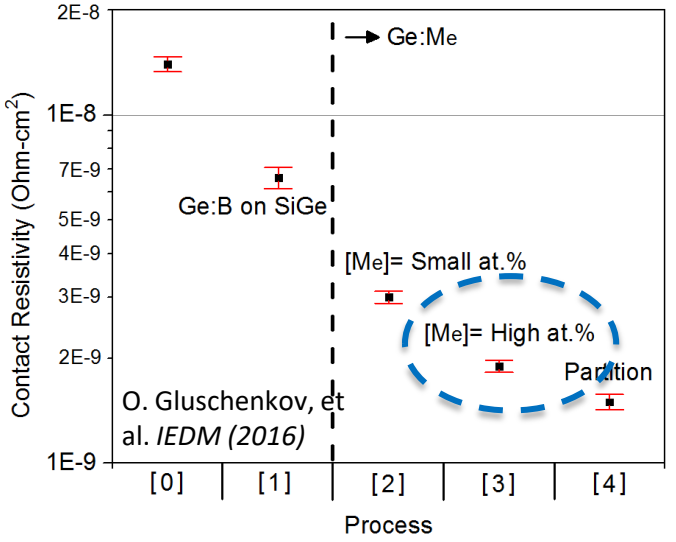
MOL Application – Contact Rc Reduction

- Contact open
- Trench EPI (optional)
- I/I
- nSec LXA

meta-stable alloy formation

- Preclean
- Metal liner/plug
- MSA





IBM Alliance record results:

- ρ_c **<1x10^{-9} Ω-cm^2** achieved for N contact
- ρ_c **<2x10^{-9} Ω-cm^2** achieved for P contact

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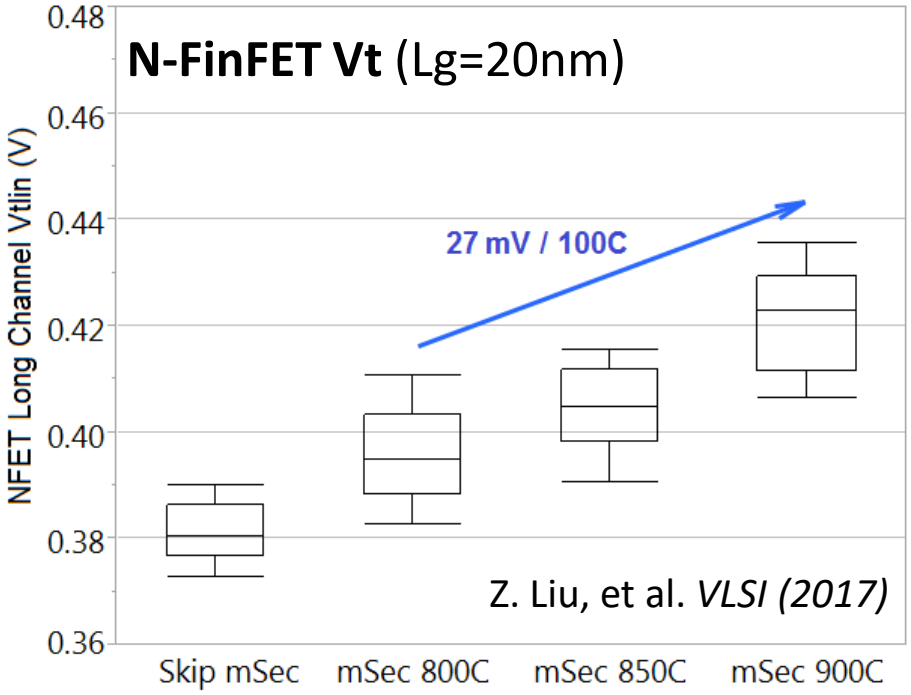
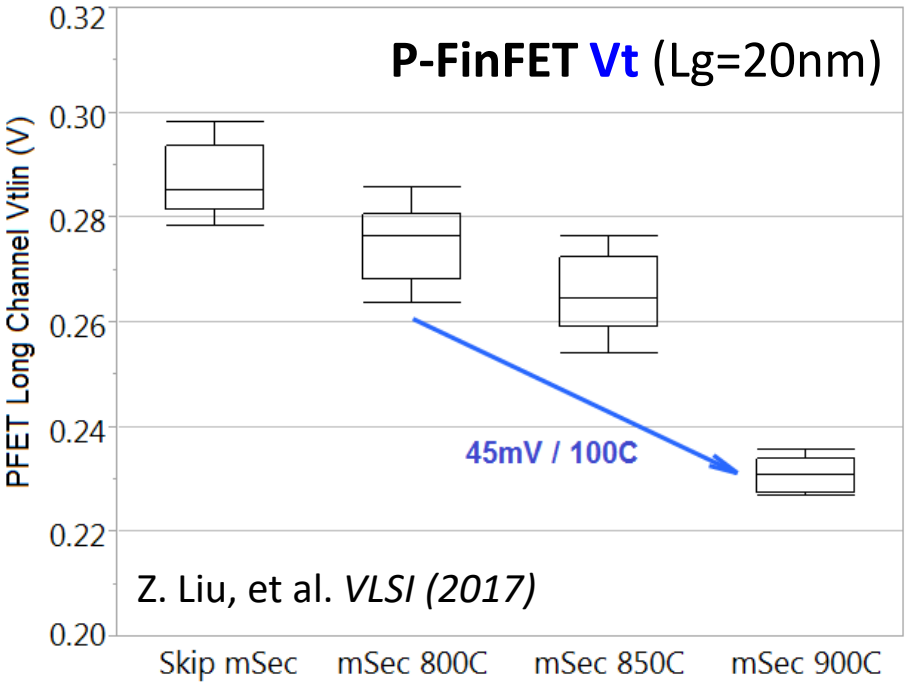
mSec MSA Impact on Vt





- Vt is sensitive to MSA temperature
- Pattern effect further limits MSA process window

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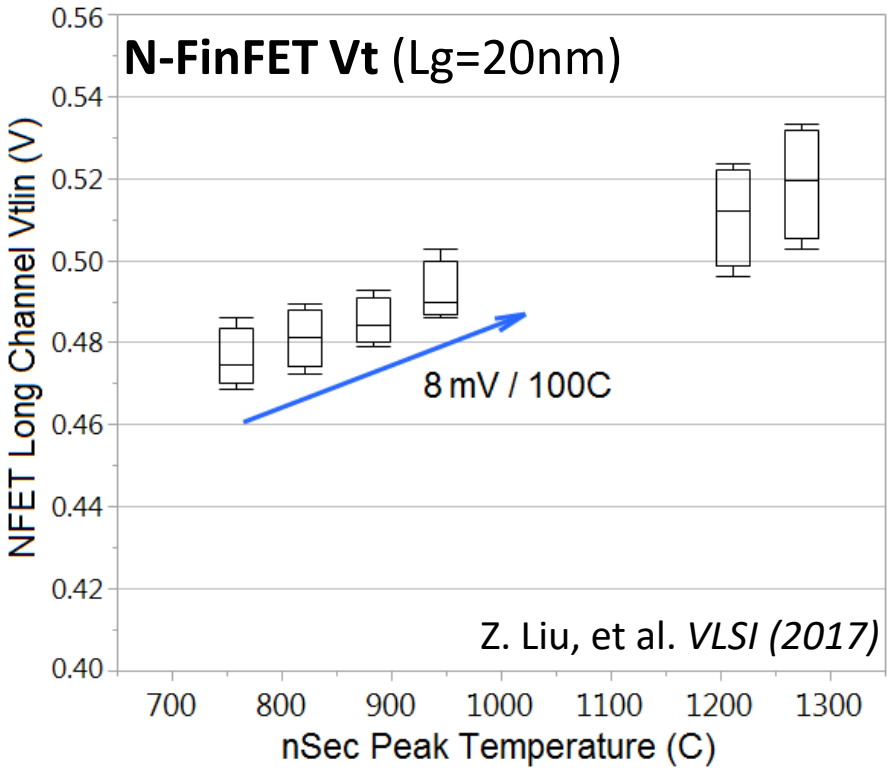
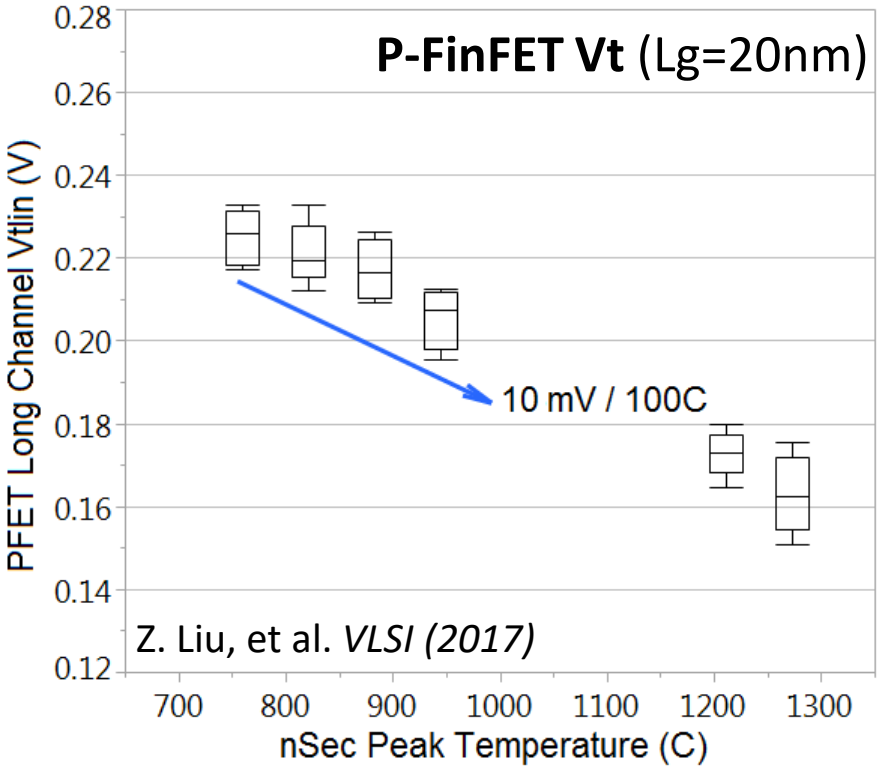
nSec LXA Impact on Vt





- nSec LXA has very low thermal budget
- 3~4X less impact on Vt than mSec anneals

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nSec Anneal for BEOL Applications

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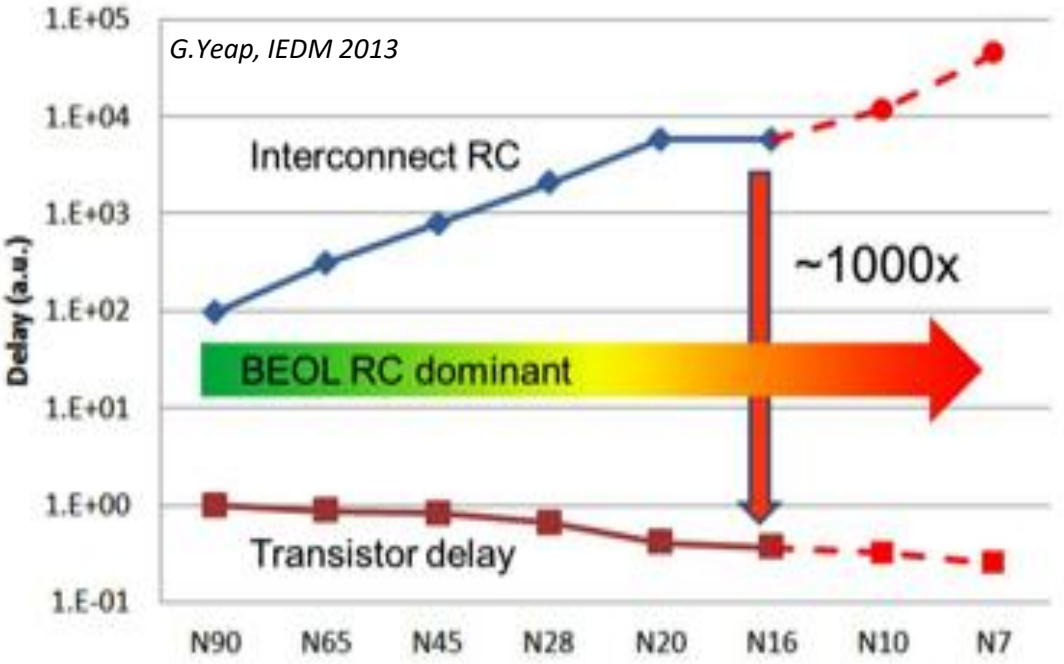
Key Issue in the Industry – BEOL RC Delay

"BEOL performance/area/cost is the foremost issue for 10/7 nm node" – G. Yeap (VP, QCOM) *IEDM 2013*



- BEOL RC delay dominating
- Faster transistors don't matter w/o fast BEOL

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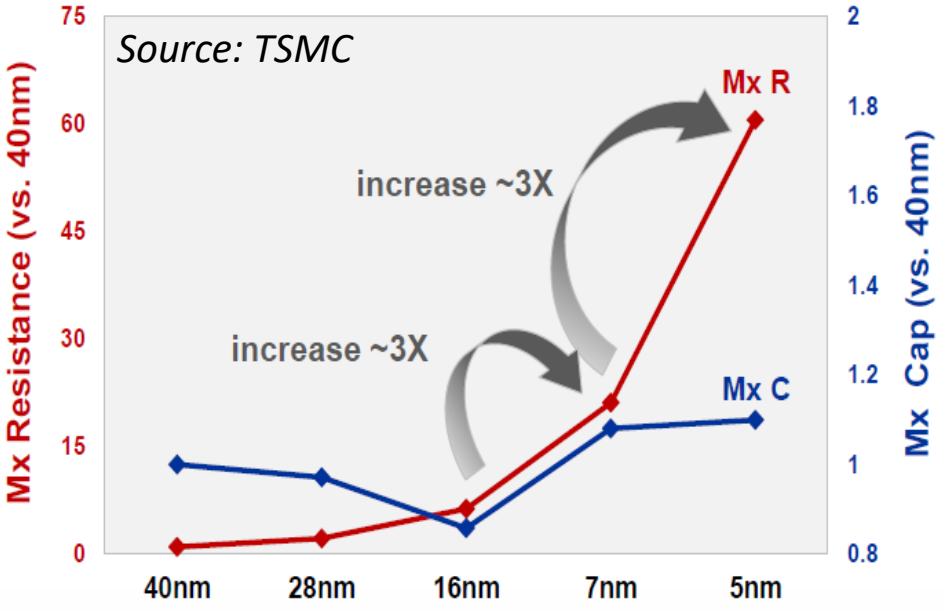
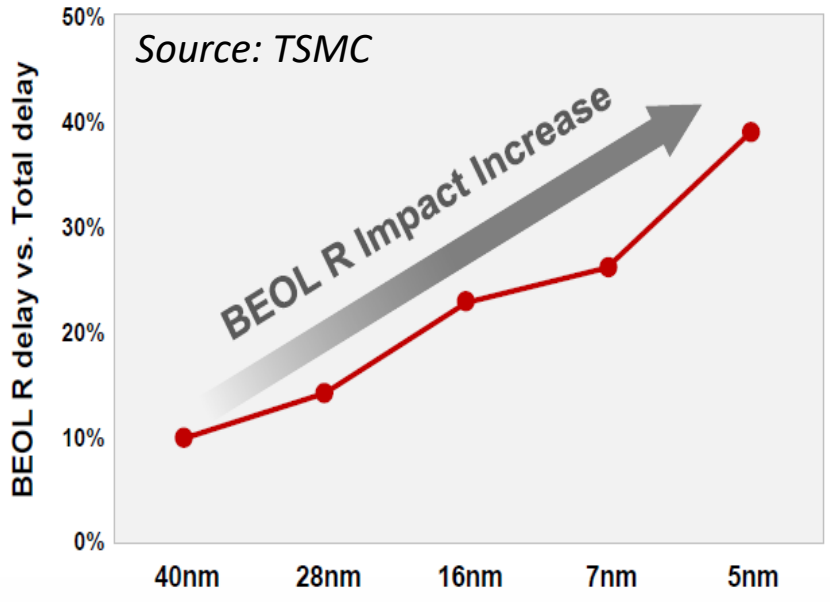
Control of BEOL Resistance Is Most CRITICAL

R increase is the root cause





- Industry is in urgent demand to control/mitigate Mx R increase

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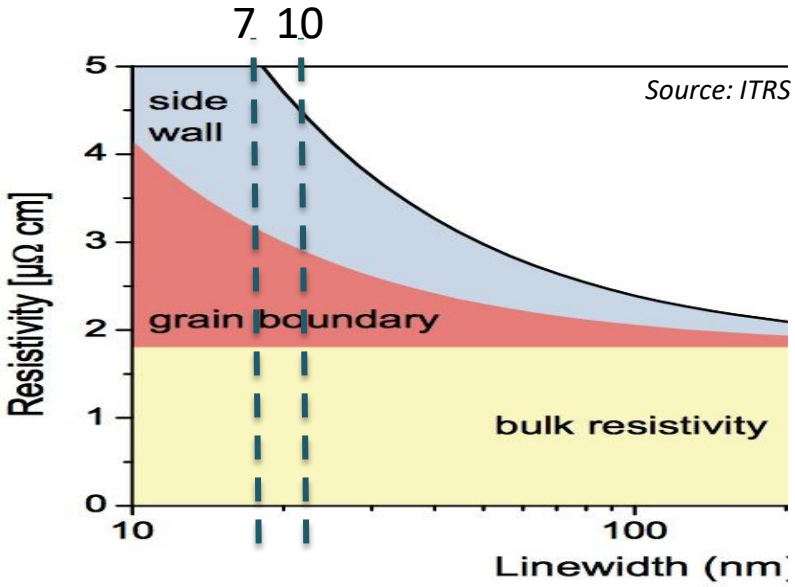
Root Causes for Cu R Skyrocketing



- Fine Cu grains → More grain boundaries → sharp R increase for narrow lines

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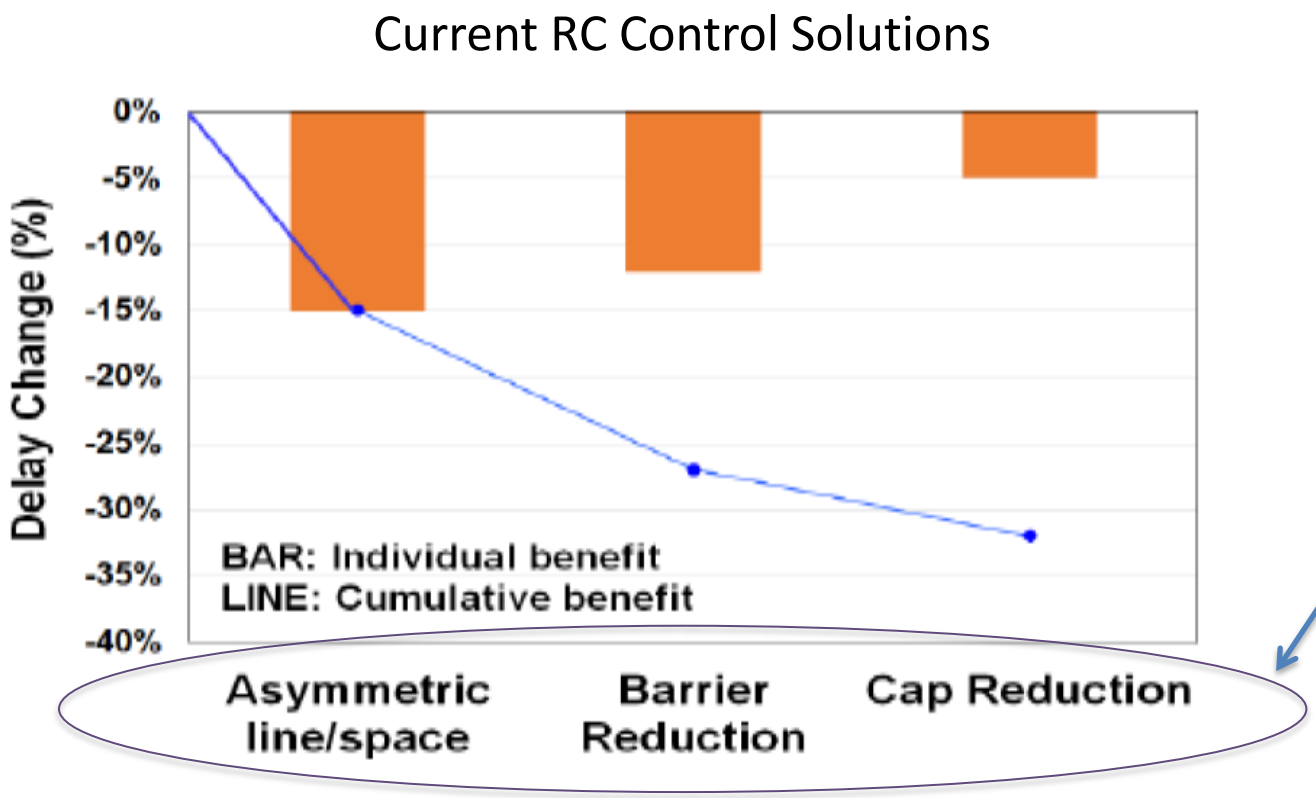
Current Cu RC Delay Improvement Schemes



No roadmap for Cu grain size

- Enlarging Cu grain, as an effective R reduction method, has been OVERLOOKED before

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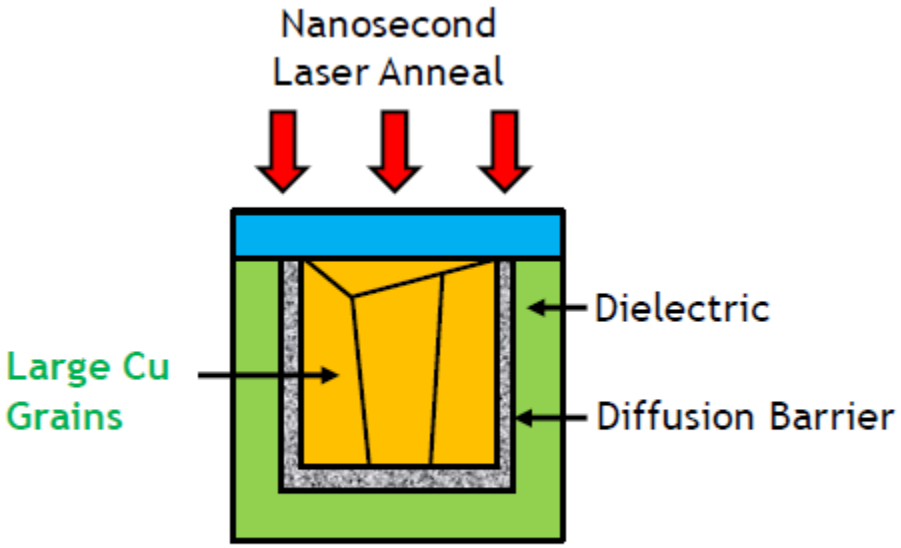
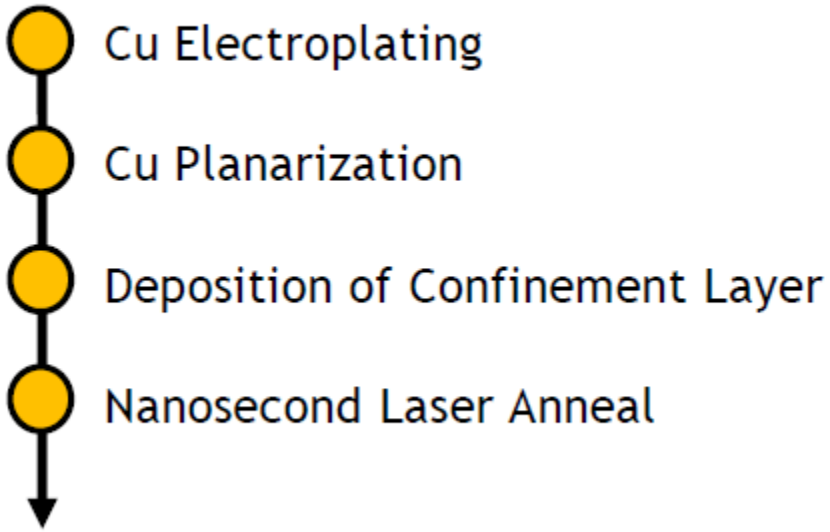
Process Flow





- Processed with 14nm BEOL process flow to 10+ Mx

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Key Metrics for Evaluation

- Key Metrics include;
  - Cu line resistance
  - M1 capacitance
  - RC performance
  - Cu Grain Size
  - Impact on FEOL FETs
  - Reliability (V_{BD}, EM Lifetime)

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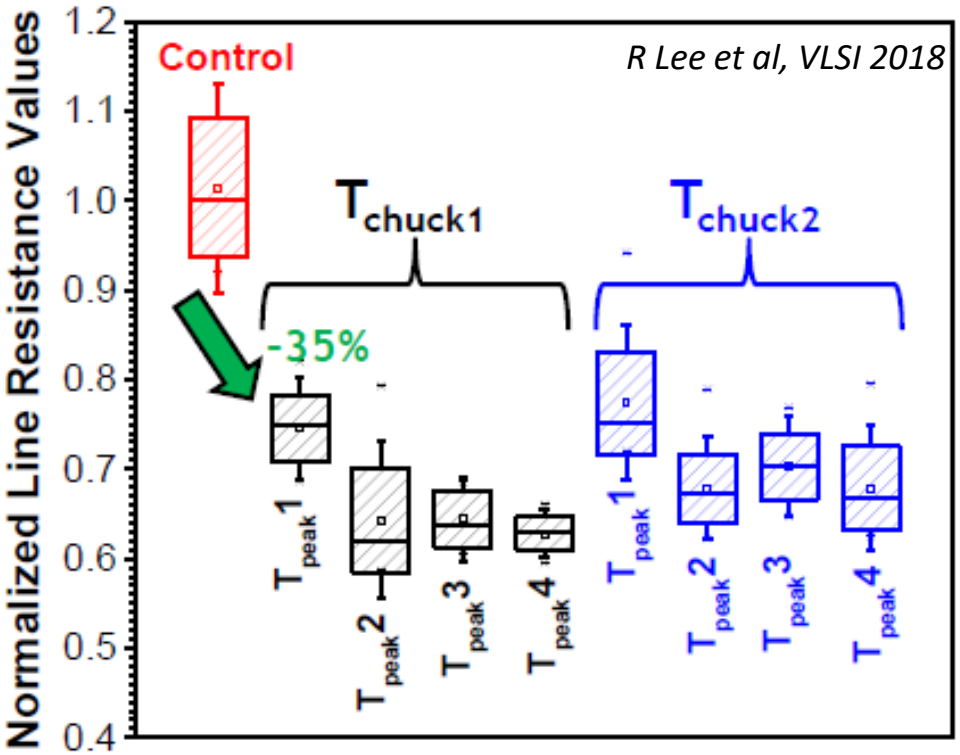
Cu Line Resistance



- nSec enables 35% R reduction

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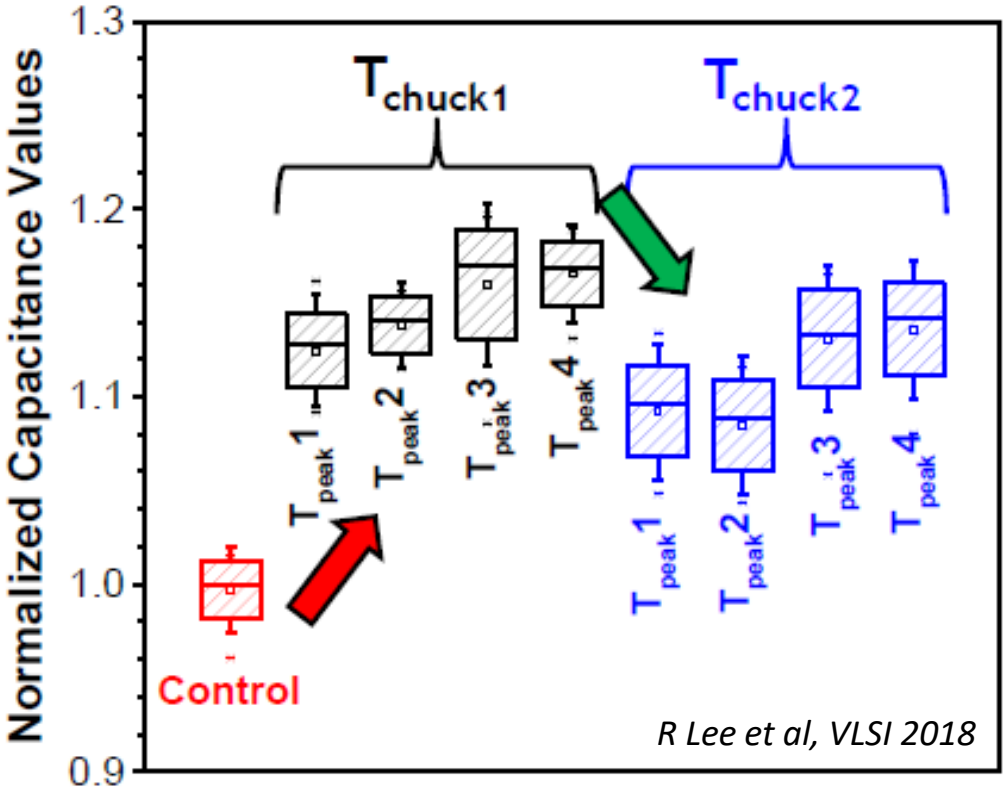
M1 Capacitance after nSec Anneal



- ULK capacitance increase 9% after nSec anneal
- Plans available to improve capacitance

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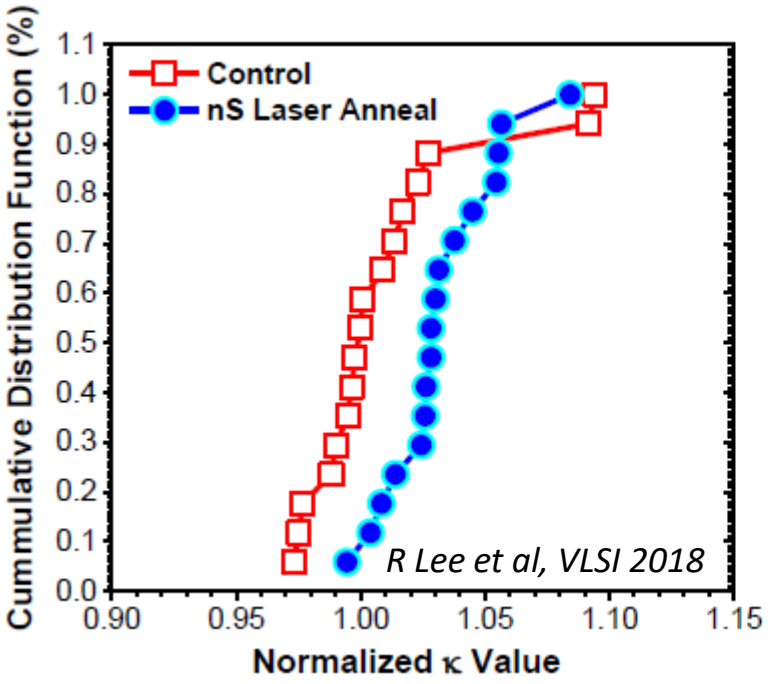
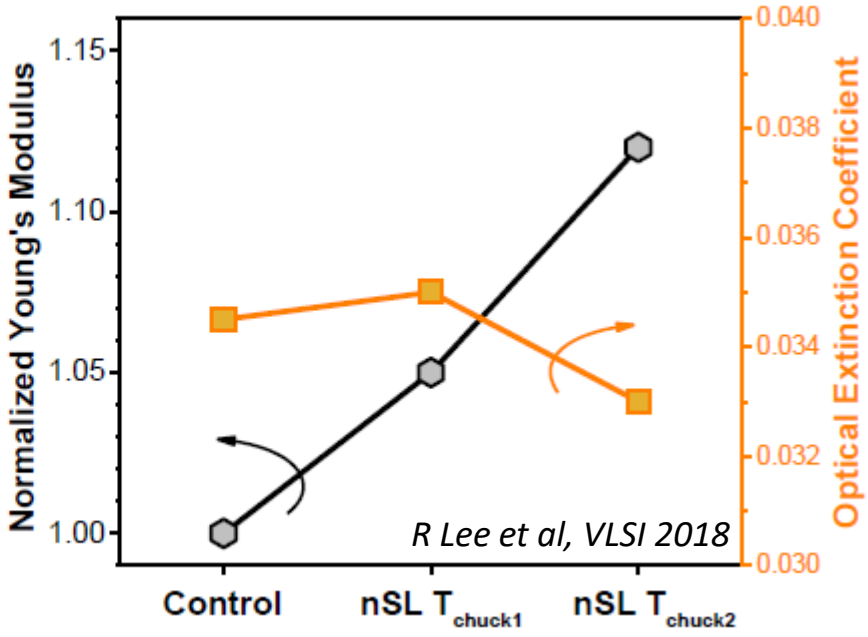
nSec Anneal Impact on ULK





- κ value increases ~3%
- Young's modulus improves ~12%

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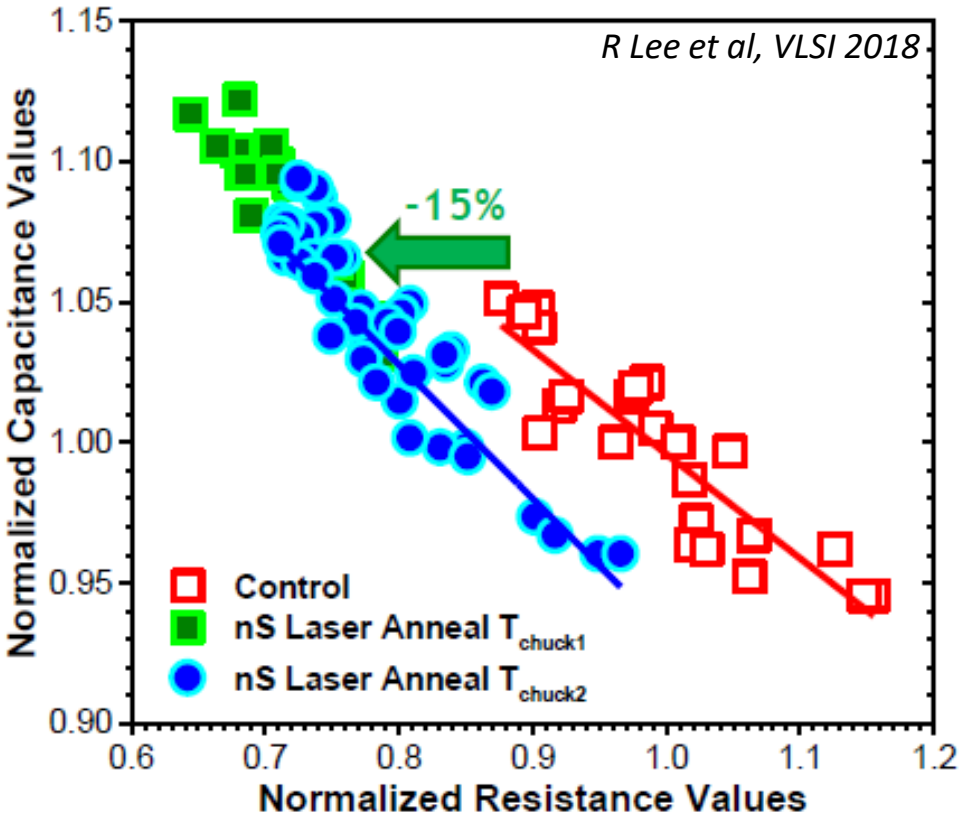
RC Improvement w/ nSec Anneal



- An impressive -15% RC improvement is achieved

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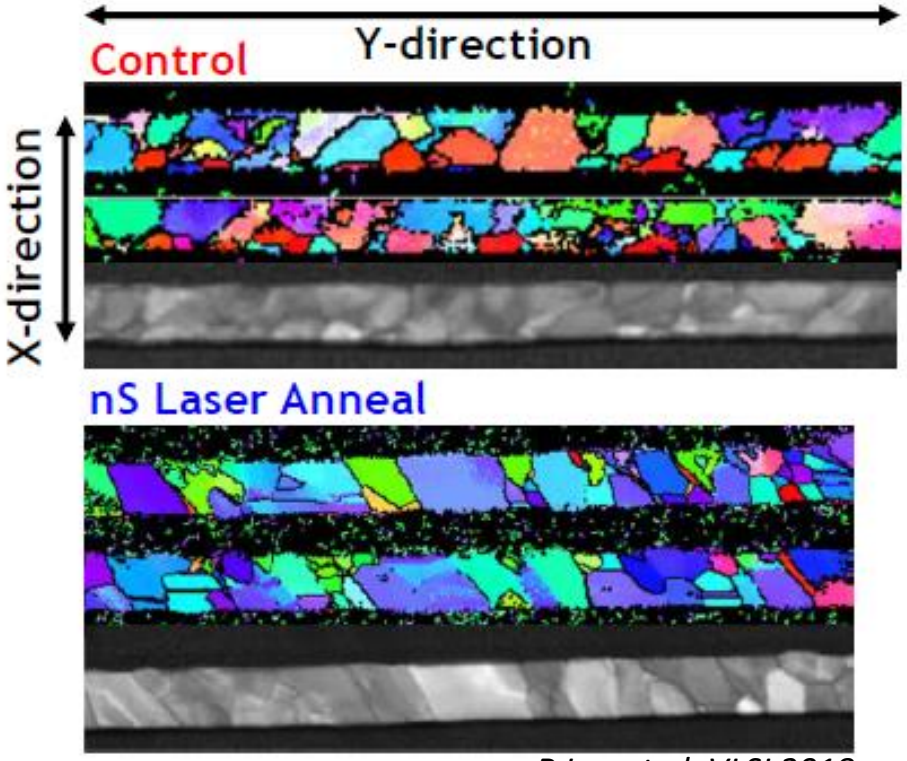
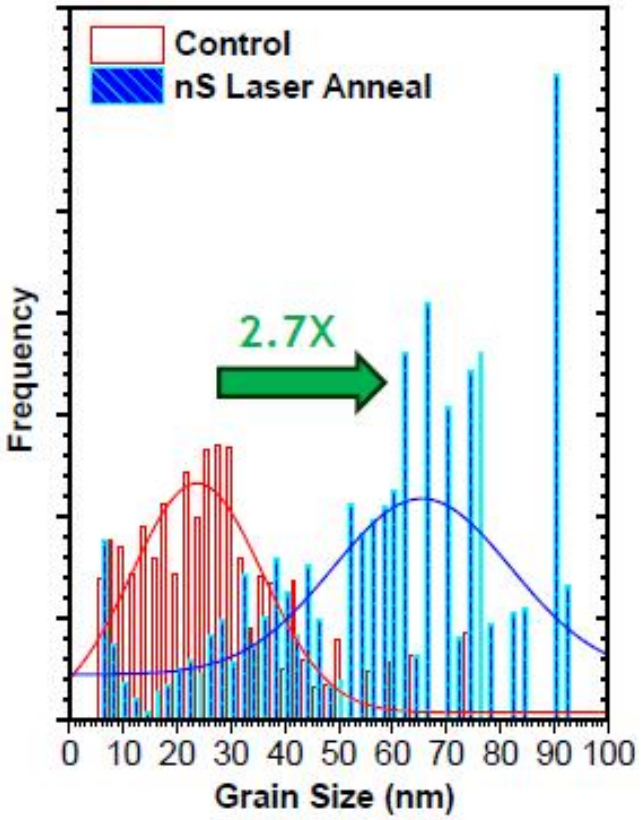
Cu Grains after nSec Anneal



R Lee et al, VLSI 2018



- 2.7X larger grains
- More bamboo like structures

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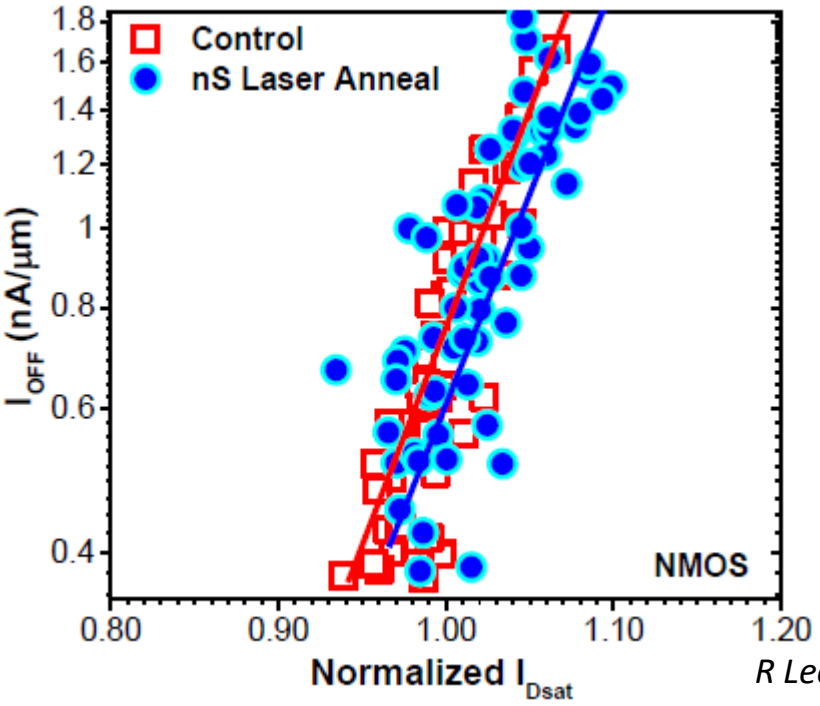
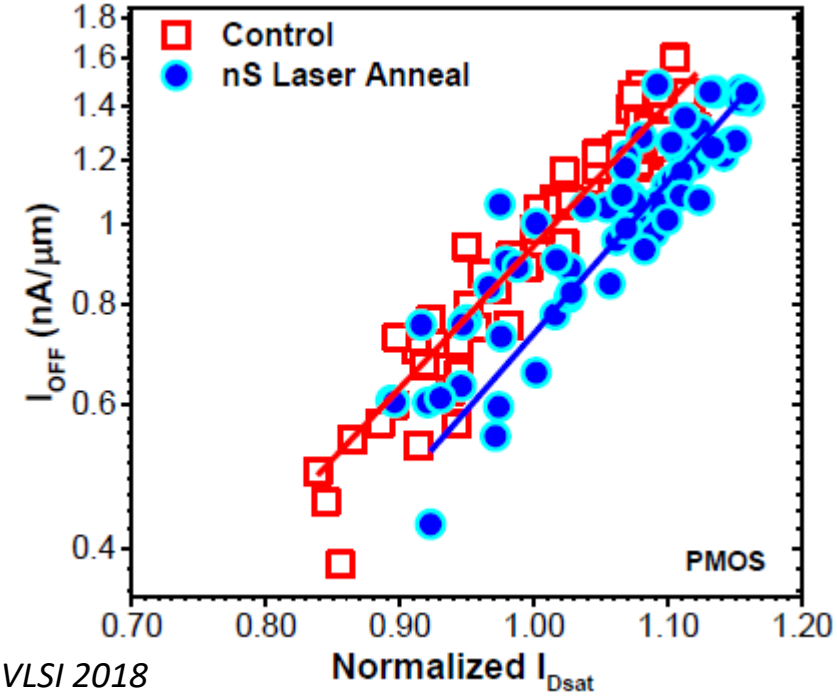
nSec Cu Anneal Impact on Devices

NMOS



PMOS



R Lee et al, VLSI 2018

- +2% for NMOS
- +5% for PMOS

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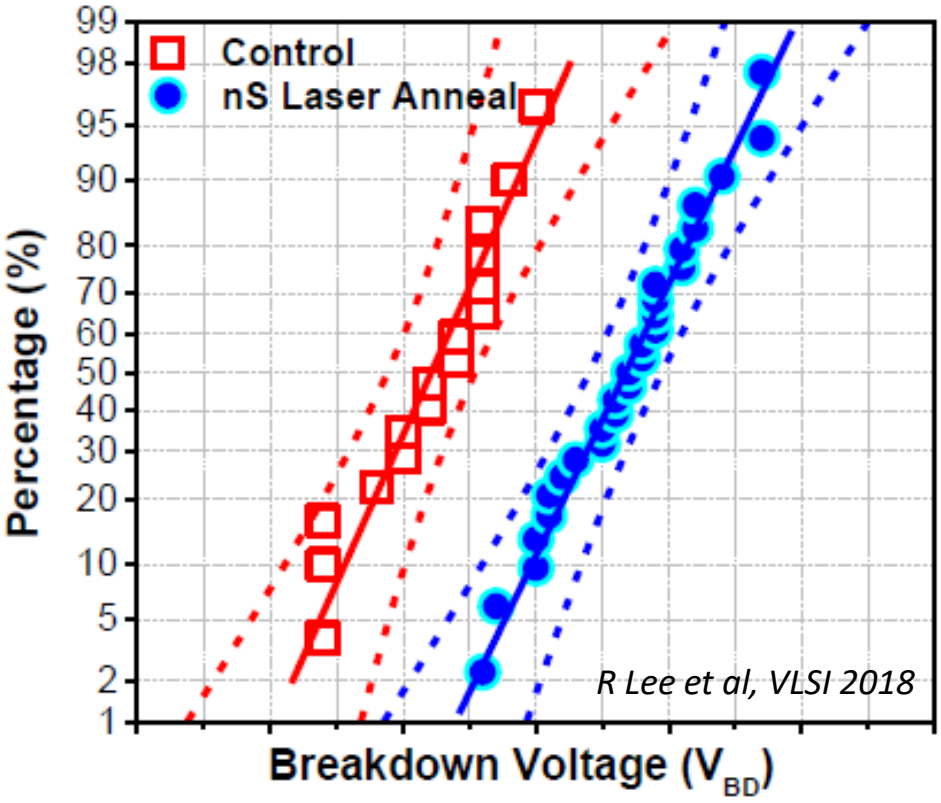
M1-M1 Dielectric V_{bd} after nSec Anneal



- 10% improvement, due to more interconnecting bonds

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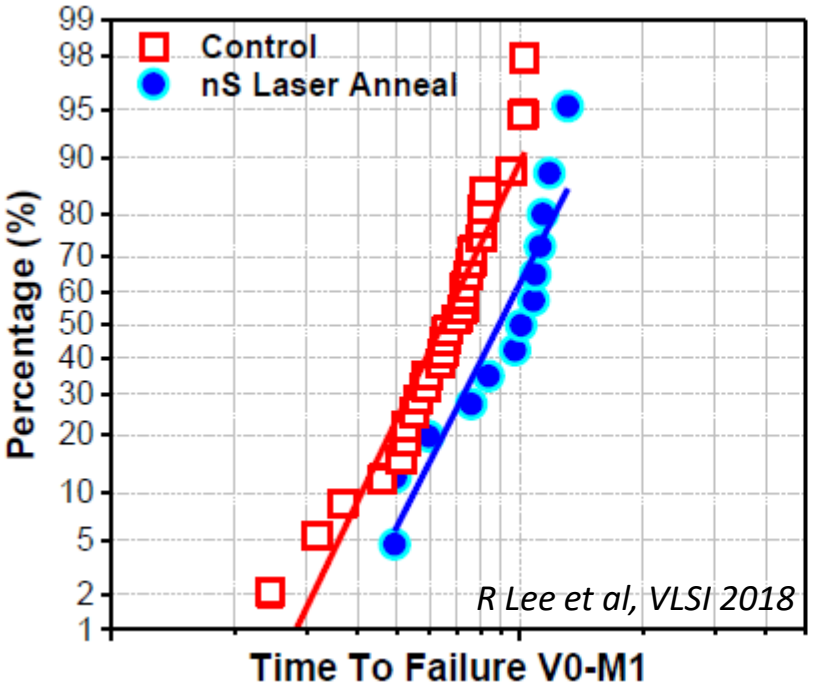
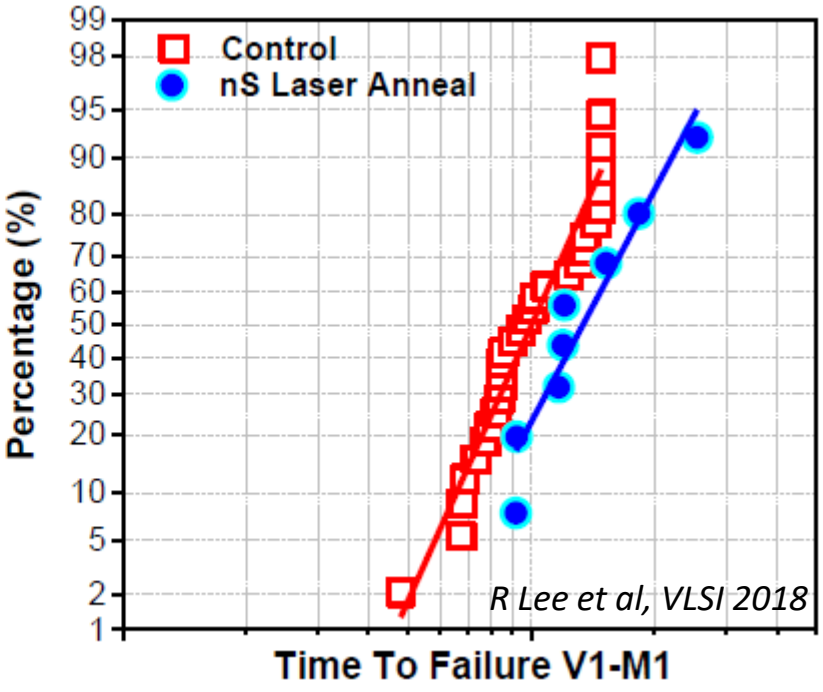
EM Lifetime





- Comparable/better EM lifetime after anneal

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Summary

Summary: nS Laser Anneal vs Conv. Anneal	
Parameters	**Performance**
Line Resistance	+ 35%
Capacitance	- 9% (tunable)
RC Performance	+ 15%
Median Cu Grain Size	+ 2.7X
N/PMOS I_{Dsat}	+ 2%, +5%
M1-M1 Dielectric V_{BD}	+ 10%
V0-M1 EM Lifetime	+ 27%
V1-M1 EM Lifetime	+ 36%

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