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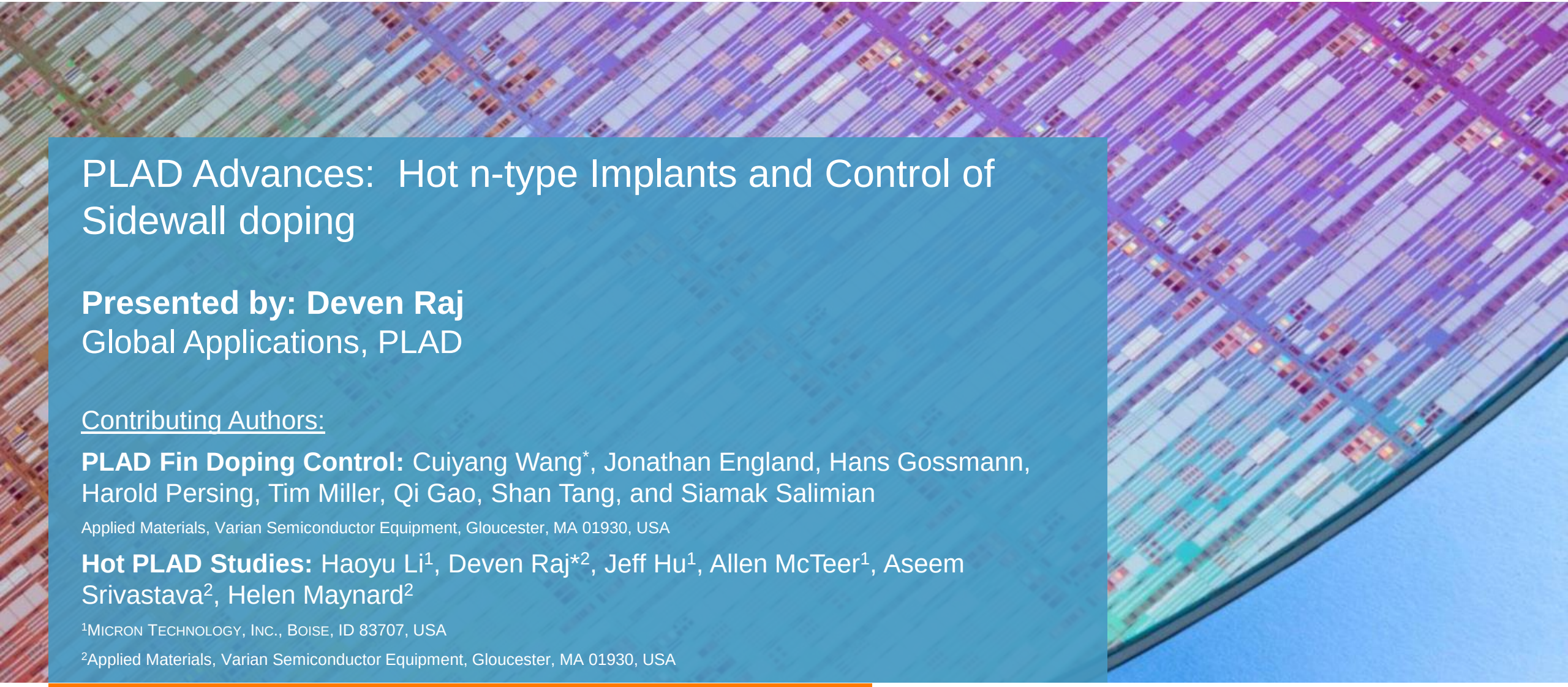

PLAD Advances: Hot n-type Implants and Control of Sidewall doping

Presented by: Deven Raj
Global Applications, PLAD

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PLAD Fin Doping Control: Cuiyang Wang*, Jonathan England, Hans Gossmann, Harold Persing, Tim Miller, Qi Gao, Shan Tang, and Siamak Salimian

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Hot PLAD Studies: Haoyu Li[1], Deven Raj*[2], Jeff Hu[1], Allen McTeer[1], Aseem Srivastava[2], Helen Maynard[2]

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Outline

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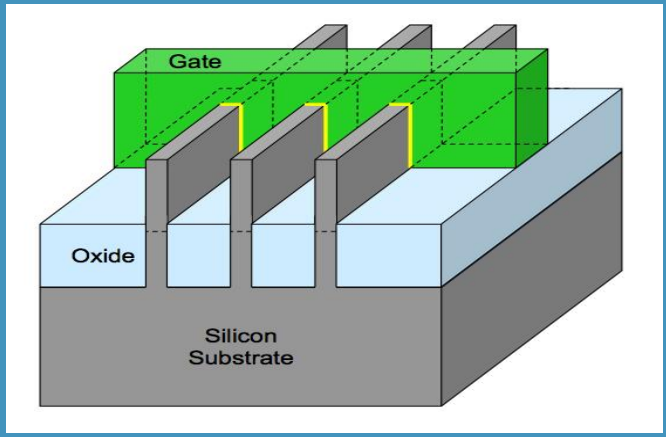
1. PLAD Overview
2. FinFET Doping by PLAD and Mechanism Study
3. N-Type PLAD Results and Characterization

3D FinFET SDE Doping Challenges

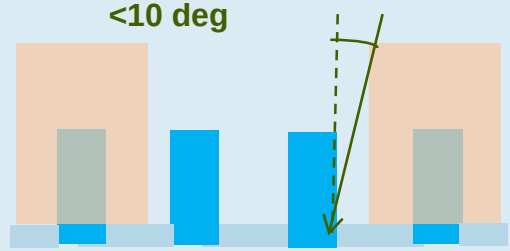
- **3D FinFET for device 20nm beyond**
- **Key Challenges**:
  - Conformal Doping
  - No Fin erosion
  - No residual defect
  - Low leakage



Beamline:

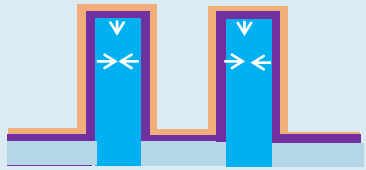
- Shadowing

Title angle of implantation <10 deg



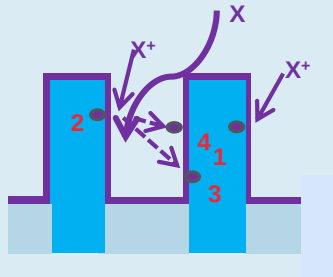
Deposition and Thermal Drive in

- Highly Conformal
- Not PR compatible
- Cap layer



Plasma Doping:

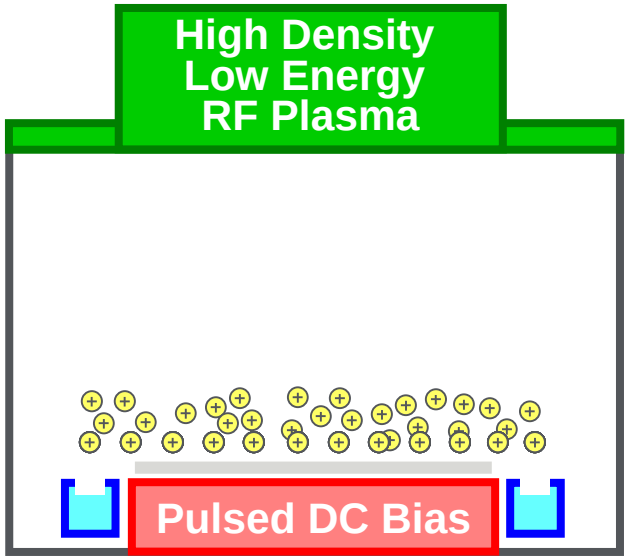
- Good conformality
- PR compatible



Plasma doping offers a simplified, photoresist compatible process

Implant Challenges and Heated Implantation

- Plasma Doping Advantages:
  - Pulsed DC bias allows for precision doping
  - Independent control of RF plasma generation and DC bias balances deposition and implant
  - Uniform and tunable sidewall or bottom doping
  - Highly productive at low energy, high dose regime



- Enabling hot technology:
  - Capable to 12 kV with up to 500 C platen temperature
  - Leverages production-proven portfolio of high temperature platen technology
  - Compatible with all available PLAD doping or materials modification chemistries
  - Meets critical backside requirements for advanced devices

PLAD Advances: Hot n-type Implants and Control of Sidewall Doping

Presented at IWJT, 2017, Kyoto:

- Sidewall Doping Mechanism and Profile Tuning on 3D Structure by Plasma Doping (PLAD)

  Cuiyang Wang*, Jonathan England, Hans Gossmann, Harold Persing, Tim Miller, Qi Gao, Shan Tang, and Siamak Salimian

  ISBN: 978-86348-626-3, *IEEE*

- Characterization of Hot N-Type Doping Plasma Implantation (PLAD)

  Haoyu Li[1], Deven Raj*[2], Jeff Hu[1], Allen McTeer[1], Aseem Srivastava[2], Helen Maynard[2]

  [1]Micron Technology, Inc., Boise, ID 83707, USA

  [2]Applied Materials, Varian Semiconductor Equipment, Gloucester, MA 01930, USA

  ISBN: 978-86348-626-3, *IEEE*

Suggested References:

- Combining Dynamic Modelling Codes with Medium Energy Ion Scattering Measurements to Characterise Plasma Doping », J. England et al., *IBMM 2016*
- NMOS Source-drain Extension Ion Implantation into Heated Substrates, L. Pipes et al. *IEEE, Ion Implant Technology Conference, IIT 2014*
- Plasma Implant Process, Z. Fang*, IIT 2016*

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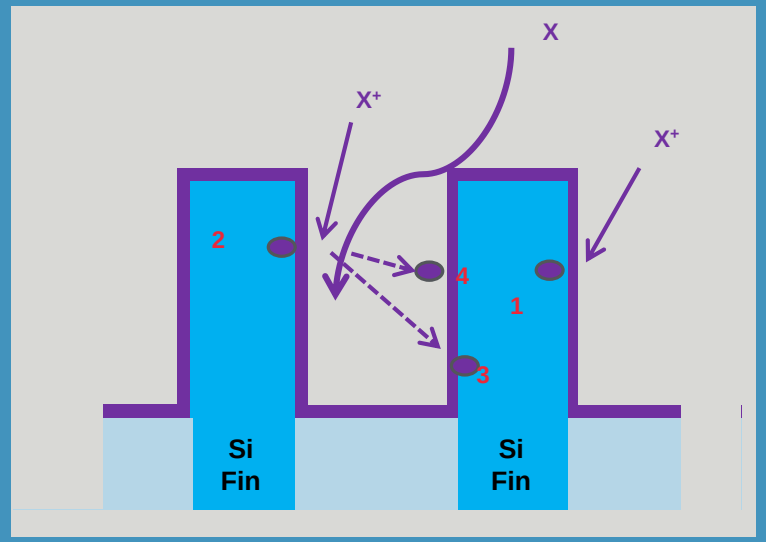
Benefits and Challenges for PLAD FinFET Doping

1: DIRECT IMPLANT

3: DEPOSITION and KNOCK-IN

2: SCATTERED ION IMPLANT

4: SPUTTERING / Etching



- **Various Process parameters:**
  - Power, Pressure, gas mixture ratio
  - Energy, Dose, PW, Frequency

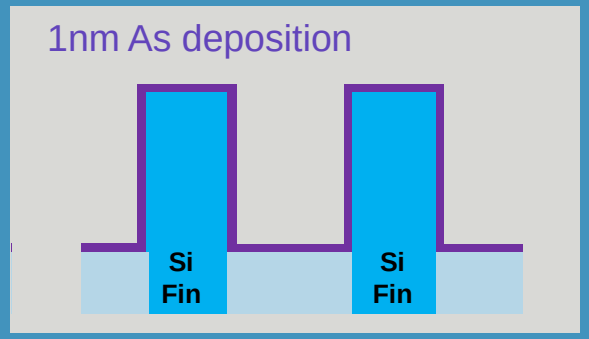
- **Multiple Mechanisms:**
  - Direct implant
  - Scattered implant
  - Deposition and knock in
  - Sputtering/Etching

- **Wafer Results:**
  - Conformality
  - Minimize fin erosion
  - Eliminate residual defects

Doping of Si Fin structures is a driven by multiple mechanisms and competing effects

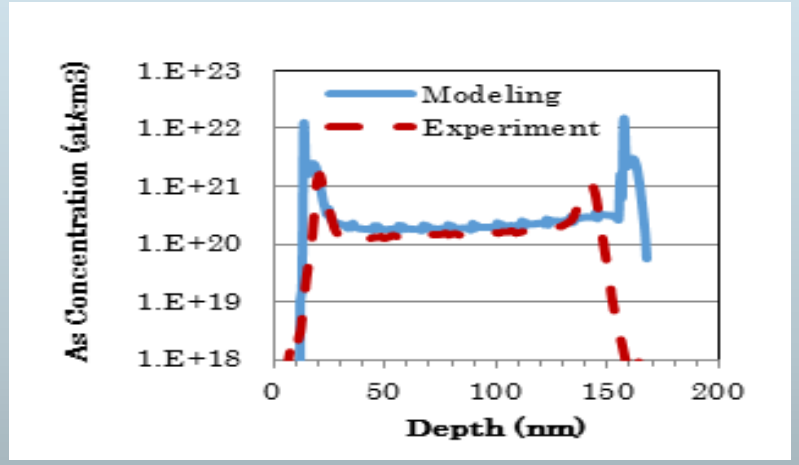
PLAD Doping Modeling

Static TRI3DYN model



- with 1nm of As neutrals on top, bottom and sidewall
- As & X* /2keV/5e15cm^{-2} implanted
- Dopant profiles shown after clean

* Knock in species



Reasonably good agreement between modeling and experiment1.5D SIMS.

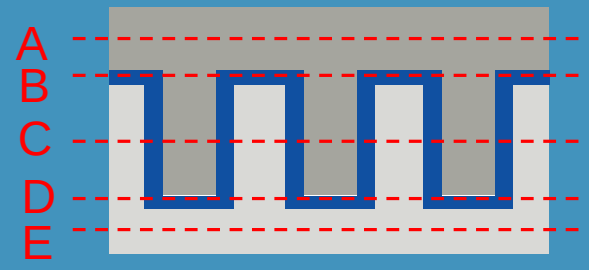
Experimental profile after clean, anneal and DHF

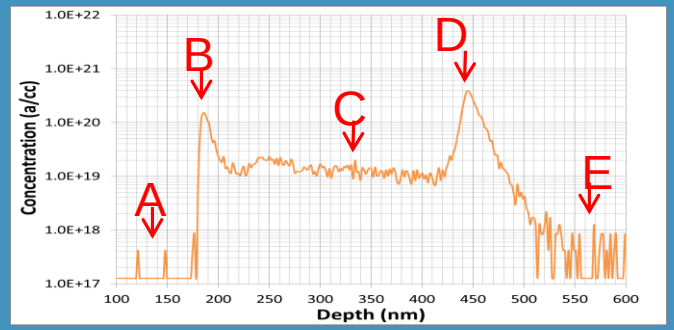
Reasonably good agreement reached between experiment and modeling

Dopant Characterization Metrology

1.5D SIMS

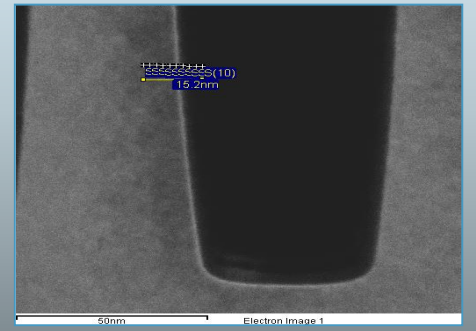
1. Lower detection limit
2. Results can be quantified
3. Average over number of fins
4. No lateral resolution



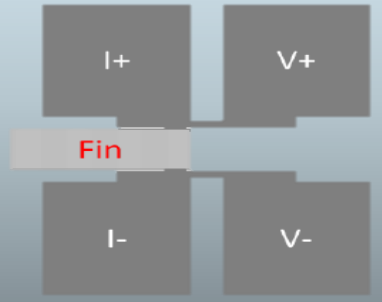


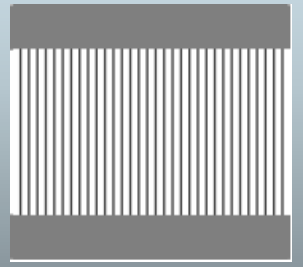
EDS mapping/EDS line scans (EELS)

1. Not good for B detection
2. Lateral resolution
3. Hard to quantify



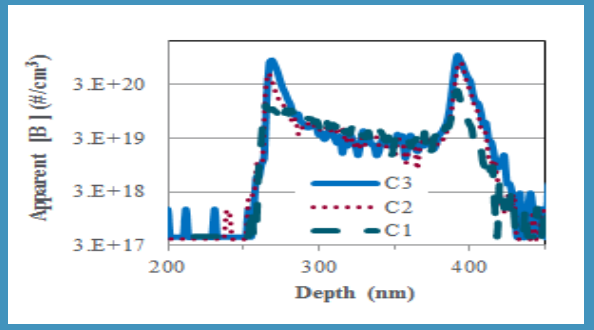
Fin resistor: active dopant

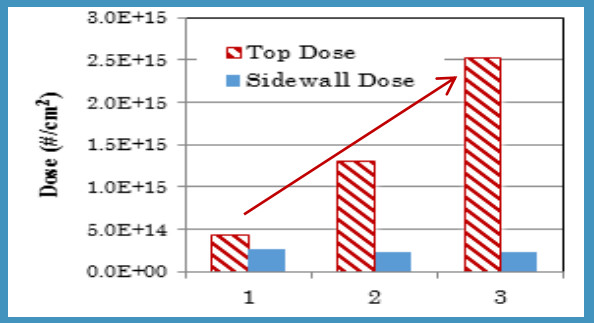




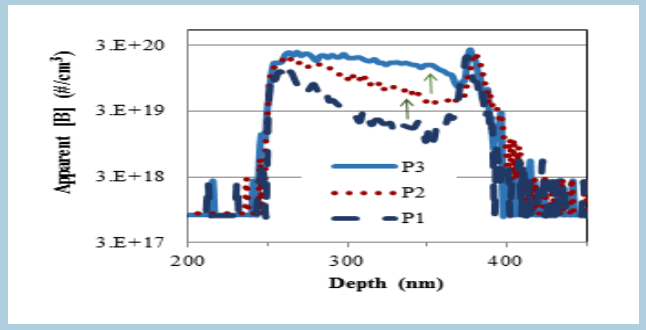
Each metrology has its limitations and the characterization results need to be interpreted carefully

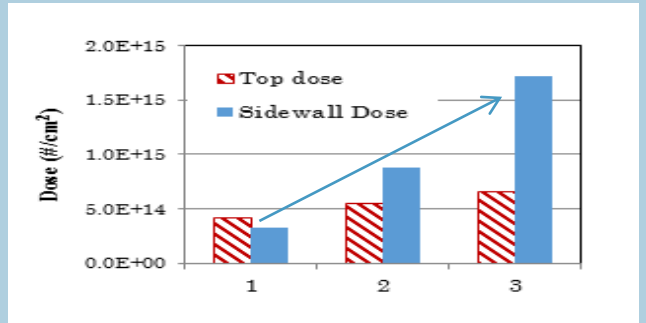
Doping Profile tuning on 3D structure _ top vs sidewall





Increase parameter C
- ~5 times fin top dose increase
- No change in fin sidewall dose





Increase parameter P
- ~5 times fin sidewall dose increase
- ~60% increase in fin top dose

Fin top and sidewall dose can be adjusted separately with different process knobs

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Background: Intel Demonstrates Improved Drive I

NMOS Source-drain Extension Ion Implantation into Heated Substrates

Leonard C. Pipes, Lisa McGill, Anant Jahagirdar
Logic Technology Development
Intel Corporation
Hillsboro, OR, USA

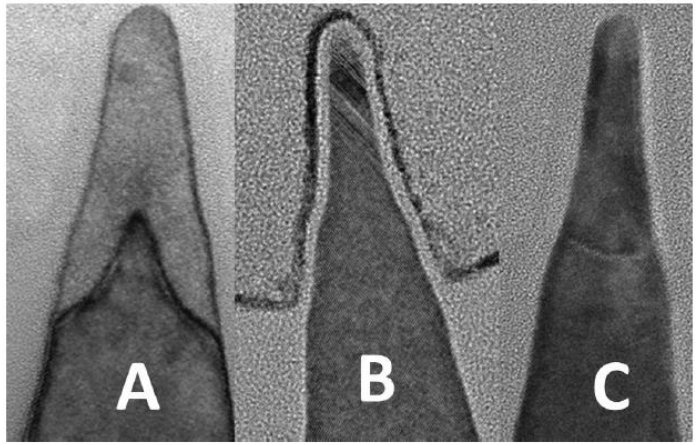


Fig. 1: TEM cross sections of silicon fins (A) immediately after room temperature implant, (B) after room temperature implant and a spike anneal (1 sec at ~1000°C), and (C) after heated implant alone (no anneal).

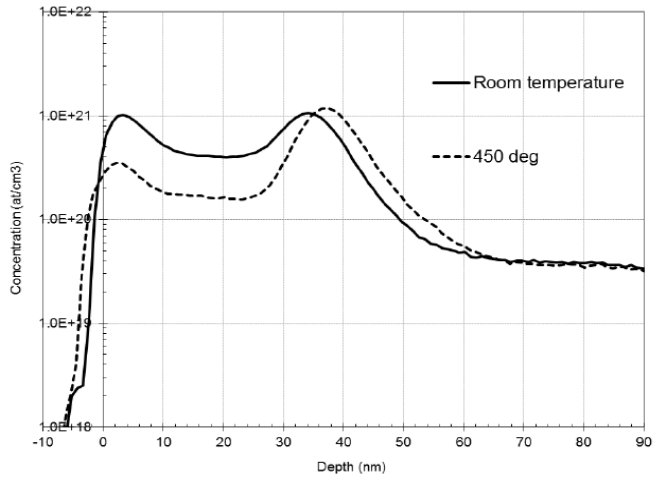


Fig. 3: SIMS profiles of 3.5 keV arsenic implanted at 30 degree incidence to wafer surface/fin top surface into fins nominally ~35 nm tall with ~42 nm pitch at room temperature and at 450 degrees.

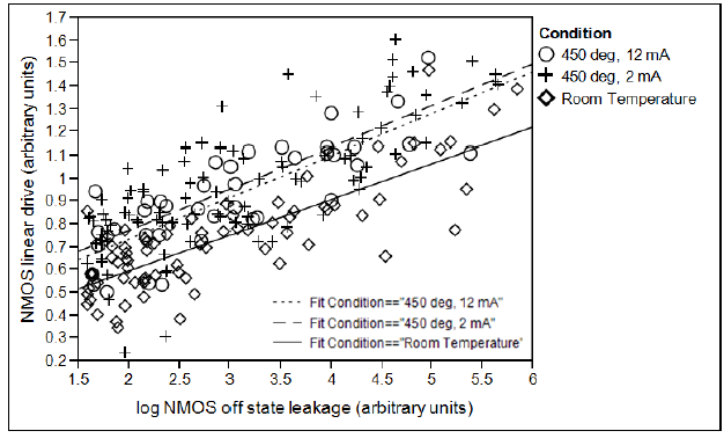
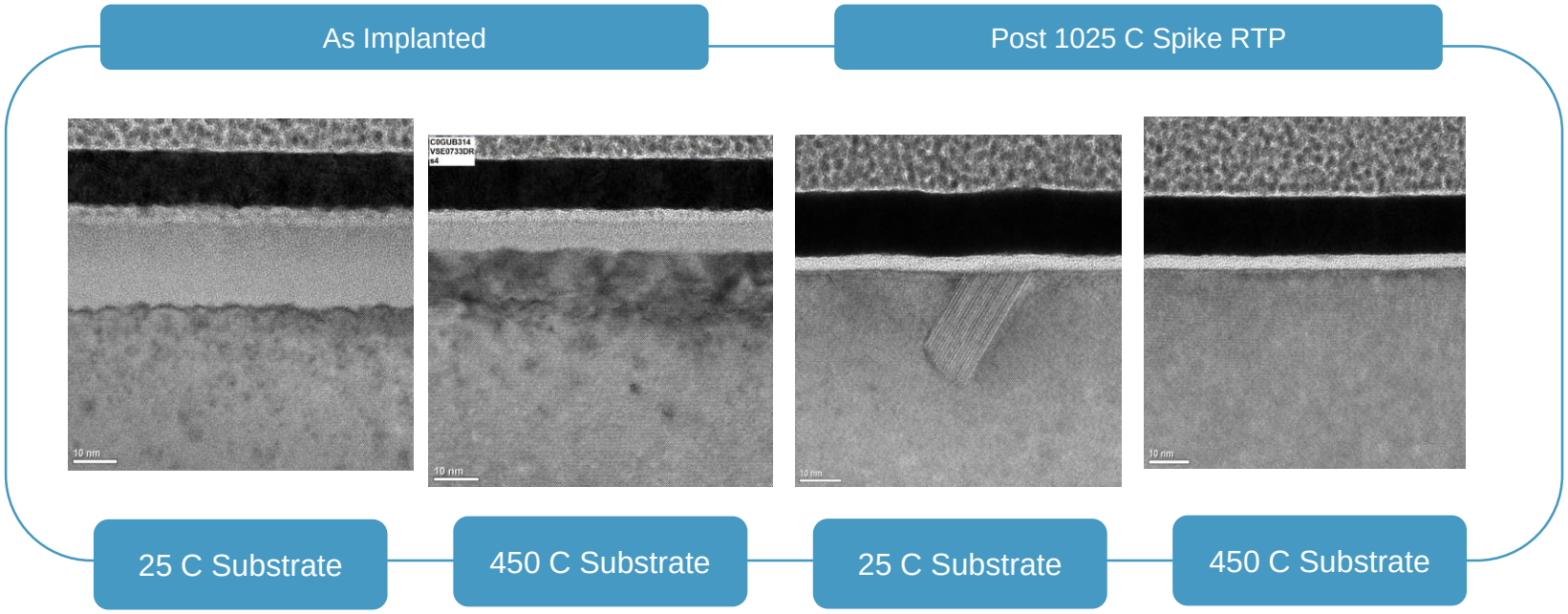


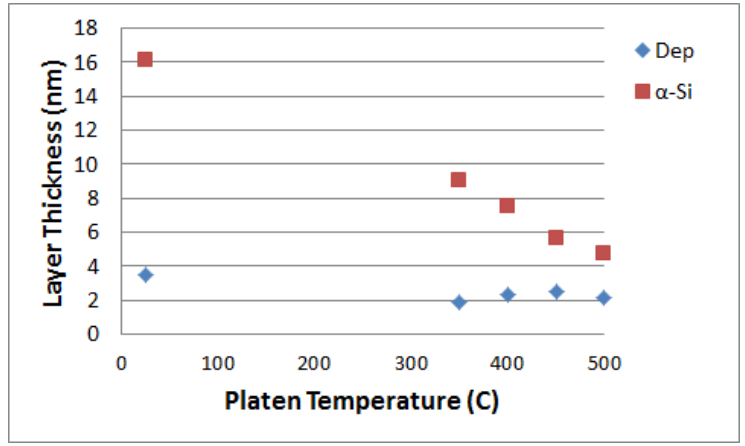
Fig. 5a: Trigate NMOS linear drive current plotted versus off state source-to-drain leakage for representative wafers at room temperature, 450 deg C at 12 mA beam current, and 450 deg C at 2 mA beam current

Higher drive current achieved by minimizing extension resistance via heated implantation

Reference: Leonard C. Pipes, et al. *NMOS Source-drain Extension Ion Implantation into Heated Substrates,* (Ion Implant Technology, 2014, IEEE)

AsH_3 PLAD: Cross-Section TEM of Damage Profile



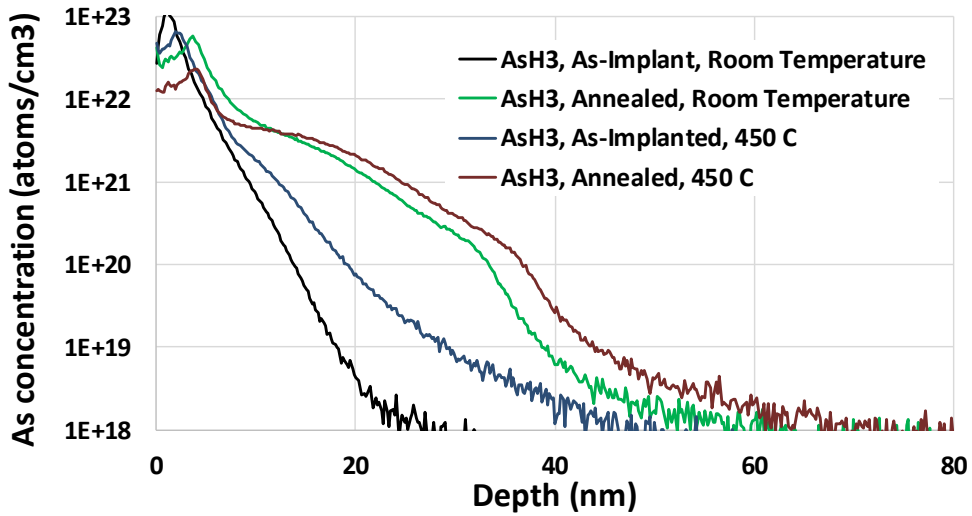


Post RTP shows clear defect after room temperature process which is not observed when substrate heated

AsH_3 PLAD, 7 kV, 4e15 a/cm^2
Cross-Section TEM

Arsenic Dopant Profile Comparison by Heated Implant

SIMS Profile



Room Temperature and 450 C Implantation
AsH_3 PLAD

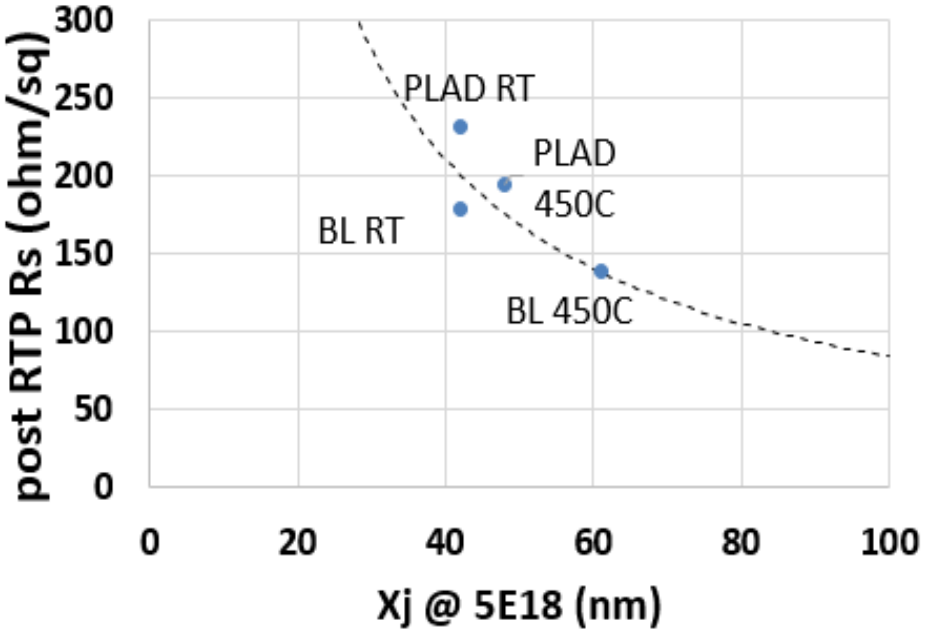
Reduced amorphous depth at 450 C evidenced by as-implant response

Less deposition observed by lower peak As in each 450 C condition

PLAD: AsH_3 PLAD, 7 kV, 4e15 a/cm^2

Rs vs. Xj of Arsenic Implanted Processes

Rs vs. Xj @ 5e18 a/cc



Fundamental Implant Damage and Recovery Model Drives Implantation and PLAD to same Rs vs. Xj Curve

Optimization Along the Curve is Achievable by Both Techniques

Implant: As+, 7 keV, 4e15 a/cm^2
PLAD: AsH_3 PLAD, 7 kV, 4e15 a/cm^2

Summary

- PLAD has been in mass production for multiple applications for several years
- Plasma doping of Fin structures by an implant based approach has been demonstrated
- Efforts to enhance fundamental understanding and to enable predictive approaches are in progress
- Dopant profile and damage control in silicon demonstrated using heated PLAD capability
- Heated implantation expands process space for next generation devices in doping and material modification applications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