Smartphone Market Driving 7nm & 5nm Node 3-D Devices and Stacked Devices

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Outline

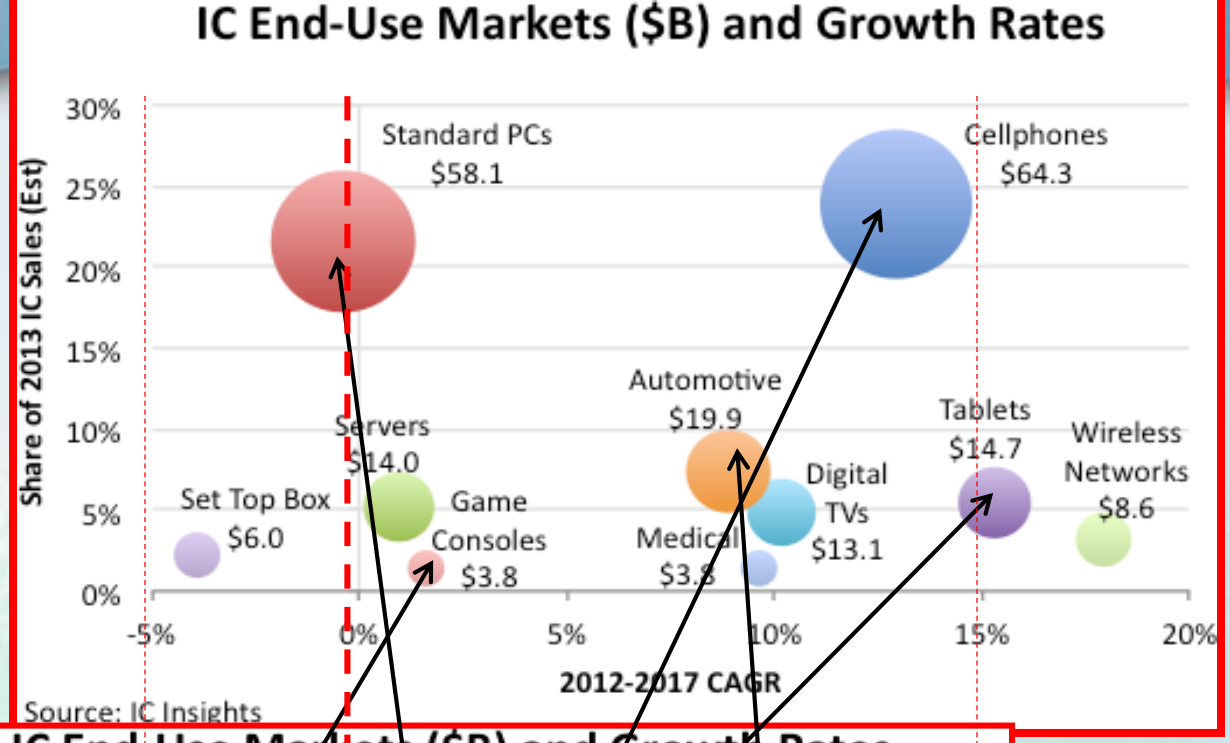
- **Introduction: Smartphone Market Driver for 3-D**
  - 2016 Semiconductor Market and Applications
    - Computation, Mobile, Automotive, Medical and IoT
  - Smartphone device technology
    - Application Processor 2-D planar (←A8: 20nm node)→3-D FinFET (A9→: 14/16nm node)
    - Rear facing camera (8Mp→12Mp←16Mp) 3-D TSV→3-D Monolithic (Direct Wafer Bonding)
    - Flash memory 2-D 13nm → 3-D 40nm with 48-layers
- **3-D Bulk FinFET Transistor Formation**
- **3-D FinFET High Mobility Channel Formation**
- **3-D Gate-All-Around Nanowire Transistor Formation for sub-5nm node or Monolithic 3-D stacking**
- **More-Than-Moore 3-D Stacked Devices**
- **Summary**

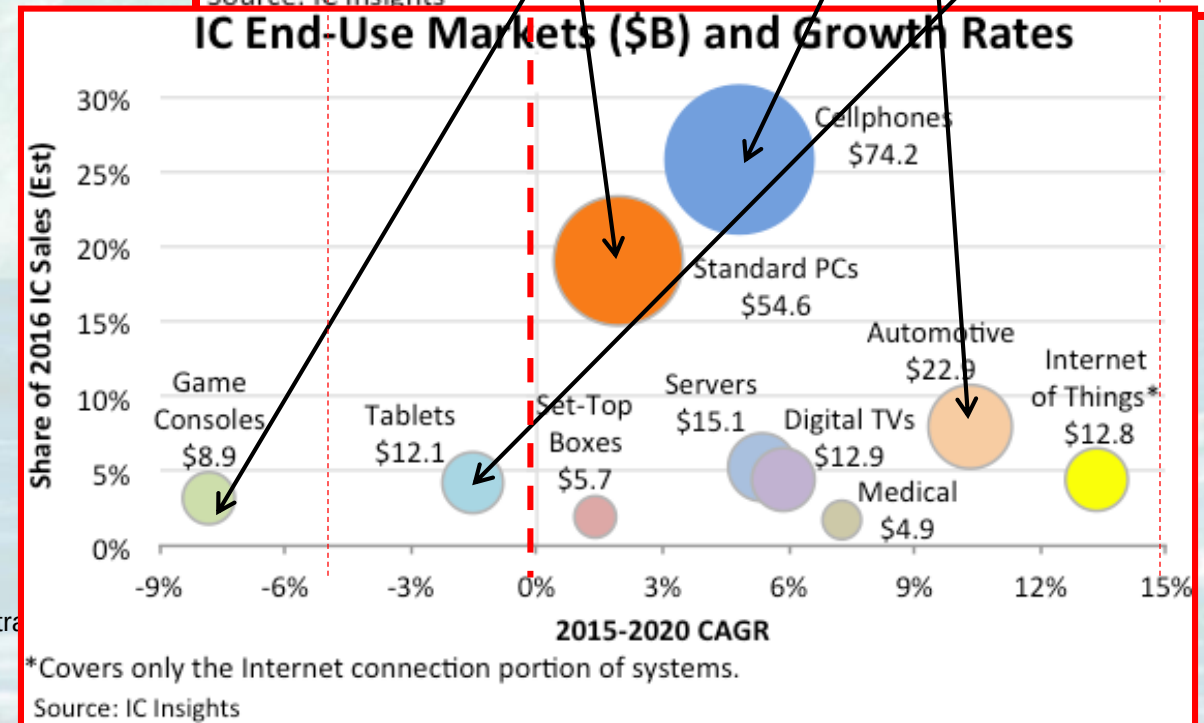
Total IC Market

2014=$340B

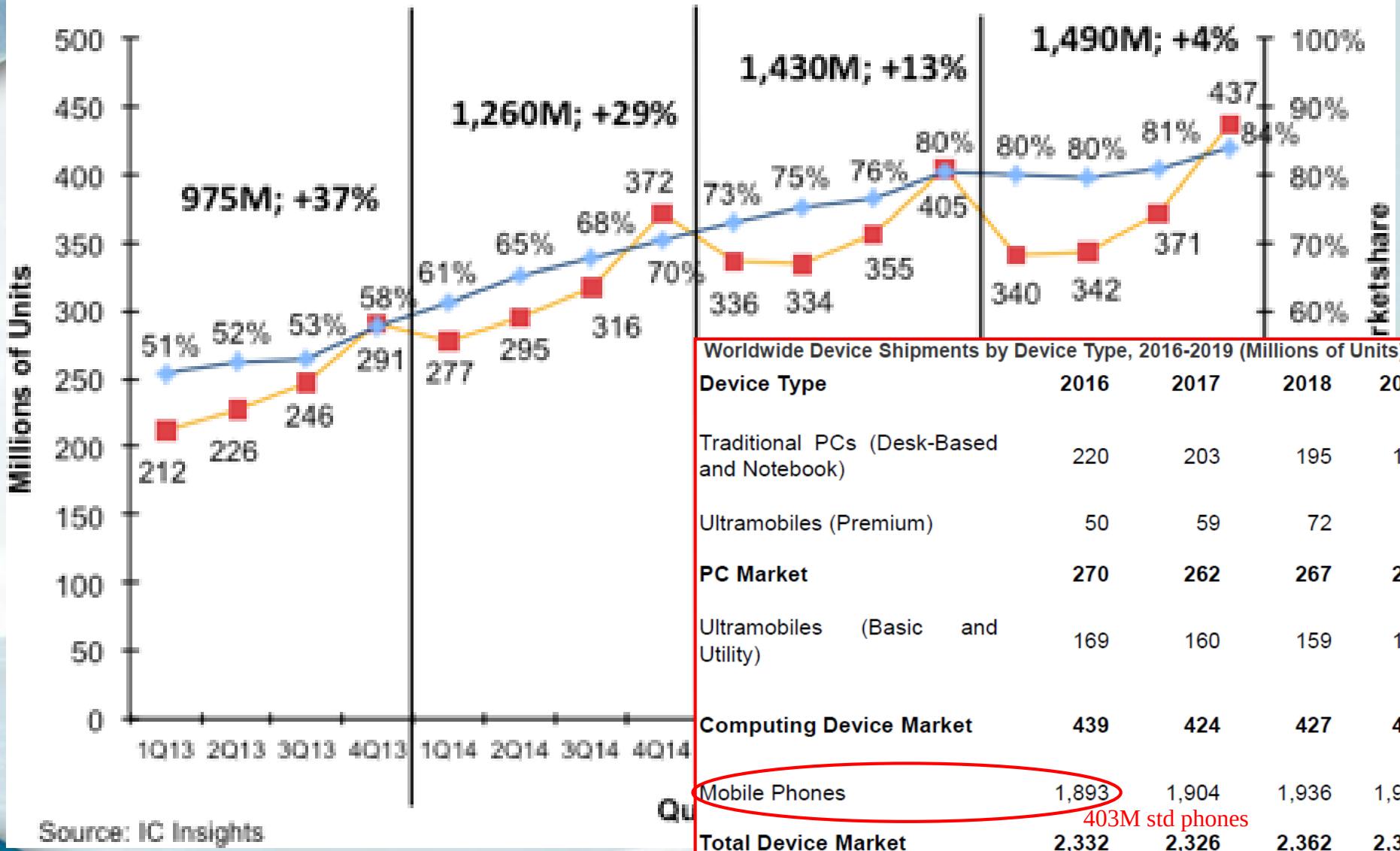
2015=$333B

2016=$343B





Smartphone Marketshare Trends



Source: IC Insights

Worldwide Device Shipments by Device Type, 2016-2019 (Millions of Units)

Device Type	2016	2017	2018	2019
Traditional PCs (Desk-Based and Notebook)	220	203	195	191
Ultramobiles (Premium)	50	59	72	82
PC Market	**270**	**262**	**267**	**272**
Ultramobiles (Basic and Utility)	169	160	159	158
Computing Device Market	**439**	**424**	**427**	**432**
Mobile Phones	1,893	1,904	1,936	1,934
Total Device Market	**2,332**	**2,326**	**2,362**	**2,363**

403M std phones

Note: The ultramobile (premium) category includes devices such as Microsoft Windows 10 Intel x86 products and the Apple MacBook Air. The ultramobile (basic and utility) category includes devices such as the Apple iPad and iPad mini, Samsung Galaxy Tab S2, Amazon Fire HD, Lenovo Yoga Tab 3 and Acer Iconia One.
Source: Gartner (July 2017)

Smartphone as new technology driver

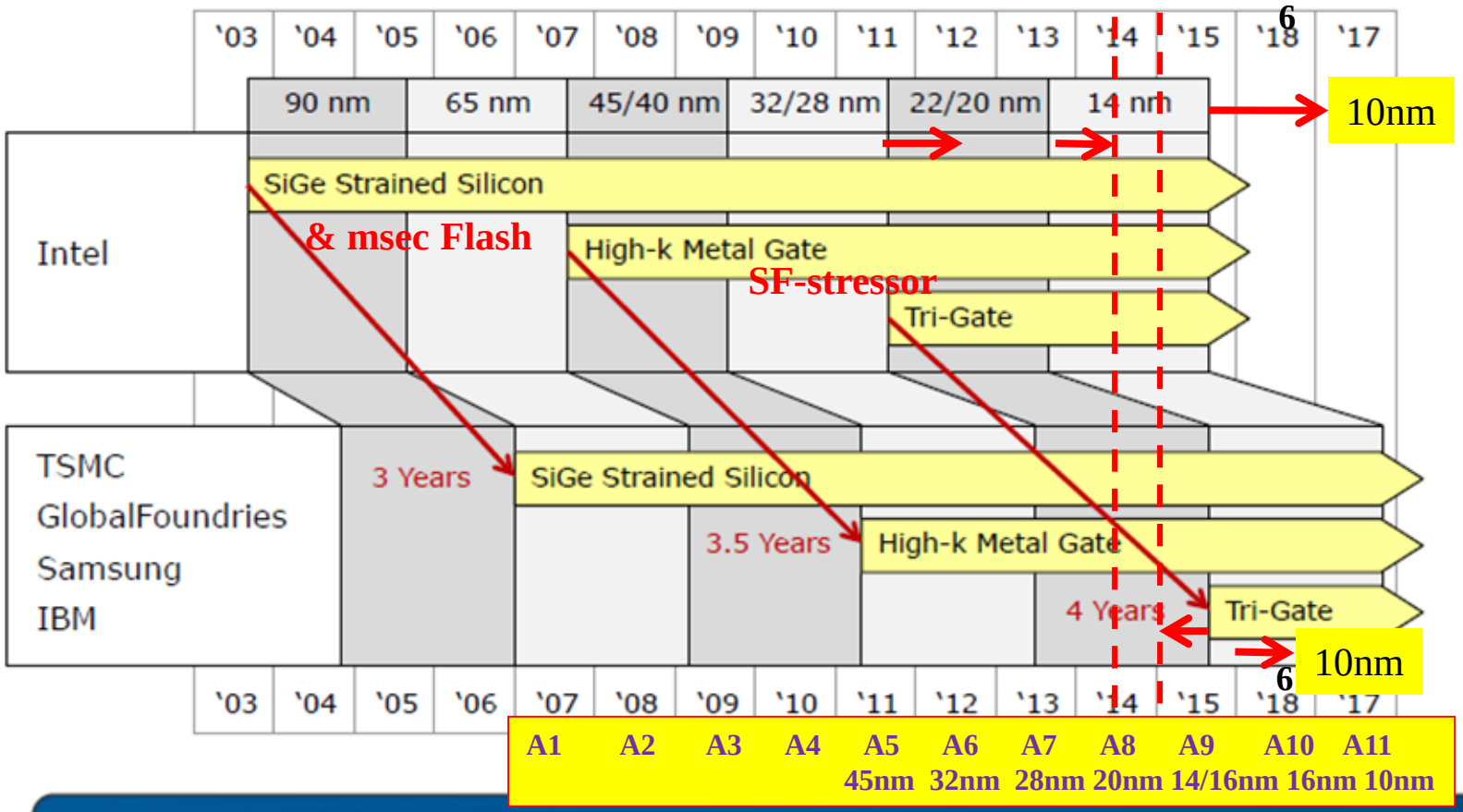
- 2011: iPhone 4s A5 and Galaxy S2→45nm (2007) 4 years old technology
- 2012: iPhone 5 A6 and Galaxy S3→32nm (2009) 3 years old tech
- 2013: April Galaxy S4 and Sept iPhone 5s/5c A7→28nm (2010) 3 years old tech
- 2014: April Galaxy S5 and Sept iPhone 6/6+ A8→20/22nm (2012) 2 years old tech
- **2015**: April Galaxy S6 and Sept iPhone 6s/6s+ A9→**14/16nm 3-D FinFET (2014)** most advanced technology node
- 2016: April Galaxy S7 and Sept iPhone 7/7+ A10→16nm (2014)
- 2017: April Galaxy S8 and Sept iPhone 7s/7s+ A11→10nm (2016) most advanced technology node

Apple SoC Evolution					
	CPU Perf	GPU Perf	Die Size	Transistors	Process
A5 2011	~13x	~20x	122m2	<1B	45nm
A6 2012	~26x	~34x	97mm2	<1B	32nm
A7 2013	40x	56x	102mm2	>1B	28nm
A8 2014	50x	84x	89mm2	~2B	20nm

A9 2015			14/16nm
A10 2016		3.3B	16nm FF+
A11 2017			10nm

Intel® Transistor Leadership

Everyone Equal at 14nm FinFET?



Intel leads the industry in introducing new technology generations and revolutionary transistor technologies

Intel, Sept. 6, 2011

IDF2011 INTEL DEVELOPER FORUM

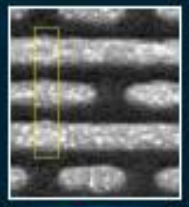
34

IBM: 1980s→1999 (1um→180nm)
Intel: 1999→Aug-2014 (180nm→14nm)
Samsung & TSMC: Oct-2016 (10nm→?)

INTEL INNOVATION LEADERSHIP

Strained Silicon

High-k Metal Gate



Self Align Via

FinFET Transistor

Hyper Scaling

Hyper Scaling

Intel	90nm		65nm		45nm		32nm		22nm		14nm				10nm				
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20	
Others		90nm			65nm		40nm		28nm		20nm		16nm		10nm				

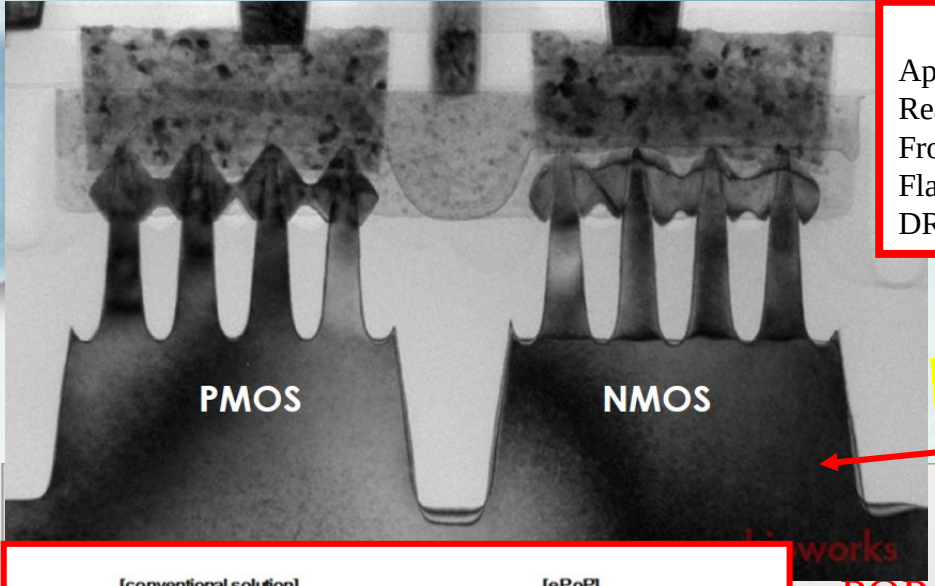
Dual FinFET

Strained Silicon	High-k Metal Gate	Self Align Via	FinFET Transistor	Hyper Scaling	Hyper Scaling
>3 years later	>3 years later	>3 years later	>3 years later	~3 years later	??

Intel leads the industry by at least 3 years in introducing major process innovations

TECHNOLOGY AND MANUFACTURING DAY

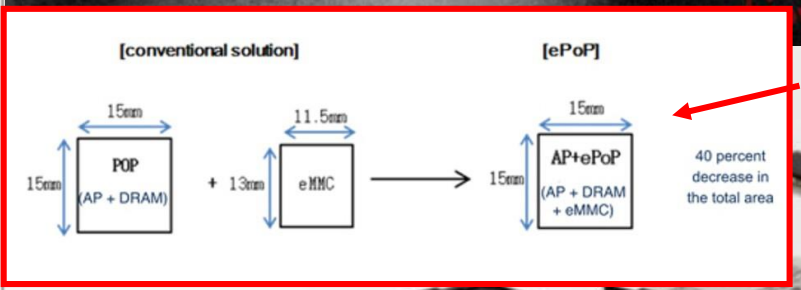
Source: Intel. 10 nm is based upon current expectations and available information.



	S6	S5
App. Processor	Samsung	Qualcomn
Rear Camera	16Mp Sony	16Mp Samsung
Front Camera	5Mp Samsung	5Mp Samsung
Flash	64Gb Samsung	64Gb Samsung
DRAM	3Gb Samsung	

14nm FinFET

Exynos 7420
PoP



ePOP

Battery

Dick James, Chipworks, April 6, 2015

Samsung Galaxy S6

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Samsung Galaxy S7 Smartphone

March 2, 2016

14nm FinFET

	S7	S6
App. Processor	Qualcomn	Samsung
Rear Camera	12Mp Sony	16Mp Sony
Front Camera	5Mp Samsung	5Mp Samsung
Flash	32Gb Samsung+microSD	64Gb Samsung
DRAM	4Gb Hynix	3Gb Samsung
Water Proof	5feet 30 minutes	No

Samsung Galaxy S7
March 2016 Sony
12Mp Rear Camera
3rd-gen Hybrid DBI
wafer to wafer
bonding

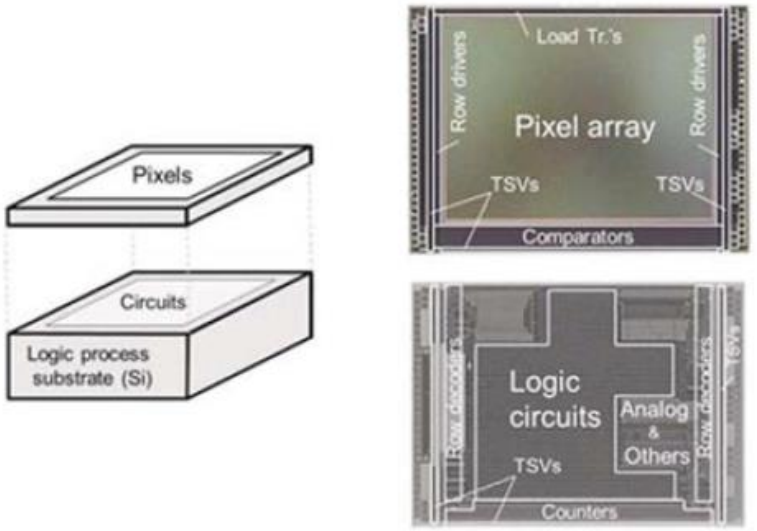


Fig. 1. Schematic diagrams of conventional stacked BI-CIS with TSVs

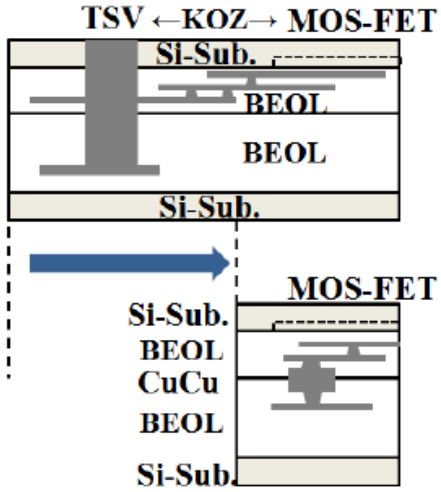
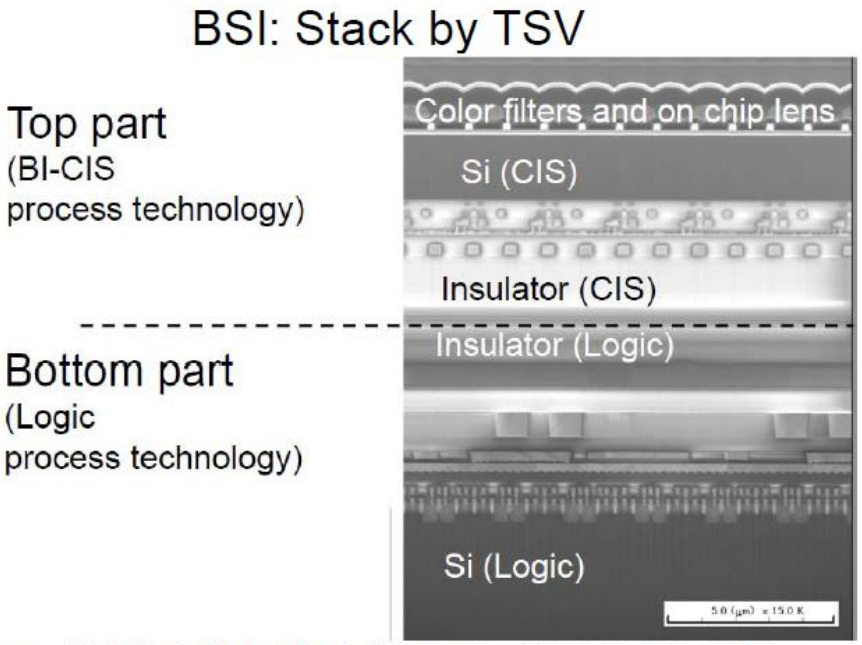


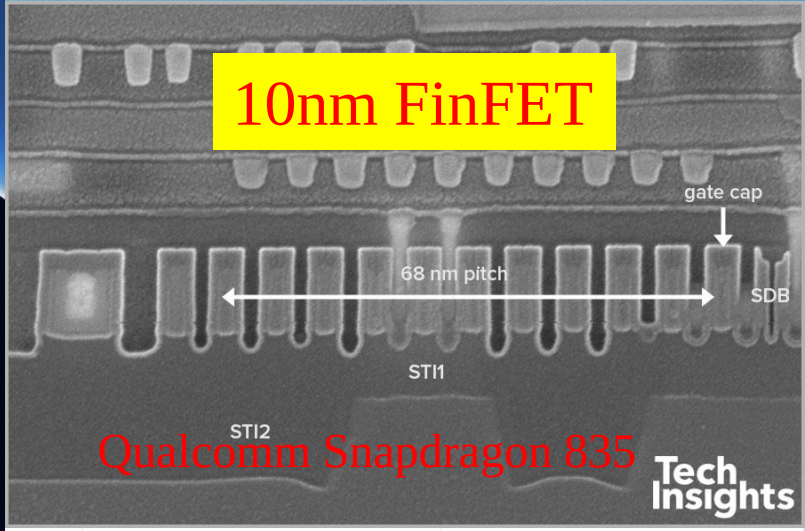
Fig. 2. Schematic diagrams of bonded substrates with TSV (upper) and with hybrid bonding (lower)

Kagawa et al., Sony, IEDM-2016 paper 8.4



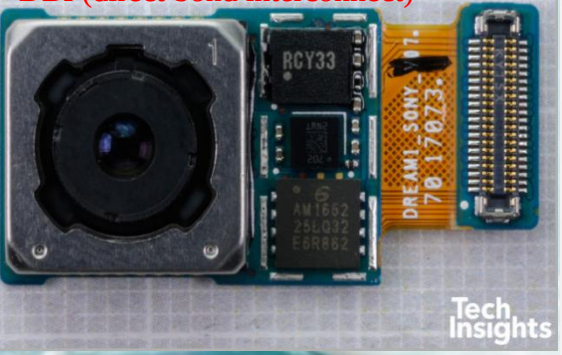
. Sukegawa, "A ¼-inch 8Mpixel Back-Illuminated..," ISSCC 2013 27.4]

Fig. 13. Cross-sectional view of new stacked BI-CIS with Cu2Cu hybrid bonding



Sony 8Mp Front facing Selfie Camera & Iris scanner

Sony 12Mp Rear facing Camera with DBI (direct bond interconnect)



	Samsung Galaxy S8 SM-G950W	Samsung Galaxy S7 SM-G930V
Applications Processor/Modems	$60.50	$40.00
Battery	$4.50	$3.50
Connectivity & Sensors	$15.00	$12.50
Cameras	$29.00	$24.50
Display	$67.00	$47.00
Memory	$42.50	$28.00
Mixed Signal/RF	$22.50	$21.00
Power Management/Audio	$9.50	$9.00
Other Electronics	$22.00	$19.50
Mechanicals/Housings	$21.00	$18.00
Test/Assembly/Supporting Materials	$20.00	$20.00
Total	$313.50	$243.00

iPhone Rear-Facing Cameras

chipworks

2.2 µm	1.75 µm	1.4 µm	1.5 µm

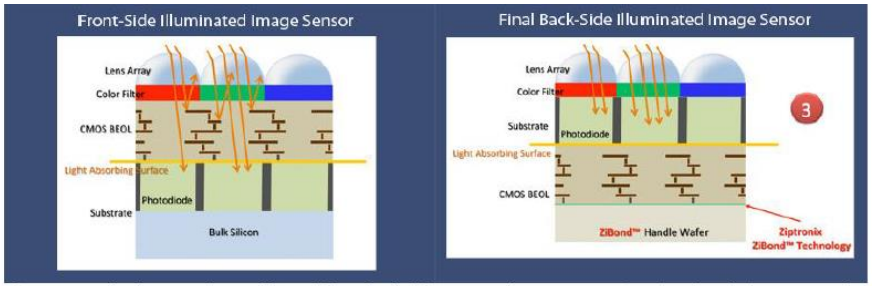


Fig.13: Standard comparison of frontside to backside CMOS image sensor showing handle/support wafer.

Thick SOI

SONY SONY SONY SONY 8 MP → 12Mp

1080

5 MP

720p@30fps

VGA@30fps

OmniVision 3.2 MP

Aptina Aptina 2 MP

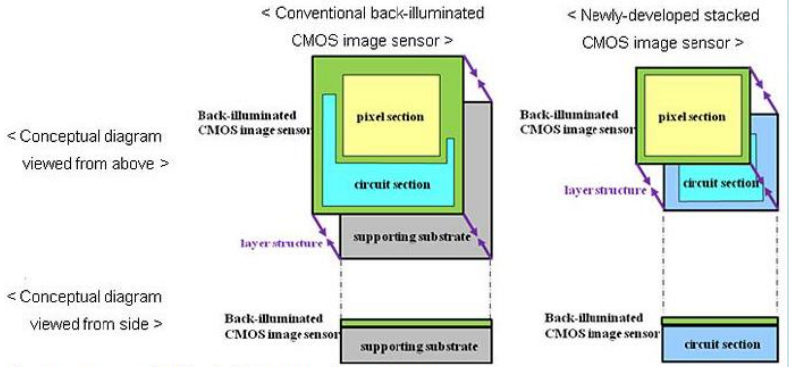


Fig.12: Sony stacked backside CMOS image sensor.

Stacked

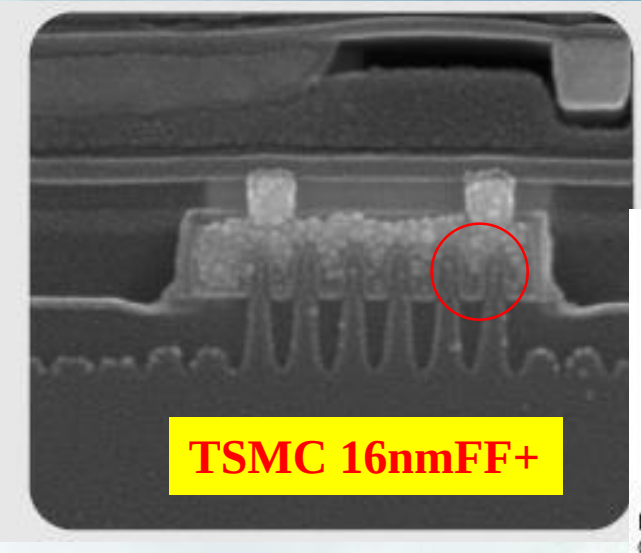
FSI → BSI

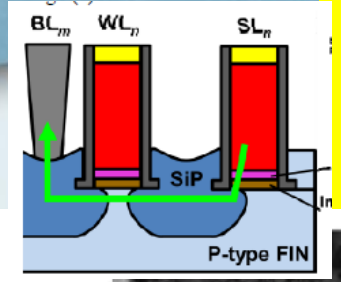
iPhone	iPhone 3G	iPhone 3GS	iPhone 4	iPhone 4s	iPhone 5	iPhone 5s / iPhone 5c	iPhone 6
2007	2008	2009	2010	2011	2012	2013	2014

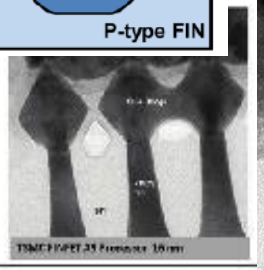
iPhone 6s 2015

Apple iPhone 6s & 6s+

Sept 9, 2015







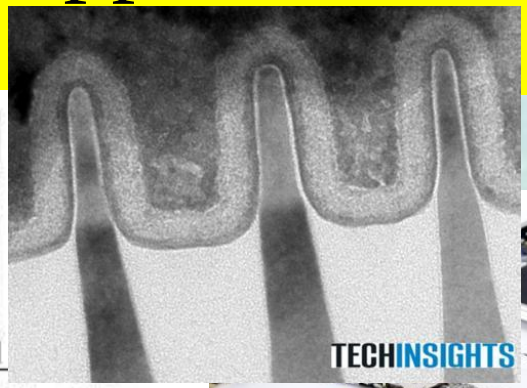
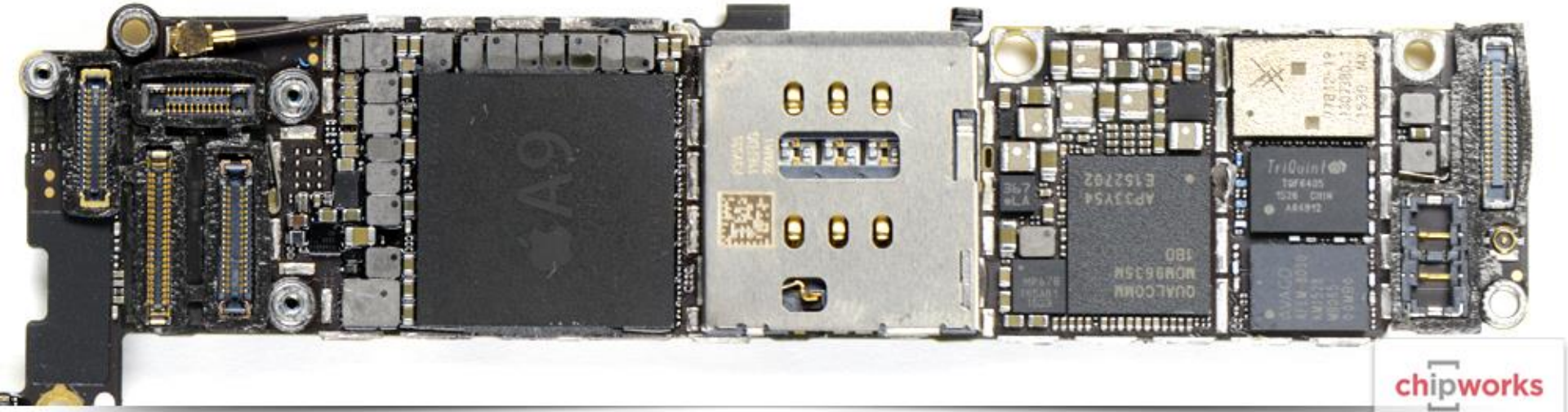


FIGURE 9. TEM cross-section 16nm finFET from TSMC. Cross-section is made along a trench contact and perpendicular to the fins. (source: TSMC 16nm finFET Process in Apple A9 Processor - Logic Detailed Structural Analysis).



Intel Inside!

Intel Mobile Cellular Platform

-Two RF transceivers

-Baseband modem

-(RF) power management IC

Samsung 2Gb LPDDR4 DRAM

Flash Memory options

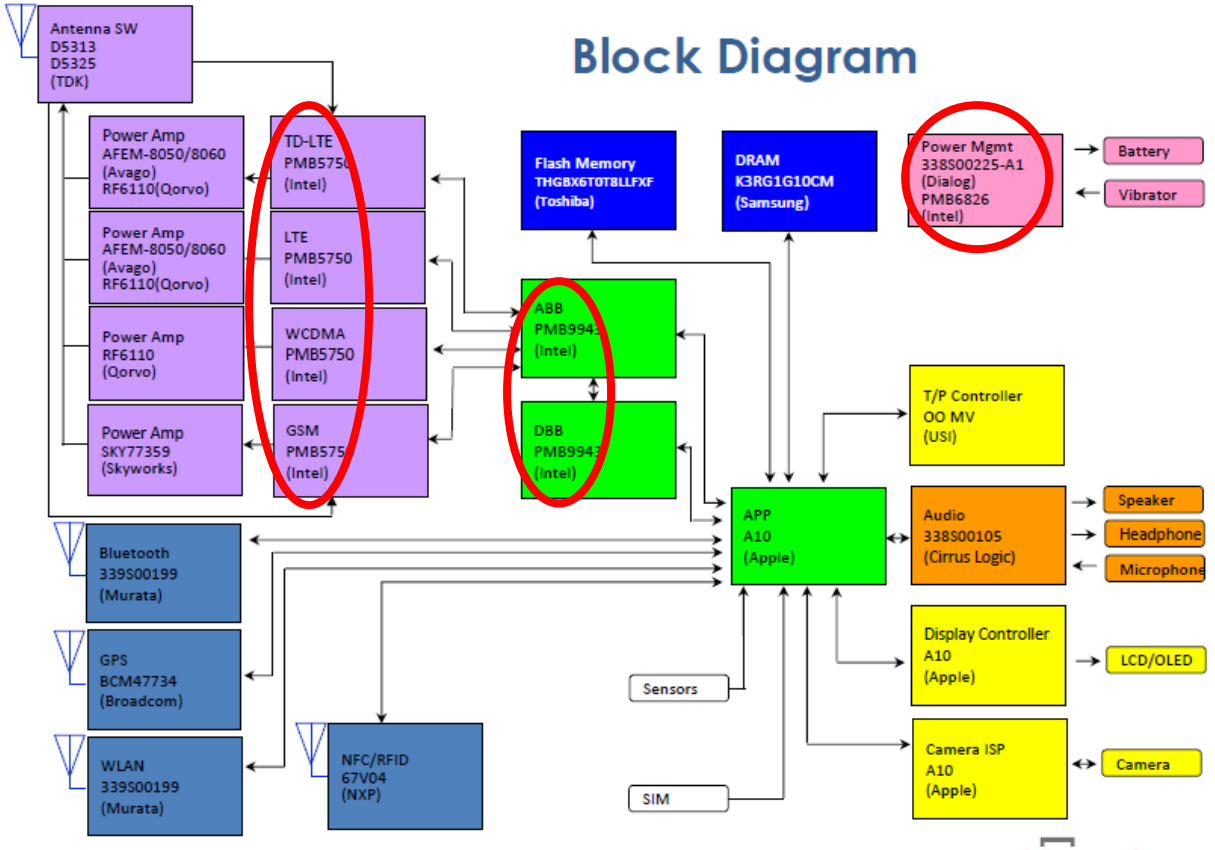
SK Hynix 128Gb (15nm)

Toshiba 128Gb (15nm)

Toshiba 48-layer 3-D NAND 256Gb

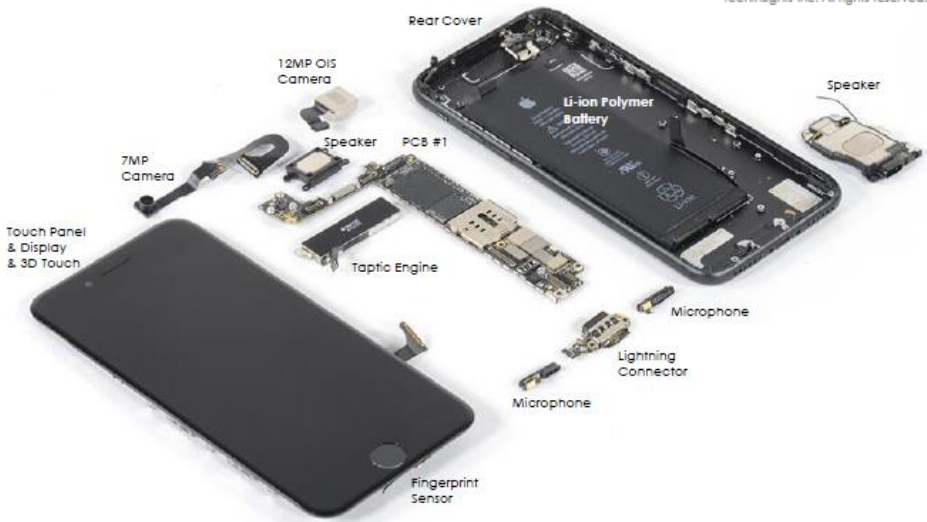
Battery 1960mAh (7.45Wh)

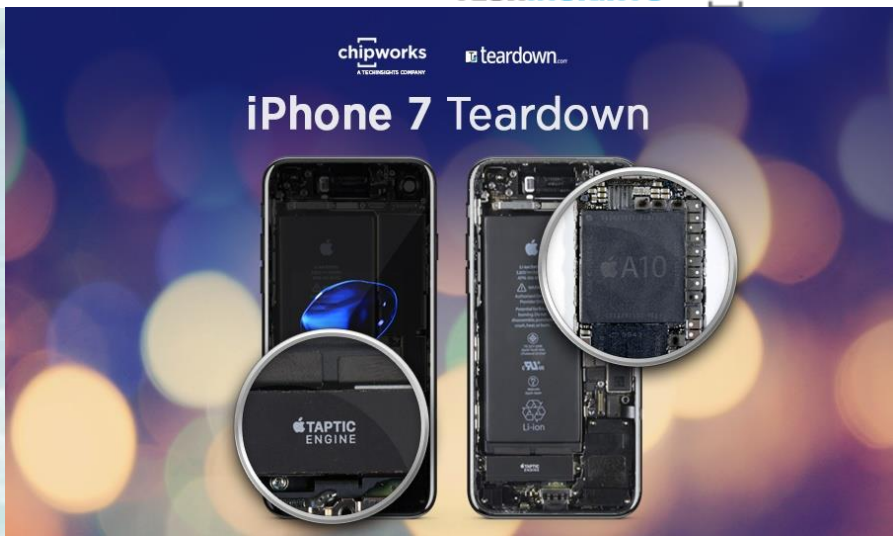
Block Diagram



TECHINSIGHTS chipworks

Teardown (Rear View)





Apple iPhone 7 Highlights

Apple iPhone 7 Technical Features

TYPE:	Phone
MODEL:	Not Available
MANUFACTURER:	Apple iPhone 7
DIMENSIONS:	138.3 x 67.1 x 7.1 mm
WEIGHT:	138 g
BATTERY SIZE:	Non-removable Li-Ion battery
SCREEN SIZE:	4.7"
DISPLAY TECHNOLOGY:	LED-backlit IPS LCD
SCREEN:	750 x 1334 pixels (~326 ppi pixel density)
FRONT CAMERA:	7 megapixels
REAR CAMERA MAIN:	12 megapixels
RAM:	2 GB
INTERNAL STORAGE:	32/128/256 GB
PLATFORM CHIPSET:	Apple A10 Fusion
CPU:	Quad-core
GPU:	Six-core graphics
CONNECTIVITY:	Wi-Fi 802.11 a/b/g/n/ac, HSPA, LTE, Bluetooth
SENSORS:	Fingerprint, accelerometer, gyro, proximity, co
SOUND:	Vibration, proprietary ringtones
	3.5mm Jack - No
SPECIAL FEATURES:	Fingerprint, accelerometer, gyro, proximity, compass, barometer
OTHER NOTES:	Water resistant up to 1 meter and 30 minutes
	IP67 certified - dust and water resistant
	iOS 10

Sony 2nd-generation
TSV 3-D stack

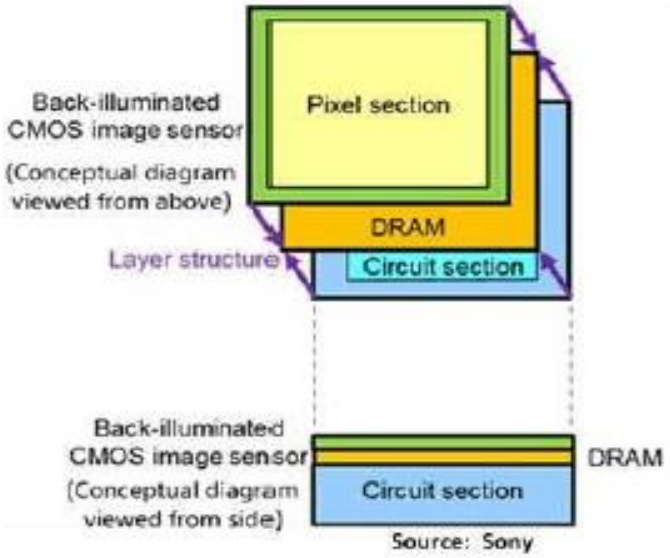
Toshiba 256Gb-Flash
48-layer 3-D NAND

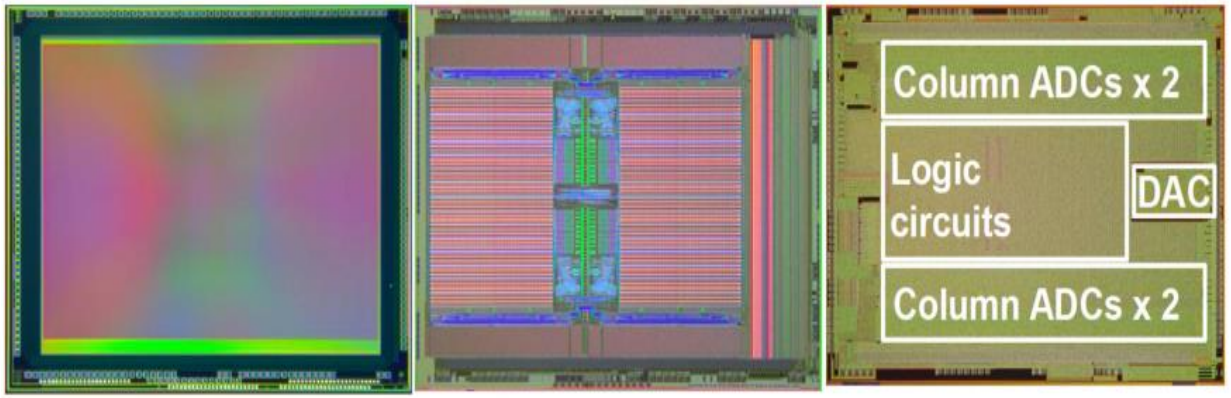
Single Device Cost*

	Apple iPhone 7
Teardown Date	September 2016
Applications Processor	$40.00
Applications / Baseband Processor	$0.00
Baseband Processor	$17.00
Battery	$4.00
Camera / Image	$26.00
Connectivity	$9.50
Display / Touchscreen	$37.00
Logic	$0.00
Memory: Mixed	$25.50
Memory: Non-Volatile	$13.00
Mixed Signals	$1.00
Non-Electronics	$22.00
Other	$15.00
Power Management / Audio	$11.50
RF Component	$23.50
Sensor	$4.50
Substrates	$5.50
Supporting Materials	$7.00
Final Assembly & Test	$13.00
Total	$275.00

TECHINSIGHTS chipworks

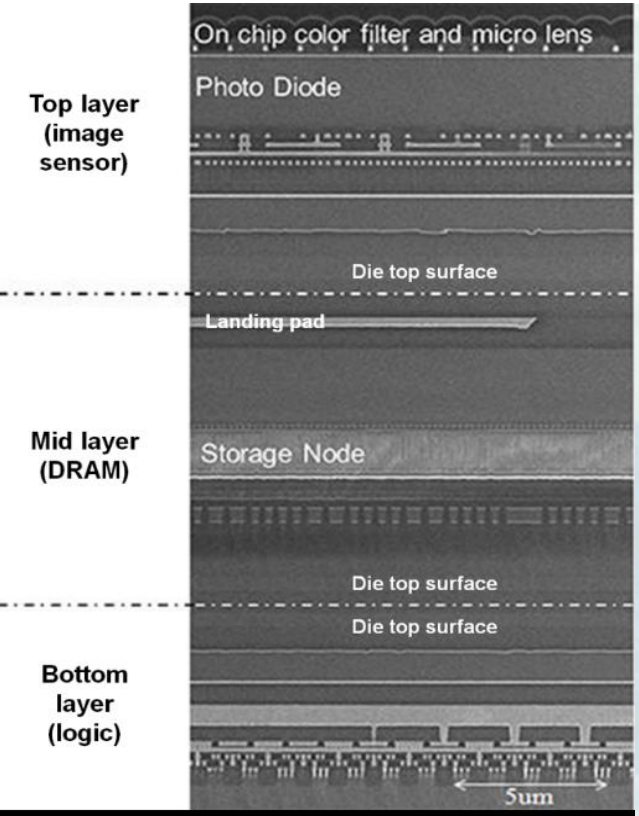
Sony's 3-Layer 20Mp CIS

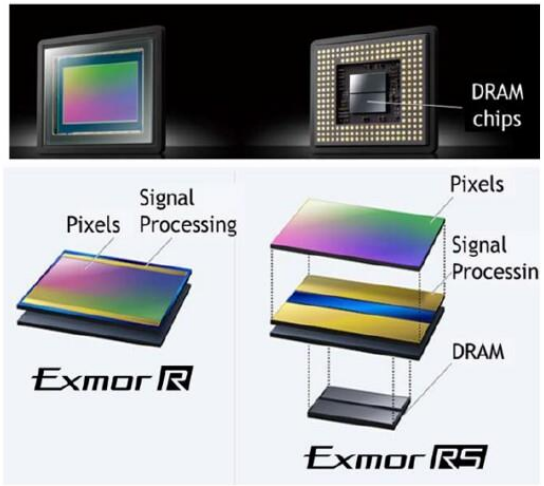


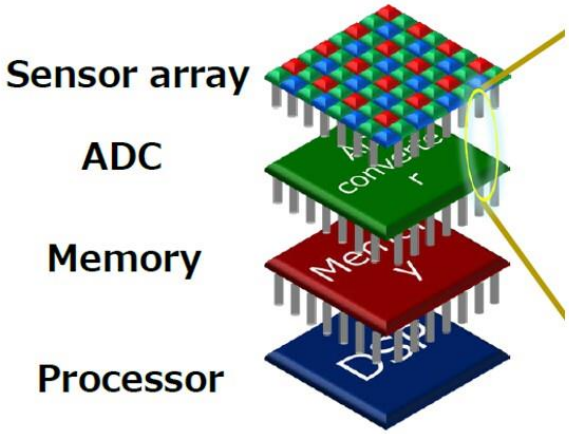


Source: Sony/ISSCC

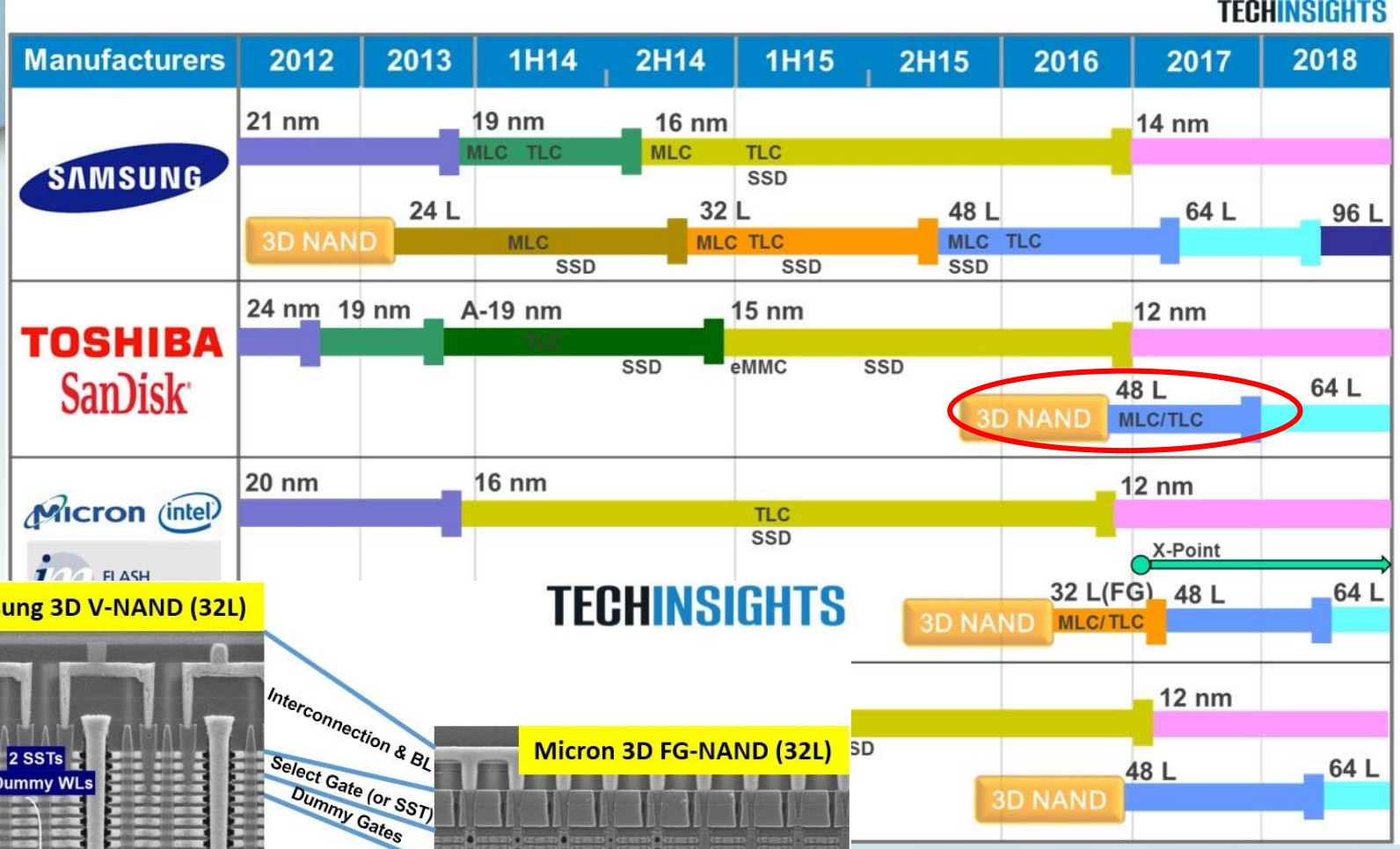
Sony's Future 4-Layer CIS

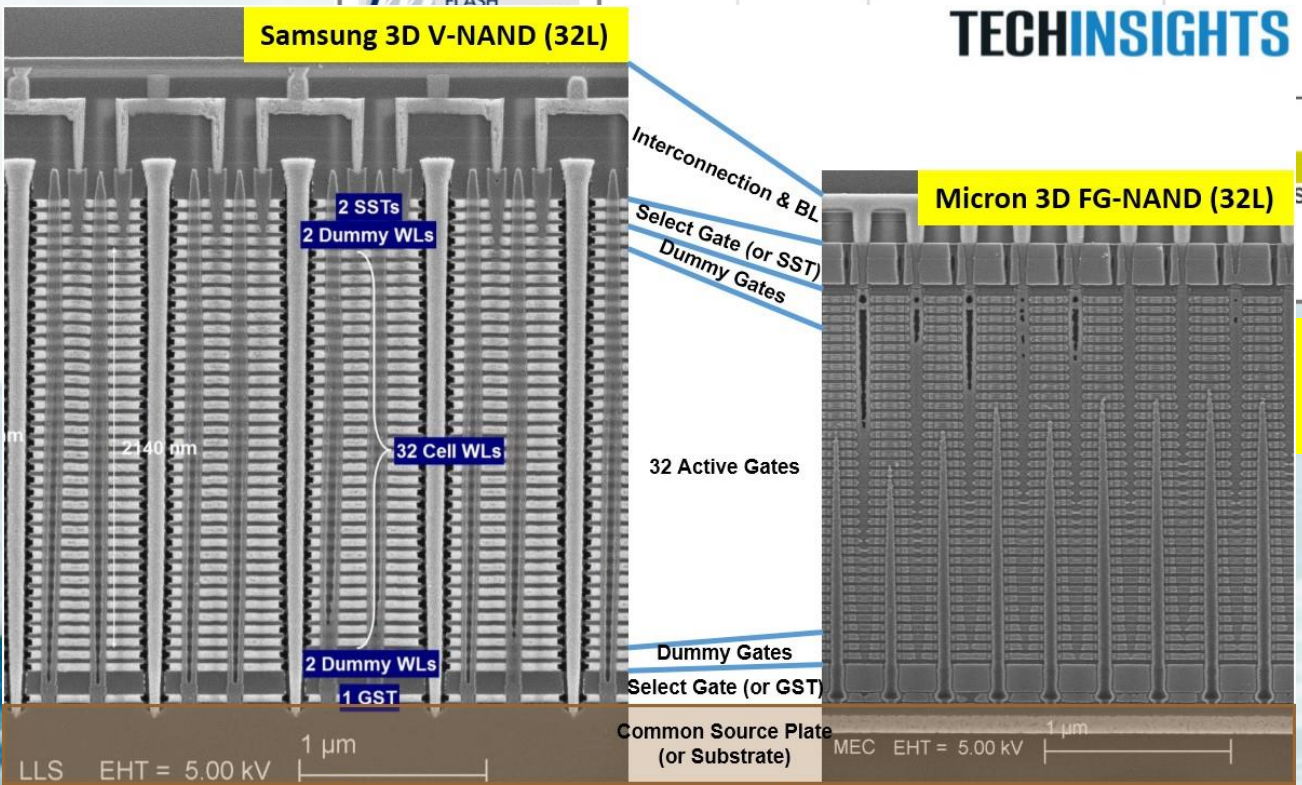






Dick James, May 2017





Best Buy PNY 256Gb=$49.99
$0.195/Gb

Techinsights Nov 2016

Outline

- **Introduction: Smartphone Market Driver for 3-D**
- **3-D Bulk FinFET Transistor Formation**
  - 22nm→14/16nm→10nm→7nm→5nm
- **3-D FinFET High Mobility Channel Formation**
- **3-D Gate-All-Around Nanowire Transistor Formation for sub-5nm node or Monolithic 3-D stacking**
- **Summary**

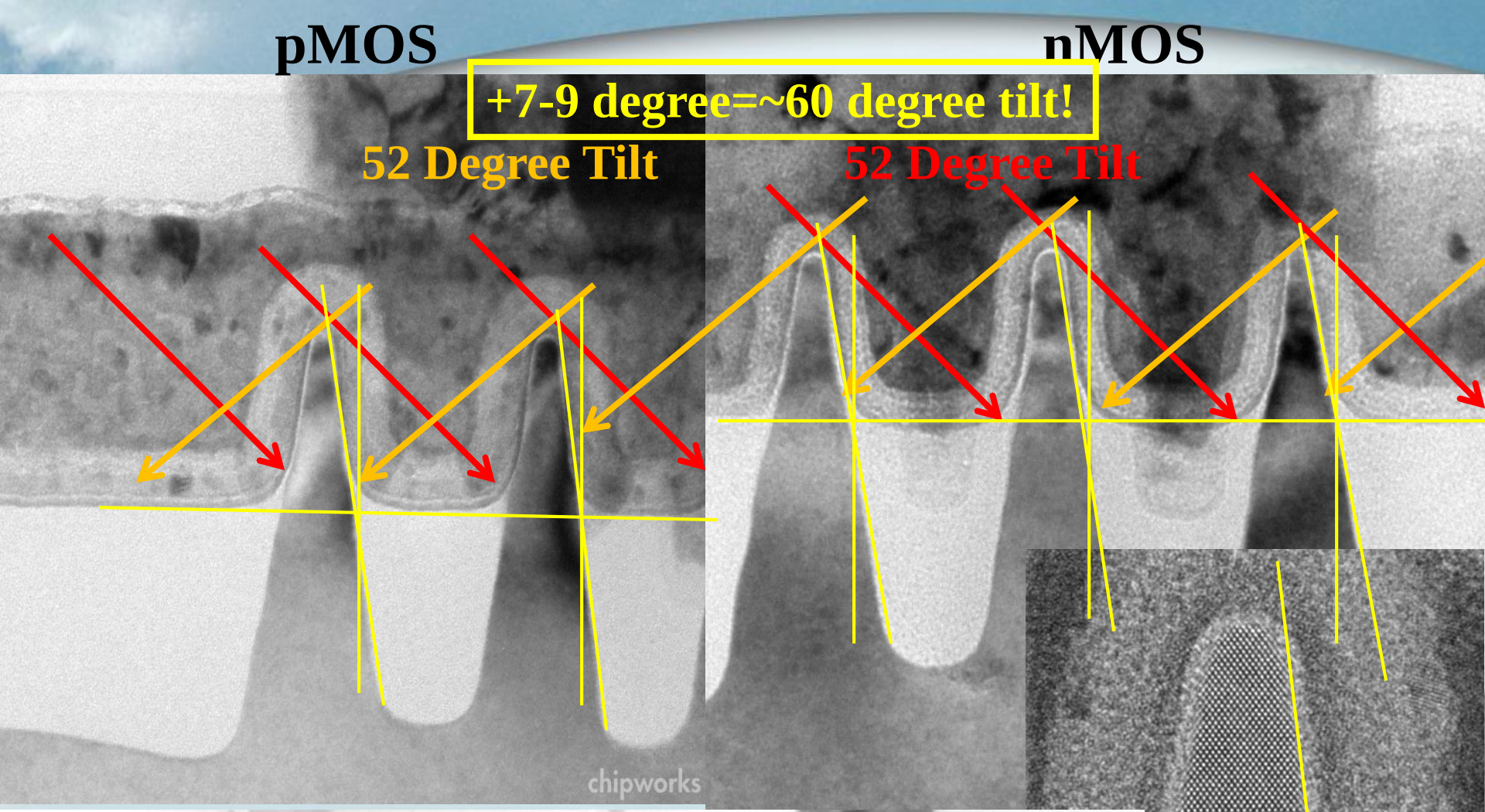
pMOS

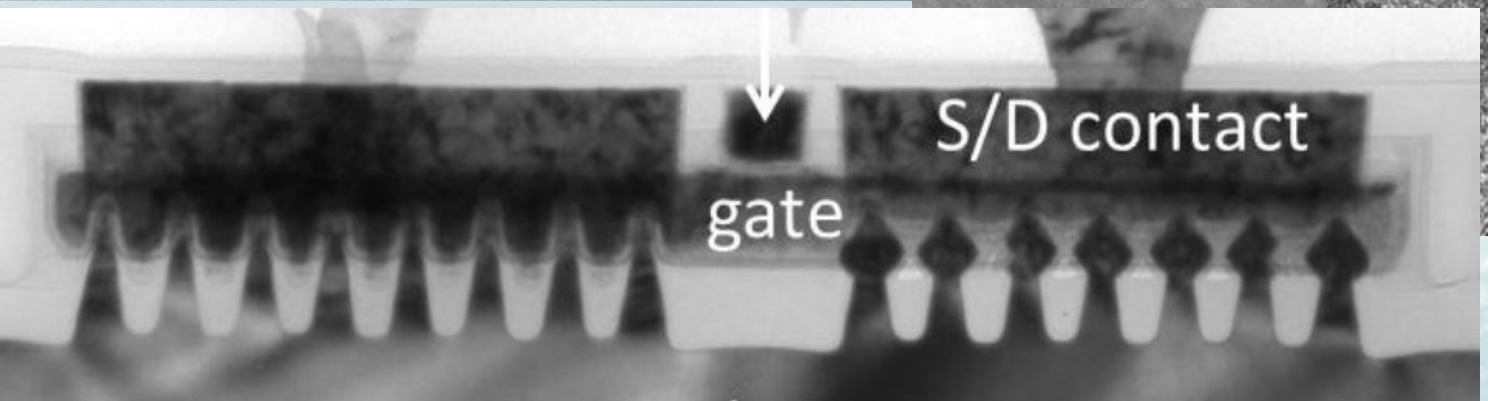
nMOS

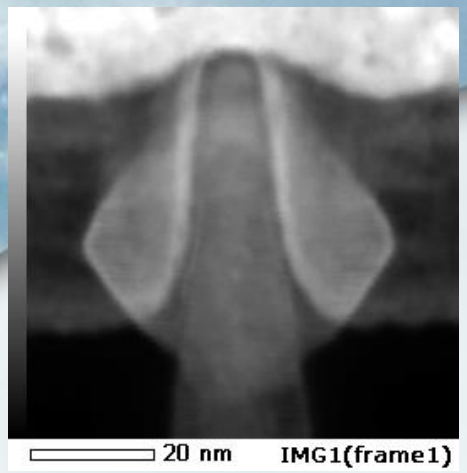
+7-9 degree=~60 degree tilt!

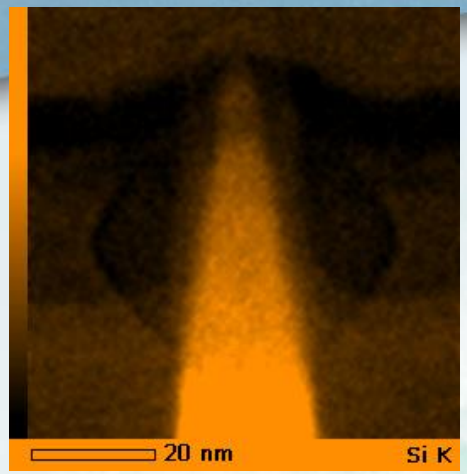
52 Degree Tilt

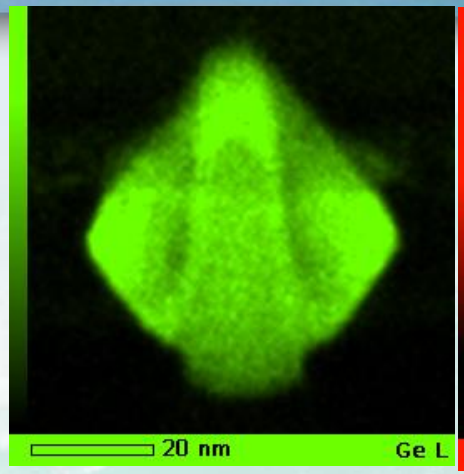
52 Degree Tilt

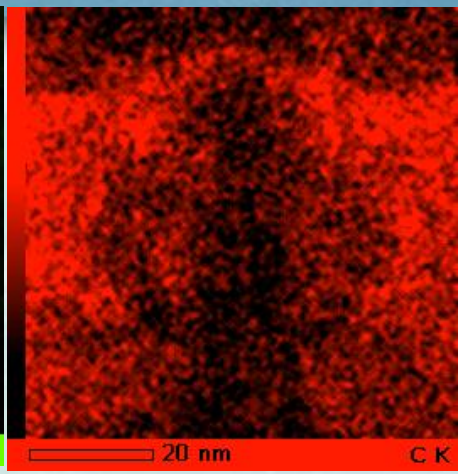


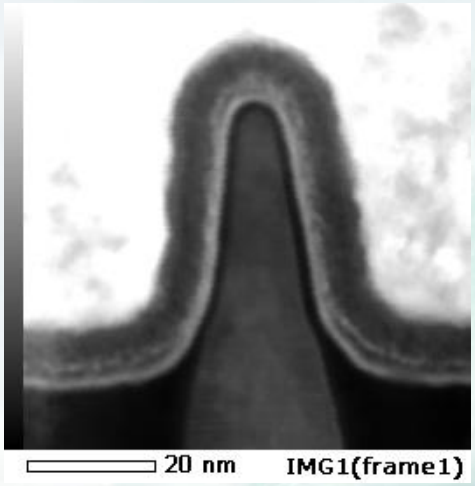


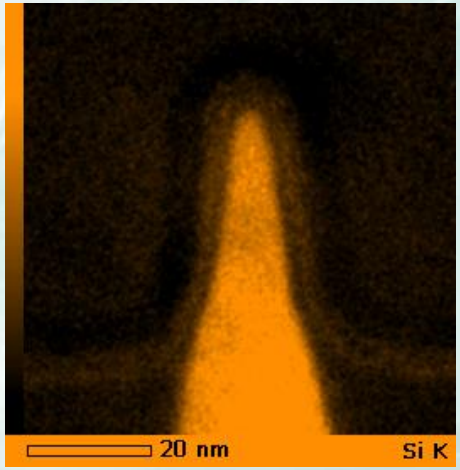


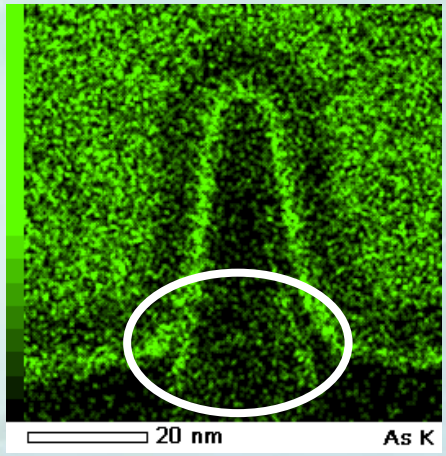


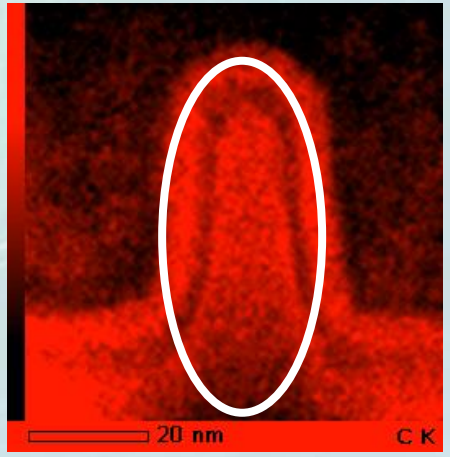




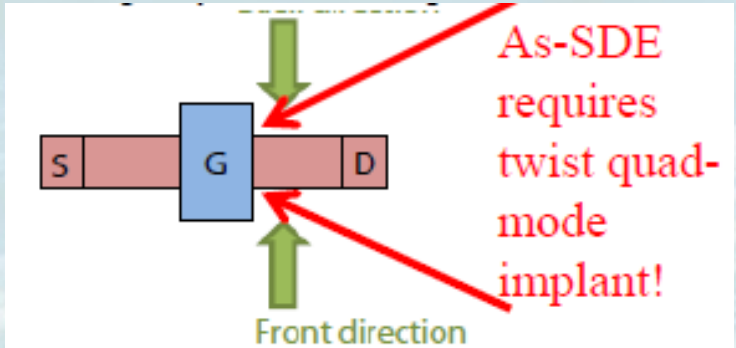


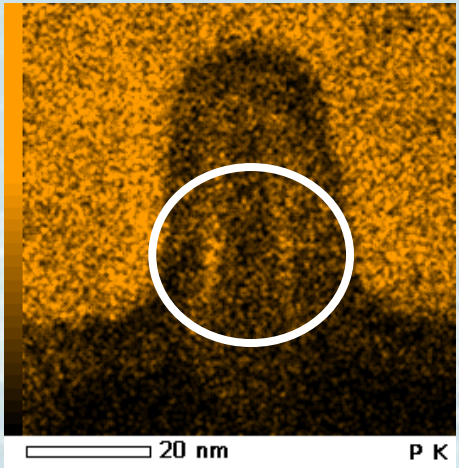




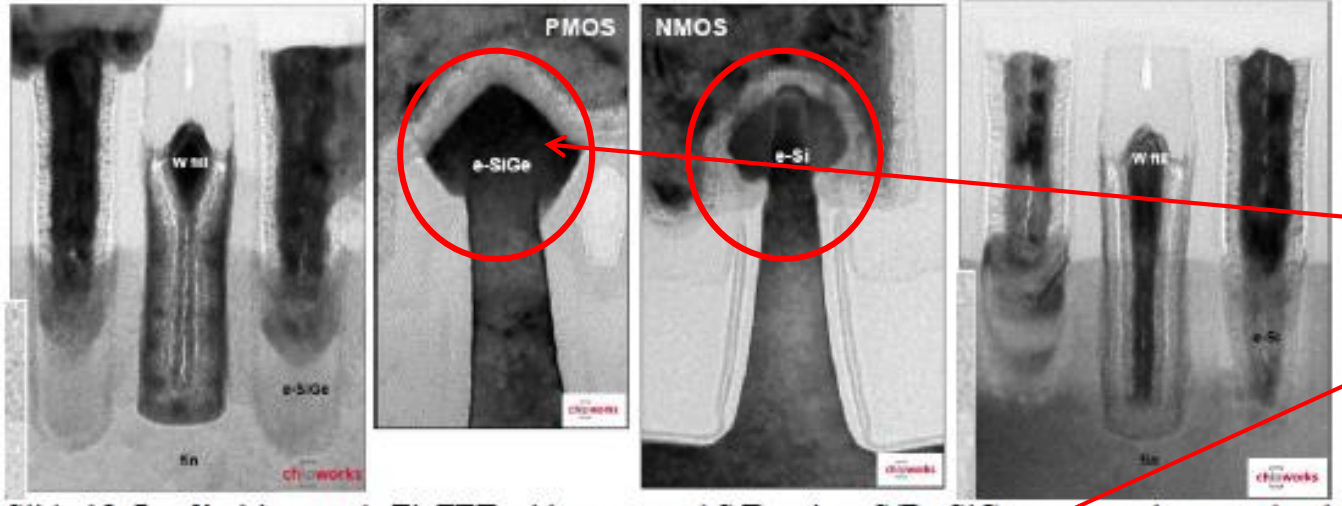


Prof. Ogura, Meiji Univ. 3/1/16





J.O.B. Technologies (Strategic Marketing, Sales & Technology)



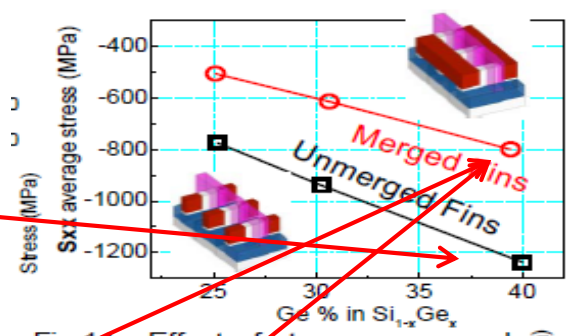
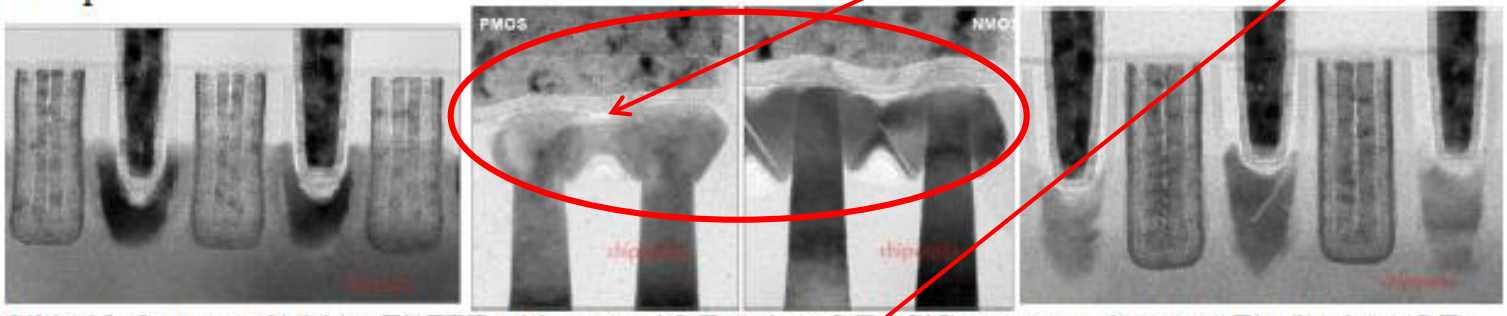
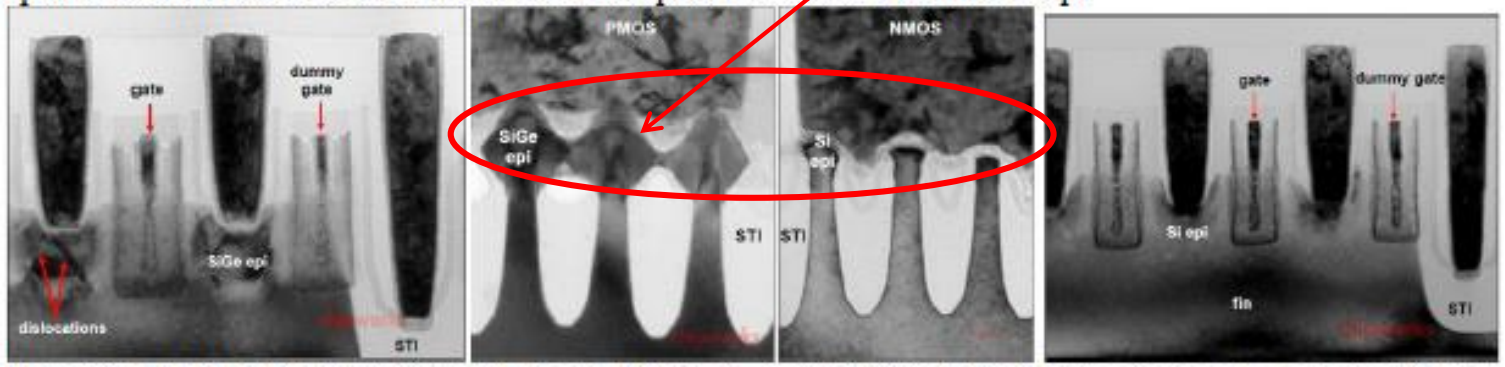


Fig 14: Effect of stress on merged vs. unmerged fins. Stress produced increases with Ge%. Efficiency of stress transfer into channel decreases when epitaxy between adjacent fins is merged.

Slide 18: **Intel**'s 14nm node FinFET with unmerged S/D-epi, p+S/D eSiGe recess etch not under the gate spacer but below gate Fin depth. Added shallow or no recess etch for n+S/D-epi. No contact etch erosion of raised S/D-epi.



Slide 19: **Samsung**'s 14nm FinFET with merged S/D-epi, p+S/D eSiGe recess etch to gate Fin depth, n+S/D-epi has shallow recess etch. Contact etch causes partial erosion of raised S/D-epi.



Slide 20: **TSMC**'s 16nm FinFET with merged S/D-epi, p+S/D eSiGe full of dislocations and no erosion from contact etch while n+S/D-epi is almost completed eroded away after contact etch.

14/16nm FinFET by Intel, Samsung & TSMC

Demonstration of a sub-0.03 um^2 High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node

Shien-Yang Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, C.H. Chang, V.S. Chang, K.H. Pa
T. Miyashita, Y.K. Wu, K.C. Ting, C.H. Hsieh, R.F. Tsui, R. Chen, C.L. Yang, H.C. Chang, C.Y. Lee, I

168, Park Ave. 2, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C., Email: shien-ya
Taiwan Semiconductor Manufacturing Company

VLSI-2016 paper 9.1

Process Enablers

Advanced pitch-splitting patterning technique with 193nm immersion lithography is used to enable pitch scaling for critical layers. Fin width and profile are carefully optimized to maintain excellent short channel with scaled gate length to reduce parasitic capacitance between contact and gate. Raised source/drain with dual epitaxy process is optimized to mitigate source/drain (S/D) parasitic resistance. Enhanced contact process is developed to enlarge manufacturing margin.

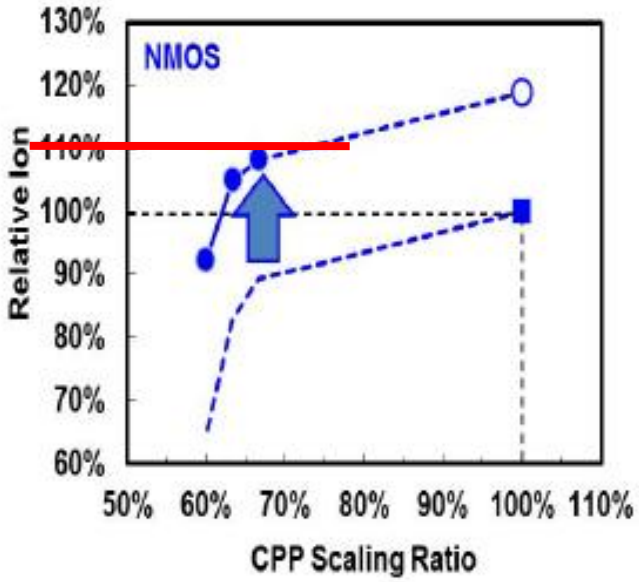


Fig.8 NMOS Ion boost with mobility enhancement and resistance reduction.

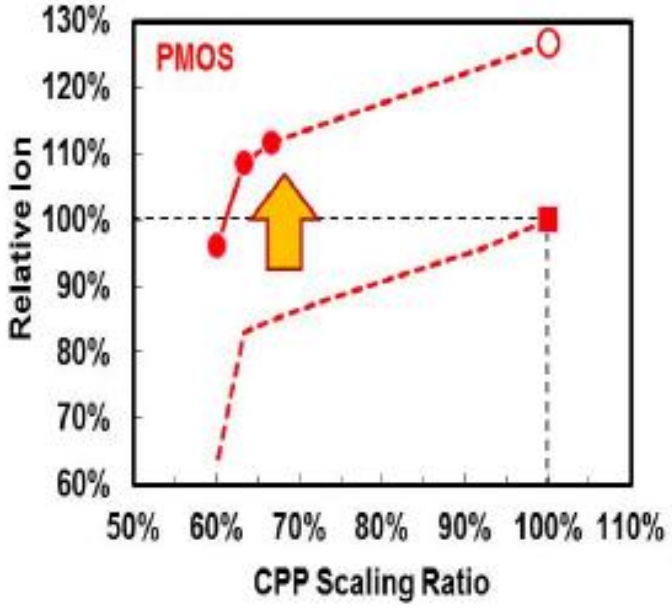


Fig.9 PMOS Ion boost with mobility enhancement and resistance reduction.

A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027um² High Density 6-T SRAM cell for Mobile SoC Applications

Shien-Yang Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, S.H. Yang, C.H. Tsai, P.N. Chen, T. Miyashita, C.H. Chang, V.S. Chang, K.H. Pan, J.H. Chen, Y.S. Mor, K.T. Lai, C.S. Liang, H.F. Chen, S.Y. Chang, C.J. Lin, C.H. Hsieh, R.F. Tsui, Chang, K.W. Chen, M.H. Tsai, K.S. Chen, Y. Ku, S. M. Jang

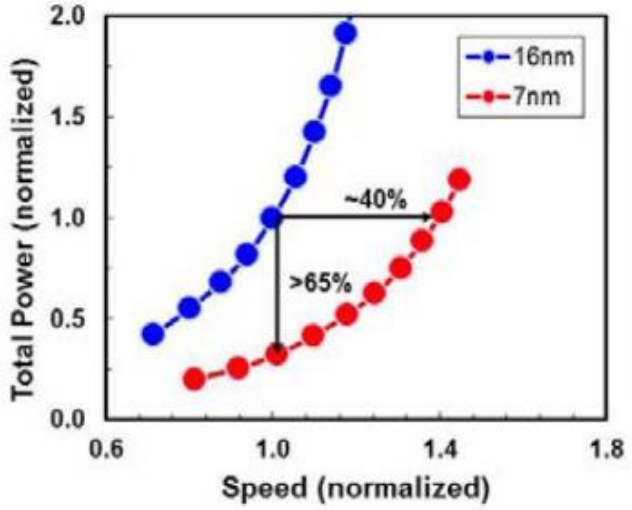


Fig. 1 FOM shows 40% speed gain or >65% power reduction over our 16nm technology.

for SoC design. Raised source/drain with dual epitaxy process is optimized in order to provide the necessary channel strain and to reduce source/drain (S/D) parasitic resistance. A novel contact process is developed to support tight CPP scaling with robust contact-to-gate isolation.

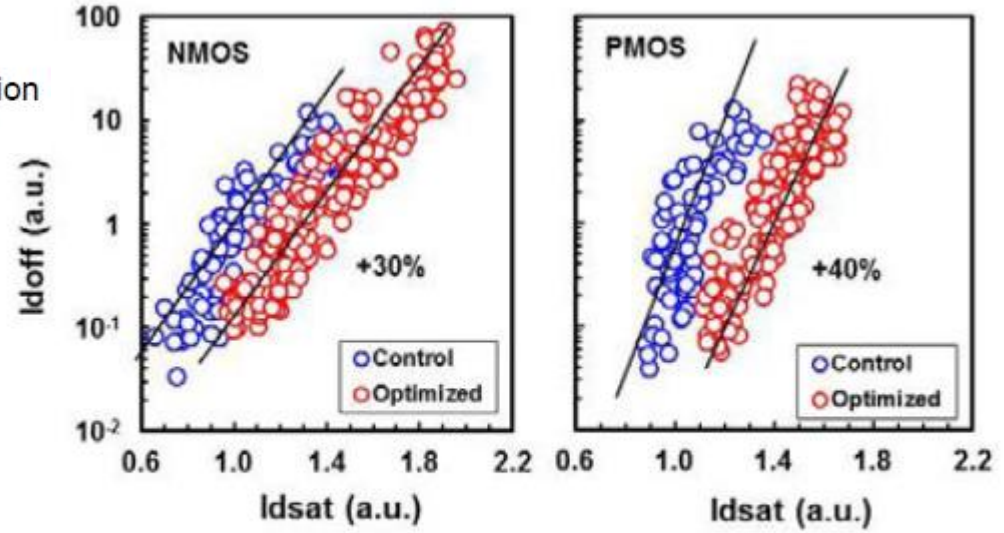


Fig. 5 Device drive current improvement via mobility boost and parasitic resistance reduction.

IEDM-2016 paper 2.6

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

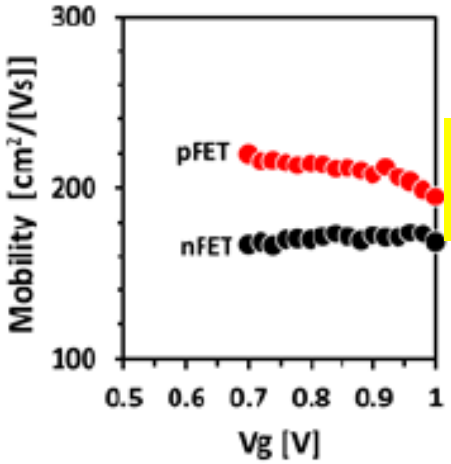
Si FinFET based 10nm Technology with Multi Vt Gate Stack for Low Power and High Performance Applications

H.-J. Cho, H.S. Oh, K.J. Nam, Y.H. Kim, K.H. Yeo, W.D. Kim, Y.S. Chung, Y.S. Nam, S.M. Kim, W.H. Kwon, M.J. Kang, I.R. Kim, H. Fukutome, C.W. Jeong, H.J. Shin, Y.S. Kim, D.W. Kim, S.H. Park, H.S. Oh, J.H. Jeong, S.B. Kim, D.W. Ha, J.H. Park, H.S. Rhee, S.J. Hyun, D.S. Shin, D.H. Kim, H.Y. Kim, S. Maeda, K.H. Lee, Y.H. Kim, M.C. Kim, Y.S. Koh, B. Yoon, K. Shin, N.I Lee, S.B. Kangh, K.H. Hwang, J.H. Lee, J.-H. Ku, S.W. Nam, S.M. Jung, H.K. Kang, J.S. Yoon, ES Jung

Semiconductor R&D Center, Samsung Electronics, San #16, Banweol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Korea,

Key module	10nm	14nm-2	14nm-1
Fin	3rd gen	2nd gen	1st gen
PC patterning	Mandrel	Single photo	
Epi growth	3rd gen	2nd gen	1st gen
Contact	Single	Trench	

Fig. 2 Process technology comparison between 10nm and 14nm technologies.



μh=220
μe=170

Fig. 6 Short channel mobility of pFET and nFET. The mobility of pFET is about 10% higher than that of nFET.

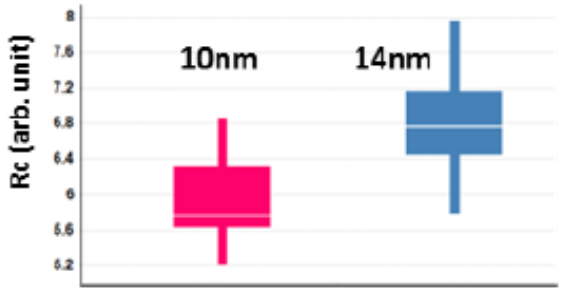


Fig. 3 pFET contact resistance (Rc) is reduced by 10% from 14nm to 10nm technology using contact process optimization.

10nm FinFET will stay with bulk Si-channels and eS/D-stressors. No SiGe channel.

VLSI-2016 paper 2.1

A. Vertical and narrow fin

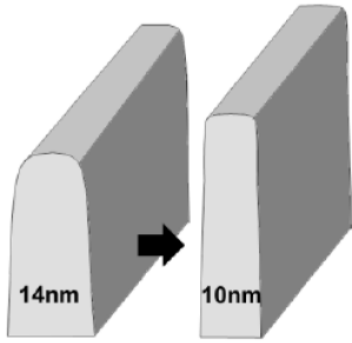


Fig.1: Taller fin height and narrower fin width leads to more vertical profile in 10nm FinFETs.

T6-1

Highly Manufacturable 7nm FinFET Technology featuring EUV lithography for Low Power and High Performance Applications

VLSI-2017

Daewon Ha, C. Yang, J. Lee, S. Lee, S. H. Lee, K.-I. Seo, H.S. Oh, E.C. Hwang, S.W. Do, S.C. Park, M.-C. Sun, D.H. Kim, J.H. Lee, M.I. Kang, S.-S. Ha, D.Y. Choi, H. Jun, H.J. Shin, Y.J. Kim, J. Lee, C.W. Moon, Y.W. Cho, S.H. Park, Y. Son, J.Y. Park †, B.C. Lee†, C. Kim†, Y.M. Oh†, J.S. Park†, S.S. Kim†, M.C. Kim†, K.H. Hwang†, S.W. Nam†, S. Maeda, D.-W. Kim, J.-H. Lee, M.S. Liang, ES Jung

Logic TD & †Process Development Team, Semiconductor R&D Center, Samsung Electronics Co. Ltd., San#16, Banweol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Republic of Korea, email: daewon.ha@samsung.com

Table I Key process features of 7nm CMOS FinFET

	7nm	10nm
Device Arch	Bulk-FinFET	Bulk-FinFET
Fin	Dual Fin	Single Fin
S/D	4th gen. Epi	3rd gen. Epi
RMG	2nd multi-eWF	1st multi-eWF
Contact	EUV	MPT
BEOL	EUV	MPT

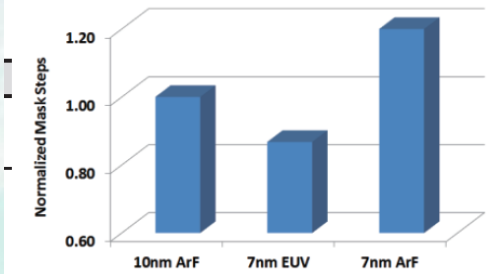


Fig. 1 EUV lithography is fully adopted for MOL contacts & minimum pitched metal/via interconnects. >25% mask steps can be reduced compared with advanced DPT using ArF immersion lithography.

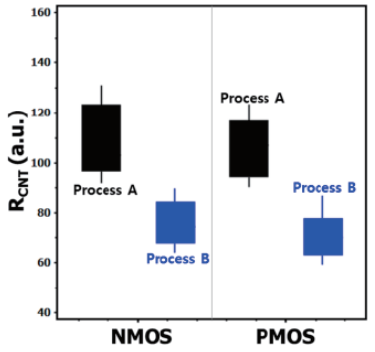


Fig. 7 The reduction of R_{CNT} can be achieved for both N- and PMOS by optimizing the contact processes.

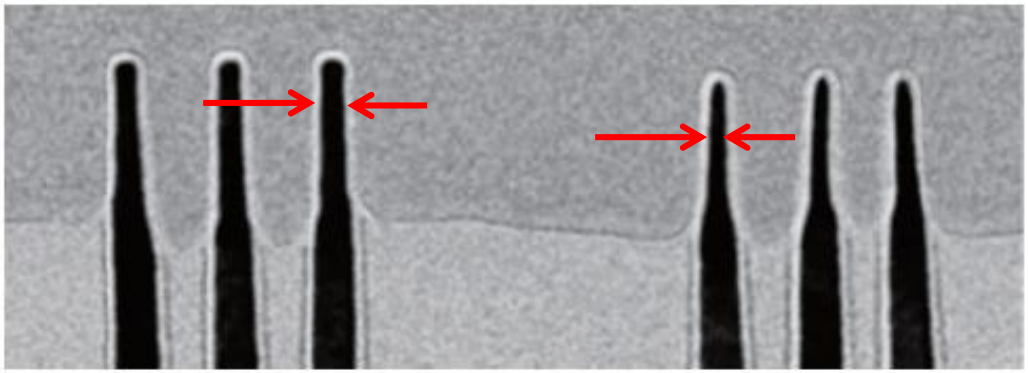


Fig. 2 4th generation Fin provides vertical and thin Fins with dual fin widths. Dual fins help optimizing SCE and R_{EXT}.

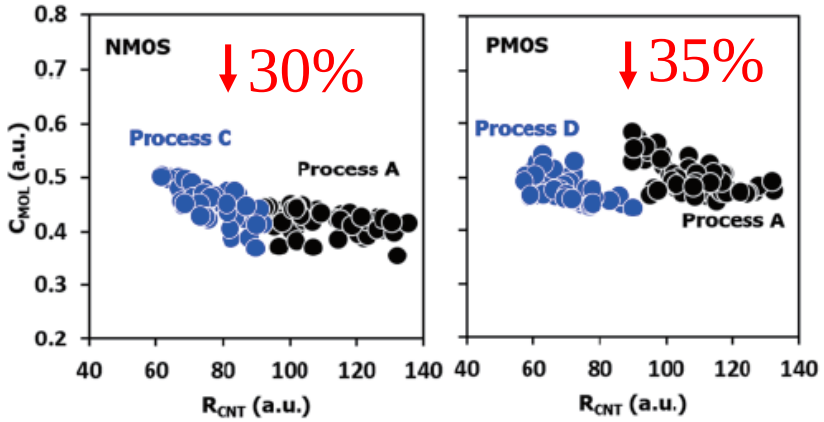
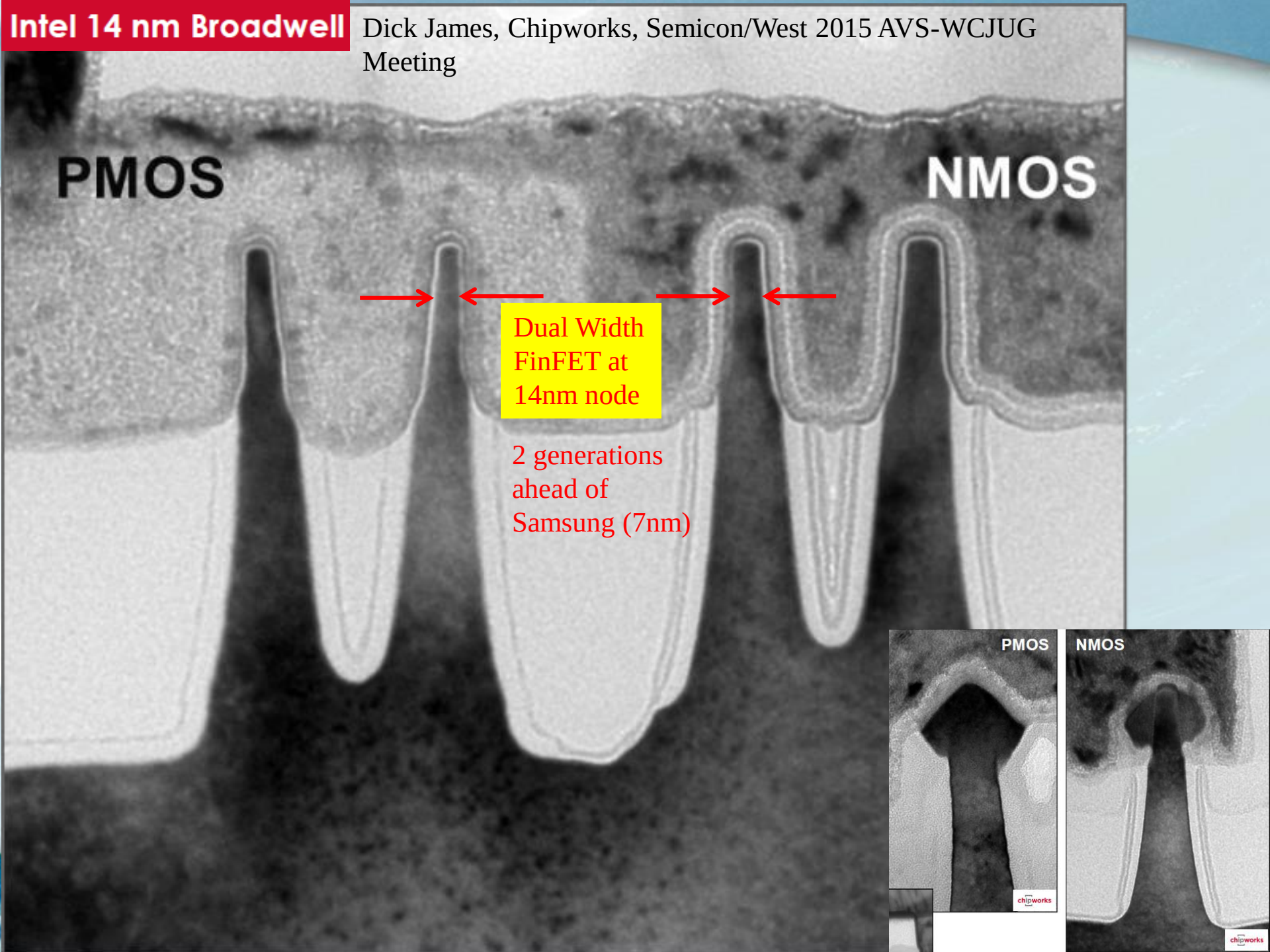
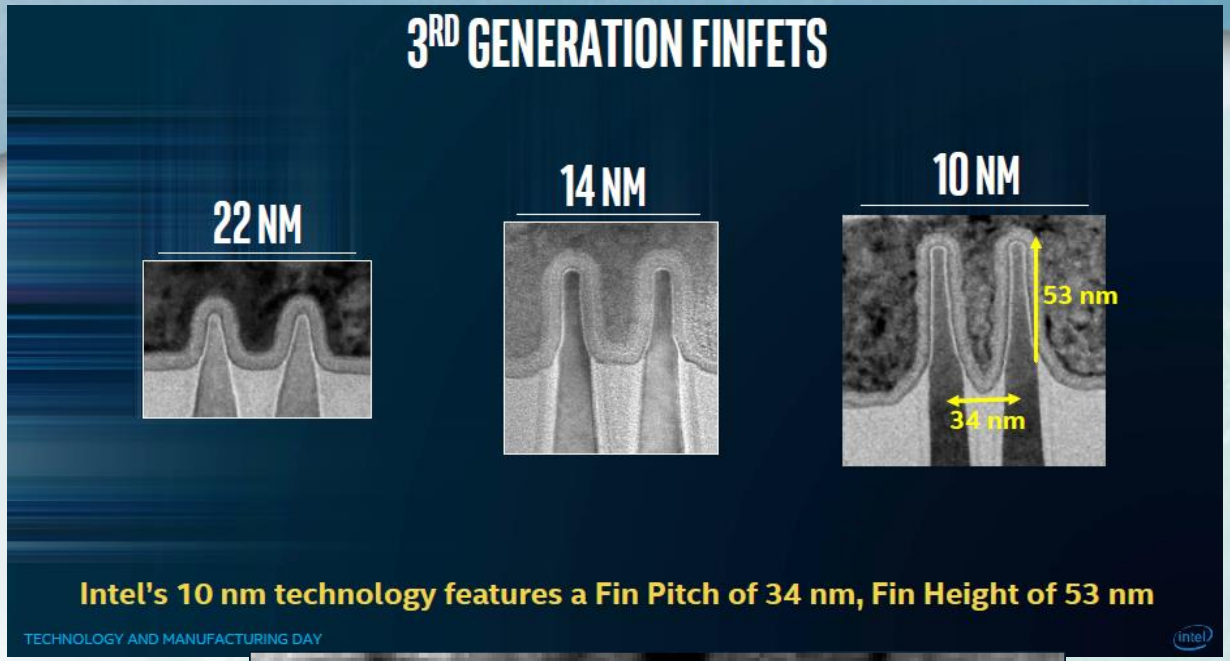


Fig. 8 The Reduction of R_{CNT} without sacrificing C_{MOL} can be achieved by optimizing the gate length, S/D epi and contact processes at the same time.

Intel 14 nm Broadwell

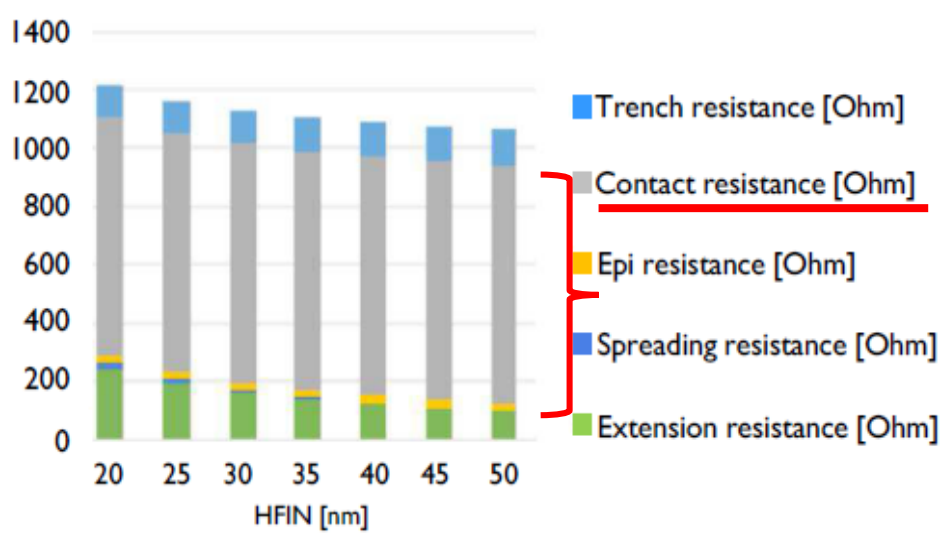
Dick James, Chipworks, Semicon/West 2015 AVS-WCJUG Meeting





NMOS only,
No Image of PMOS

From Dick James
March 28, 2017: **Intel** *Technology and Manufacturing Day*



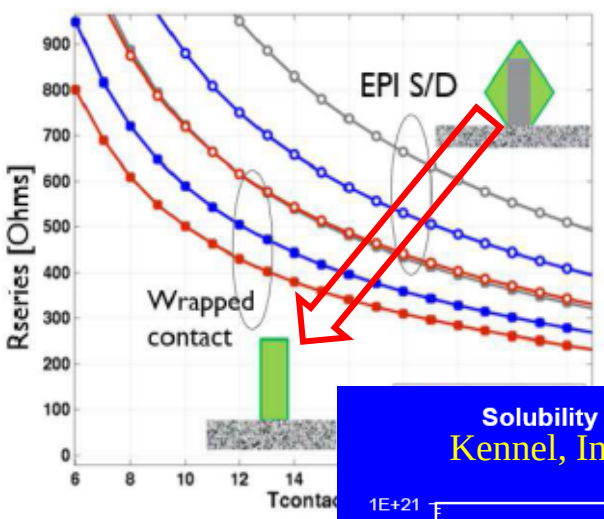
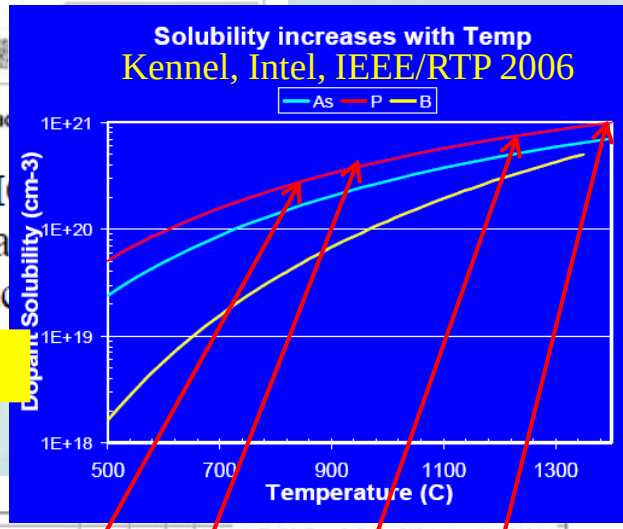
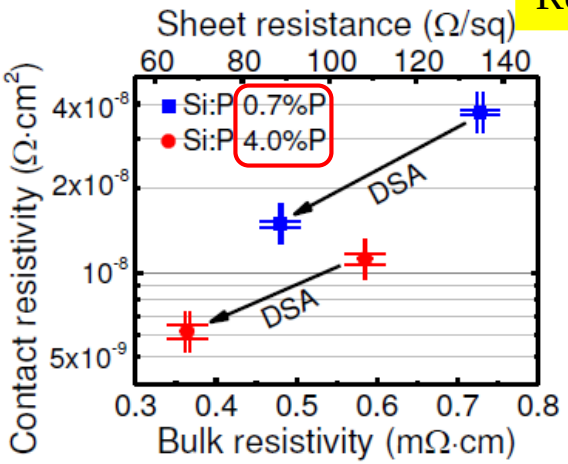
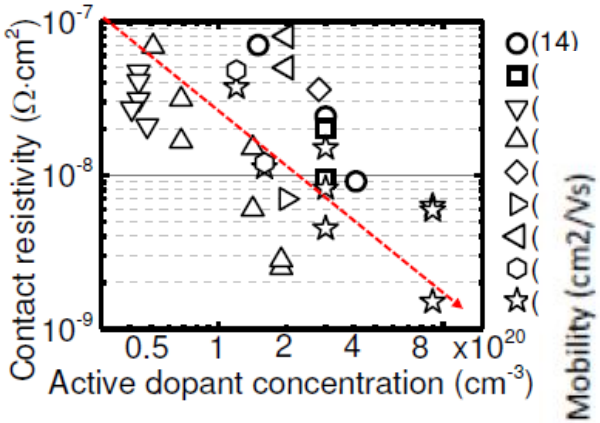


Figure 1. From (1). Left : N7 Series resistance simulations for a 4 fin PM parts of the device as function of the fin height. Right : N7 Series resista versus contact width for standard epi S/D contacts and wrapped contac contact resistivities.



Rosseel et al., IMEC/ASM, ECS Oct 2016





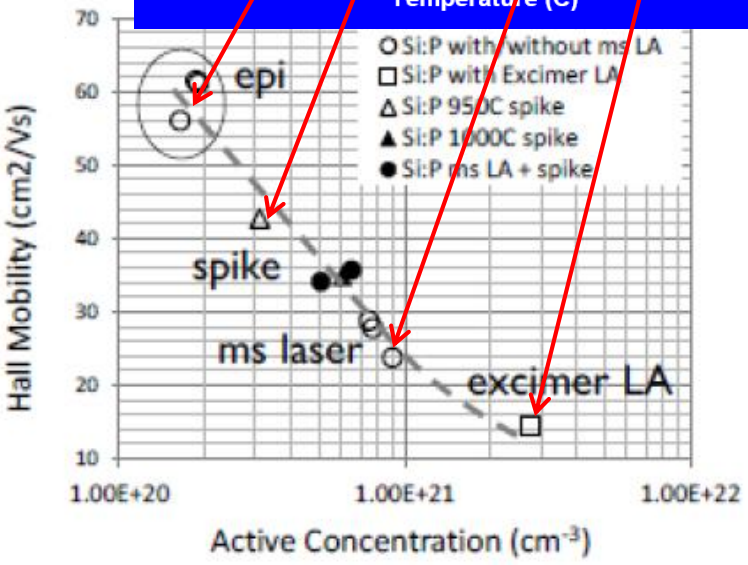


Figure 7. From (22). Left : MR-CTLM based contact resistivity versus sheet resis layers with different P concentrations ($3 \cdot 10^{20}$ cm^{-3} or 0.7% vs $2 \cdot 10^{21}$ cm^{-3} or 4%). contact metal. Right : Contact resistivity benchmark plot on n-Si indicating th importance of the active dopant concentration.

VLSI Sym June 2016

Session 7: Contact Resistance Innovations for Sub-10nm Scaling

Paper 7.5: UMC/AMAT ultralow p+ SiGe contact resistivity (5.9E-9Ω-cm2)

Paper 7.1: IMEC/AMAT/Samsung ultralow resistivity contacts (2.1E-9Ω-cm2)

Pre-contact PAI

SiP =2E21/cm^3 + **Ge-PAI**=2.1x10^{-9} Ω-cm^2
70%-SiGeB + **Ge-PAI**= 2.1x10^{-9} Ω-cm^2

Paper 7.3: AMAT 7nm node ultralow n+ contact resistivity (<1.0E-9Ω-cm2)

DSA versus nsec laser annealing

Paper 7.4: GF/IBM canceled: Sub-2x10^{-9} Ω-cm^2 N- and P-Contact Resistivity with Si:P and Ge:Ga Metastable Alloys for FinFET CMOS Technology

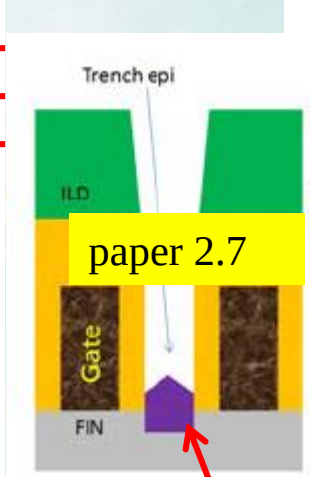
FinFET performance with Si:P and Ge:Group-III-Metal Metastable Contact Trench Alloys

O. Gluschenkov[1], Z. Liu[1], H. Niimi[2], S. Mochizuki[1], J. Fronheiser[2], X. Miao[1], J. Li[1], J. Demarest[1], C. Zhang[1], C. Niu[2], B. Liu[2], A. Petrescu[1], P. Adusumilli[1], J. Yang[1], H. Jagannathan[1], H. Bu[1], and T. Yamashita[1]

[1]IBM Research at Albany NanoTech, 257 Fuller Road, Albany NY 12203, email: olegg@
[2]GLOBALFOUNDRIES Inc., 257 Fuller Road, Albany NY 12203

IEDM-2016 paper 17.2

Abstract— We achieved mid-10^{-10} Ω-cm^2 n-type S/D contact resistivity ($n\rho_c$) and 1.9x10^{-9} Ω-cm^2 p-type S/D contact resistivity ($p\rho_c$) by employing laser-induced liquid or solid phase epitaxy (LPE/SPE) of Si:P and Ge:Group-III-Metal metastable alloys inside nano-scale contact trenches. The Ge:Group-III-Metal alloy allows for a metal-Ge Fermi level pinning effect to lower Schottky barrier height (SBH) while reducing both bulk and unipolar heterojunction resistances. Correspondingly, large R_{on} reduction and I_d gain have been realized in scaled n- and p-FinFETs with the contact length of less than 20nm.



paper 2.7

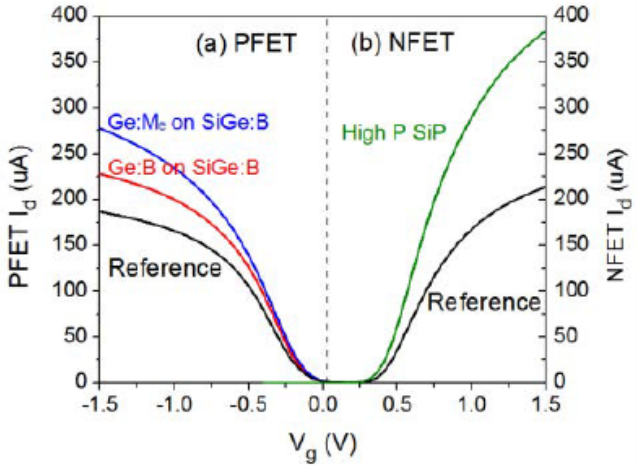


Fig. 7. I_d/V_g characteristics of (a) PFET and (b) NFET. L_g at 20nm, and V_{ds} at 0.05V. Both Ge:Group-III-Metal and Si:P metastable alloys improve electrical properties. NFET and PFET devices are the same as in Fig. 5 and Fig. 16, respectively.

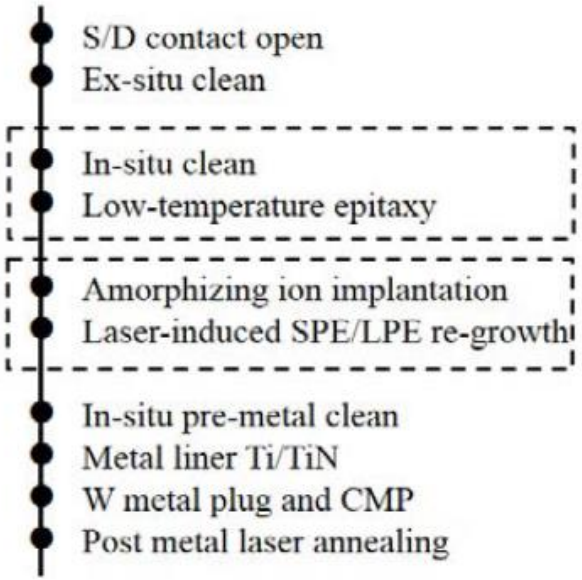


Fig. 2. Process flow for metastable alloy formation.

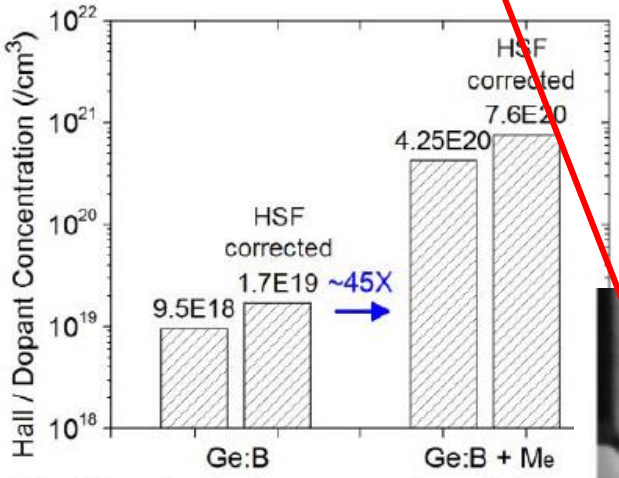


Fig. 12. Active hole concentrations for B ar Group-III-Metal in Ge by Hall measuremen Group-III-Metal chemical concentration [M is ~1x10^{21} cm^{-3} while [B] is ~2x10^{19} cm^{-3}. H scattering factor (HSF) is 1.8.

B=2E19/cm3
Group III-Me=1E21/cm3

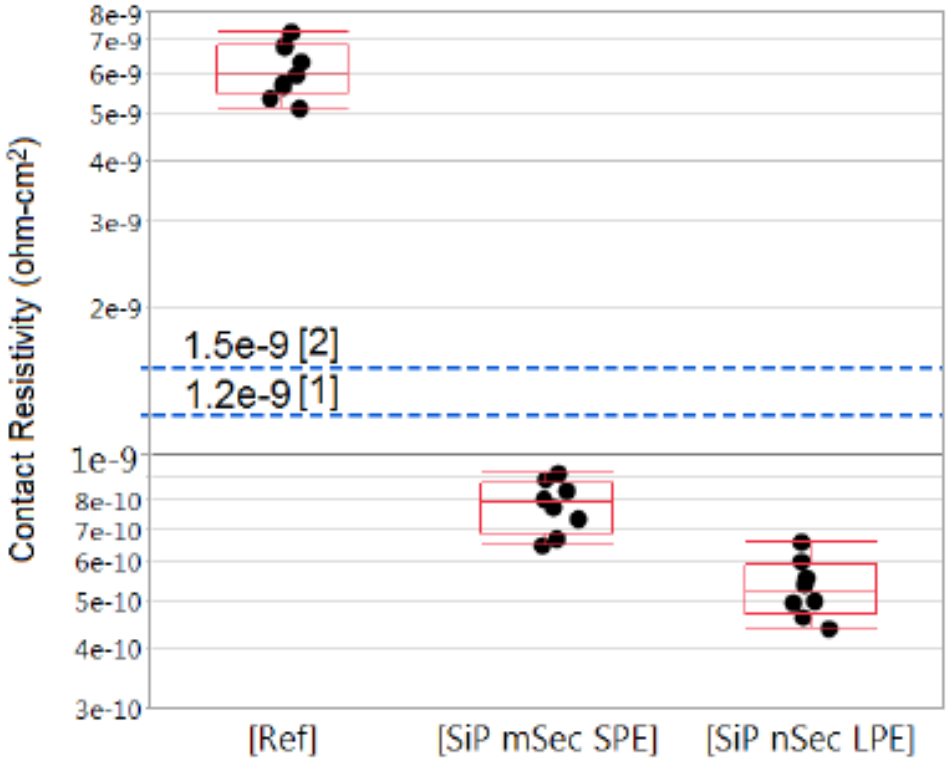


Fig. 5. Distribution of $n\rho_c$ extracted from nFinFET Kelvin probing, as shown in Fig. 3. Cases [Ref], [SiP mSec SPE], and [SiP nSec LPE] correspond to cases [a], [c], and [d] of Fig. 4, respectively. Data from references[1],[2] are shown by dotted lines.

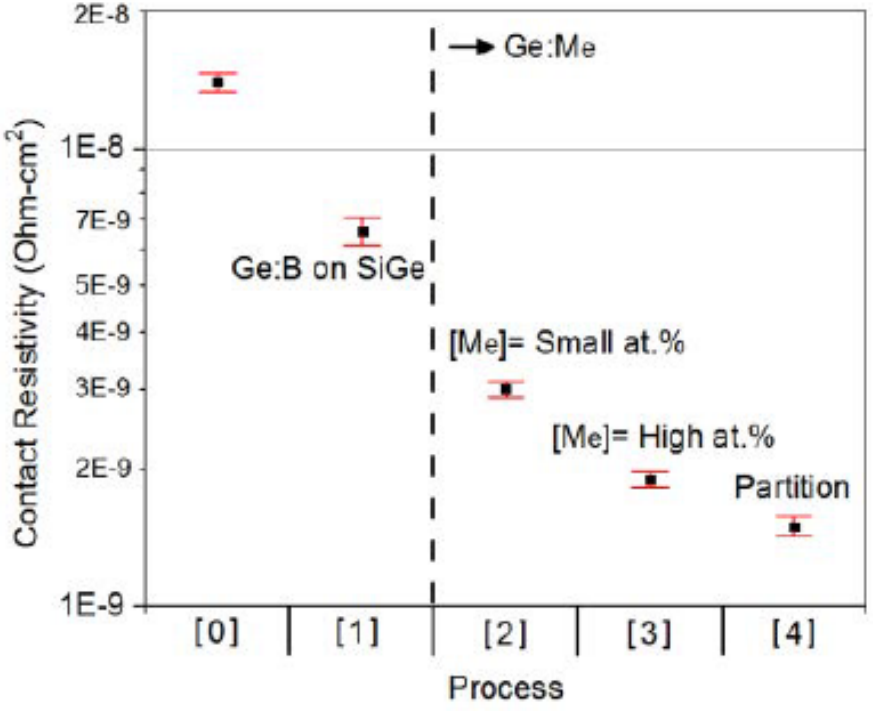


Fig. 14. Improvement of $p\rho_c$ with metastable Ge:Group-III alloys. Case [0] is the SiGe:B reference. Case [1] is the Ge:B trench epitaxial layer. Cases [2]-[3] are Ge:B:Group-III-Metal metastable alloys where [Me] is above chemical solubility in Ge and $[Me]_{case[3]}$ is twice of $[Me]_{case[2]}$. Case [4] is an upper bound estimate for metal-to-semiconductor-alloy contact resistance of case [3].

Technology viable DC performance elements for Si/SiGe channel CMOS FinFET

Gen Tsutsui, Ruqiang Bao, *Kwan-yong Lim, Robert R. Robison, Reinaldo A. Vega, Jie Yang, Zuoguang Liu, Miaomiao Wang, Oleg Gluschenkov, Chun Wing Yeung, Koji Watanabe, *Steven Bentley, *Hiroaki Niimi, Derrick Liu, Huimei Zhou, *Shariq Siddiqui, *Hoon Kim, *Rohit Galatage, Rajasekhar Venigalla, *Mark Raymond, Praneet Adusumilli, Shogo Mochizuki, Thamarai S. Devarajan, Bruce Miao, *Bei Liu, Andrew Greene, Jeffrey Shearer, Pietro Montanini, Jay W. Strane, *Christopher Prindle, Eric R. Miller, *Jody Fronheiser, *Chengyu C. Niu, Kisup Chung, James J. Kelly, Hemanth Jagannathan, Sivananda Kanakasabapathy, Gauri Karve, Fee Li Lie, Philip Oldiges, Vijay Narayanan, Terence B. Hook, *Andreas Knorr, Dinesh Gupta, Dechao Guo, Rama Divakaruni, Huiming Bu, and Mukesh Khare
IBM Research, 257 Fuller Rd, Albany NY 12203, USA, * GLOBALFOUNDRIES Inc., NY, USA, email: gtsutsu@us.ibm.com

IEDM-2016 paper 17.4

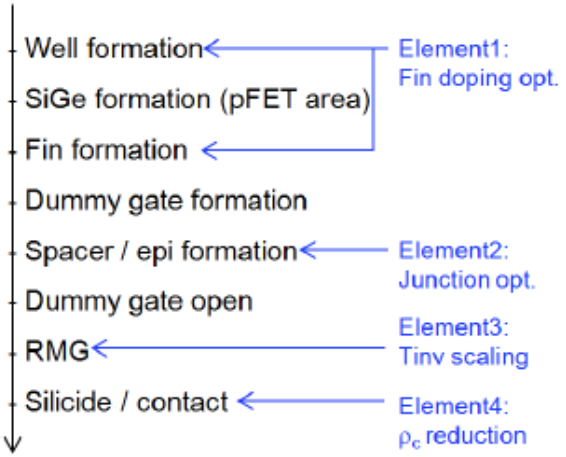


Fig. 1. Baseline integration flow with performance elements insertion shown in blue.

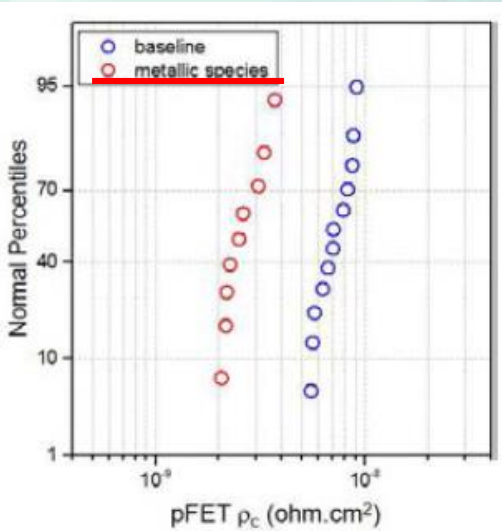


Fig. 10. SiGe-pFinFET ρ_c comparison between baseline and metallic species rich silicide interface.

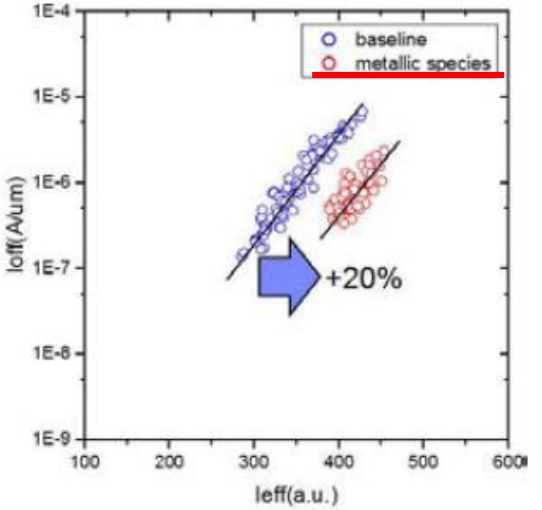


Fig. 11. SiGe-pFiNFET Ioff – Ieff characteristics. DC performance is improved by 20% by ρ_c reduction.

Paper S2-3: Chang of **AMAT** reported 1.2E-9 Ω-cm^2 contact resistivity for 45% p+SiGe using nano-sec laser melt annealing. The process flow is shown in Fig.1 below and the comparison results between control (no contact implant) to B and Ga are shown in Fig. 2a below. Their results actually show that Ga implant was worse than B implant and for some laser fluence conditions the control no contact implant achieved very good contact resistivity! Table I below summaries the comparison between B and Ga contact implants with msec non-melt laser annealing to nsec melt laser annealing. Fig. 5 shows if the laser fluence is too high a void is actually created under the contact region leading to failure.

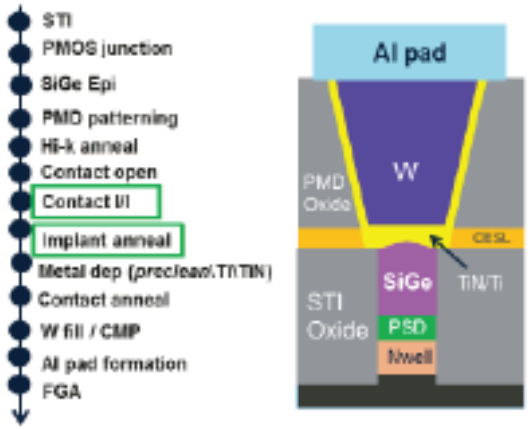


Fig. 1. p-$Si_{0.55}Ge_{0.45}$ contact process flow and cross-sectional schematic of the contact structure.

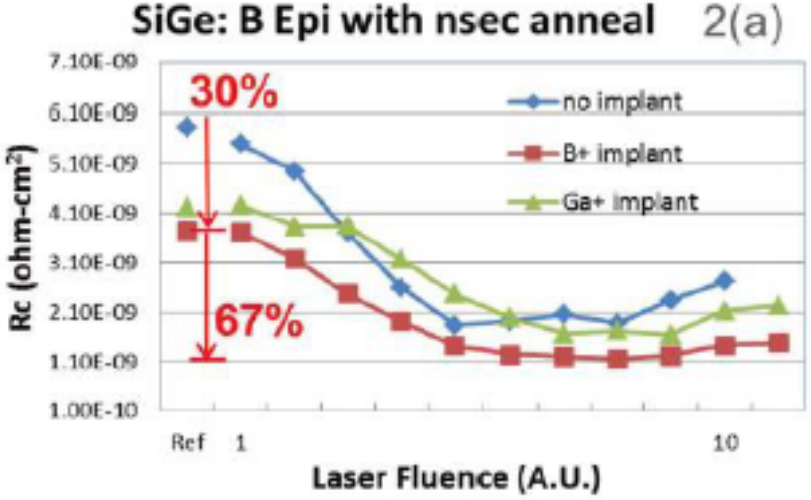


Table I. Summary of ρ_c results for p-$Si_{0.55}Ge_{0.45}$ for various splits

Anneal	Implant	ρ_c (ohm-cm^2)
None	B implant	3.74×10^{-8}
None	Ga implant	4.21×10^{-8}
nsec	B implant	1.24×10^{-9}
nsec	Ga implant	1.63×10^{-9}
msec	B implant	3.59×10^{-9}
msec	Ga implant	3.95×10^{-9}

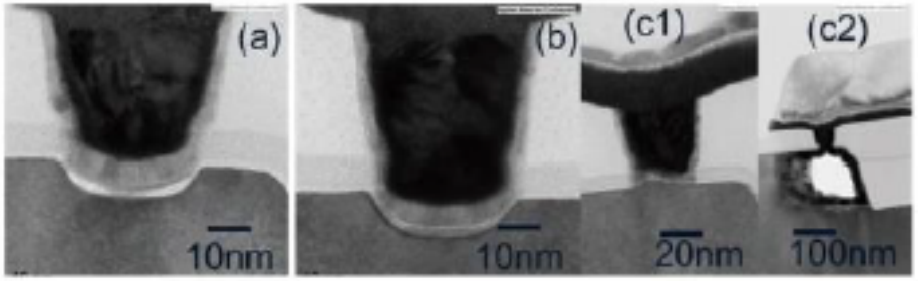


Fig. 5. TEM images of contact chain with NLA (a) no anneal, (b) optimal laser fluence, (c1) (c2) higher laser fluence (TEM images were taken at two different locations on the same wafer).

Paper 16.1: Liu of **IBM/GF/UTEK** reported on their study using UltraTech's non-melt msec laser (LSA) versus melt nsec 532nm laser for low n+ and p+ contact resistance. Fig.2 below shows the process flow of S/D contact formation by SPE and LPE using an amorphous-SiP pocket on n+ SiP-S/D or amorphous-Ge pocket on p+ SiGe-S/D. The process window for LPE (liquid phase epi) is shown in Fig.5 versus Ge content and Table 1 shows actual results for specific laser power levels. Fig.7 shows X-TEM for the n+ contact using SiP with non-melt msec LSA. Fig.9 below shows n+ contact resistance results with melt laser values much lower than non-melt msec LSA result but yield fails for nsec laser anneal temperatures >1300C due to gate stack damage. Fig.8 shows p+ contact resistance results with non-melt msec LSA showing best result at 800C while all the nsec laser melt results were worse also for Fig.11. Gate stack yield failure occurs also at >1300C.

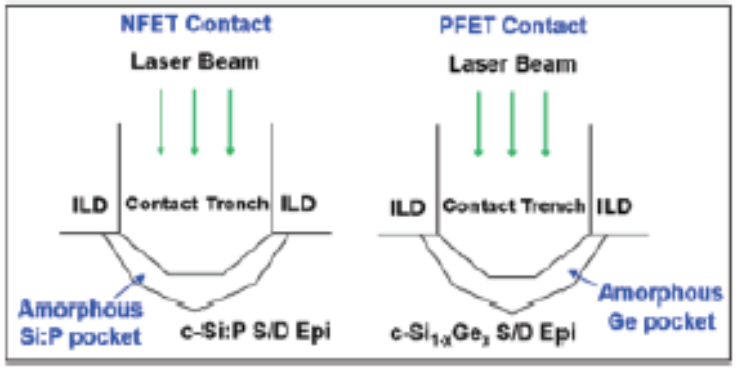


Fig.2 Process flow of S/D contact formation by SPE/LPE.

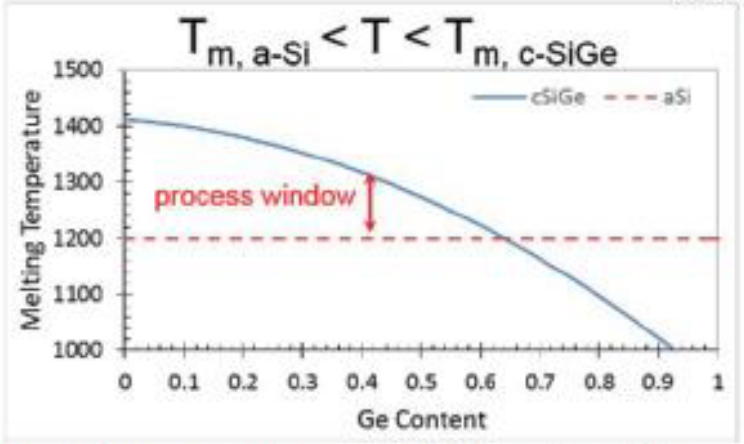


Fig.5 Process window of LPE: a-Si, SiGe.

Wafer	Pre-heat	Power%	Target T
A	700 C	90	1396 C
		82	1335 C
		74	1273 C
		66	1211 C
B	450 C	64	945 C
		56	883 C
		48	821 C
		40	759 C

Si(1-x)	Ge(x)	liquidus
1	0	1412
0.8	0.2	1380
0.5	0.5	1274
0	1	940

Table.1 (a) pre-heat & nSec laser power settings and interpolated temperatures, (b) Si & SiGe liquidus vs Ge content.

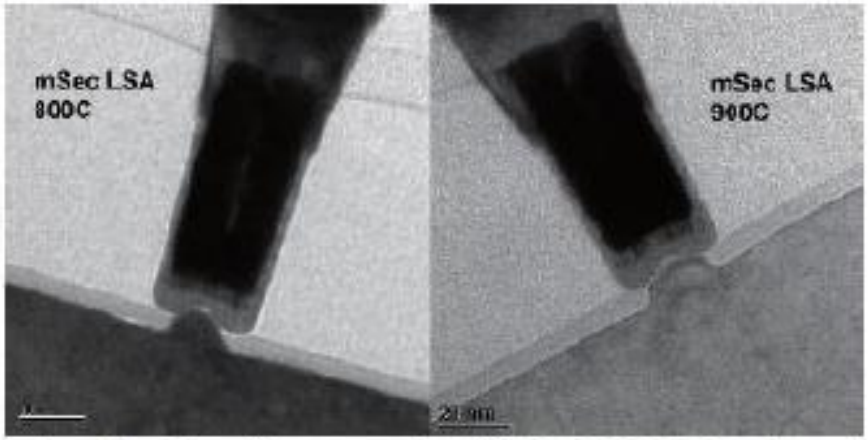


Fig.7 Partial re-growth of Si:P at 800C DB mSec LSA and full re-growth at 900C.

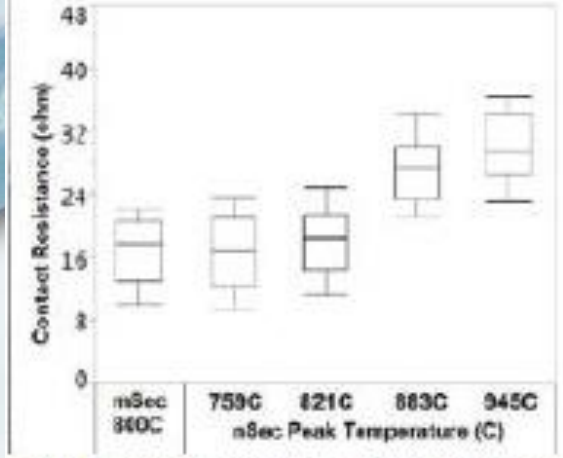


Fig.8 p-type contact resistance trend on TLM (contact W~20nm L=1um).

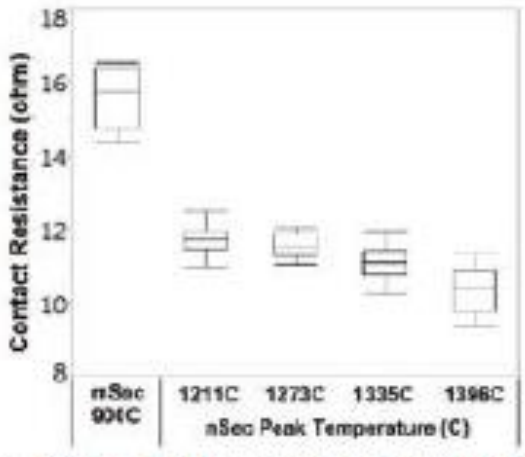
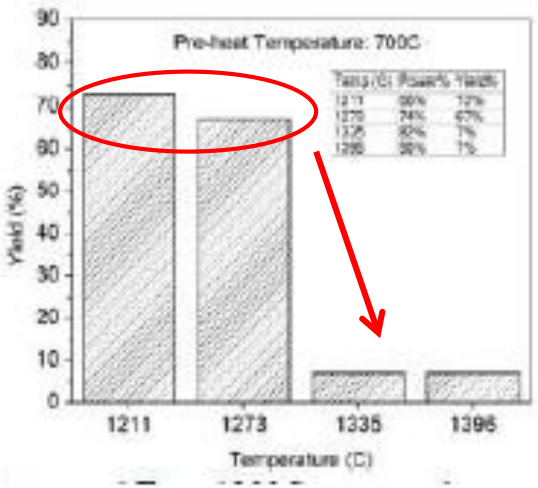


Fig.9 n-type contact resistance trend on TLM (contact W~20nm L=1um).



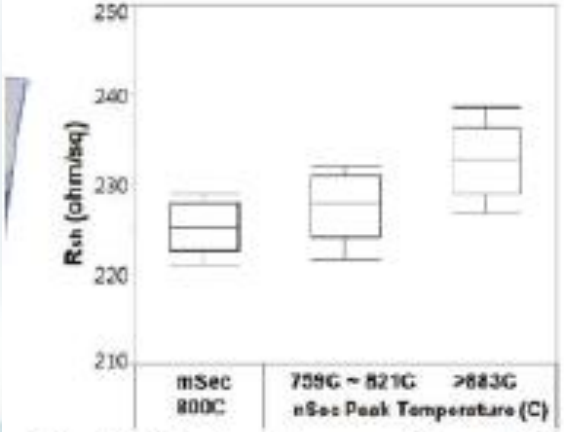
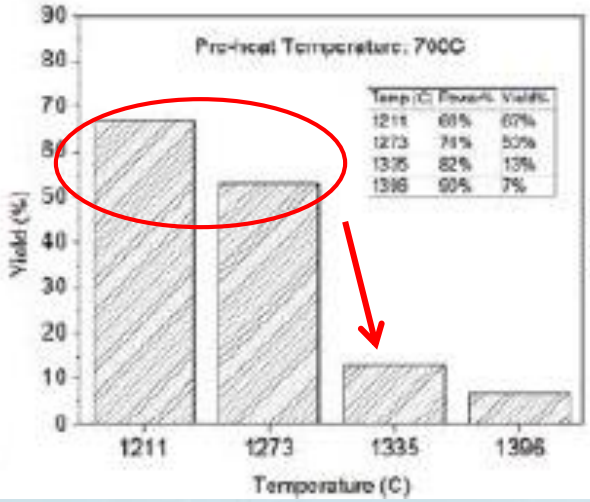
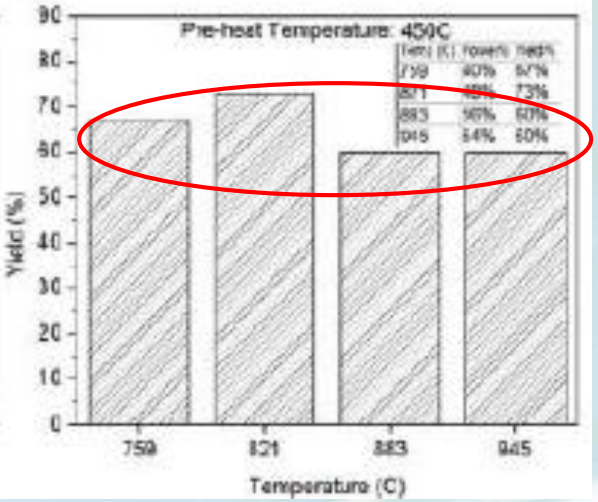


Fig.11 Sheet resistance of base SiGe S/D in mSec & nSec laser annealing.





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Paper 16.2: Everaert of **IMEC/Fudan/AMAT** reported sub-10^{-9} Ω-cm^2 contact resistivity on p-SiGe with Ga doping and nsec laser annealing in comparison to B. Fig.2 shows the process flow and Fig.5 shows the SIMS profiles for B and Ga implants into the 60%-SiGe material after 1000C spike RTA. Enhanced diffusion of Ga is seen compared to B in the SiGe region. Fig.4 shows the Rs and Rc results for B and Ga with spike RTA and DSA laser annealing. With spike RTA, B results were always better than Ga for both Rs and Rc but with msec laser annealing only at the lower temperature of 800C was Ga better than B but at 900C and 1000C DSA Ga again was better than B. However the results with nsec melt laser annealing were different with Ga showing best Rc in the upper E-10Ω-cm^2 range as shown in Fig.6 below although Rs were similar to worse. They explain this difference based on the Ge & Ga EDS profiles showing a surface pile-up at the SiGe/Ti interface in Fig.8 and Fig.7. Table 2 and Fig.9 shows Ga ~11.6% pile-up results in Rc of 1.3E-10Ω-cm^2.

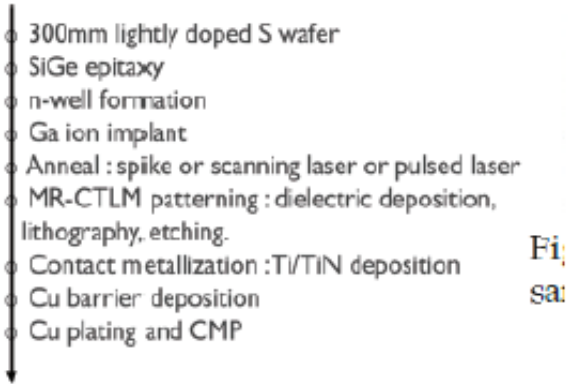

Fig. 2 The process flow for making the MR-CTLM structures.

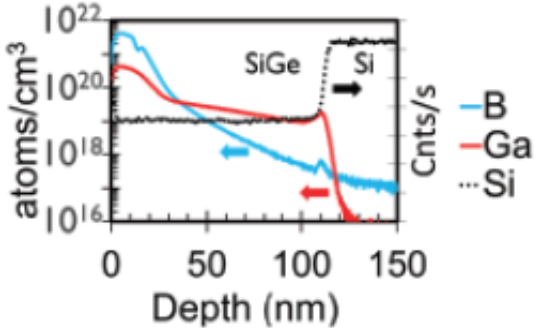

Fig. 5 SIMS profiles of B and Ga doped SiGe after 1000°C spike.

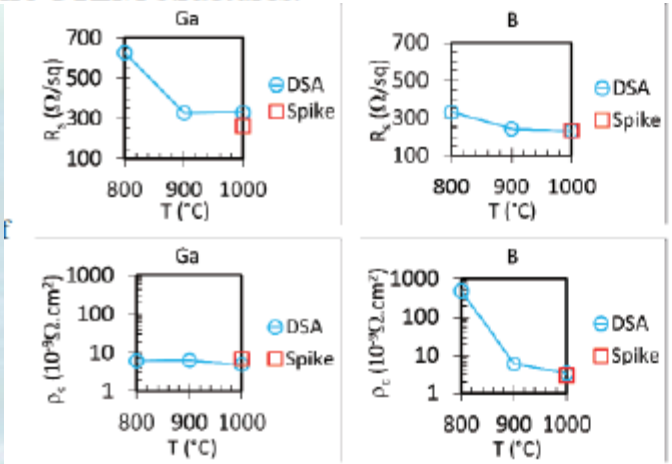

Fig. 4 Comparison of R_s and ρ_c obtained for spike and DSA anneals for Ga and B implanted SiGe

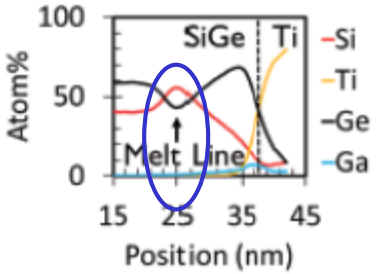

Fig. 8 EDS profile along the melt line towards the Ti/SiGe interface, sample 4.

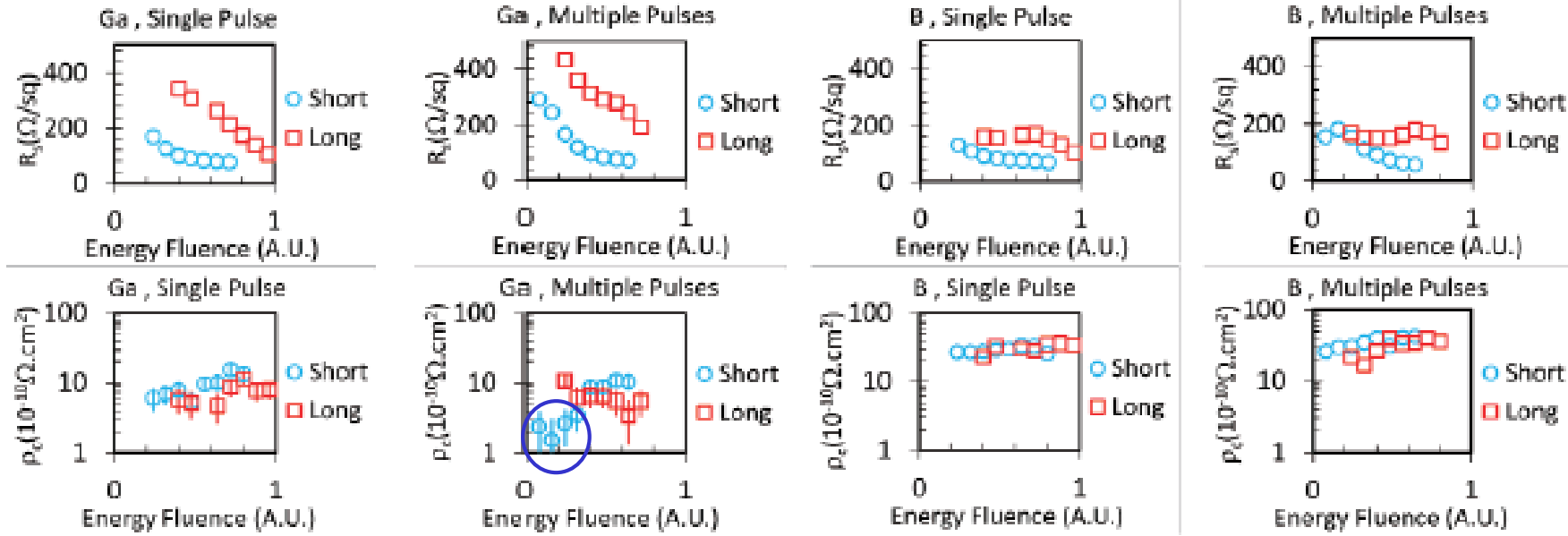

Fig. 6 Comparison of R_s and ρ_c obtained for Ga and B implant with different NLA settings: energy fluence (arbitrary units), th amount of pulses (single / multiple), the pulse length (short / long).

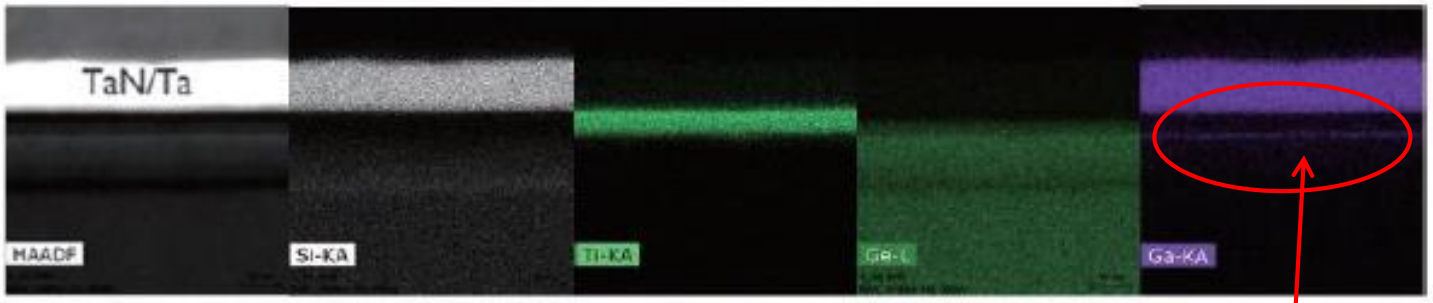

Fig. 7 Dark-field XTEM and EDS maps on sample 4 (see table II) for Si, Ti, Ge and Ga, scaled to the same depth for comparison. The Si and Ga observed in the TaN/Ta is not real, but due to peak overlap.

TABLE II
OVERVIEW OF NLA CONDITIONS WITH EDS AND ELECTRICAL RESULTS

Sample#	Pulse Length	Energy Fluence (A.U.)	# Pulses	Melt Depth (nm)	%Ga	R_s (Ω/sq)	ρ_c (10^{-10}Ω.cm^2)
1	short	0.16	Multiple	15	11.6	246	1.3
2	short	0.48	Multiple	55	5.1	84	8.4
3	long	0.32	Multiple	13	8.3	360	6.1
4	long	0.64	Single	13	7.1	264	4.7
5	long	0.64	Multiple	15	7.7	246	3.4

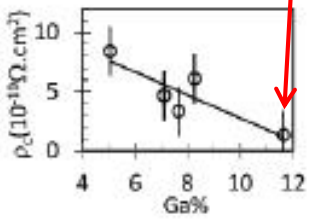

Fig. 9 ρ_c as function of Ga% at the Ti / SiGe interface

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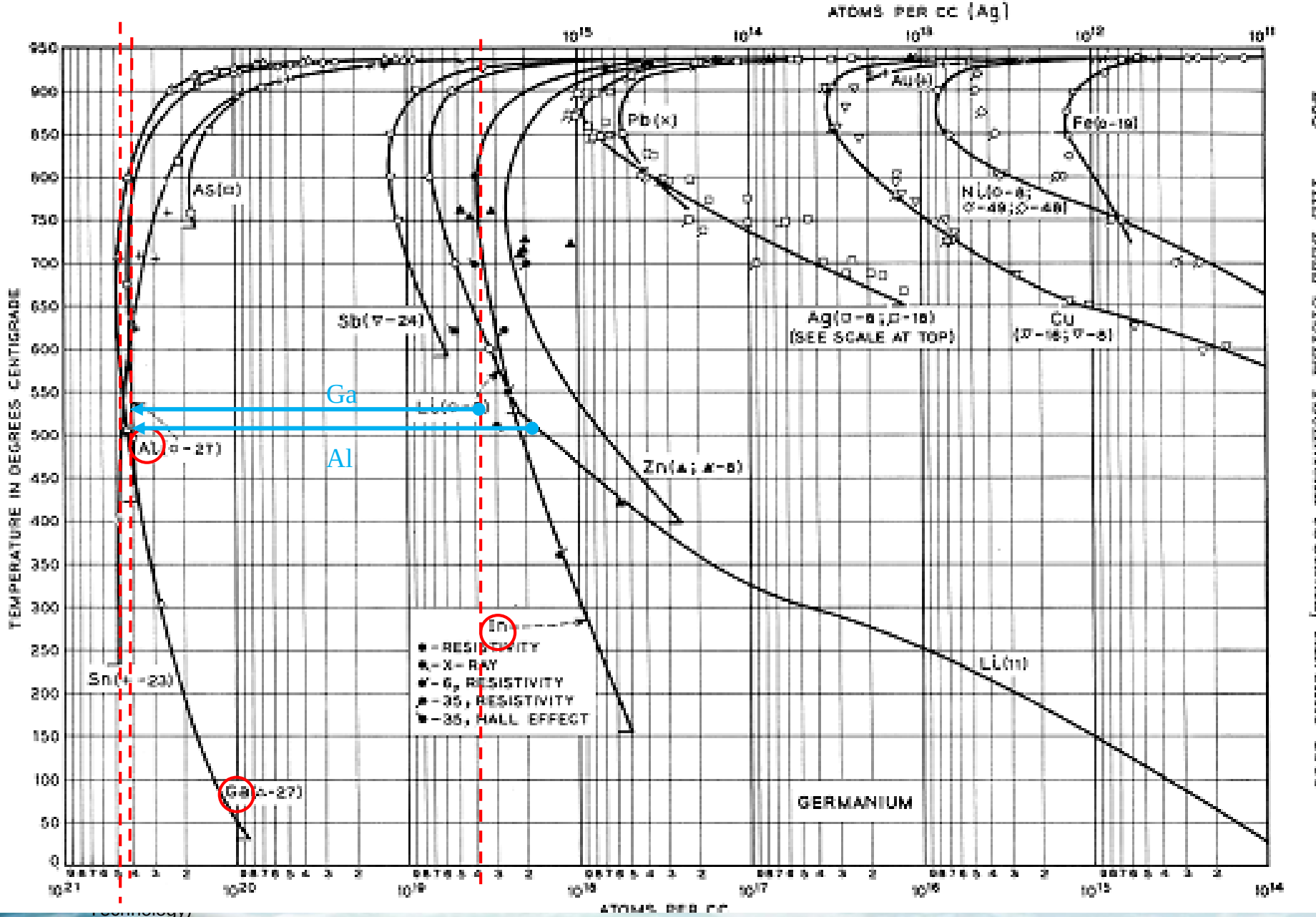
Ge: Trumbore, Bell Labs, 1959



Oral paper by Nakashima of **Nissin** joint paper with **ALP** and **Nagoya Univ** on Al p+ USJ in Ge-Cz wafer. The simulated p+ dopant profiles in Ge are shown in Fig. 7 for B=3keV, Al=7keV and Ga=13keV along with PAI amorphizing implants of Ge and C. Fig.8 shows the Rs-vs-Xj for 30 sec RTA annealing at 500C, 600C and 700C. In the paper they said the Ga Rs data is too high to include in the chart and B_{18} Rs was just slightly lower than monomer B with Al best overall. These results are very different from my results on the 200mm Ge-epi wafers from **NDL** shown in Figs. 9 & 10 below. With low temperature 10 sec RTA down to 550C Ga was best followed by B18 then BF2 and In in Fig.9 while with laser annealing, sub-melt annealing best Rs was for B_{18} but with melt annealing In was best followed by Ga as shown in Fig.10.

Sept IIT-2016

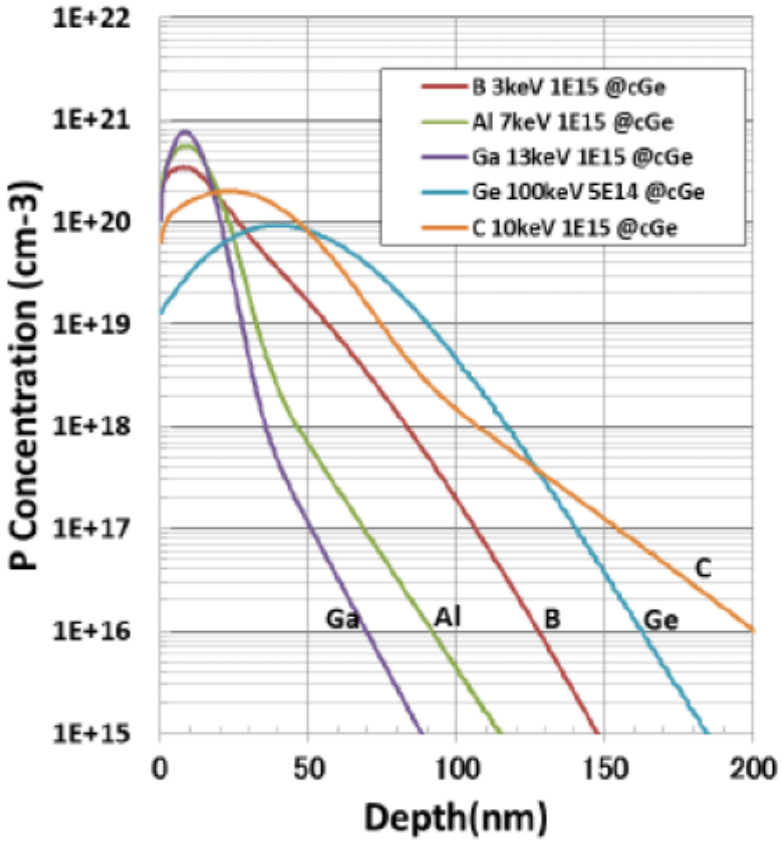


Fig.7: Simulated p+ profiles for B, Ga and Al.

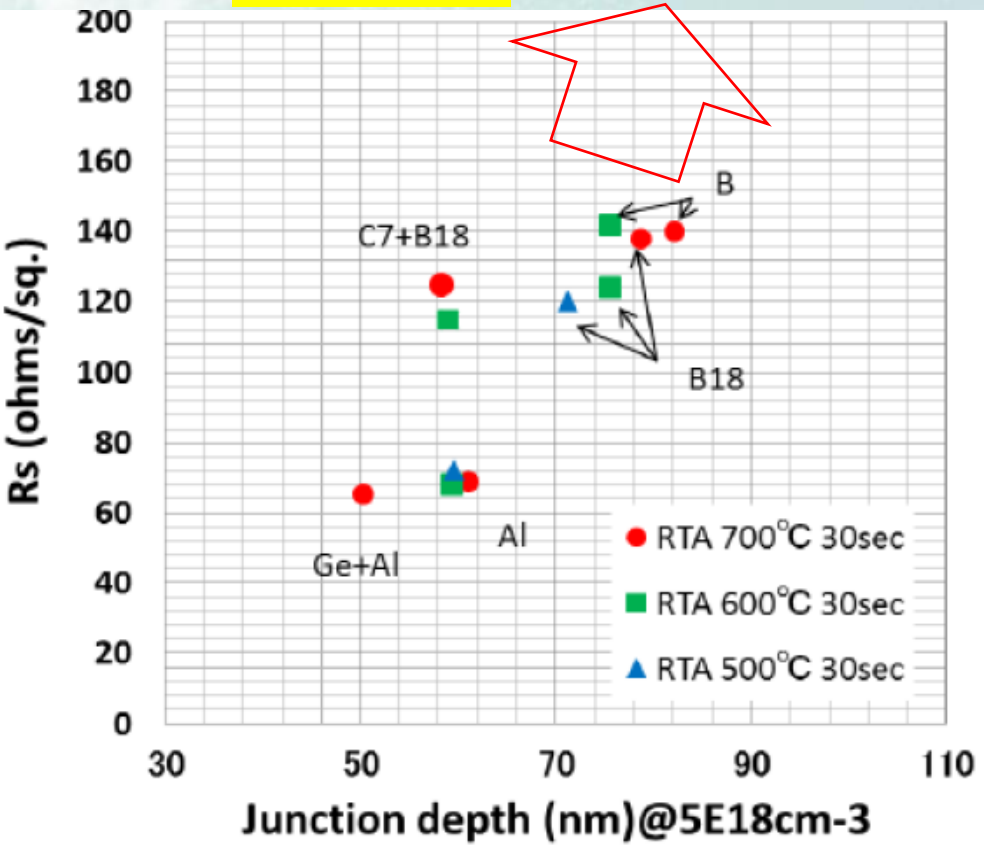


Fig.8: Rs-vs-Xj chart for B, B_{18} and Al.

Solid Solubility Limited Dopant Activation of Group III (B, Ga & In) in Ge Targeting sub-7nm Node Low p+ Contact Resistance

IWJT June 2, 2017

John Borland, J.O.B. Technologies, Aiea, HI

Yao-Jen Lee, NDL, Hsinchu, Taiwan

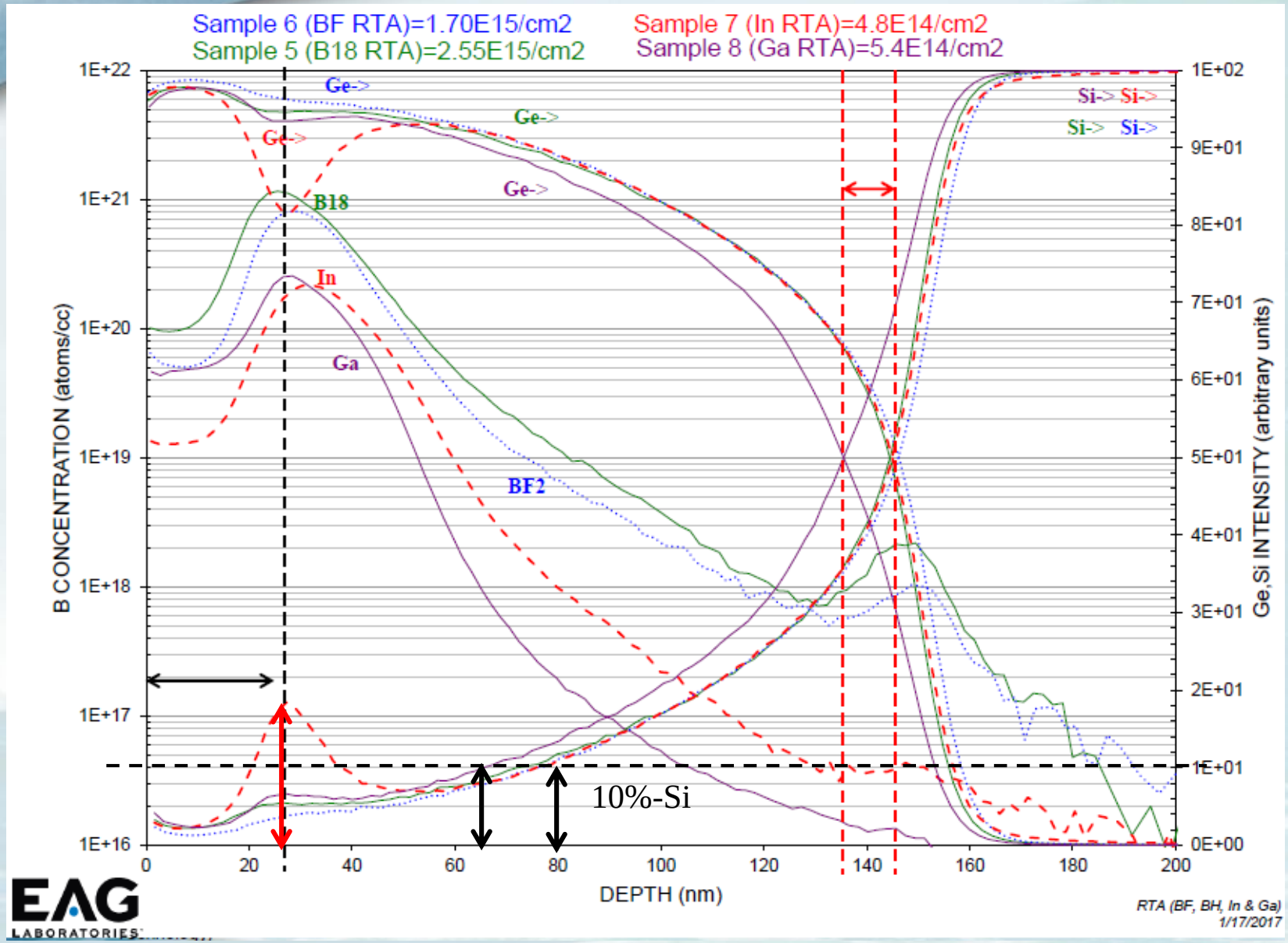
Shang-Shiun Chuang & Tseung-Yuen Tseng, National Chiao Tung University, Hsinchu, Taiwan

Chee-Wee Liu, National Taiwan University, Taipei, Taiwan

Karim Huet, LASSE/Screen, France

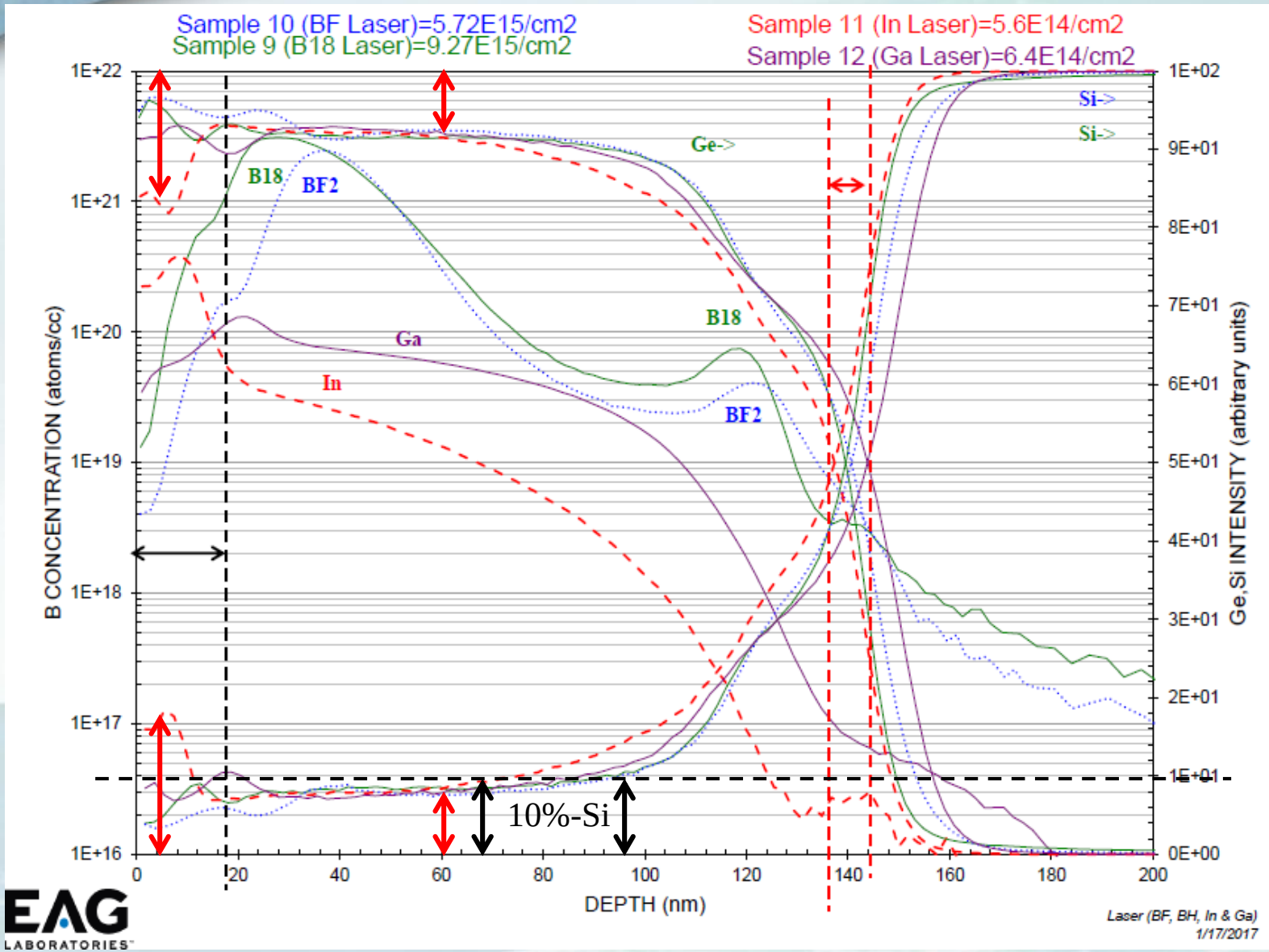
Gary Goodman & John Marino, EAG Laboratories, East Windsor, NJ

55OC/10 sec RTA Anneal SIMS

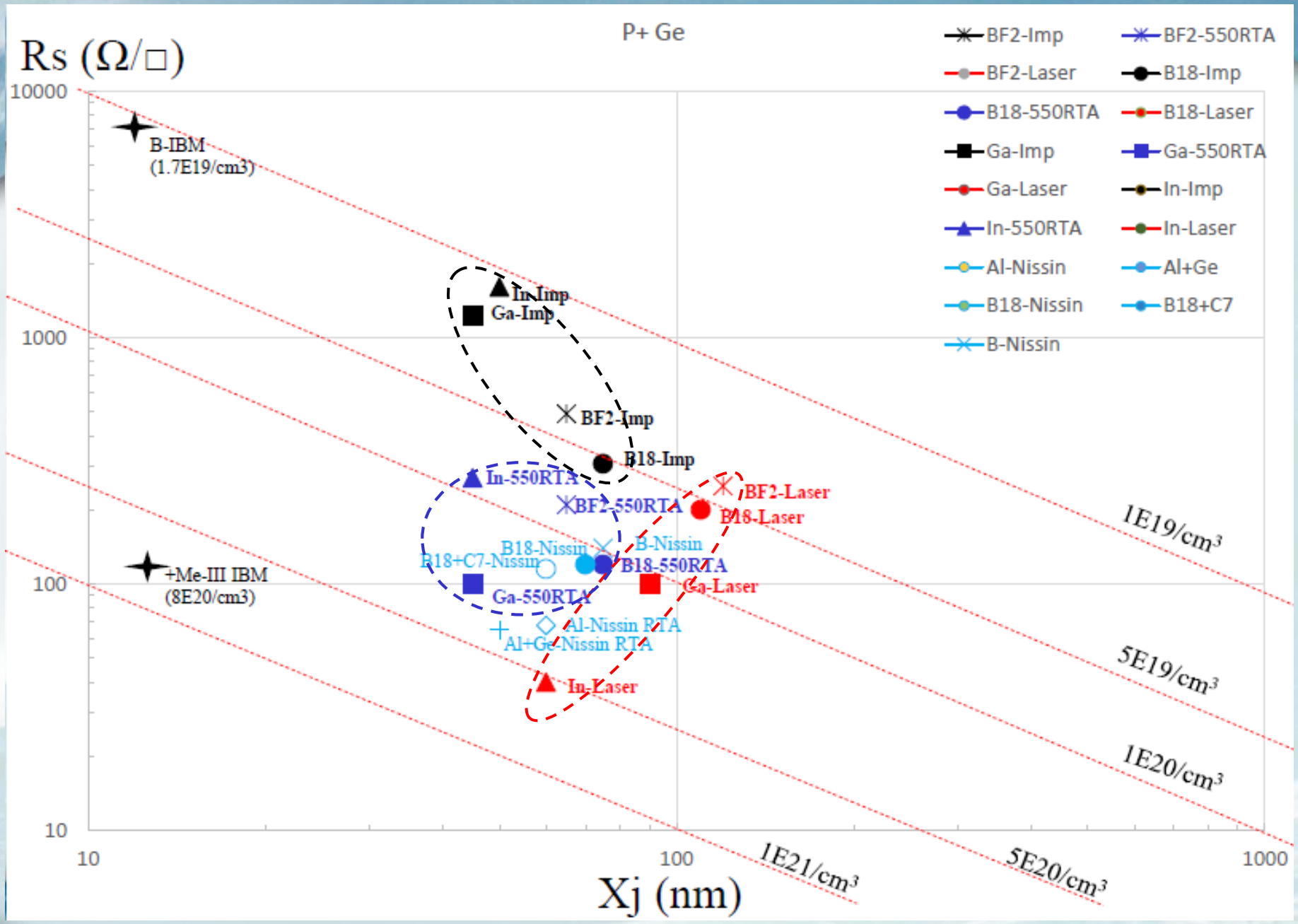


EAG LABORATORIES

308nm Laser Anneal SIMS (1.7J/cm2)



EAG LABORATORIES


P+ Ge
Rs (Ω/□)
Xj (nm)
10000
1000
100
10
10
100
1000
BF2-Imp
BF2-550RTA
BF2-Laser
B18-Imp
B18-550RTA
B18-Laser
Ga-Imp
Ga-550RTA
Ga-Laser
In-Imp
In-550RTA
In-Laser
Al-Nissin
Al+Ge
B18-Nissin
B18+C7
B-Nissin
B-IBM
(1.7E19/cm3)
+Me-III IBM
(8E20/cm3)
Al-Nissin RTA
Al+Ge-Nissin RTA
1E19/cm3
5E19/cm3
1E20/cm3
1E21/cm3
5E20/cm3

Outline

- **Introduction: Smartphone Market Driver for 3-D**
- **3-D Bulk FinFET Transistor Formation**
- **3-D FinFET High Mobility Channel Formation (7nm→)**
  - Strain-Si (tensile or compressive stress)
  - Strain-SiGe (tensile or compressive stress)
  - Strain-Ge (tensile or compressive stress)
- **3-D Gate-All-Around Nanowire Transistor Formation for sub-5nm node or Monolithic 3-D stacking**
- **Summary**

GF/IBM/Samsung IEDM-2016 paper 2.7 on 7nm FinFET with sSi and sSiGe high mobility channels

IEDM-2016 paper 2.7

- SRB Growth
- SSRW formation
- Dual Channel Active FIN Formation
- Dummy Gate Deposition & RIE
- Equal Spacer Formation
- eSiGe(P) /eSD (N) Growth
- ILD & CMP
- Gate Cut
- Dummy Gate Open & Removal
- HKMG formation and recess
- Self Aligned Contact (SAC) Formation
- Dual Damascene MOL local interconnect
- BEOL (Cu metallization)

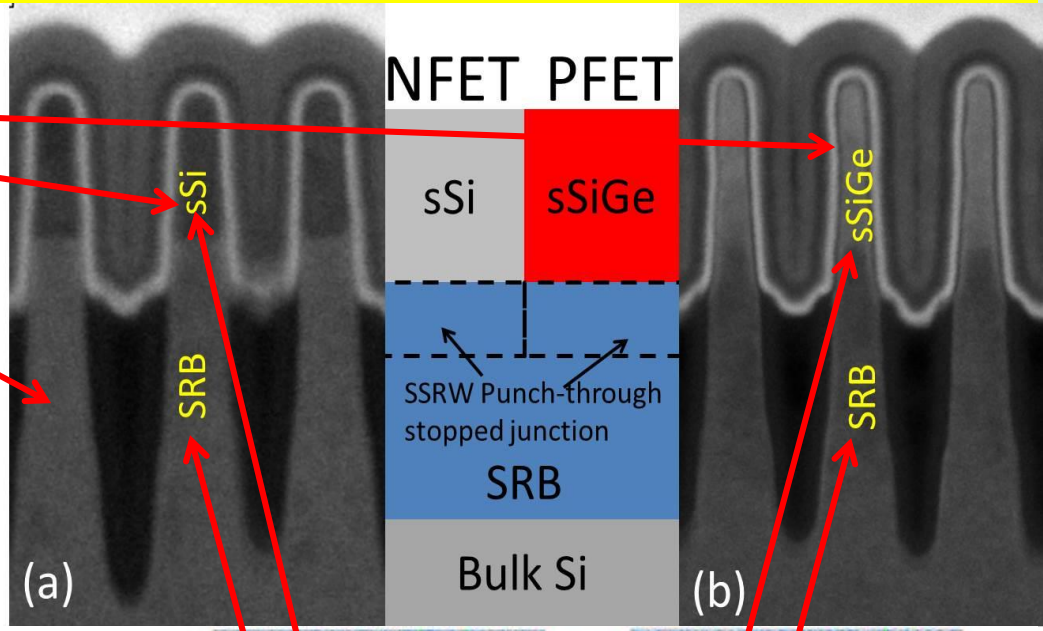


Fig. 2. 7nm CMOS fabrication flow.

Thick 25%-SiGe SRB (strain relaxed buffer) epilayer on Si with multi-step 4 layer SRB. SiGe TDD (threading dislocation density) defect level from E8/cm^2 to E4/cm^2 and the 1.6GPa tensile sSi (t-Si) channel electron mobility boost is 40% up to 100% while the -1.6GPa compressive 50%-sSiGe (c-SiGe) channel hole mobility boost varies from 10% up to 60%.

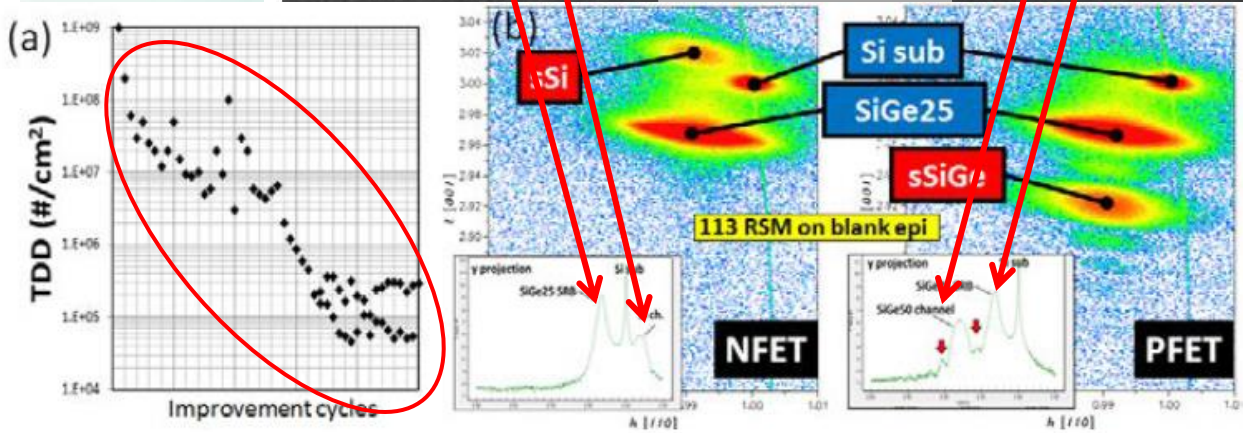


Fig. 17. (a) Significant SRB epi TDD defects reduction through process optimization. (b) HRXRD 113 RSM confirming tensile strained Si, and compressively strained $SiGe_{50}$ channel layers on a common relaxed virtual $SiGe_{25}$.

ECS Transactions, 69 (10) 119-130 (2015)
10.1149/06910.0119ecst ©The Electrochemical Society

On the Electrical Activity of Extended Defects in High-Mobility Channel Materials

E. Simoen[a], G. Eneman, A. Hikavyy, R. Loo, S. Gupta, C. Merckling, A. Alian, A. Schulze, M. Caymax, R. Langer, K. Barla, and C. Claeys[b],

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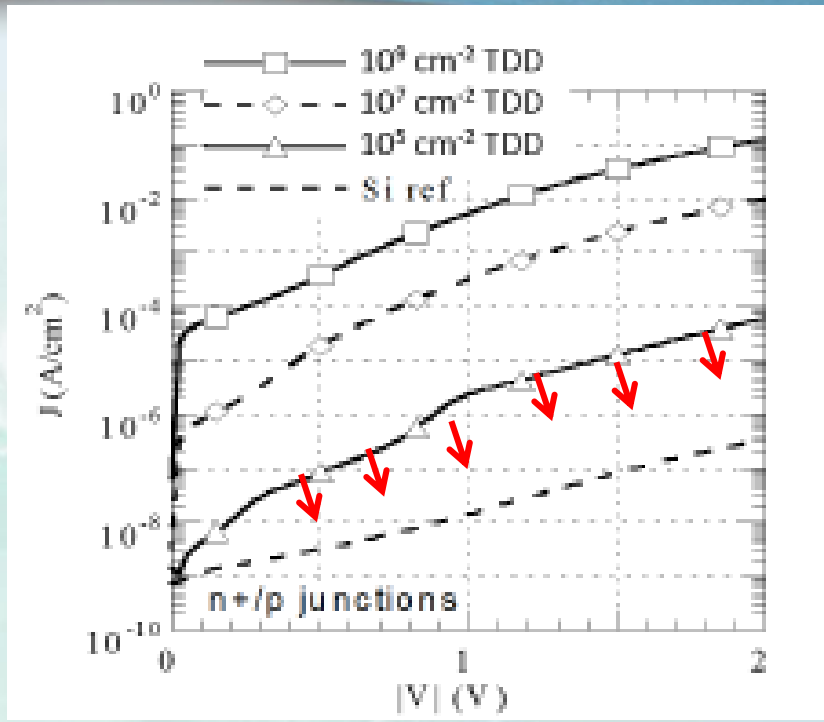
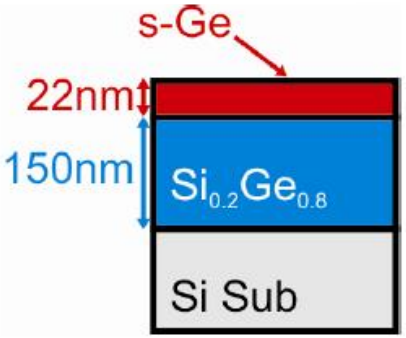
The electrical activity of extended defects (dislocations; antiphase boundaries;...) in high-mobility channel materials (strained-Si; (strained)-Ge, GaAs and InGaAs) is investigated by means of simple device structures (p-n diodes and MOS capacitors). These are fabricated in substrates with a well-controlled density of predominant extended defects, enabling the determination of a specific leakage current contribution per defect. It is shown that there is a linear relationship between the area leakage current density and the threading dislocation density for a wide range of group IV p^+n junctions. In the case of antiphase boundaries (APBs) of GaAs on Ge substrates, only a moderate electrical activity has been derived from these studies. On the other hand, a clear band of deep states has been demonstrated for TDs in InGaAs layers on GaAs substrates.





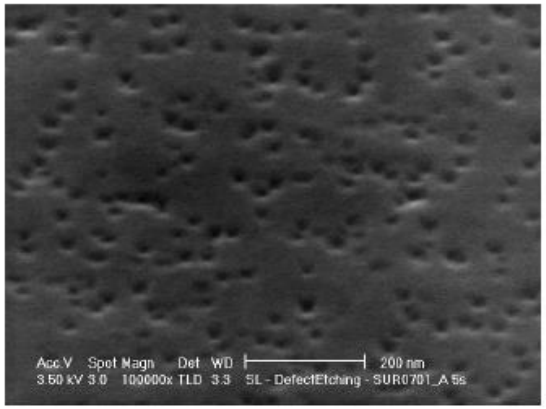


Fig. 4. Schematic structure of the strained-Ge layer on top of the $Si_{0.2}Ge_{0.8}$ SRB (left) and corresponding top view Scanning Electron Micrograph of a selectively etched sGe layer, showing a huge density of dislocation-related etch pits (right).

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

A novel tensile Si (n) and compressive SiGe (p) dual-channel CMOS FinFET co-integration scheme for 5nm logic applications and beyond

IEDM-2016 paper 28.1

Dong-il Bae, Geumjong Bae, Krishna K Bhuwalka, Seung-Hun Lee, Myung-Geun Song, Taek-soo Jeon, Cheol Kim, Wookje Kim, Jaeyoung Park, Sunjung Kim, Uihui Kwon, Jongwook Jeon, Kab-Jin Nam, Sangwoo Lee, Sean Lian, Kang-ill Seo, Sun-Ghil Lee, Jae Hoo Park, Yeon-Cheol Heo, *Mark S. Rodder, *Jorge A. Kittl, Yihwan Kim, Kihyun Hwang, Dong-Won Kim, Mong-song Liang and ES Jung

Samsung R&D Center, Samsung Electronics, Hwasung-City, Gyeonggi-Do, Republic of Korea, *Advanced Logic Labs, 12100 Samsung Blvd, Austin, TX, USA, email: equal72@samsung.com

Abstract— A novel tensile Si (tSi) and compressive SiGe (cSiGe) dual-channel FinFET CMOS co-integration scheme, aimed at logic applications for the 5nm technology node and beyond, is demonstrated for the first time, showing electrical performance benefits and excellent co-integration feasibility. A Strain-Relaxed SiGe Buffer (SRB) layer is introduced as buried stressor and successfully transfers up to ~1 GPa uniaxial tensile and compressive stress to the Si/SiGe n-/p-channels simultaneously. As the result, both tSi and cSiGe devices show a 40% and 10% electron and hole mobility gain over unstrained Si, respectively. Through a novel gate stack

A. *Device design*

Fig. 1(a) illustrates the tSi/cSiGe-channel CMOS device design with a global buried SiGe SRB stressor and a common gate stack (MG/HK/IL). A comprehensive TCAD simulation was carried out to evaluate the strain induced by the SRB stressor, as shown in Fig. 1(b). A ~1 GPa tensile and compressive stress are predicted, respectively for nFET and pFET, including the use of an eSiGe stressor. Figs. 2(a,b,c) show the corresponding predicted channel mobility enhancement in tSi and cSiGe of 40% (electron mobility) and 60% (hole mobility), respectively.

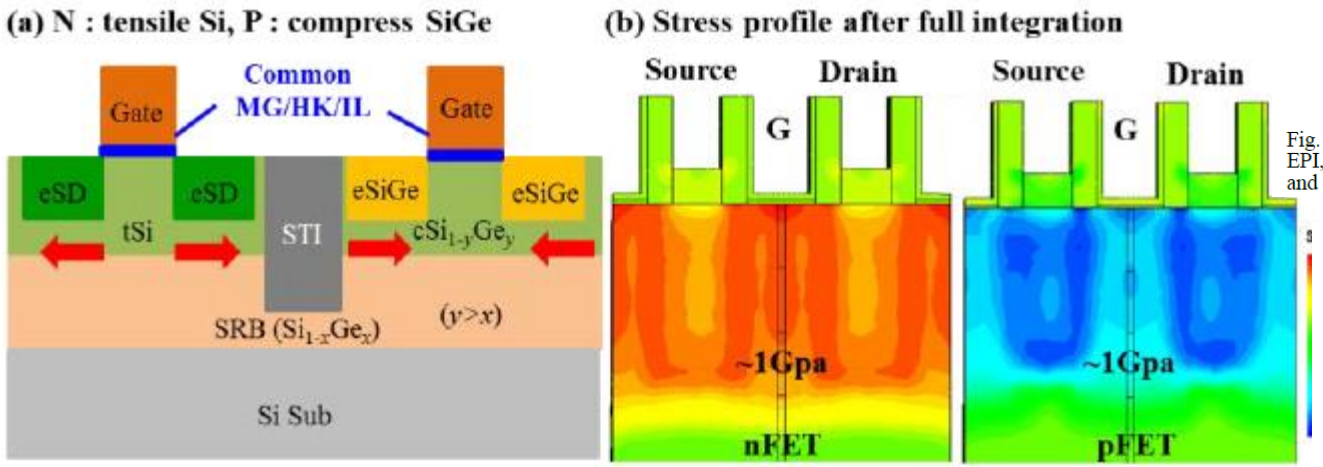


Fig. 1(a). CMOS design concepts for logic 5nm and beyond application: SiGe S as global stressor for both Si channel nFET and SiGe channel pFET. (b) TC simulation indicates that SRB stressor can transfer over 1 GPa tensile stress nFET and compressive stress (including eSiGe stressor) for pFET.

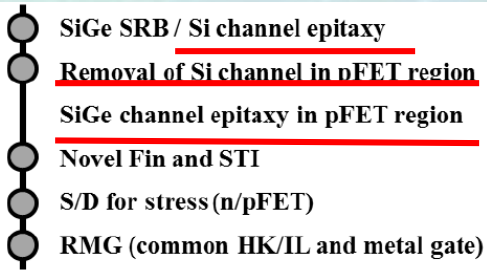


Fig. 3. Key steps to enable tSi/cSiGe CMOS, including new SiGe EPI, pFET SiGe replacement, novel STI, S/D engineering for stress and common RMG process considering both Si/SiGe channel.

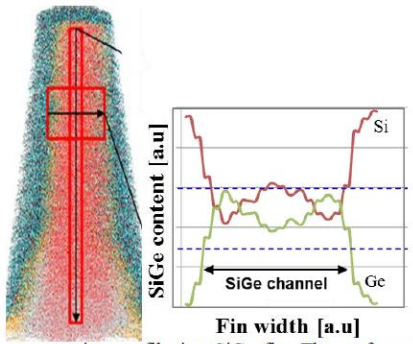


Fig. 6 Ge concentration profile in cSiGe fin. The surface shows higher Ge content than center because of subsequent thermal process

(12) **United States Patent**
Borland et al.

(10) **Patent No.: US 7,259,036 B2**
(45) **Date of Patent: Aug. 21, 2007**

(54) **METHODS OF FORMING DOPED AND UN-DOPED STRAINED SEMICONDUCTOR MATERIALS AND SEMICONDUCTOR FILMS BY GAS-CLUSTER-ION-BEAM IRRADIATION AND MATERIALS AND FILM PRODUCTS**

(75) Inventors: **John O. Borland**, South Hamilton, MA (US); **John J. Hautala**, Beverly, MA (US); **Wesley J. Skinner**, Andover, MA (US); **Martin D. Tabat**, Nashua, NH (US)

(73) Assignee: **TEL Epion Inc.**, Billerica, MA (US)

(58) **Field of Classification Search** 438/36, 438/37, 45, 87, 473, 474, 795; 427/562, 427/585

See application file for complete search history.

(56) **References Cited**

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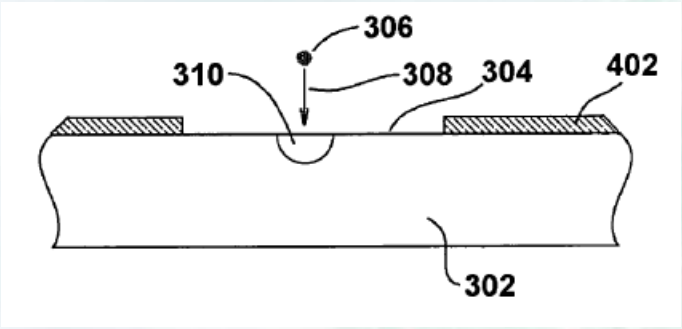
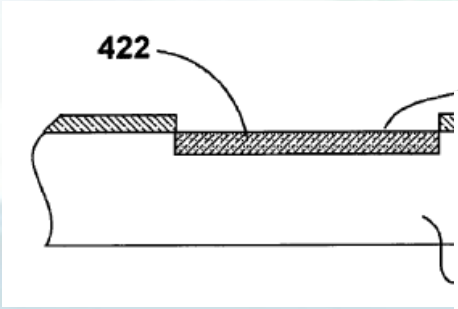
2002/0070361	A1	6/2002	Mack et al.	250/
2003/0109092	A1	6/2003	Choi et al.	43

(57) **ABSTRACT**

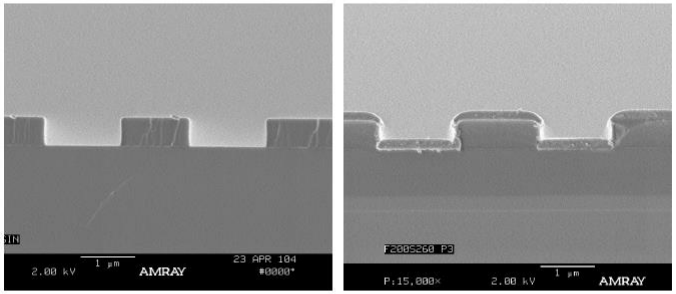
Methods and apparatus are described for irradiating one or more substrate surfaces with accelerated gas clusters including strain-inducing atoms for blanket and/or localized introduction of such atoms into semiconductor substrates, with additional, optional introduction of dopant atoms and/or C. Processes for forming semiconductor films infused into and/or deposited onto the surfaces of semiconductor and/or dielectric substrates are also described. Such films may be doped and/or strained as well.

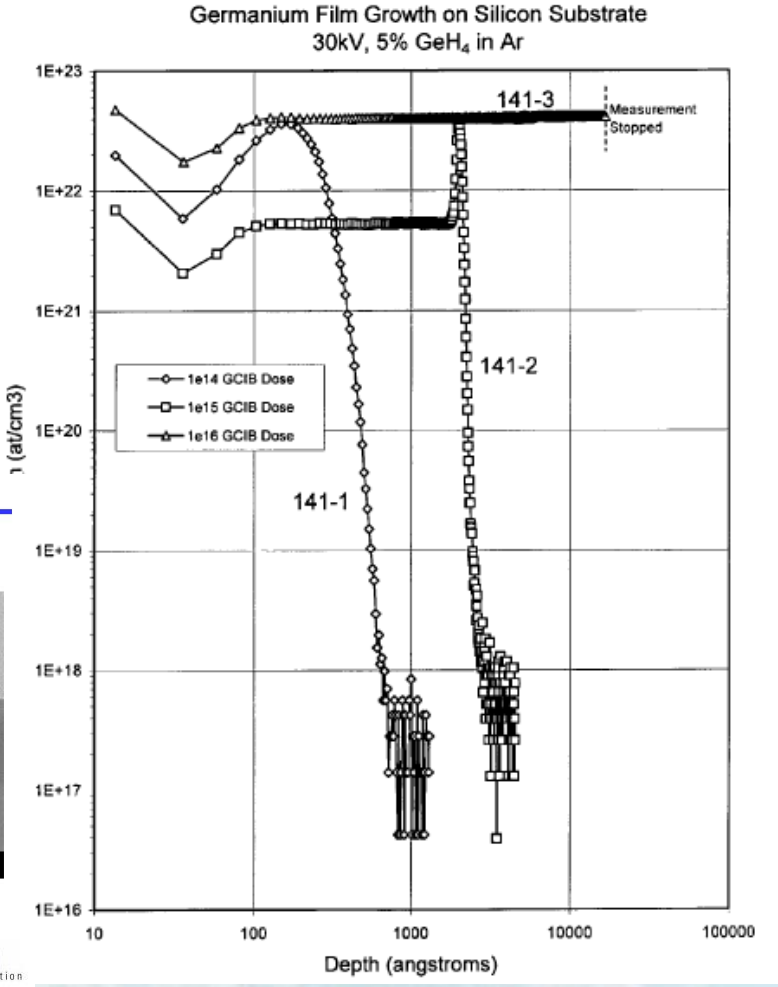




Room Temperature Processing : PR compatible

200nm Ge Infusion Deposition On Photo Resist





J.O.B. Technologies (Strategy, Marketing, Sales & Technology)

Borland et al., ECS Oct 2004

epion corporation

(57) **ABSTRACT**

A method of making a semiconductor device patterns a first fin in a pFET region, and patterns a second fin in an nFET region. A plurality of conformal microlayers containing a straining material are deposited on the first and second fins. A protective cap material is formed on the first fin, and the conformal layers are selectively removed from the second fin. The straining material is then thermally diffused into the first fin. The protective cap material is removed from the first fin after the thermal annealing and after the conformal micro layers are selectively removed from the second fin.

(12) **United States Patent**
Berliner et al.

(10) **Patent No.: US 8,900,973 B2**
(45) **Date of Patent: Dec. 2, 2014**

(54) **METHOD TO ENABLE COMPRESSIVELY STRAINED PFET CHANNEL IN A FINFET STRUCTURE BY IMPLANT AND THERMAL DIFFUSION**

(75) Inventors: **Nathaniel C. Berliner**, Albany, NY (US); **Pranita Kulkarni**, Slingerlands, NY (US); **Nicolas Loubet**, Albany, NY (US); **Kingsuk Maitra**, Guilderland, NY (US); **Sanjay C. Mehta**, Niskayuna, NY (US); **Paul A. Ronsheim**, Hopewell Junction, NY (US); **Toyoji Yamamoto**, Yokohama (JP); **Zhengmao Zhu**, Pougkeepsie, NY (US)

Assignees: **International Business Machines Corporation**, Armonk, NY (US); **Globalfoundries Inc.**, Santa Clara, CA (US); **Renesas Electronics America Inc.**, Santa Clara, CA (US); **STMicroelectronics, Inc.**, Coppell, TX (US)

(58) **Field of Classification Search**
CPC H01L 21/845; H01L 27/1211; H01L 29/7848
USPC 438/468
IPC H01L 21/845, 27/1211, 29/7848
See application file for complete search history.

(56) **References Cited**

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(Continued)

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Tezuka, et al., "Strain analysis in ultrathin SiGe-on-Insulator layers formed from strained Si-on-Insulator substrates by Ge-condensation process," Applied PHysics Letters 90, 181918, 2007, pp. 90, 181918-

extension and source/drain regions. A process referred to herein as Plasma Doping (PD) can be used as one method for the deposition/implantation of the Ge layers. PD uses plasma to generate active radicals of species to be deposited. For Germanium, PD uses GeH4 precursor. PD can be operated both in the implant mode as well as un-biased deposition mode (to minimize damage to substrate). The methods described herein are not limited to the FinFET or TriGATE geometries, but also extend to the fully depleted planar extremely thin silicon-on-insulator (ETSOI) devices where the operation in the implant mode can cause irreparable damage to the thin substrate, potentially amorphizing the entire substrate.

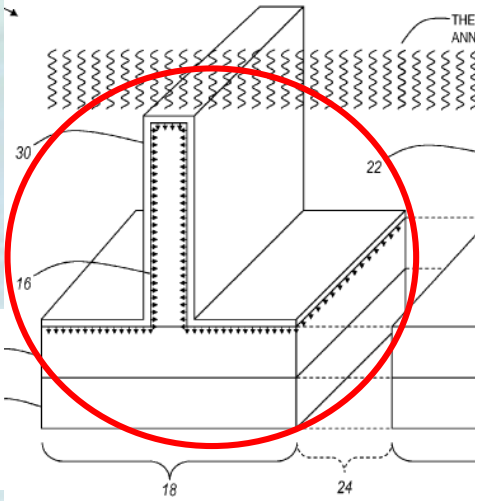
The straining material imparts a compressive strain to the surface Si channel of the first FinFET device and converts a portion of the surface Si of the fin into an alloy of silicon. By introducing Ge in the channel by Ge diffusion in pFET fins prior to the gate patterning, this processing lowers the threshold voltage and enhances carrier mobility. The straining material may comprise, for example, Germanium or Carbon.

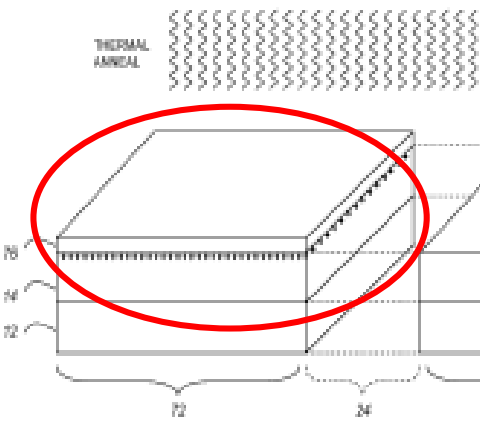
16 is a schematic diagram illustrating the selective removal of the monolayers **76** from the nFET region **74** such that the monolayers **76** remain on the pFET region **72** of the planar device **70**. This selective removal of the layer **76** is accom-

2. The method of making a semiconductor device according to claim **1**, said conformal layers comprising several monolayers of conformal material.

3. The method of making a semiconductor device according to claim **1**, said bias charge comprising a bias below 3 kV.

plasma doping an impurity layer on said first FinFET said nFET

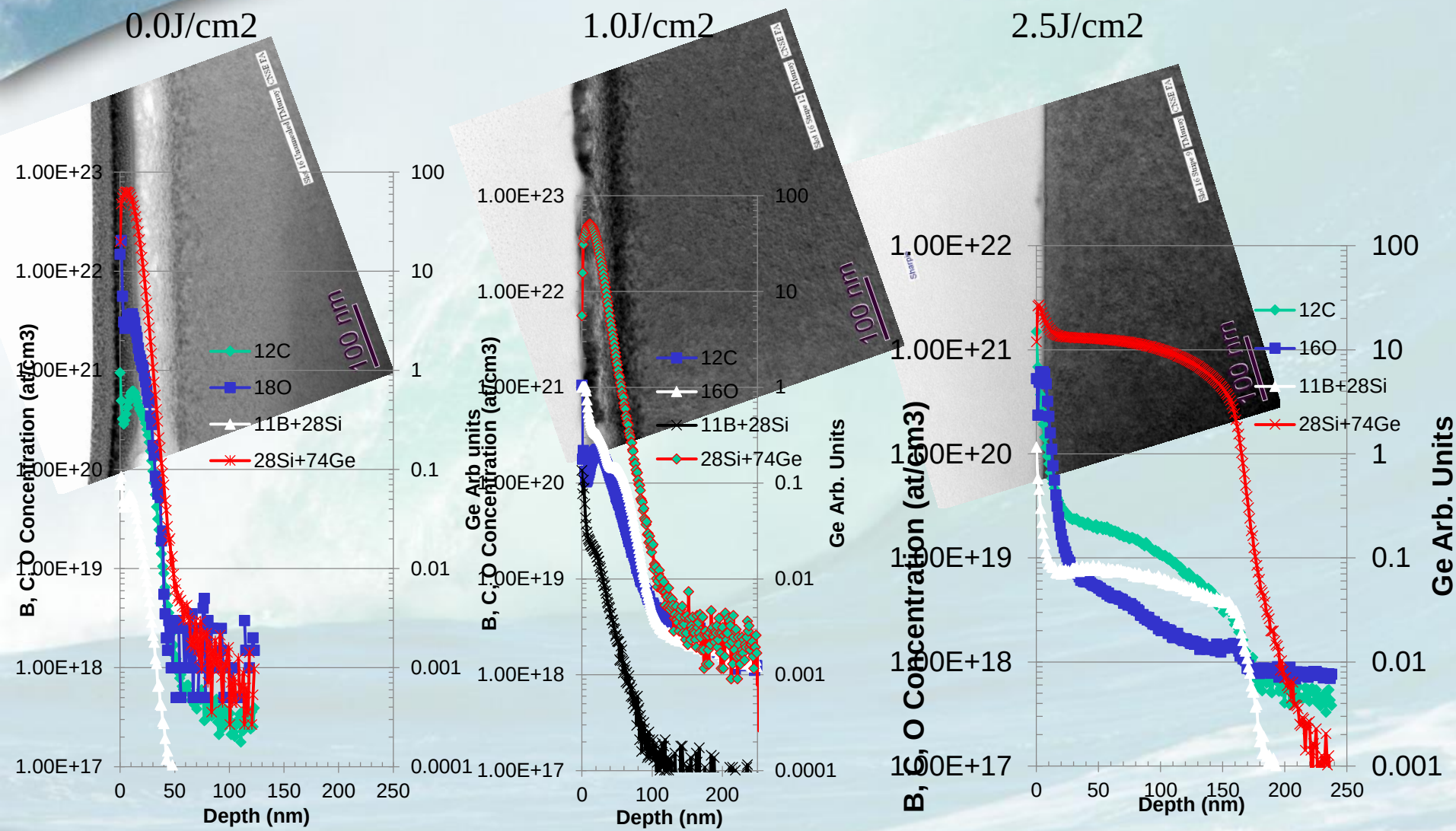




55%-aSiGe

40%-polySiGe

25% LPE-SiGe



Ge-plasma Implantation

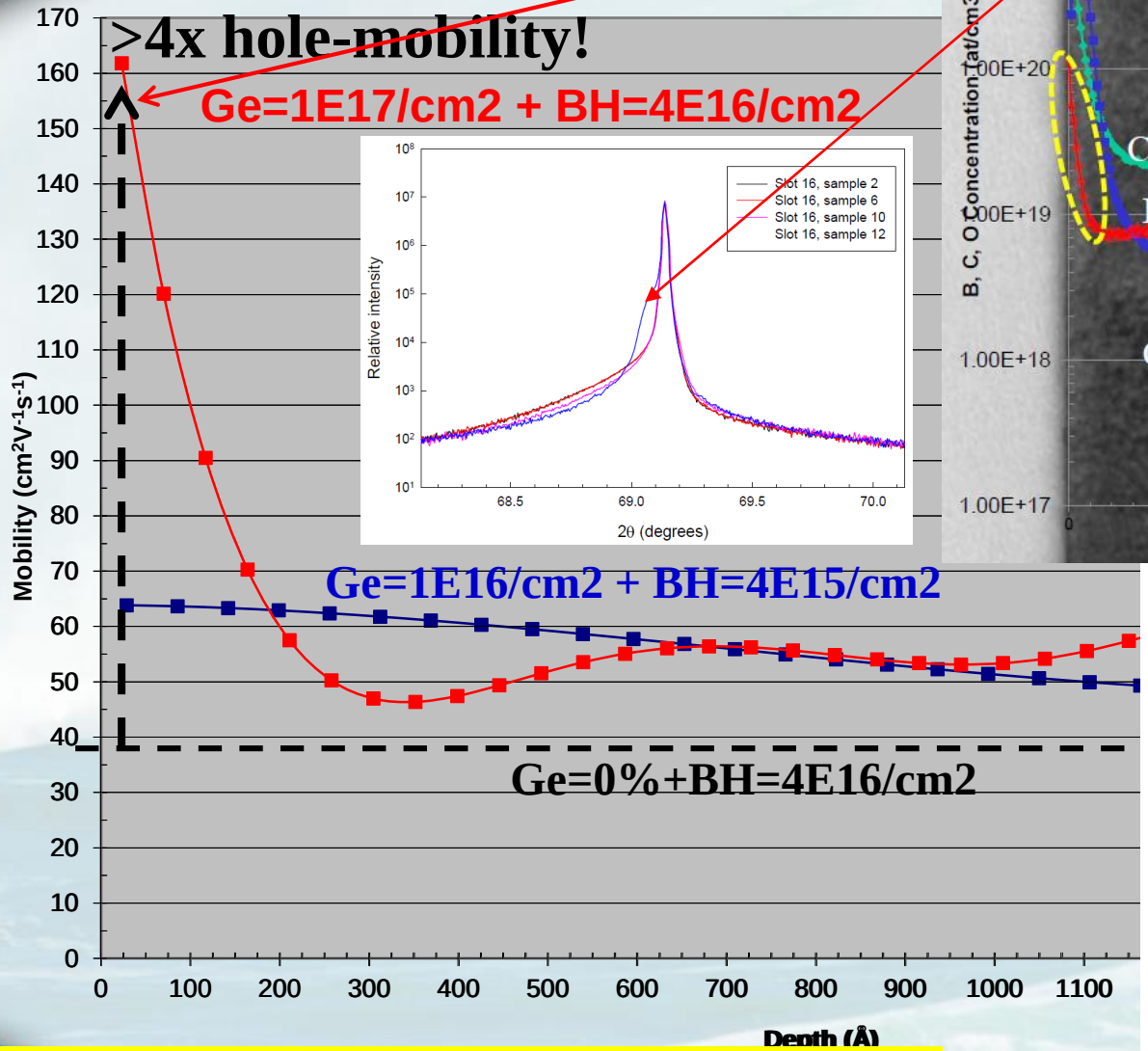
Borland et al., JOB-Tech/Micron/Innovavent/Excico/EAG/CNSE-SUNNY/KT/ALP, IWJT-2013, paper S4-4, p.49

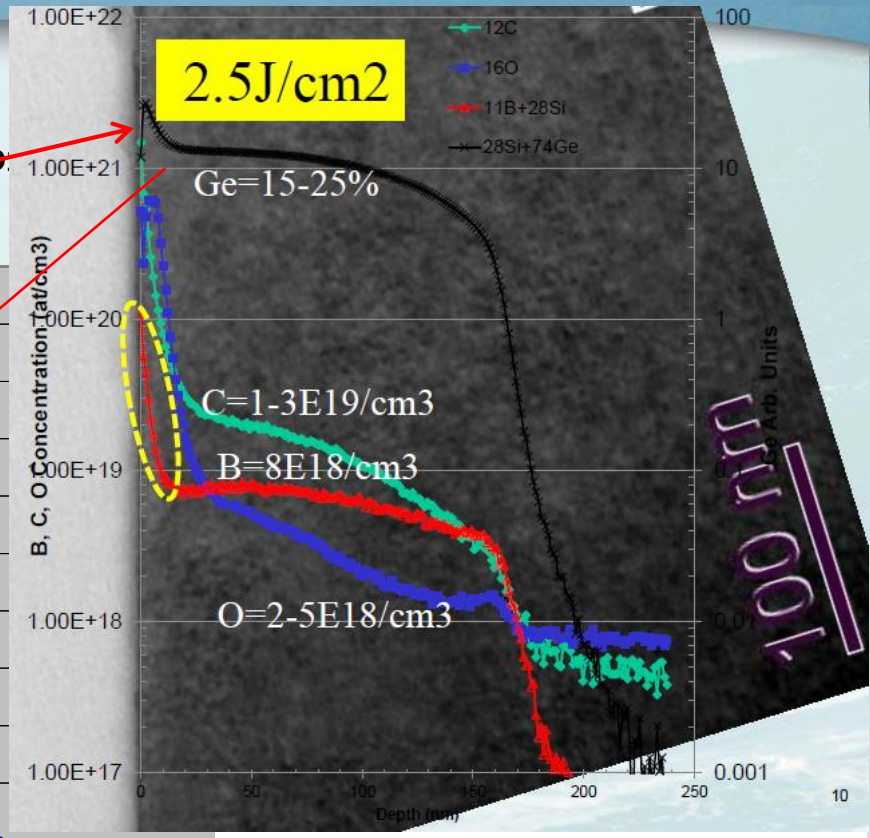
ALP Hall Analysis of 308nm

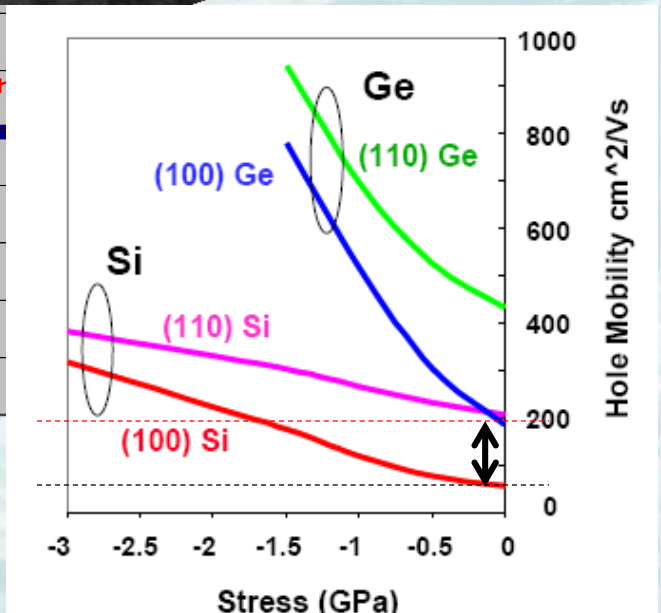
Slot#14:Ge=1E16+B=4E15

Slot#18: **Ge=1E17**+B=4E16

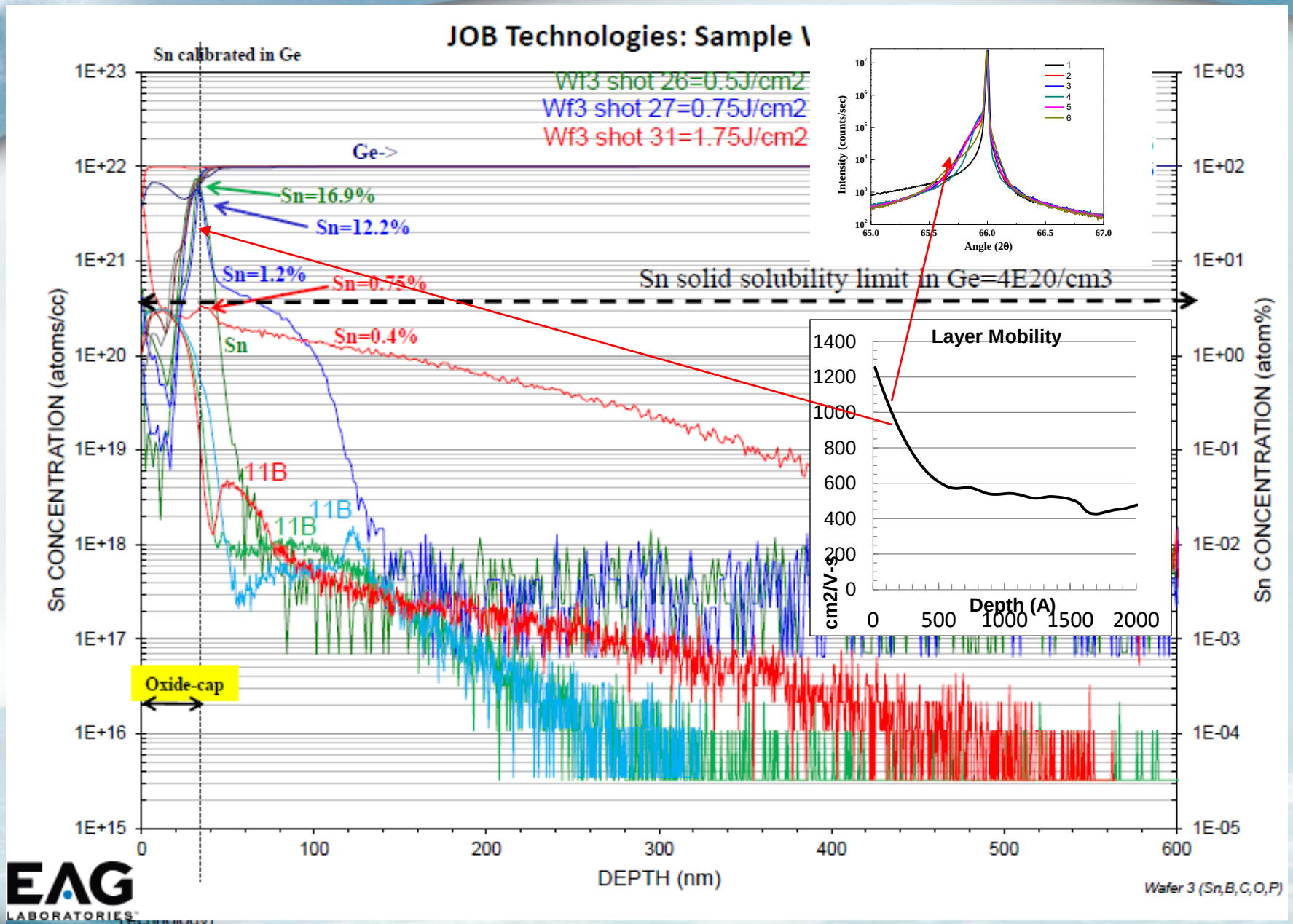
Mobility JA14ED:





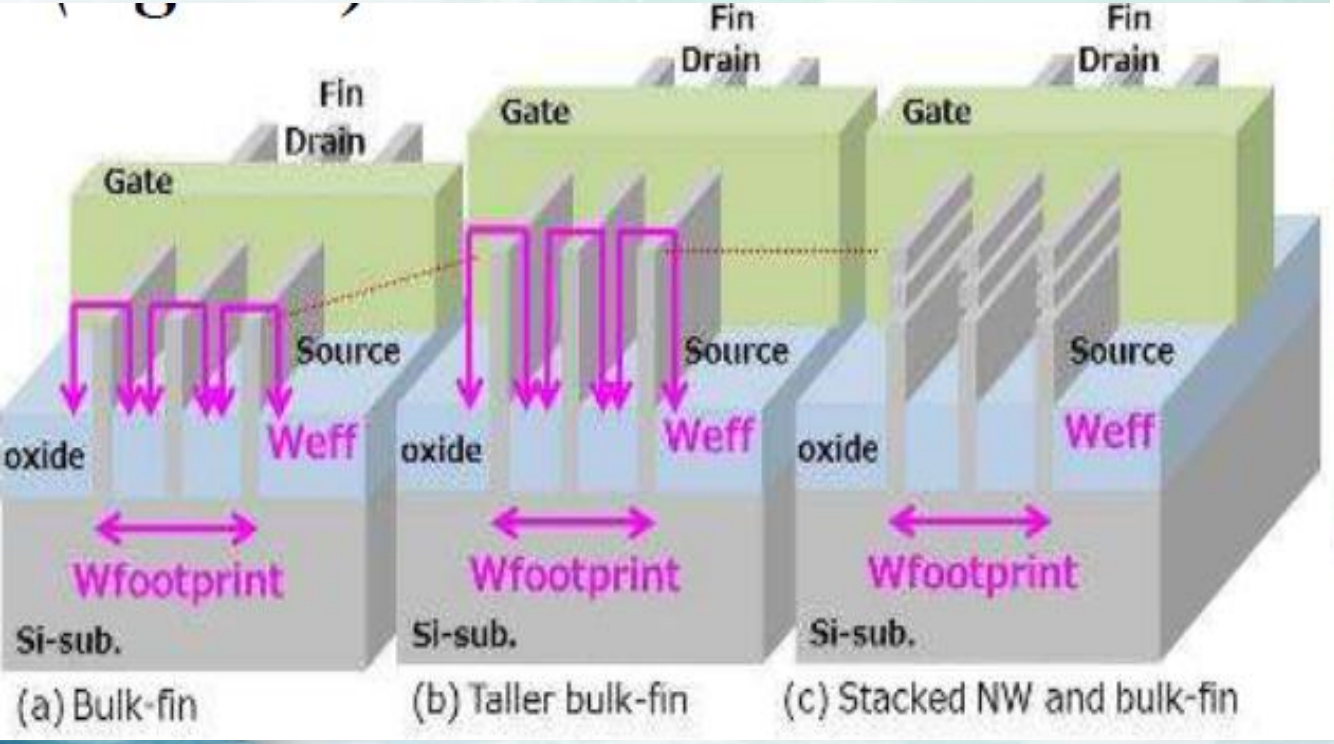


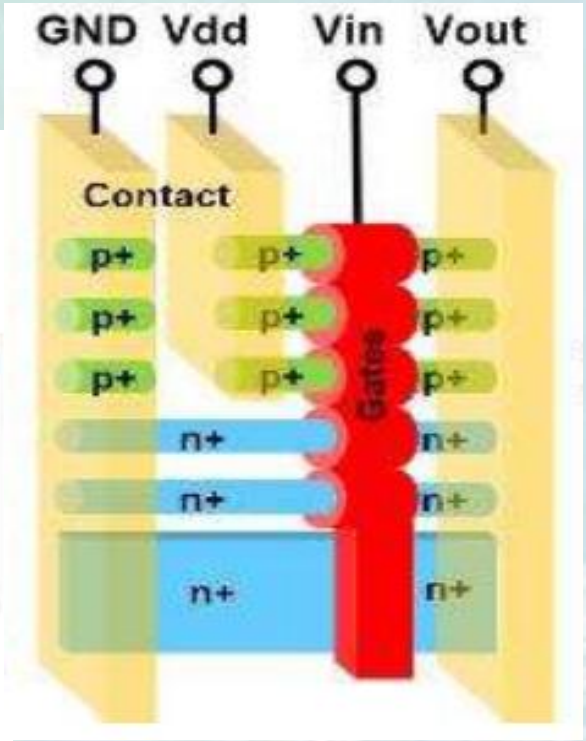
Borland et al., JOB-Tech/Micron/Innovavent/Excico/EAG/CNSE-SUNNY/KT/ALP, IWJT-2013, paper S4-4, p.49


JOB Technologies: Sample \
Sn calibrated in Ge
Wf3 shot 26=0.5J/cm2
Wf3 shot 27=0.75J/cm2
Wf3 shot 31=1.75J/cm2
Ge->
Sn=16.9%
Sn=12.2%
Sn=1.2%
Sn=0.75%
Sn=0.4%
Sn
11B
11B
11B
Sn solid solubility limit in Ge=4E20/cm3
Oxide-cap
Sn CONCENTRATION (atoms/cc)
Sn CONCENTRATION (atom%)
DEPTH (nm)
Intensity (counts/sec)
Angle (2θ)
Layer Mobility
cm2/V-s
Depth (A)
Wafer 3 (Sn,B,C,O,P)

Outline

- **Introduction: Smartphone Market Driver for 3-D**
- **3-D Bulk FinFET Transistor Formation**
- **3-D FinFET High Mobility Channel Formation**
- **3-D Gate-All-Around Nanowire Transistor Formation for sub-5nm node or Monolithic 3-D stacking**
  - Si-nanowire
  - Ge-nanowire
  - CoolCube 3-D stacking





Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates

H. Mertens, R. Ritzenthaler, A. Hikavyy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel, T. Schram, K. Devriendt, D. Tsvetanova, H. Dekkers, S. Demuynck, A. Chasin, E. Van Besien, A. Dangol, S. Godny, B. Douhard, N. Bosman, O. Richard, J. Geypen, H. Bender, K. Barla, D. Mocuta, N. Horiguchi, A.V-Y Thean

Starting material: Bulk Si wafer
Ground plane I/I + anneal (a)
SiGe/Si/SiGe/Si epitaxy (b)
Spacer-defined fin patterning (SADP)
Low-temperature STI filling (c)
Dummy gate patterning
Extension I/I + Spacer formation
Embedded Si S/D epitaxy (d)
HDD I/I + activation
ILD0 deposition/CMP
Dummy poly/oxide removal
Si nanowire formation by SiGe etch (e)
Gate dielectric (IL-SiO_2/HfO_2) dep.
Work function (WF) metal deposition
Fill metal (W) deposition/CMP (f)
Contact formation + M1 BEOL

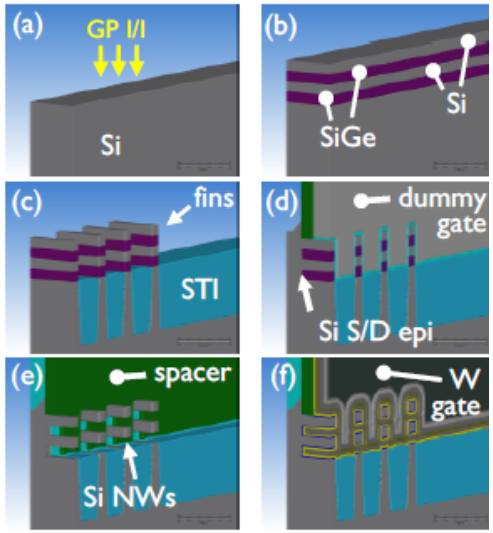


Fig. 1. Process flow for the fabrication of GAA Si NWFETs. **(a)** – **(f)** Coventor® images that illustrate the critical steps. The Ge concentration in the SiGe layers is 27%. The thickness of the SiGe and Si layers is ~10 nm.

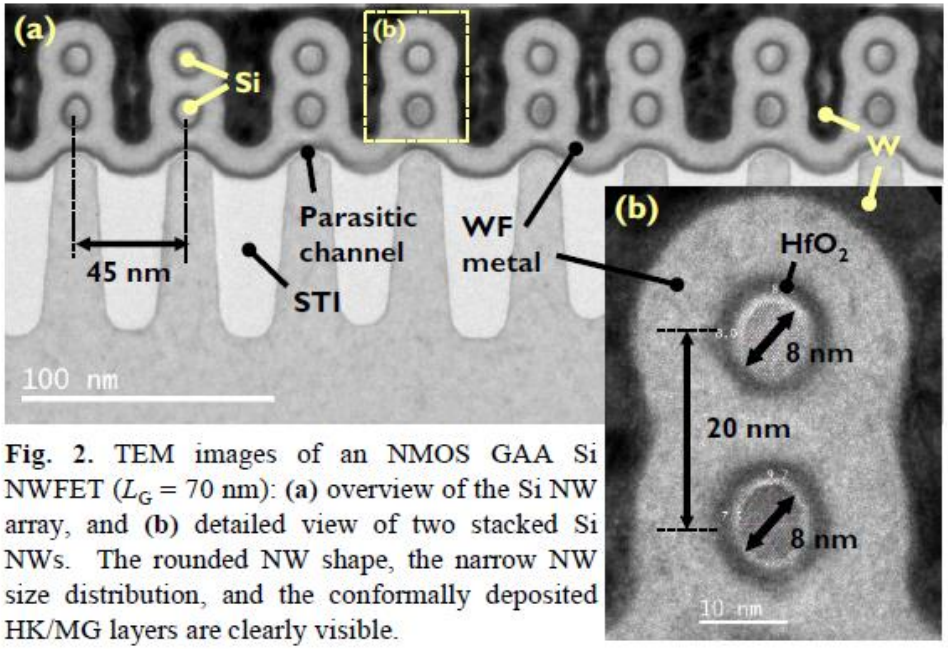


Fig. 2. TEM images of an NMOS GAA Si NWFET (L_G = 70 nm): **(a)** overview of the Si NW array, and **(b)** detailed view of two stacked Si NWs. The rounded NW shape, the narrow NW size distribution, and the conformally deposited HK/MG layers are clearly visible.

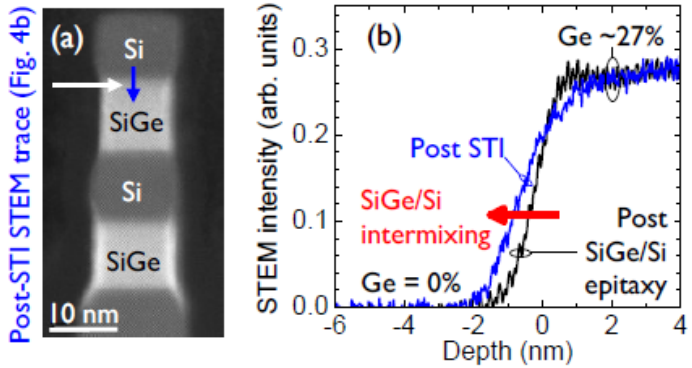


Fig. 4. **(a)** STEM image of a post-STI fin showing the SiGe and Si segments. **(b)** STEM intensity trace showing limited SiGe/Si intermixing by STI densification at 750 °C for 30 minutes. Junction activation spike annealing has low impact on SiGe/Si intermixing as well, which is attributed to short anneal duration.

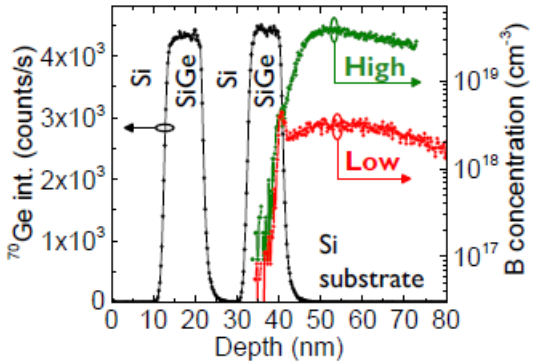
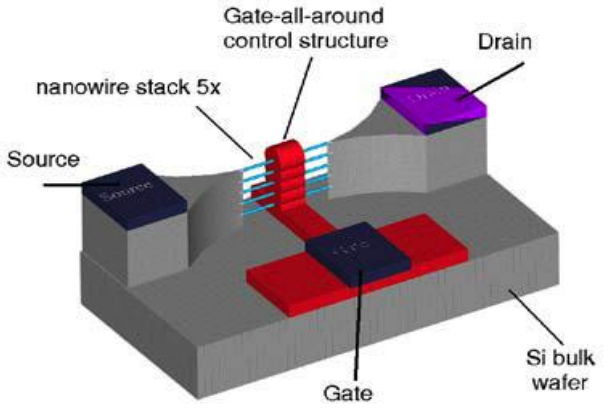
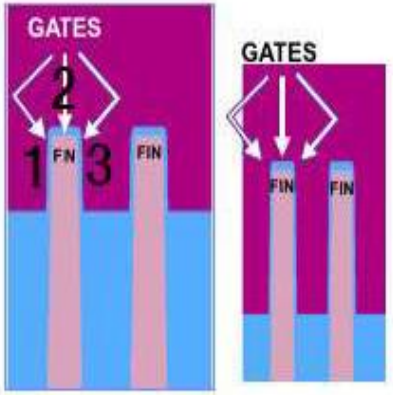


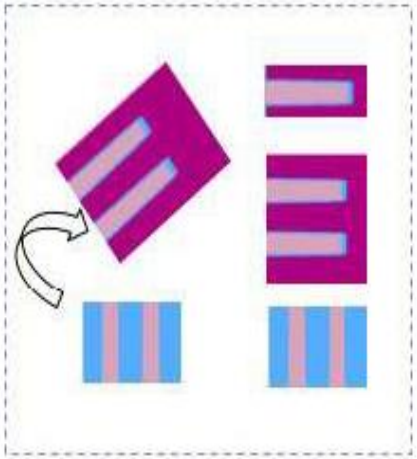
Fig. 5. SIMS profiles for Ge (left axis) and for NMOS GP doping (right axis) collected after SiGe/Si epi for two boron GP concentrations showing the steep profiles in the Si substrate below the SiGe/Si stack.



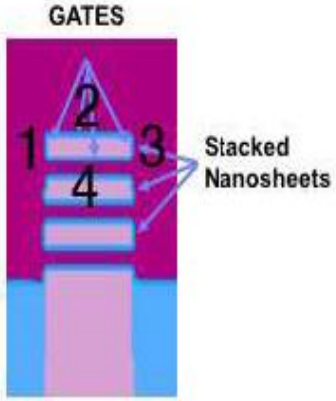
Tri-Gate FinFET | 4-Gate Silicon Nanosheet



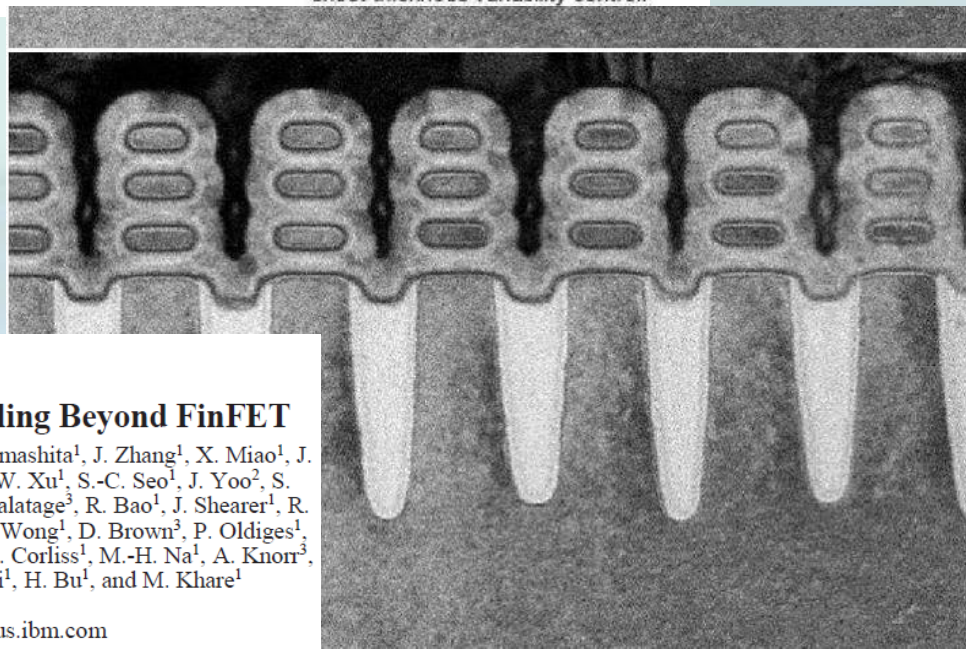
Each fin is surrounded by a gate in three directions: one on each side, and one on top. Tighter fin pitch, taller fin height, and thinner fin width deliver performance improvement and area scaling; However, the high process challenge and lack of further scaling improvements have pushed the industry to look for new device architecture, post FINFET.



Conceptually, a nanosheet transistor is created by flipping the fins from vertical, to horizontal sheets. Another "fin" can be added on top, in the same footprint.



In stacked nanosheets, each sheet is surrounded by a gate in all directions. The sheet-to-sheet gap is optimized to reduce parasitic capacitance. Sheet thickness changes to epitaxy-controlled, instead of patterning-controlled (fin) for better sheet thickness variability control.



T17-5 (Late News) VLSI-2017

Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET

N. Loubet[1], T. Hook[1], P. Montanini[1], C.-W. Yeung[1], S. Kanakasabapathy[1], M. Guillorn[1], T. Yamashita[1], J. Zhang[1], X. Miao[1], J. Wang[1], A. Young[1], R. Chao[1], M. Kang[2], Z. Liu[1], S. Fan[1], B. Hamieh[1], S. Sieg[1], Y. Mignot[1], W. Xu[1], S.-C. Seo[1], J. Yoo[2], S. Mochizuki[1], M. Sankarapandian[1], O. Kwon[2], A. Carr[1], A. Greene[1], Y. Park[2], J. Frougier[3], R. Galatage[3], R. Bao[1], J. Shearer[1], R. Conti[1], H. Song[2], D. Lee[2], D. Kong[1], Y. Xu[1], A. Arceo[1], Z. Bi[1], P. Xu[1], R. Muthinti[1], J. Li[1], R. Wong[1], D. Brown[3], P. Oldiges[1], R. Robison[1], J. Arnold[1], N. Felix[1], S. Skordas[1], J. Gaudiello[1], T. Standaert[1], H. Jagannathan[1], D. Corliss[1], M.-H. Na[1], A. Knorr[3], T. Wu[1], D. Gupta[1], S. Lian[2], R. Divakaruni[1], T. Gow[1], C. Labelle[3], S. Lee[2], V. Paruchuri[1], H. Bu[1], and M. Khare[1]
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[1]IBM, [2]Samsung Electronics, [3]GLOBALFOUNDRIES, email: njloubet@us.ibm.com

Heterogeneous 3D Integration Faster than Moore

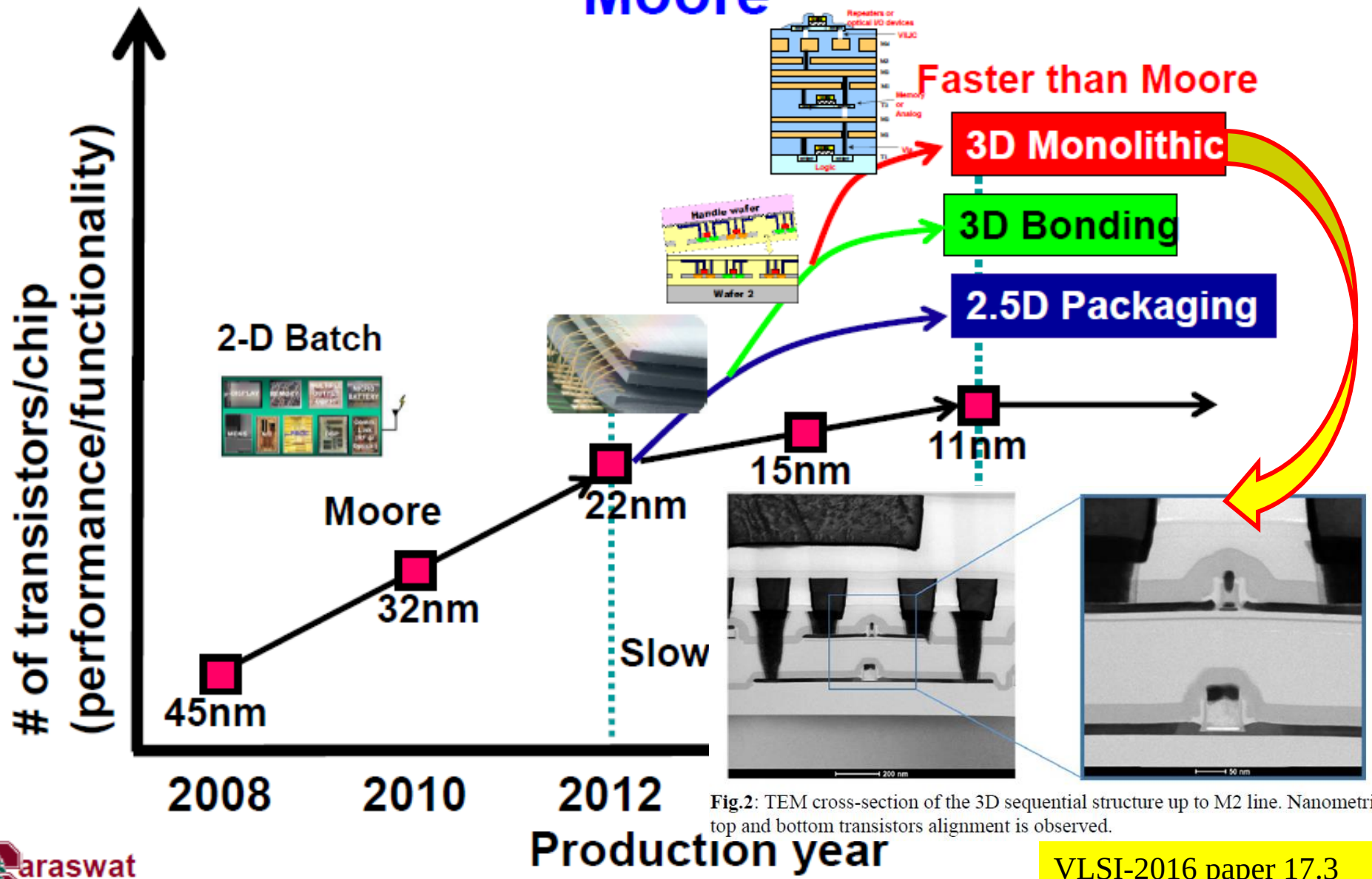

Fig.2: TEM cross-section of the 3D sequential structure up to M2 line. Nanometric top and bottom transistors alignment is observed.

VLSI-2016 paper 17.3

T17-3

VLSI-2017

Key process steps for high performance and reliable 3D Sequential Integration

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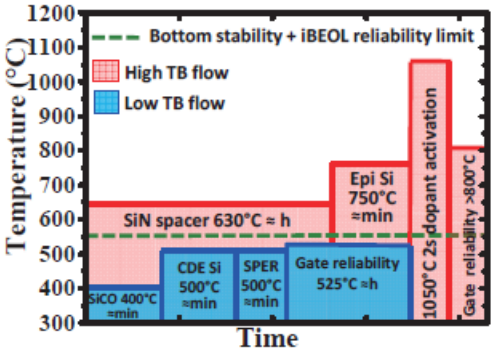

Fig. 17: Summary of high or low TB process flows taking into account reliability issues (gate stack and iBEOL ULK reliability).

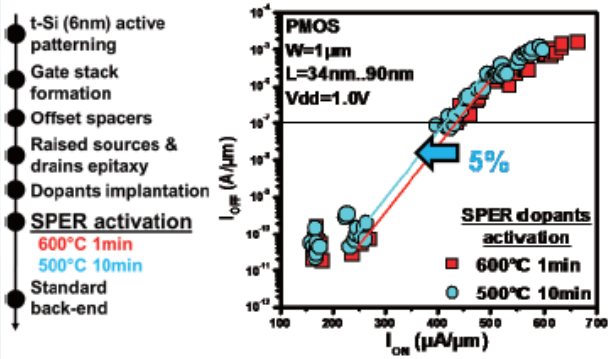

Fig. 3: Process flow and Ion/Ioff for 28nm p-type FDSOI devices integrating low thermal budget SPER.

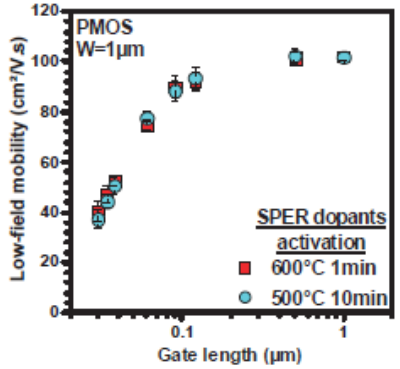

Fig. 4: Extracted low-field mobility vs gate length using Y-function method.

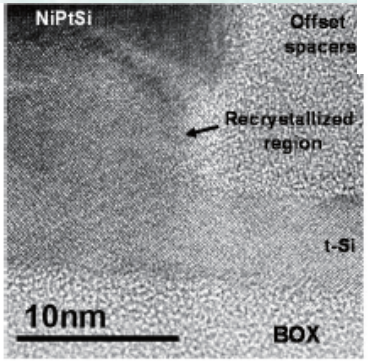

Fig. 5: TEM picture of S/D after SPER at 500°C 10min.

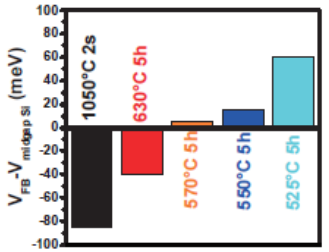

Fig. 7: V_{FB} shift induced by TB.

Top FET

	HT process flow	LT process flow
Offset spacers	SiN - 630°C ~2h	SiCO - 400°C → +5% ring oscillator speed [2]
		SiCBN - 550°C → +20% ring oscillator speed [3]
Raised sources and drains epitaxy	Si - 750°C ~15min	Si - 500°C ~30min [4]
	SiC:P - 600°C ~15min	
	SiGe:B – 630 to 650°C ~15min	SiGe:B - 500°C ~20min [5]
Dopants activation	1050°C ~2s	Xfirst+SPER - 600°C 1min → 95% of HT perf [6]
		Nanoseconds laser anneal [7] - Top~1200°C; Bottom<500°C
Reliability	1050°C ~2s = Dopants activation	Degradation below 800°C [8]

Fig. 1: Summary of low TB processes for top FDSOI devices. **Dopants activation and gate stack reliability are the two last points to address to obtain a complete process flow below 525°C.**

Bottom FET + iBEOL

Silicide	$NiPt_{10\%}Si$ [9]	FET stable up to 500°C few hours
	PAI + NiPt(SiC:P) [10]	R_{sheet} stable up to 700°C 2h
	Si-cap/PAI /NiCo(SiGe:B) [10]	R_{sheet} stable up to 600°C 2h
iBEOL	Cu/ULK [11]	Stable up to 500°C 2h
	W/ULK [11]	Stable up to 550°C 5h
	Metal/ULK reliability	No demonstration above 400°C

Fig. 2: Summary of maximum TB allowed for bottom transistors and iBEOL. **Reliability of ULK at 550°C needs to be evaluated.**

Summary: Smartphone the technology driver for 3-D More Moore and More Than Moore in this Decade!

- March 2017 Samsung Galaxy S8 using 10nm 3-D FinFET, 12M pixel 3rd generation hybrid wafer bonding 3-D stacked backside CMOS image sensor camera from **Sony** and thin 3-D ePoP (embedded package on package).
- Sept 2016 Apple iPhone 7 A10-AP uses 3-D FinFET 16nm from **TSMC**, 12M pixel 2nd generation 3-D stacked backside CMOS image sensor camera from **Sony** and 256Gb 48-layer 3-D NAND Flash memory from **Toshiba**.
- 10nm node production started in Oct-2016 at **Samsung** and **TSMC** for 2017 smartphone market but **Intel** delay to March 2017, industry focus is lower contact resistance (Rc) with slight channel mobility boost with S/D stressor.
- 7nm node in 2018/19 and localized high mobility tensile and compressive strain channel with the end of S/D stressor to improve Rc with S/D rap-around contacts.
- 5nm node in 2020/21 will still be FinFET
- Sub-5nm will be Si or Ge GAA nano-wire, GAA nano-sheet or 3-D stack transistor.