Ion Implant Applications to Enable Advances in Semiconductor Technologies

K.V. (“Vivek”) Rao, Ph.D.
Applied Materials, Inc.

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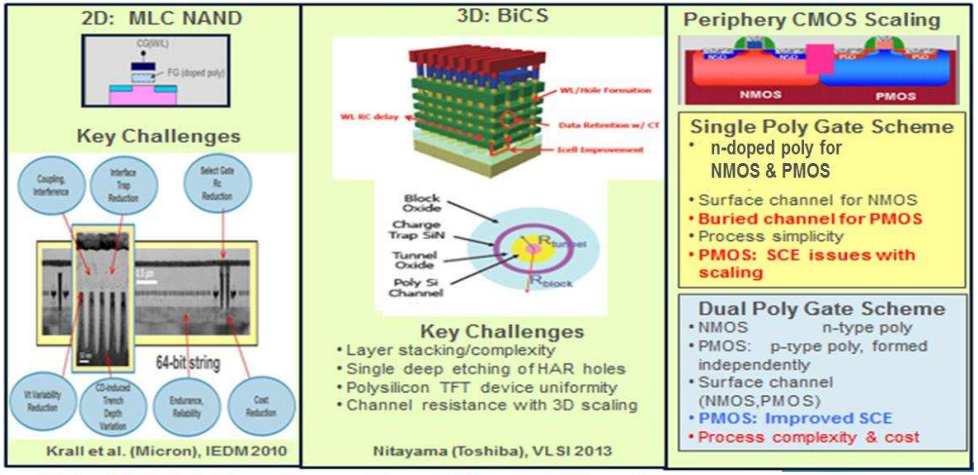
Outline

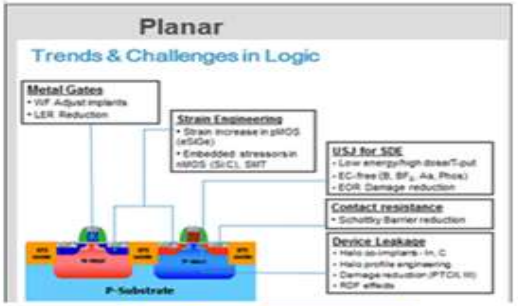
- Technology Scaling Challenges
- Implant Damage and Profile Engineering
- Stress Memorization Technique
- Fin Damage & Strain Engineering
- Work Function Engineering
- Contact Engineering
- Uniformity Improvement with Implants
- Summary

Key Device Scaling Challenges

NAND Technology Trend and Challenges



Logic/Foundry Device Scaling Challenges



Ion/Ioff
VtU/IdU Variability
Vccmin
Leakage
HKMG reliability
Rc reduction

Ion/Ioff
VtU/IdU Variability
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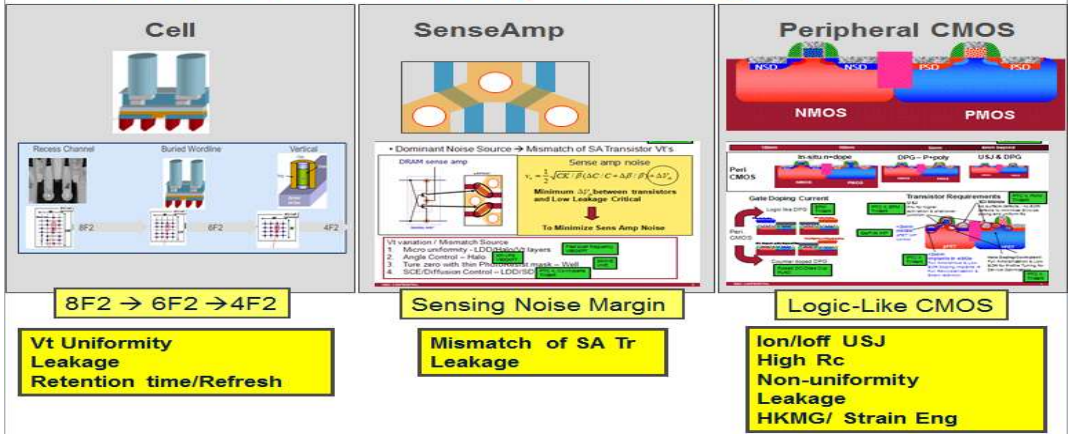
Rc reduction

+

Fin Doping
Fin Defects

DRAM Device Scaling Challenges



8F2 → 6F2 →4F2

Vt Uniformity
Leakage
Retention time/Refresh

Sensing Noise Margin

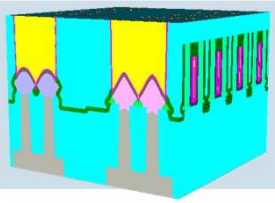
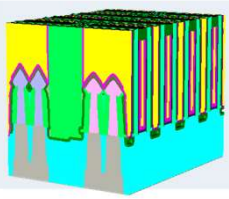
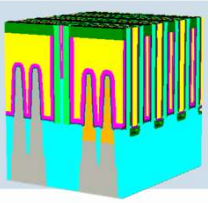
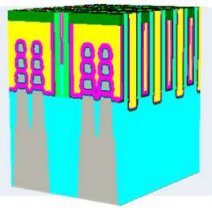
Mismatch of SA Tr
Leakage

Logic-Like CMOS

Ion/Ioff USJ
High Rc
Non-uniformity
Leakage
HKMG/ Strain Eng

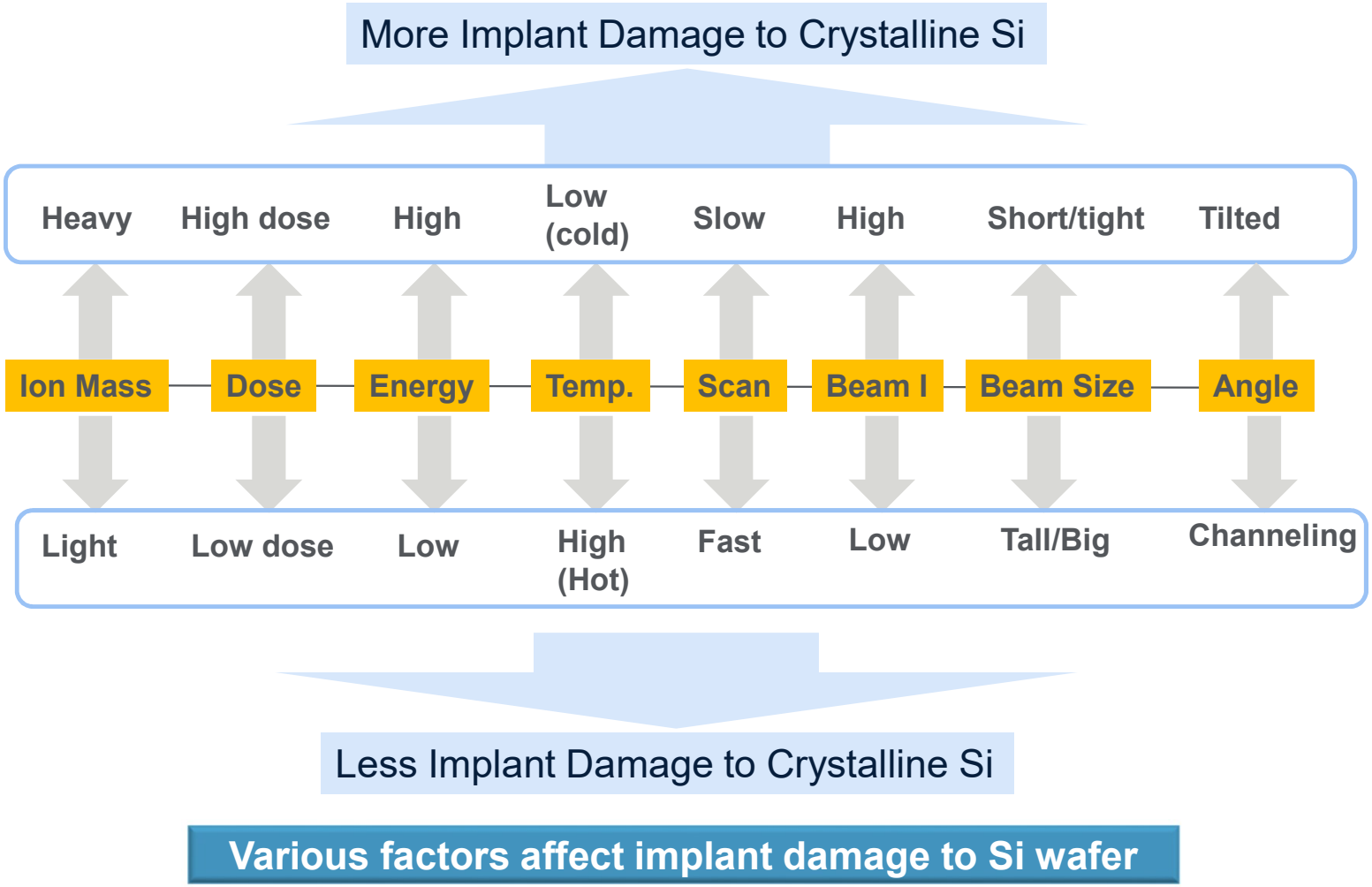
- Junction/Damage Engineering (Ion/Ioff)
- Rc Reduction
- Uniformity (micro, macro)
- Reliability
- Strain Engineering
- Process Margin (litho, etch, CMP..)

Transistor Roadmap

Node	N	N+1	N+2	N+3
				
Architecture	FinFET	Scaled tall vertical FinFET		Gate All Around (hGAA)
Channel	Silicon		SiGe p-channel	Si / SiGe superlattice
Extension I/I	Beam Line		PLAD Non-line-of-sight doping	
Contact	Trench Contact		Replacement Contact / Wrap Around Contact (WAC)	
Contact I/I	Ge PSI, Beam line		Beam line / PLAD, SBH	

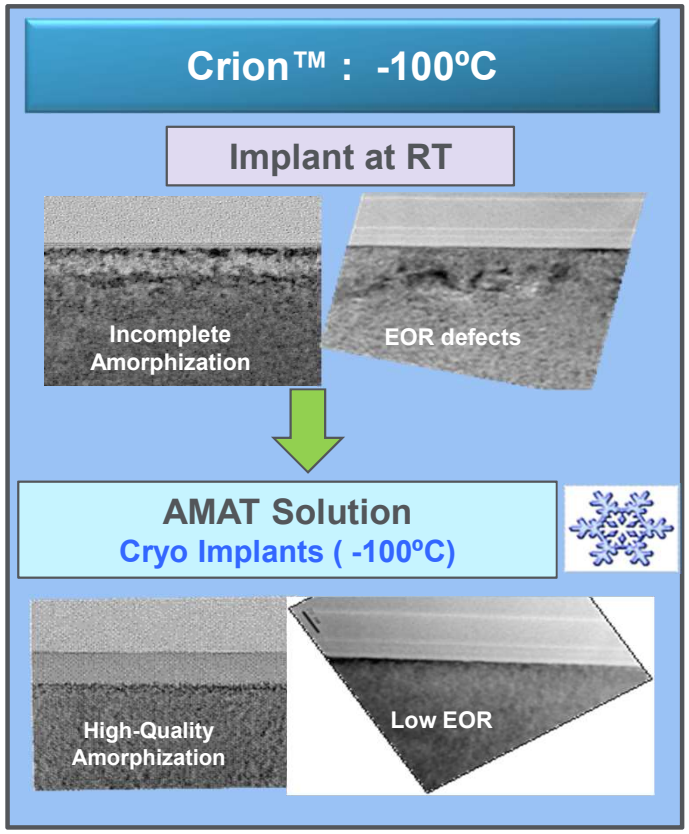
Architecture and materials changes with CMOS scaling
➔ incorporate damage engineering and conformal implant solutions

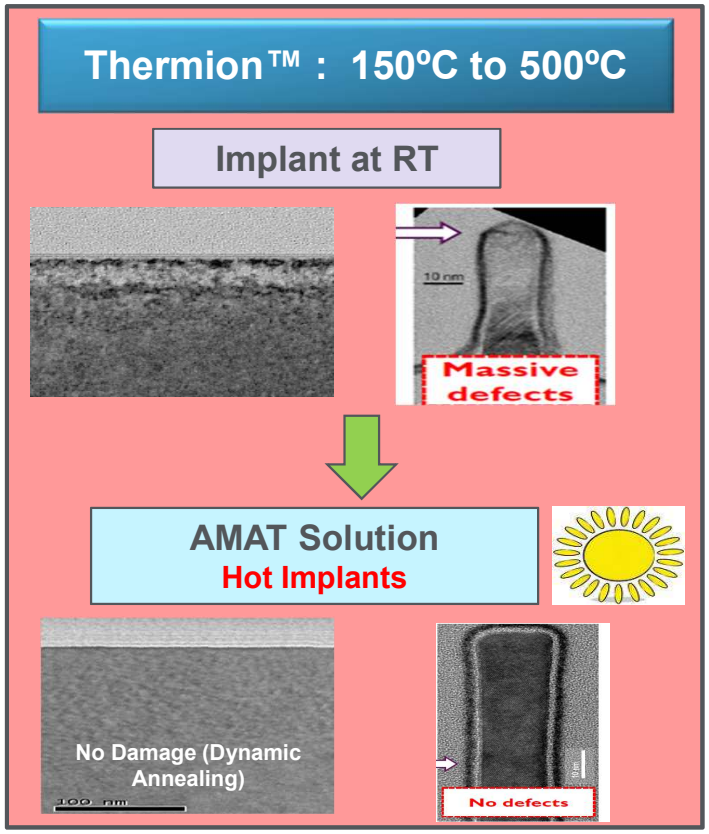
Implant Damage Engineering Knobs



Various factors affect implant damage to Si wafer

Damage Engineering with Thermal Implants

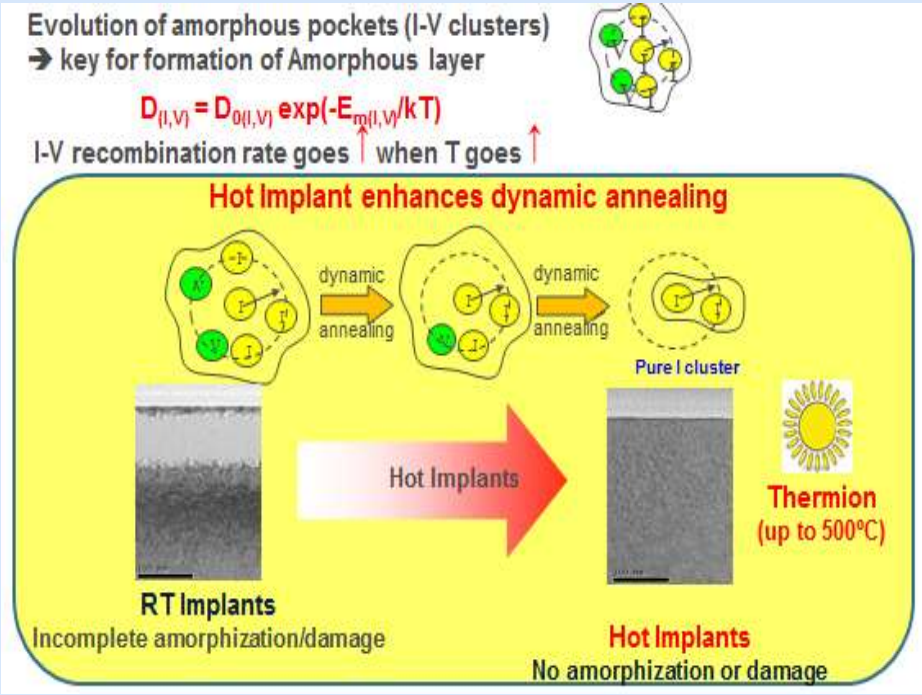




Damage Engineering delivers:
(a) improved activation (b) reduced damage (c) reduced variability

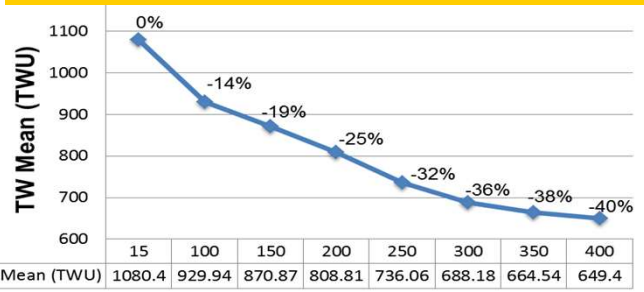
Thermion™ (Hot Implants): Damage Reduction

Hot Implant
Reduces Growth of Amorphous Pockets



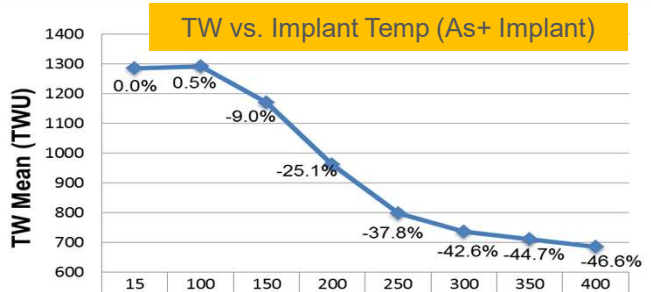
Thermion™ Reduces Implant Damage

ThermaWave (TW) Signal vs. Implant Temp (B+ Implant)



	15	100	150	200	250	300	350	400
TW Mean (TWU)	1080.4	929.94	870.87	808.81	736.06	688.18	664.54	649.4

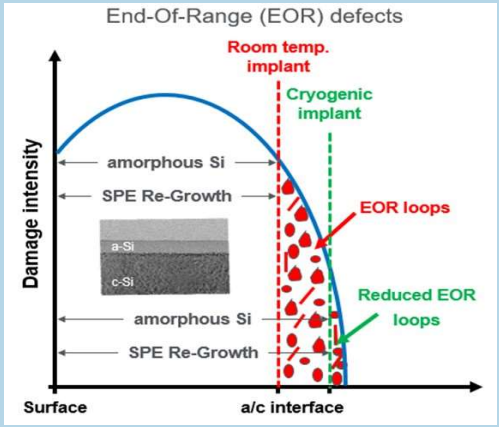
TW vs. Implant Temp (As+ Implant)

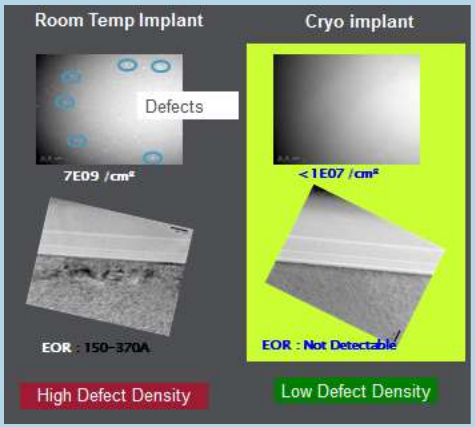


	15	100	150	200	250	300	350	400
TW Mean (TWU)	1284.2	1290.8	1169.1	962.24	798.18	737.23	710.22	686.17

Damage reduced as implant temp is increased

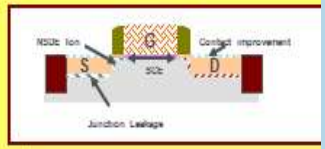
Source/Drain Engineering: Cryo & Co-Implant Solutions



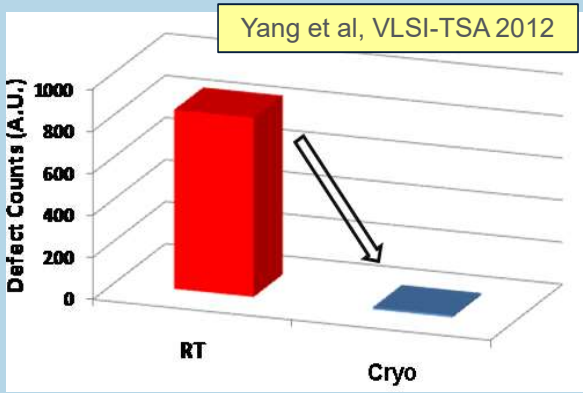


Cryo Damage Eng Improves :

- Leakage Current
  - Ioff
  - Iboff
  - GIDL
  - DIBL
- Rc improvement
- SCE Control
- Increase drive current
- Variability

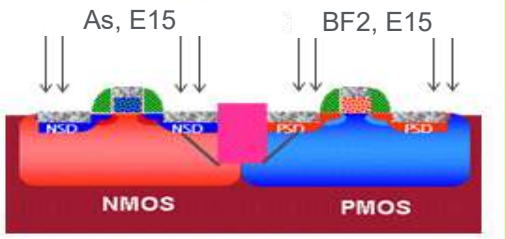


Yang et al, VLSI-TSA 2012



Cryo Ge PAI implant reduced NiSi piping defects (EBIC) by 90%

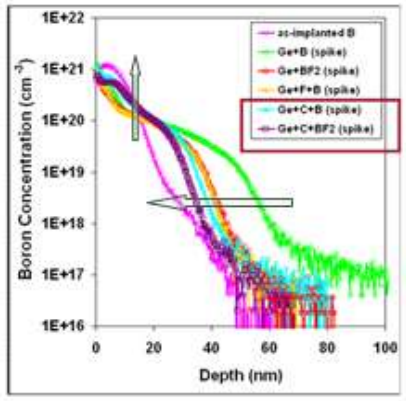
Cryo Implants ➔ Reduced EOR & Defects, Improved Activation, better silicidation, improved variability, SCE, drive current



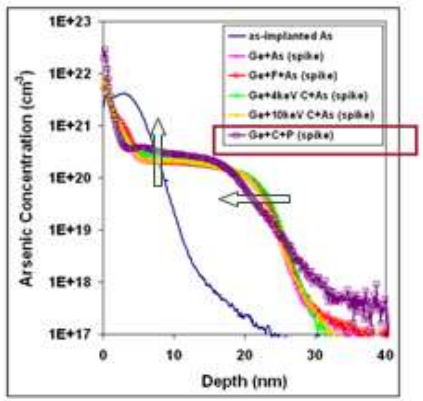
Heavy SD Implants induce dislocations ➔ Leakage Issue

- **NMOS solution: C + P (cryo)**
- **PMOS Solution: BF2 (cryo)**

PMOS USJ



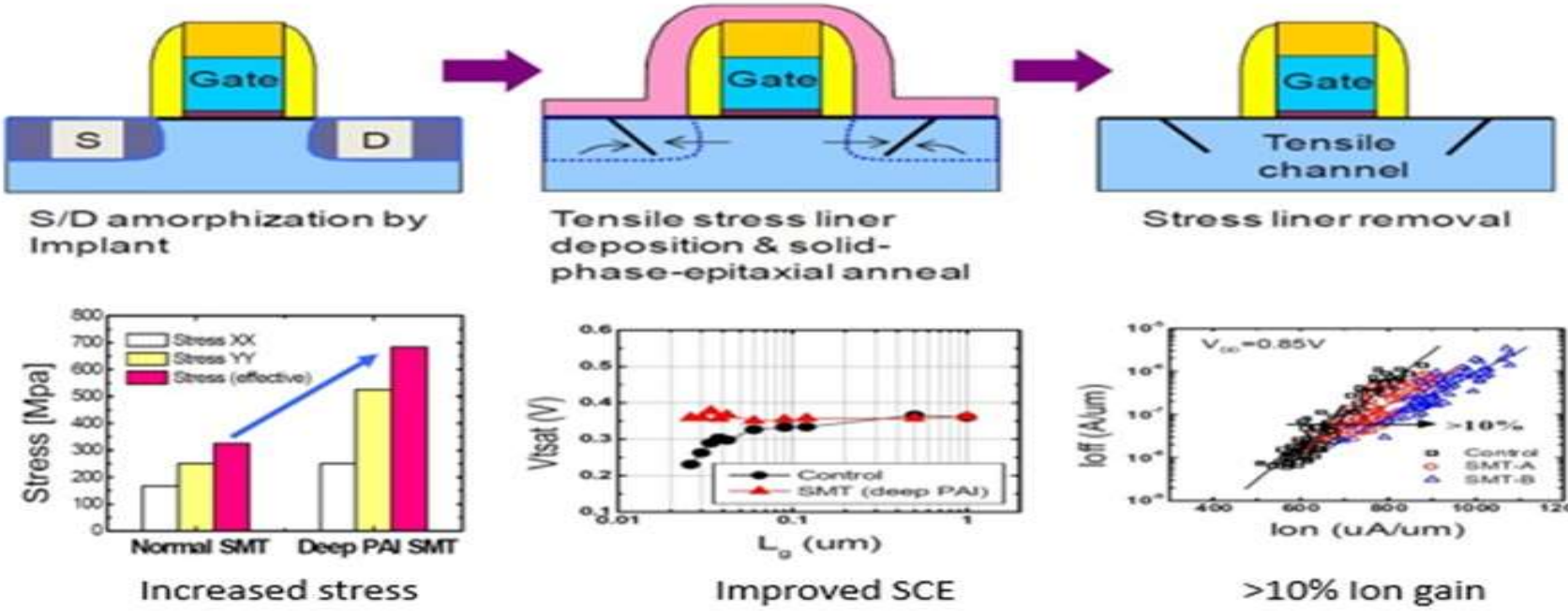
NMOS USJ



Ge PAI + C co-implant for USJ

- ❑ Ge PAI creates a-Si layer for ideal implant junction (no channeling)
- ❑ As can be replaced by P ➔ reduced defects, increased solubility
- ❑ Boron and Phos diffusion retarded by C
- ❑ Shallow junction with improved abruptness, enhanced activation

Strain Engineering for Planar NFET



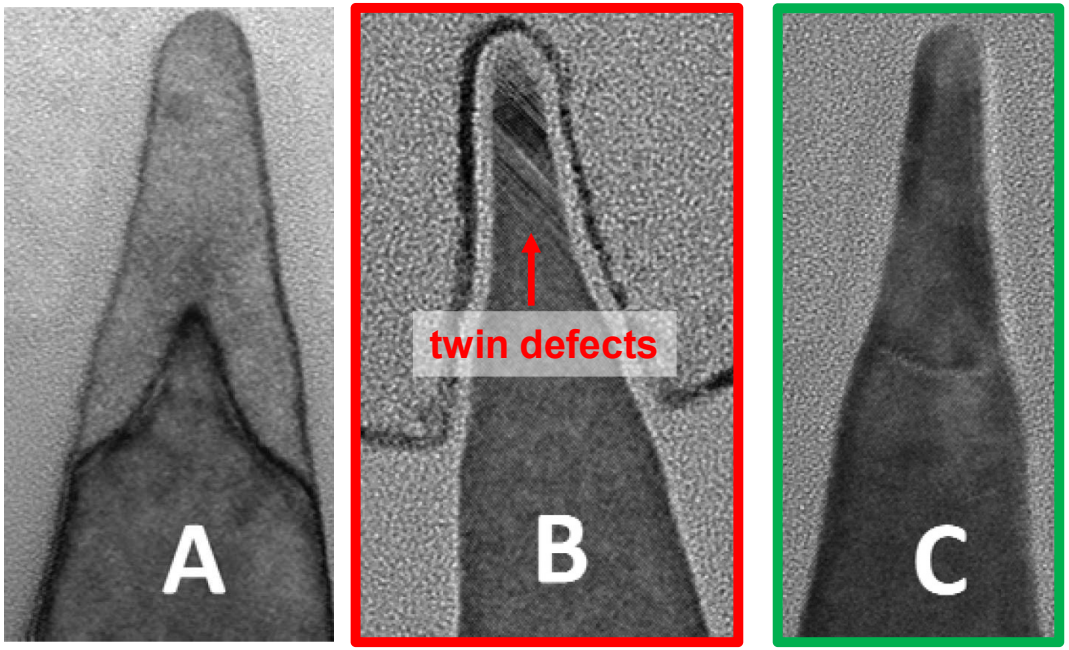
[1] Lim et al, IEDM 2010

32nm NFET SD stress memorization technique (SMT) with deep amorphization with cryo Ge PAI

- Resulted in 10% Ion gain
- Potential application of SMT to n-FinFET

Si Channel: Hot Implants (As or P) for Extension or WAC

TEM cross sections of Silicon Fins

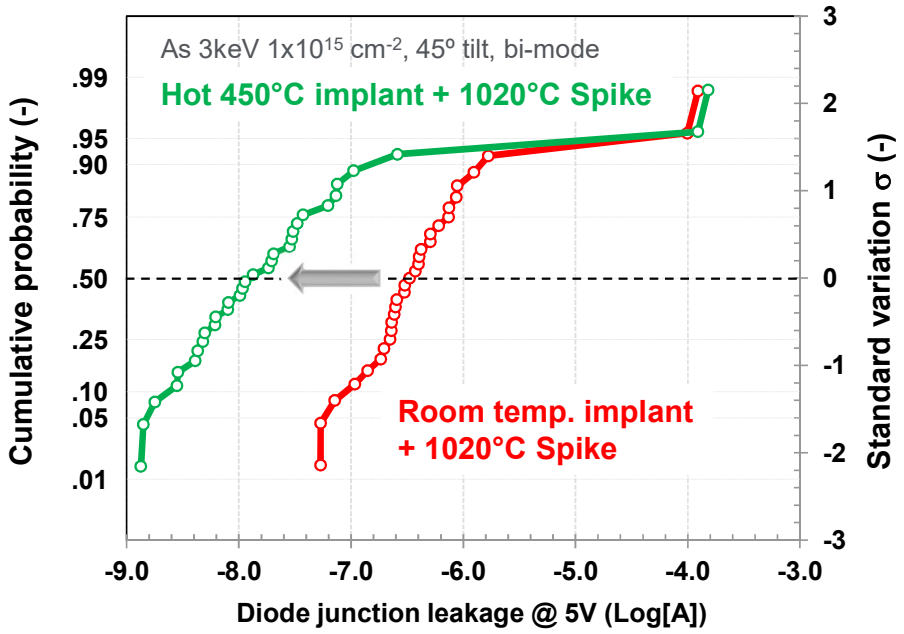


Room temp. I/I | Room temp. I/I + 1000°C spike | Hot 450°C I/I

Implant condition: As 3keV 2x10^{15} cm^{-2}, 30-45deg tilt, bi-mode

[2] L. Pipes, IIT 2014

Diode junction leakage: Room temp. vs. hot I/I

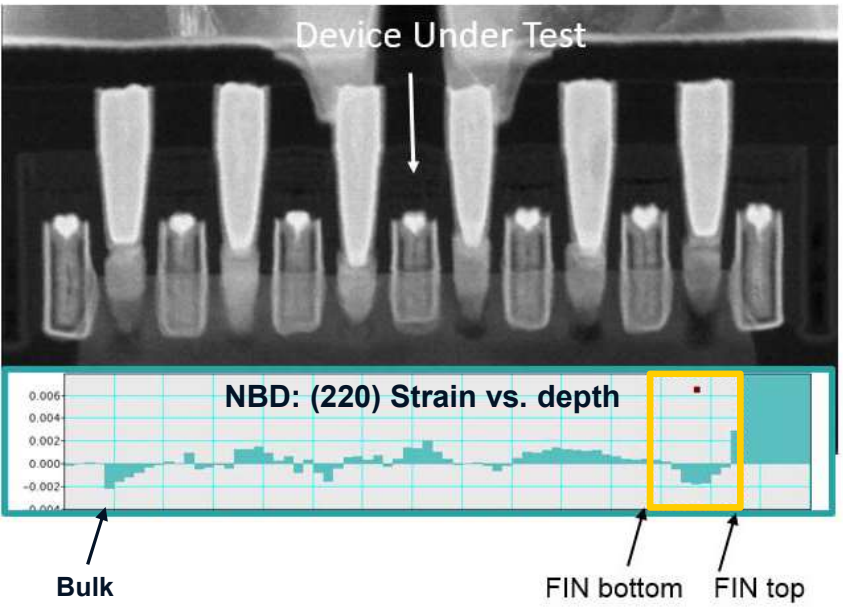


[3] B. Wood et al, ECS 2013

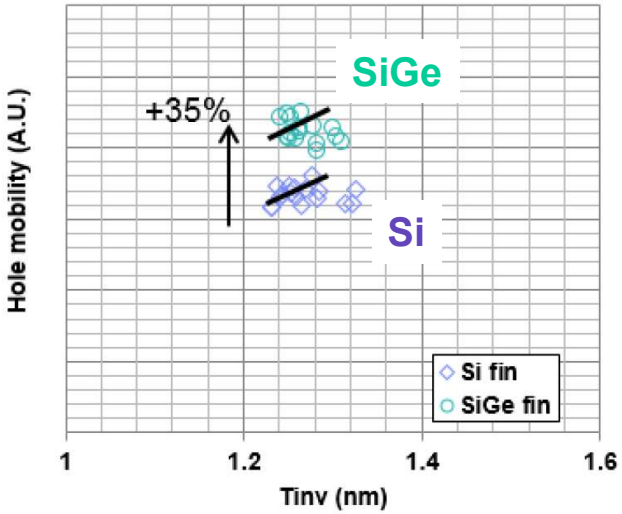
- S/D ext or WAC implant can amorphize the fin, which results in twin defects after anneal
- Hot implant can eliminate the formation of amorphous Si and twin defects

P-FinFET: SiGe Channel Performance Benefit over Si

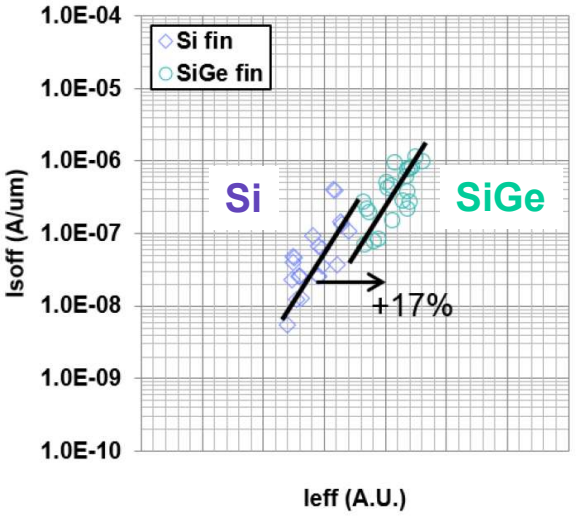
TEM along the Fin
NBD profile for SiGe Fin post M1



Hole mobility vs. Tinv



Isoff vs. Ieff

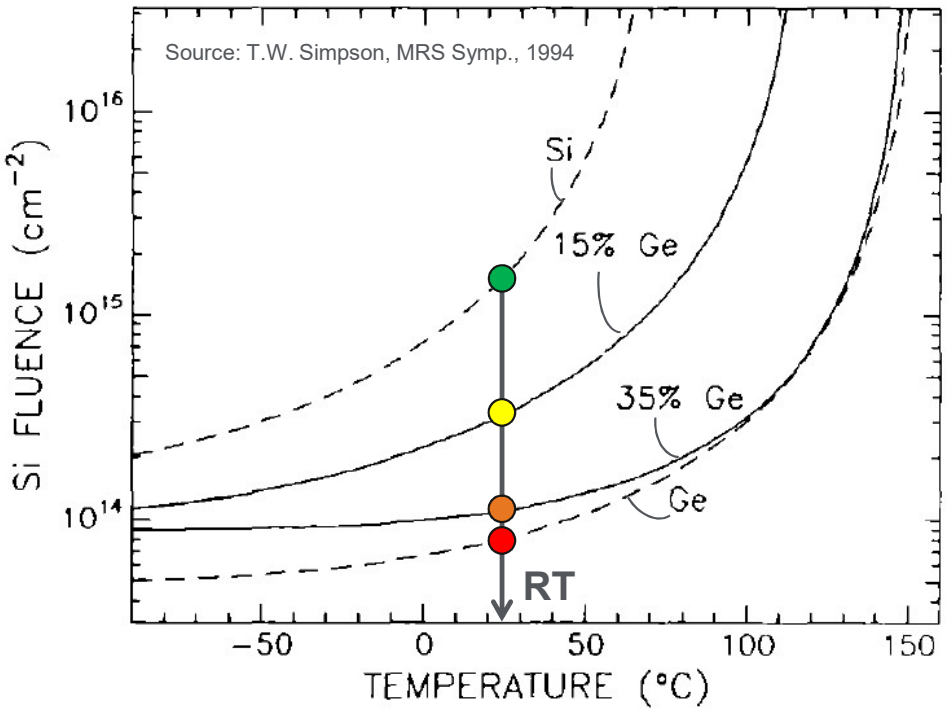


[4] Guo et al, VLSI 2016

- Strained SiGe results in compressive strain, which results in hole mobility enhancement
- 17% PFET Ieff benefit can be observed for SiGe over Si channel for long-channel devices

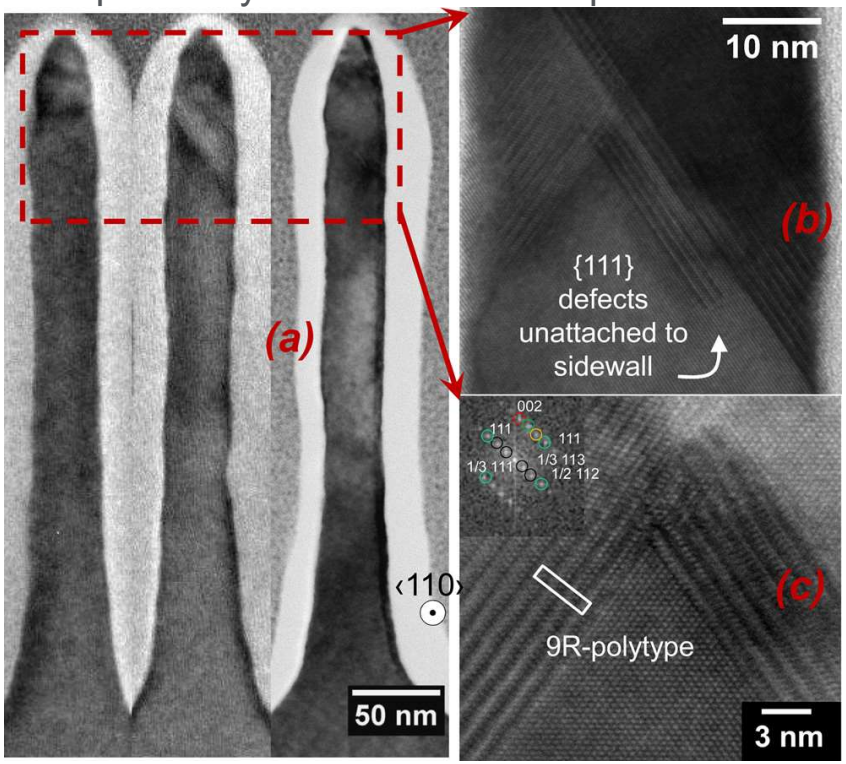
SiGe Channel: More Sensitive to Amorphization and Defects

Critical dose for amorphization



[5] T. Simpson, MRS Symp.,1994

Example: recrystallization of amorphous Ge Fins

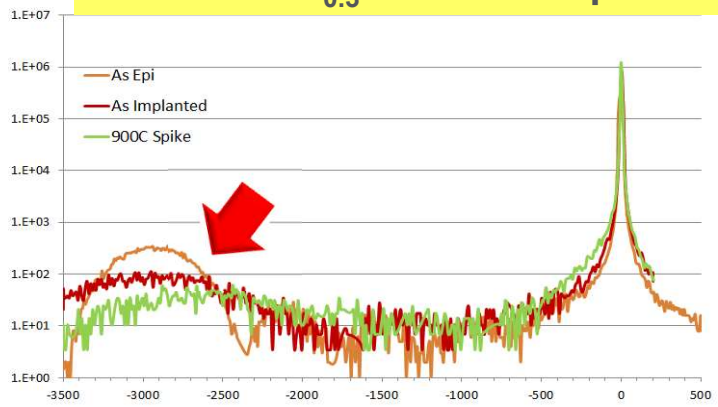


[6] Duffy et al. (2011)

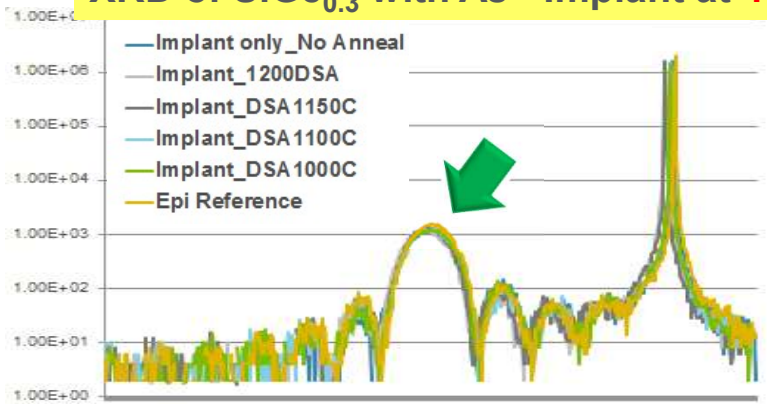
- Critical dose for amorphization of $SiGe_{0.3}$ is only ~10^{14} cm^{-2}; for silicon it is ~10^{15} cm^{-2}
- This makes SiGe fins even more vulnerable for amorphization and defects than Si fins

SiGe Channel: Hot Implant to Avoid Relaxation & Defects

XRD of $SiGe_{0.3}$ with As+ implant at RT

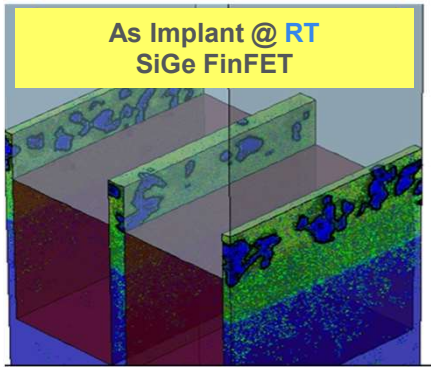


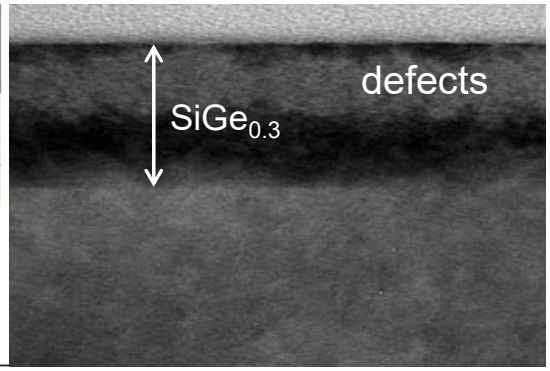
XRD of $SiGe_{0.3}$ with As+ Implant at 450C



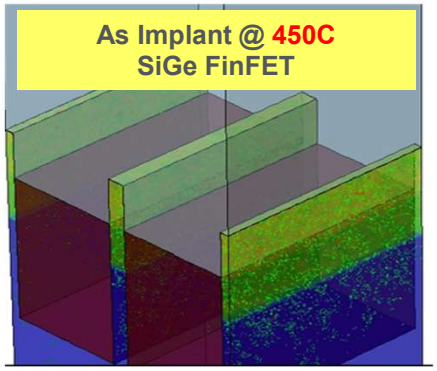
AMAT Data

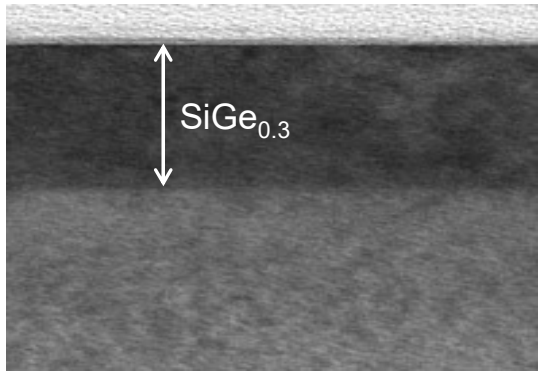
As Implant @ RT
SiGe FinFET





As Implant @ 450C
SiGe FinFET



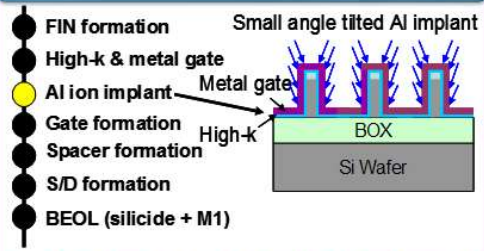


- **RT implant** ➔ SiGe channel strain is lost. Even after 900°C spike anneal, strain does not recover
- **Hot 450°C implant** ➔ channel strain is retained. SiGe has not relaxed

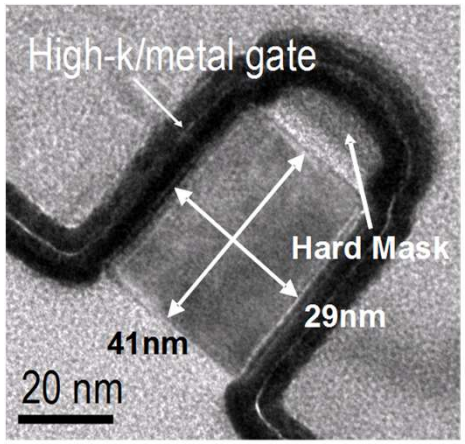
HKMG Work Function Engineering

Multi-Vt Offerings for SOC by Changing the Al+ implant conditions

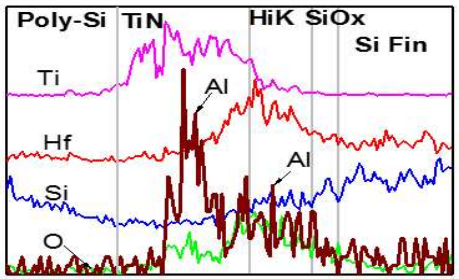
Process Flow



- Small angle tilted Al implant performed after metal gate dep
- Implant places Al near metal gate/high-K interface

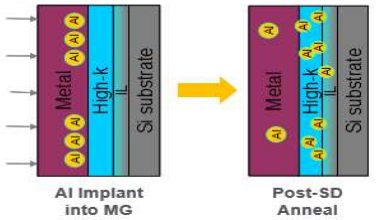


EDX Analysis (Post-SD Anneal)

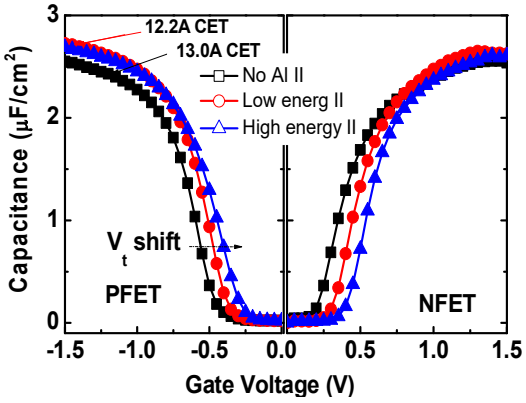


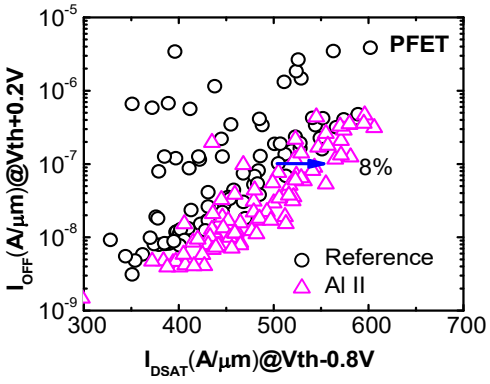
- Al presence at HK/SiO_x interface is responsible for dipole formation
- No Al contamination in Si channel

Dipole Formation with Al Implant & Thermal Drive



- Implant places Al in TiN metal gate
- During SD activation anneal, Al is driven to HK/SiO_x interface for dipole formation

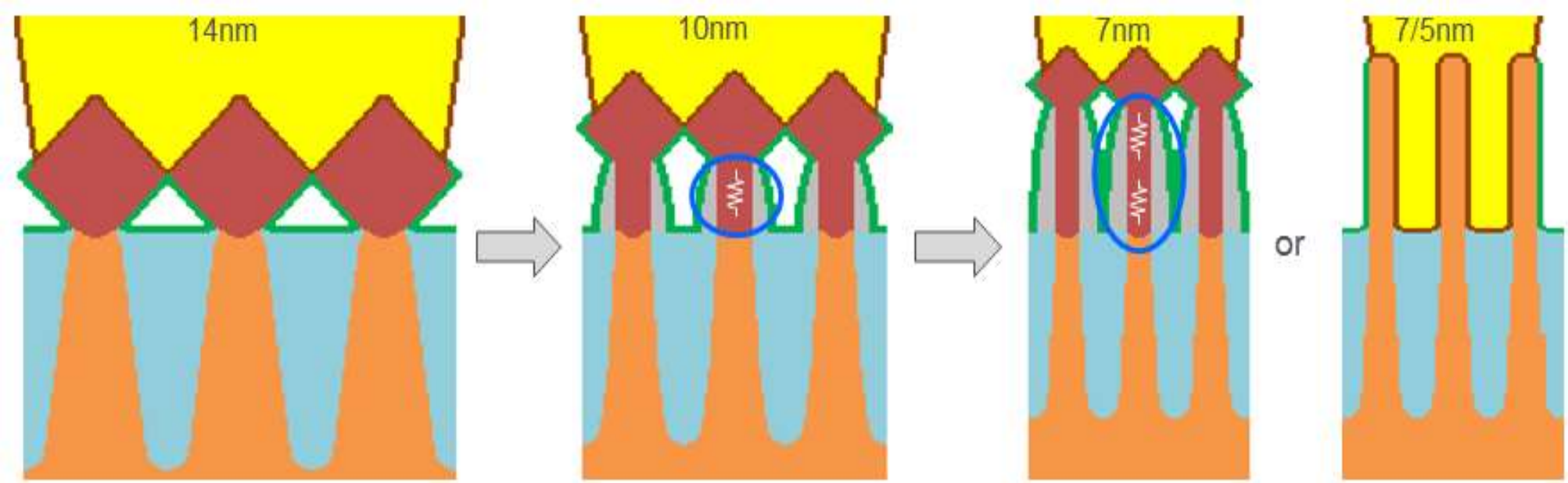




[7] Rao et al, IIT 2012

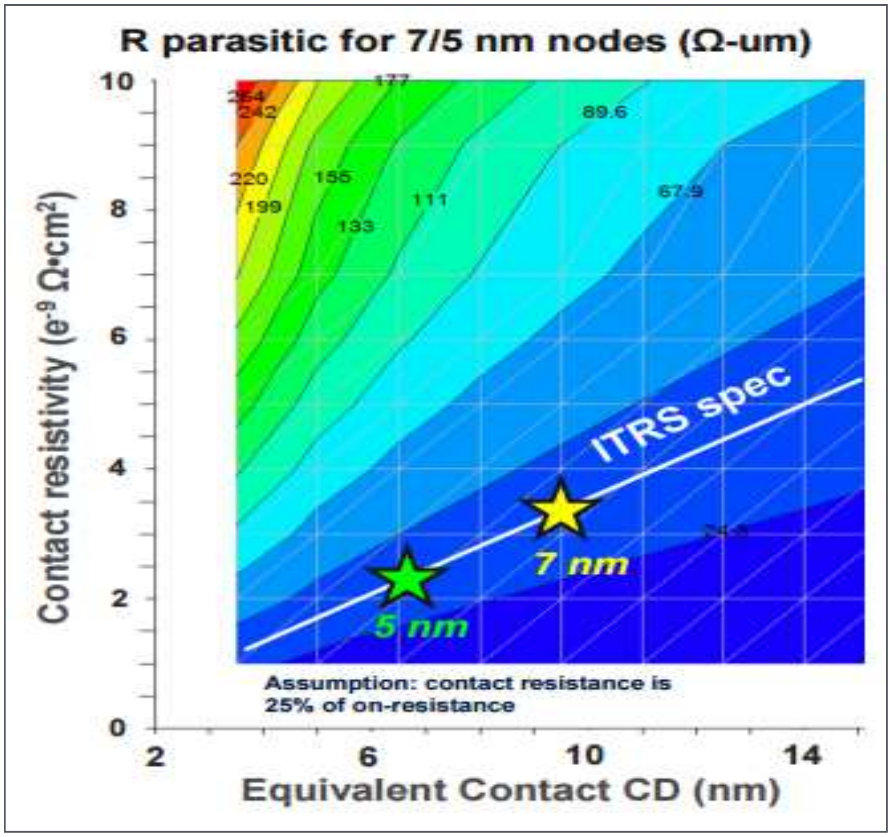
- +170mV V_{FB} shift achieved with Al implant
- No CV stretch-out; CET_{inv} was reduced by 0.8Å with Al implant
  - ***Better EOT scalability compared to Al-based cap***
- 8% PFET I_{on}-I_{off} improvement with Al implant

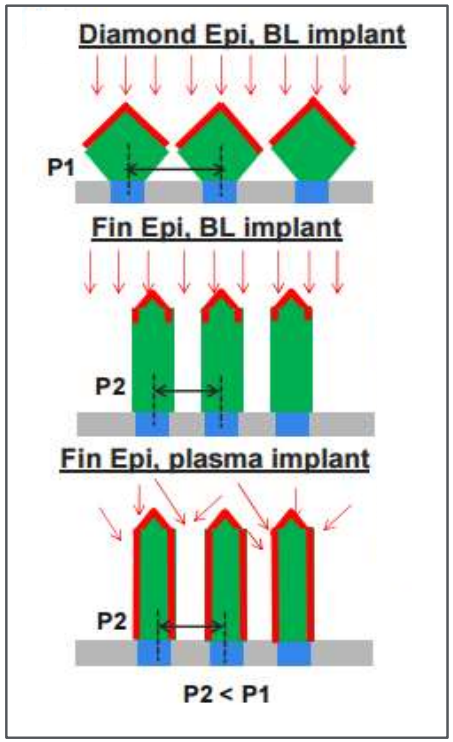
Impact of Scaling on External Resistance

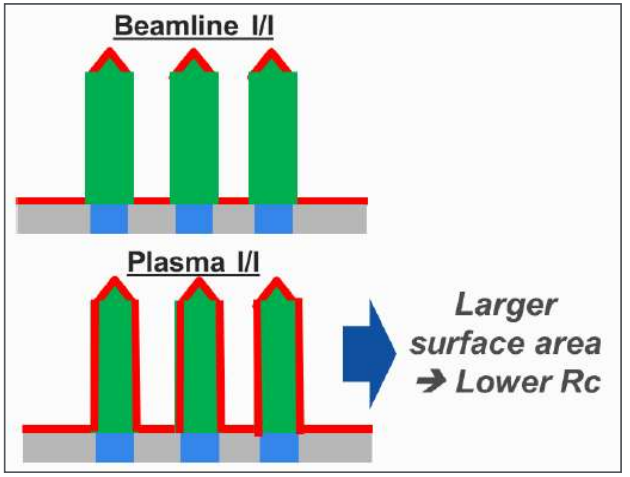


- Fin pitch scaling reduces contact area ➔ increases Rc
- Tall fin height results in increase of S/D resistance (RSD)
- Need Wrap-Around-Contact (WAC) to break trend of increasing Rc and RSD
  - ➢ Requires uniform top / sidewall doping solutions for NFET & PFET

PLAD for n-FinFET Contacts: Future Requirements for Rc



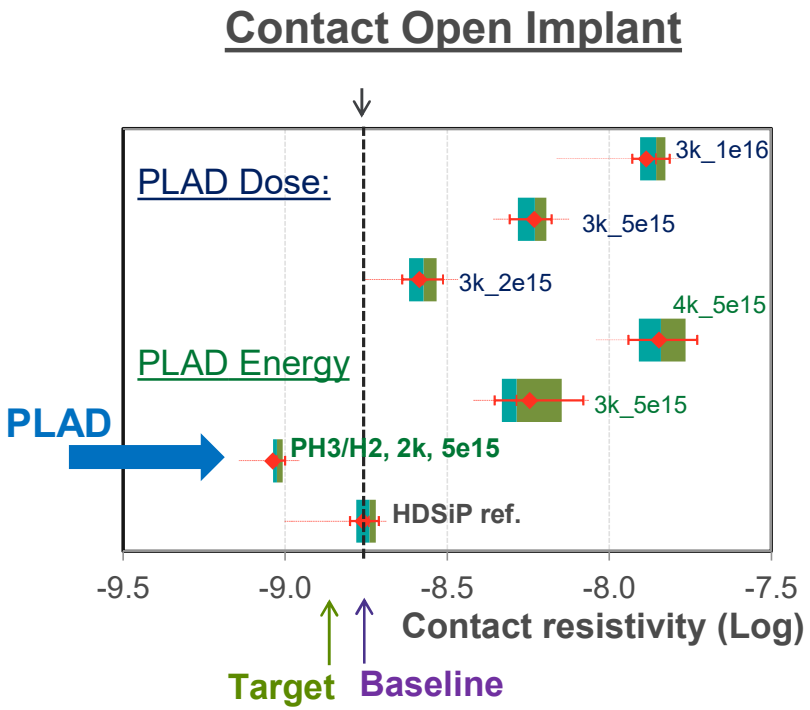




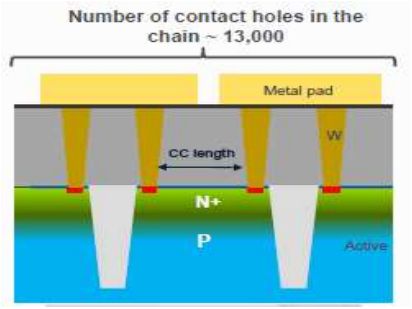
[8] Ni et al., VLSI (2016)

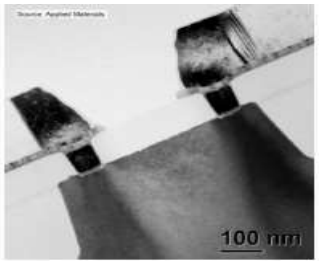
High aspect ratio (HAR) contacts ➔ Wrap-around contacts (WAC) ➔ PLAD conformal doping

Plasma Doping (PLAD) for nFET Contact Implant



- HD:SiP epi (High Dose) 2.5e21/cm^3 P
- PMD Dep
- RMG Anneal
- Contact pattern, open, and strip
- PLAD PH3 implant → wet clean (SPM&SC1)
- Siconi pre-clean/Ti/TiN Dep
- DSA 800°C contact anneal





[8] Ni et al., VLSI (2016)

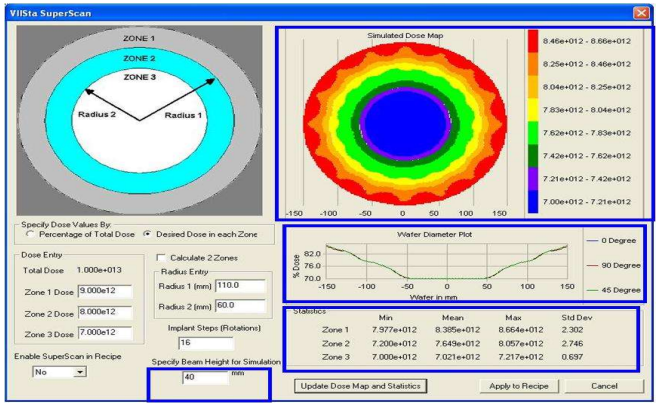
- PLAD PH3 doping into contact resulted in NMOS contact resistivity, ρc < 1E-9 Ω.cm^2
- High Dose: May cause P agglomeration
- High E: May amorphize Si beyond SPE regrowth and $TiSi_x$ consumption

SuperScan for Yield Improvement

Ability to Vary Dose Across Wafer

Custom dose patterns to Improve device performance & die yield

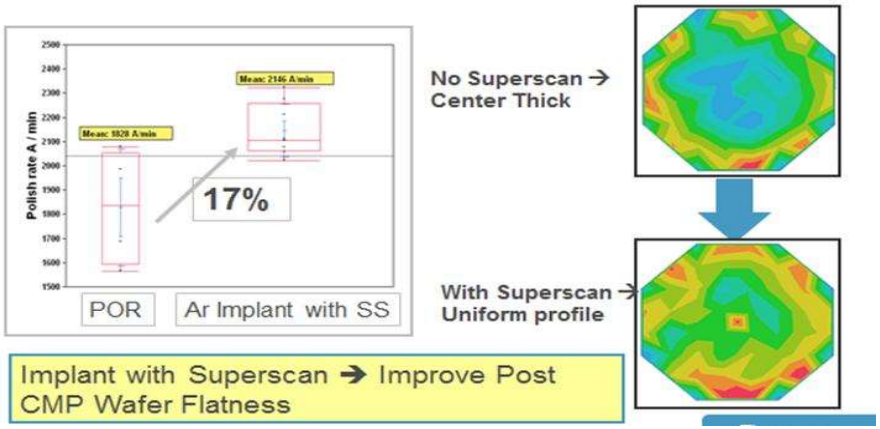
- Compensates for CMP/etch/thin film/thermal variations
- Designed for R&D and production apps
- Independent NMOS & PMOS Vt and Id uniformity tuning
- Available on VIISta HC, MC and HE implanters



Custom dose pattern with SuperScan

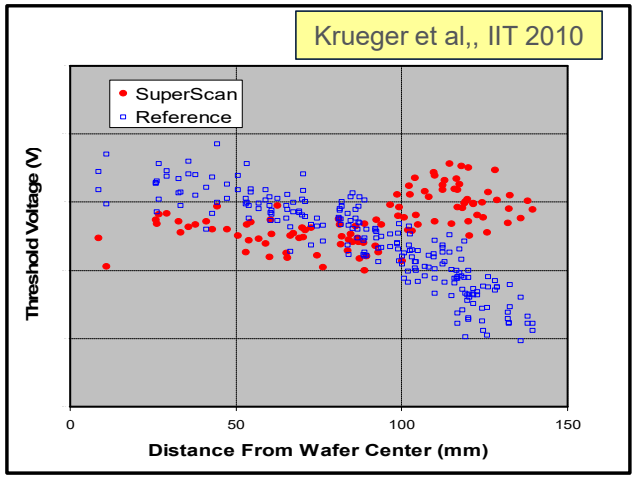
STI CMP - HDP Oxide

Macro Rate Polish Rate Modulation with Superscan



Implant with Superscan → Improve Post CMP Wafer Flatness

CMP uniformity improvement with SuperScan



28nm PMOS Vt radial uniformity improvement with halo implant with SuperScan

Summary

- Changes in architecture and materials being incorporated with technology scaling
- Ion implant solutions enable technology scaling
- Implant damage engineering is key to improve device performance, reduce variability and improve yield
- Optimization of ion implant conditions for various applications; examples:
  - Cryo/co-implants for profile and junction engineering
  - Stress Memorization Technique for planar CMOS
  - Hot implants for fin defect reduction and reduced leakage
  - HKMG work function engineering for Vt tuning
  - Rc reduction with contact implants (including PLAD for conformal doping for Wrap-Around Contacts)

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[7] K.V. Rao et al, IIT 2012, p38-41.

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