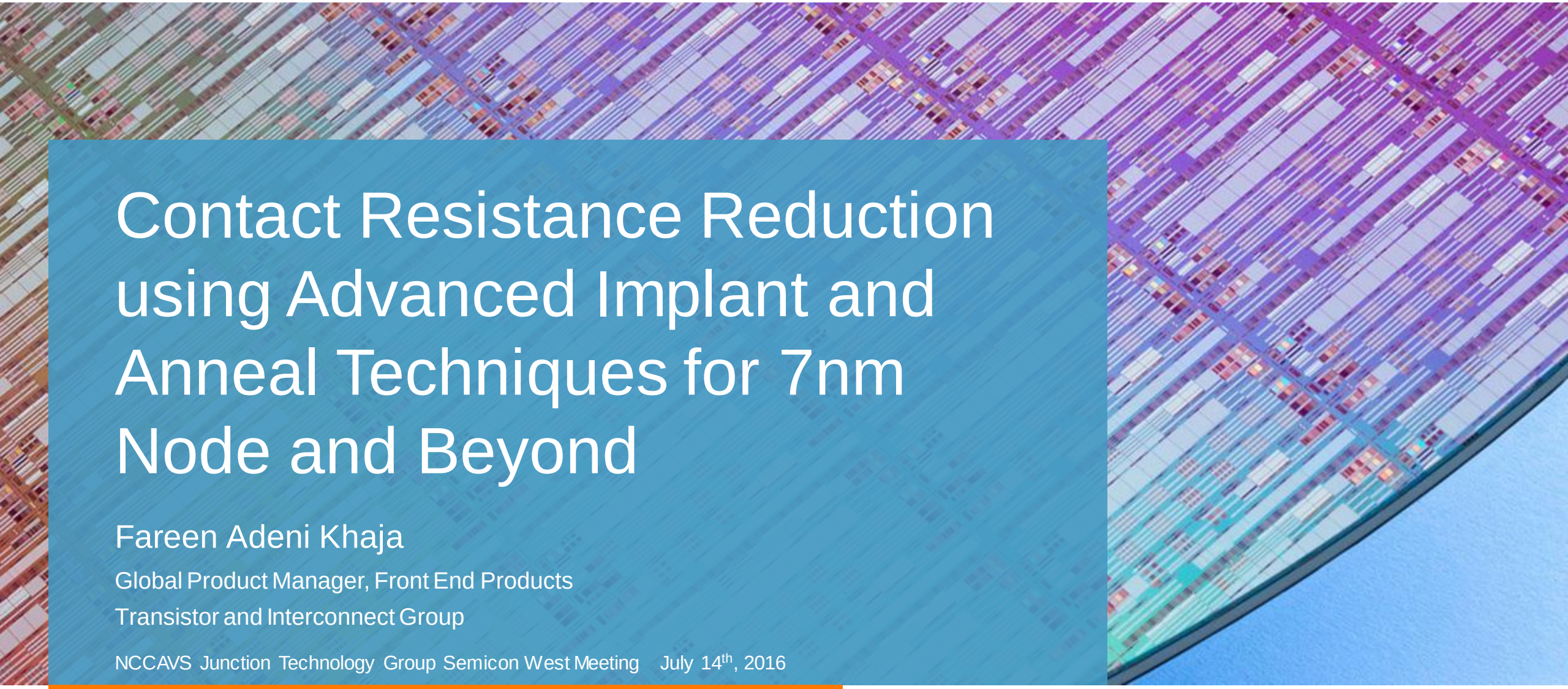


Contact Resistance Reduction using Advanced Implant and Anneal Techniques for 7nm Node and Beyond

Fareen Adeni Khaja

Global Product Manager, Front End Products

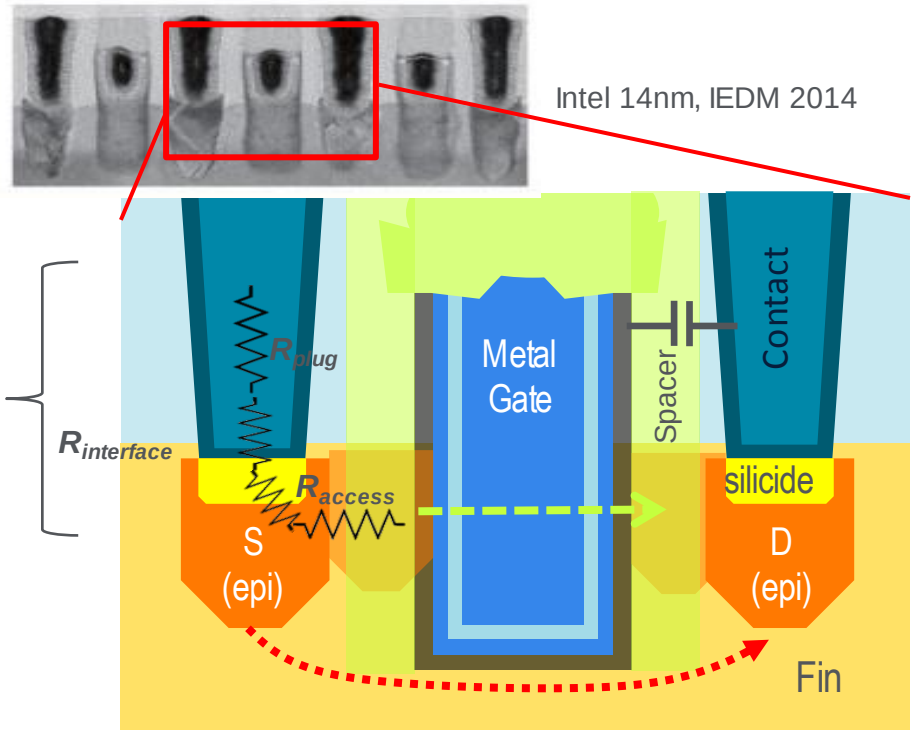
Transistor and Interconnect Group

NCCAVS Junction Technology Group Semicon West Meeting July 14th, 2016

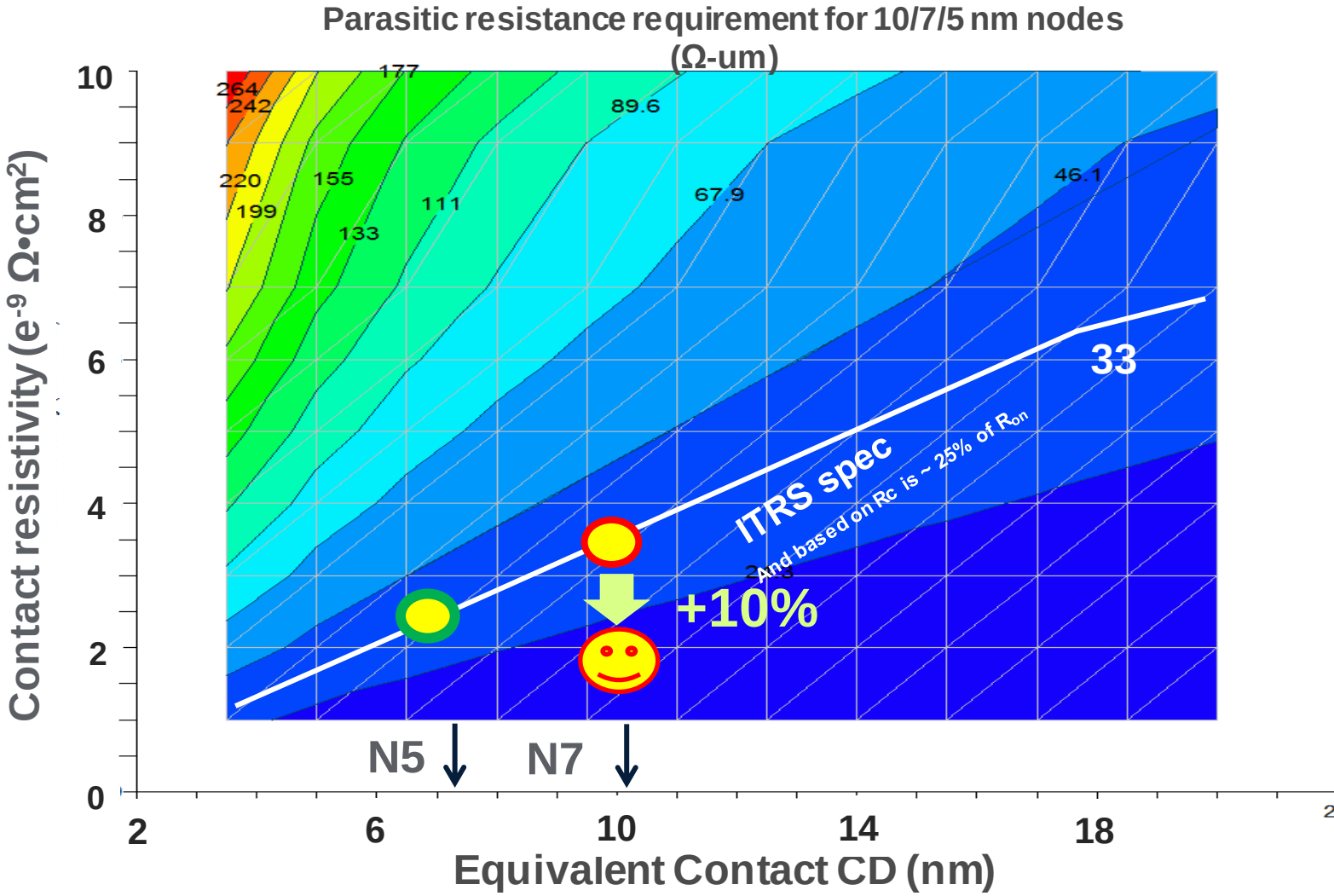
Outline

- Motivation for Contact Resistivity (ρc) Reduction
- Advanced Implant Techniques for ρc Reduction
- Nanosecond Laser Anneal for PMOS and NMOS ρc Reduction
- Summary

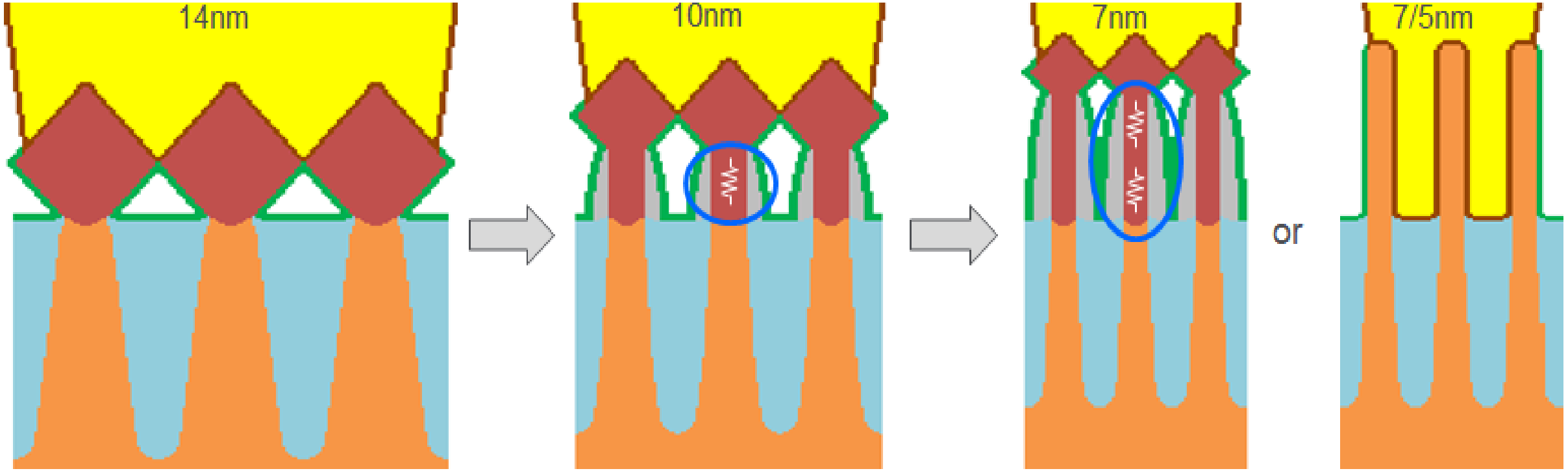
Low Contact Resistance Requirement for Transistor Continuous Scaling



- R_{Plug}
- $R_{Interface}$
- R_{access}



Impact of Scaling on External Resistance



- Fin pitch scaling reduces contact area ➔ increases Rc
- Tall fin height results in increase of S/D resistance (RSD)
- External resistance is limiting transistor performance

Require Innovative doping and Annealing solutions for NFET & PFET to reduce Rc and RSD

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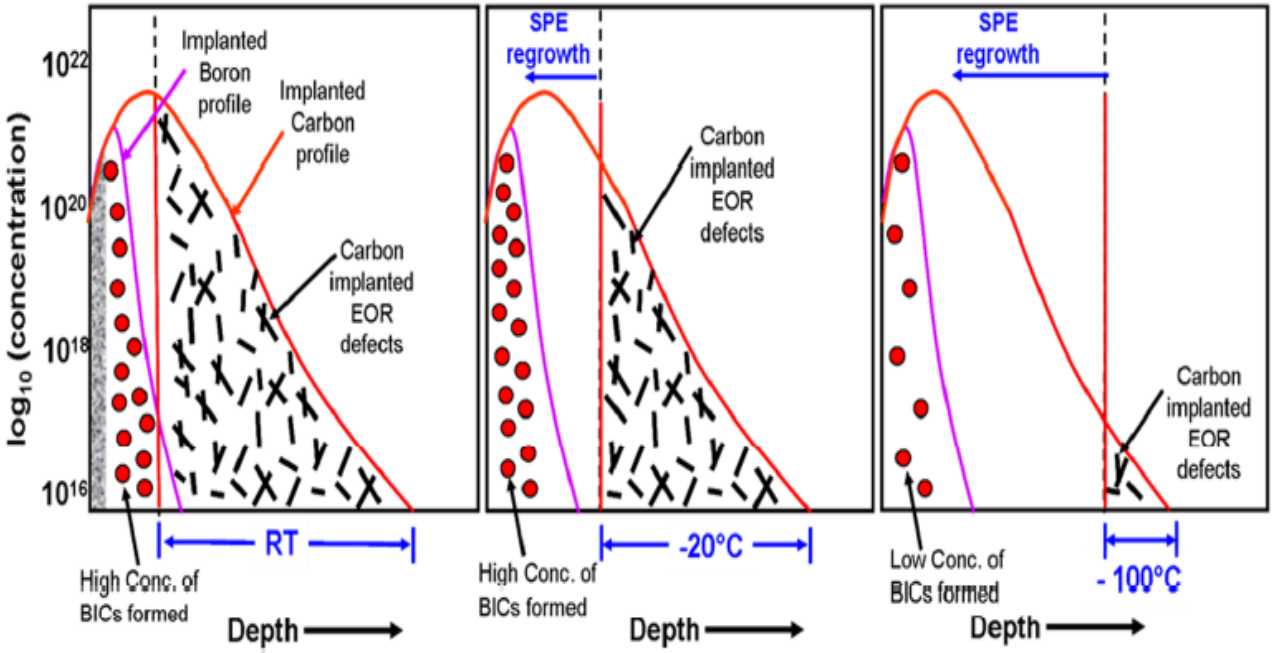
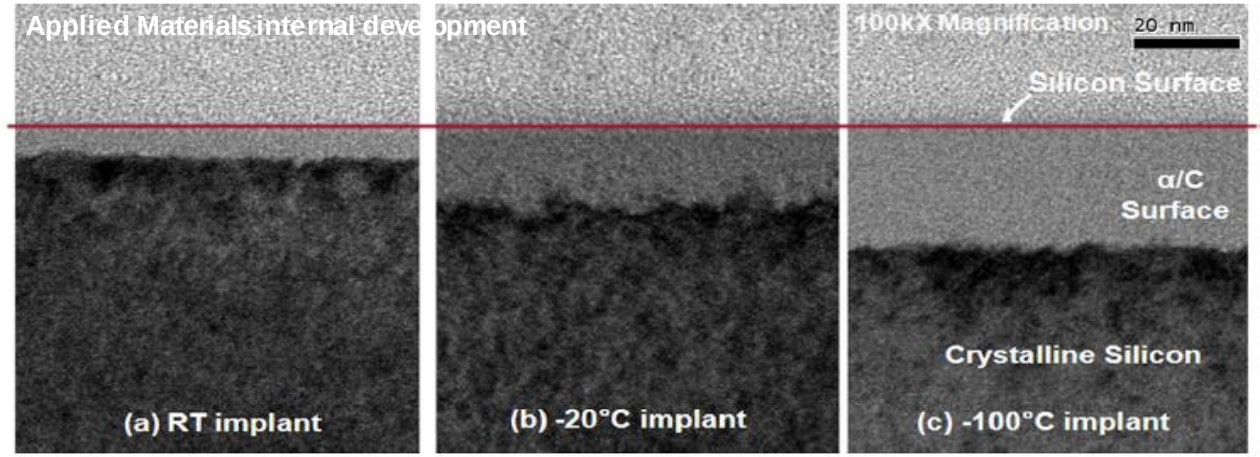
Damage Engineering with Cryogenic Implants

Physical Mechanism





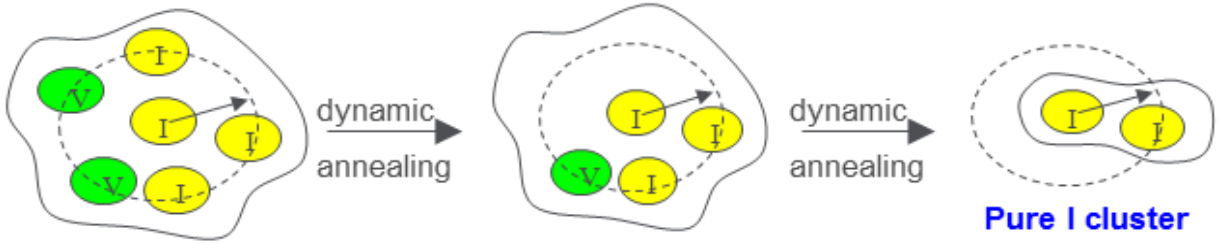
F. Khaja et al., APL 2012

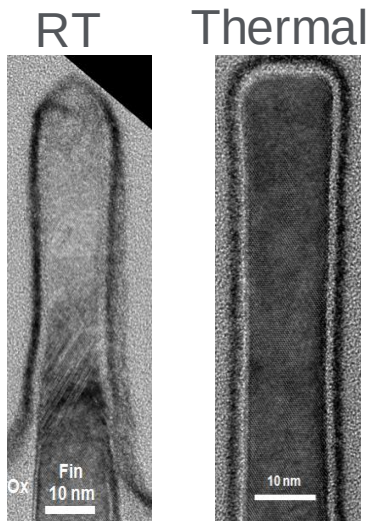
Cryo Implants Reduced EOR & Defects, Improved Activation, Yielded Better Silicidation, Less Variability, High Drive Current

Damage Engineering with Thermal Implants

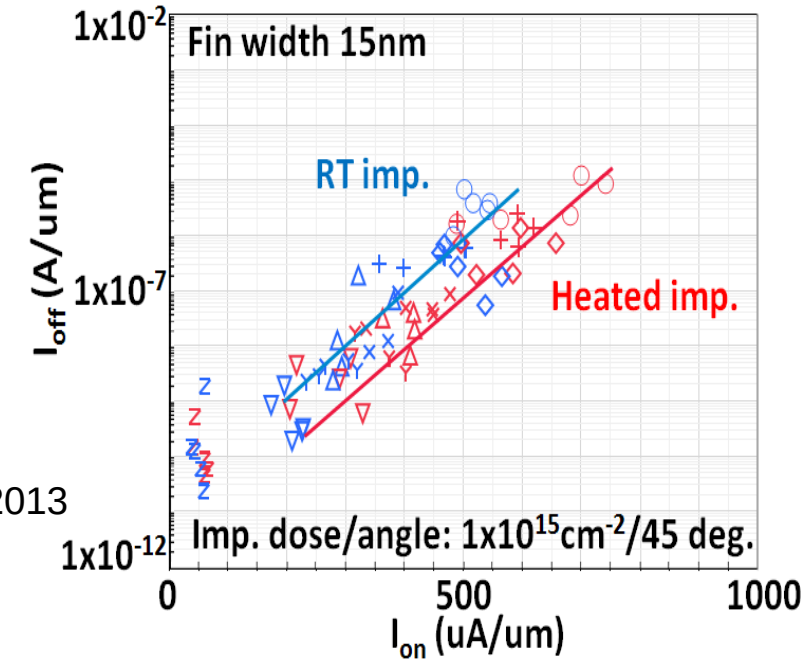
Physical Mechanism

- interstitials (I) and vacancies (V) form amorphous pockets (AP) when they are within a capture distance
- Amorphous pockets (Is-Vs clusters) evolve to form Amorphous layer
- I-V fast recombination (jump frequency↑ when T↑)





M. Togo et al., IMEC, VLSI 2013



M. Togo et al., IMEC, VLSI 2013

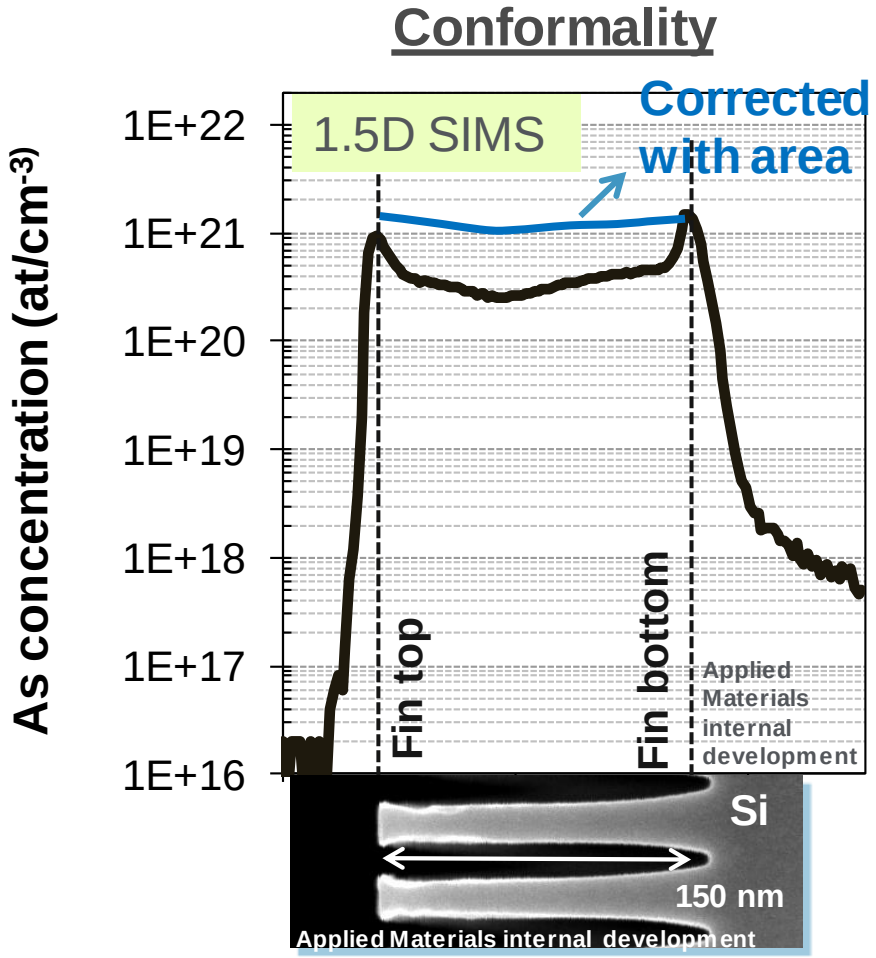
Hot implant reduces Amorphous Pocket Growth

Hot Implant enhances dynamic annealing

Thermal implant reduces Damage → Improve Device performance >15%

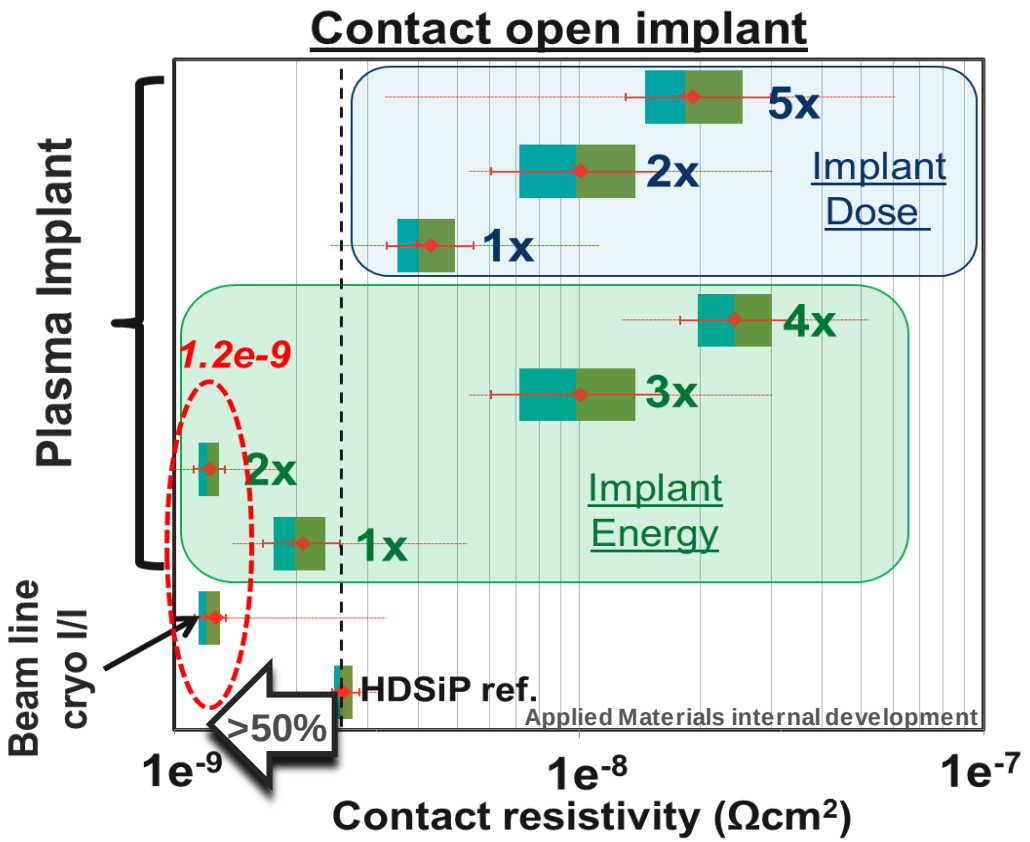
Thermal Implant Reduces Crystal Damage, Reduces Device Leakage

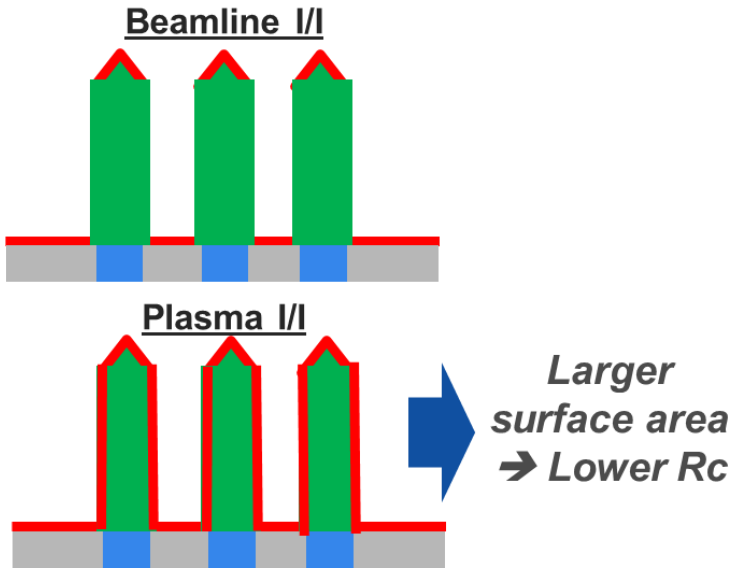
Plasma Doping: Shallow & Conformal Implant



Plasma doping enables high doping concentration on surface and is a promising enabler for conformal contact

Implant Effect to Rc on HDSiP





C.N.Ni et al., VLSI 2016

Plasma implant is a promising enabler for conformal contact

Outline

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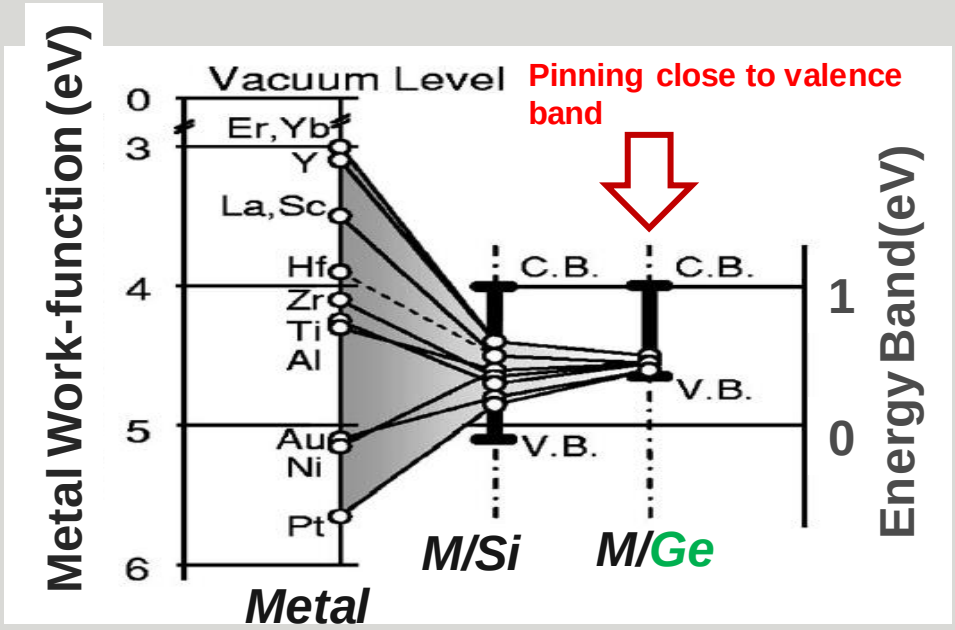
Ge-rich contact interface for PMOS ρc reduction

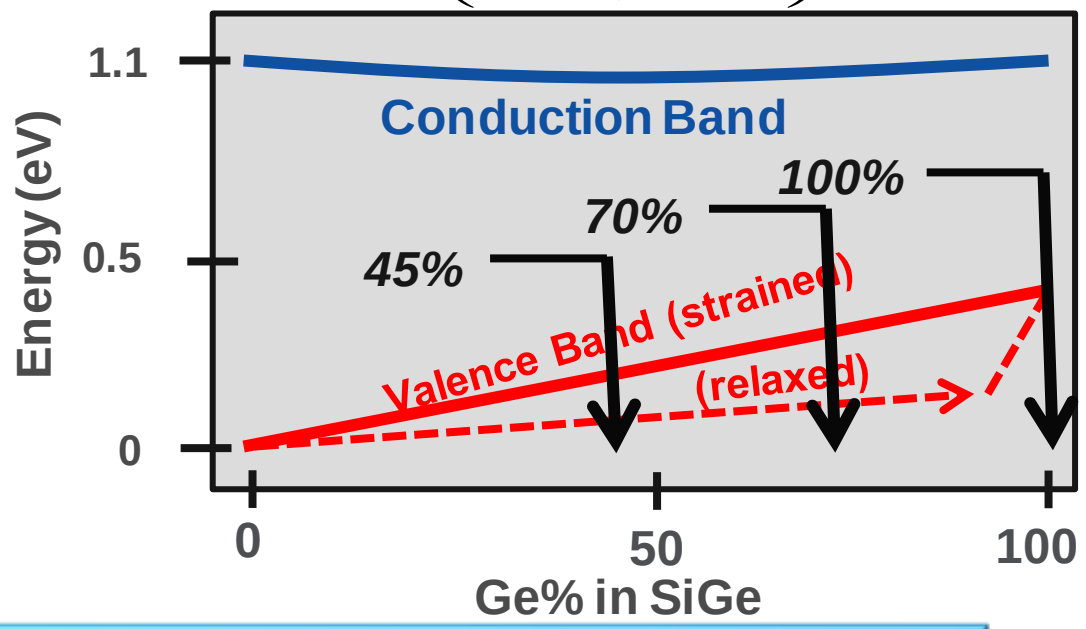
Band Gap Modulation by Ge in SiGe



Lower Rc (SBH, DSS)

- High Surface Doping
- Narrow Bandgap(Ge)

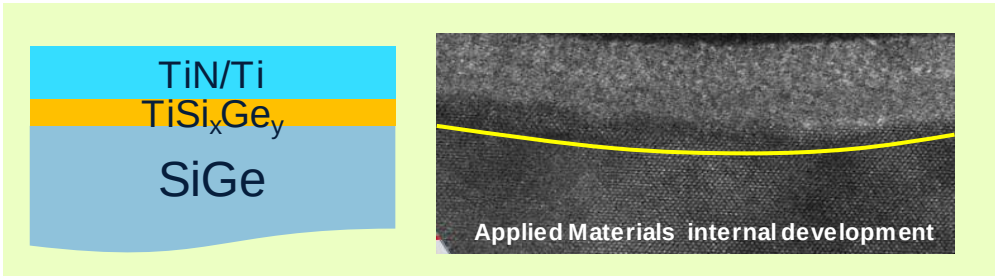
$$R_c = C_1 \exp\left(C_2 \frac{q\phi_B}{\sqrt{N_{if}}} \right) \times Area^{-1}$$

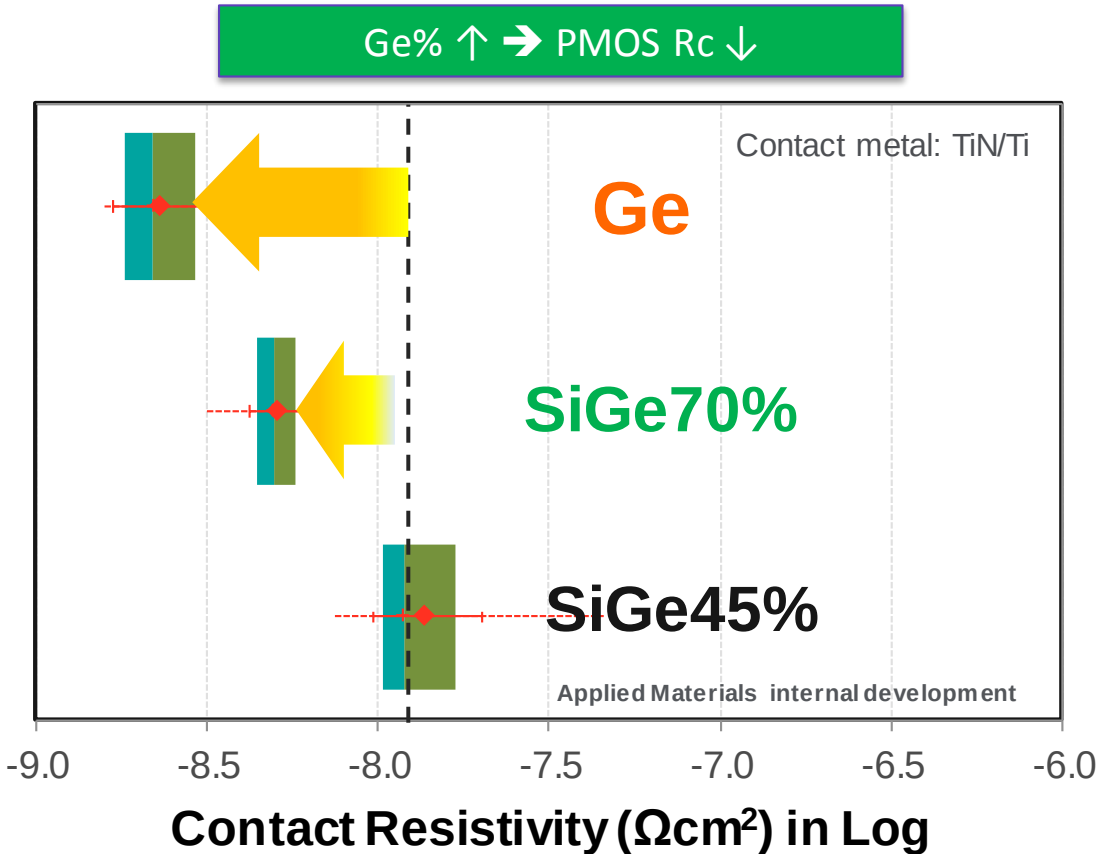


Ge% reduces PMOS contact SBH → PMOS ρc reduction

Contact Resistivity vs. Ge%

AMAT Ti/SiGe contact test vehicle





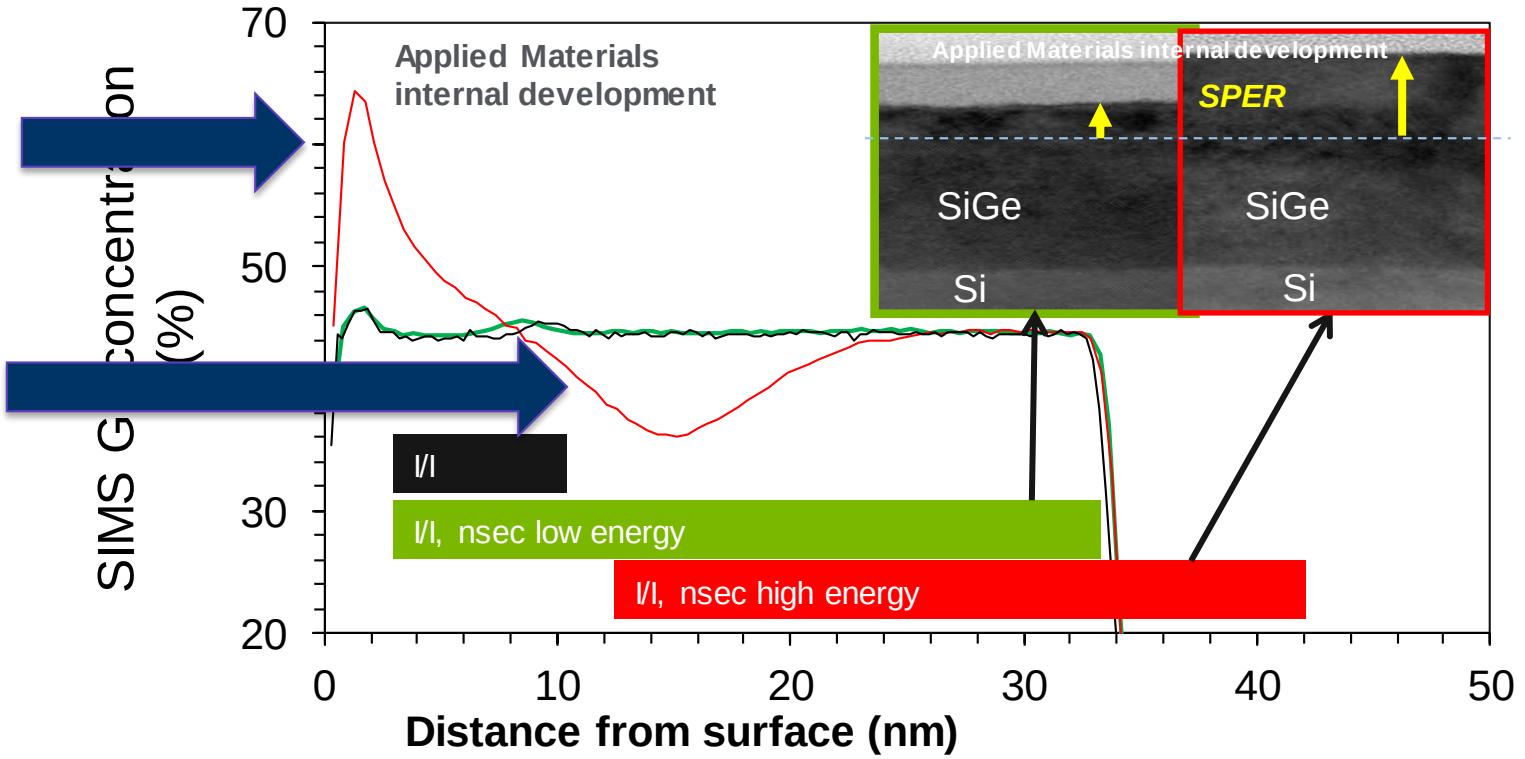
C.N.Ni et al., VLSI-TSA 2016

P contact ρc reduces with increase in Ge at contact.
ρ_c = 3e-9 Ωcm² with Ge:B PSD

Ge-rich Surface Formation by Nanosecond Laser Anneal

Ge segregation at surface

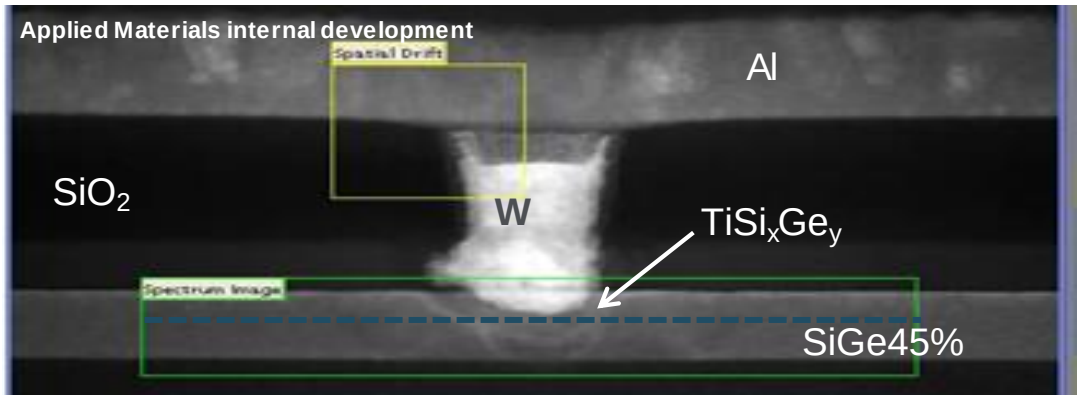
Ge depletion at bulk

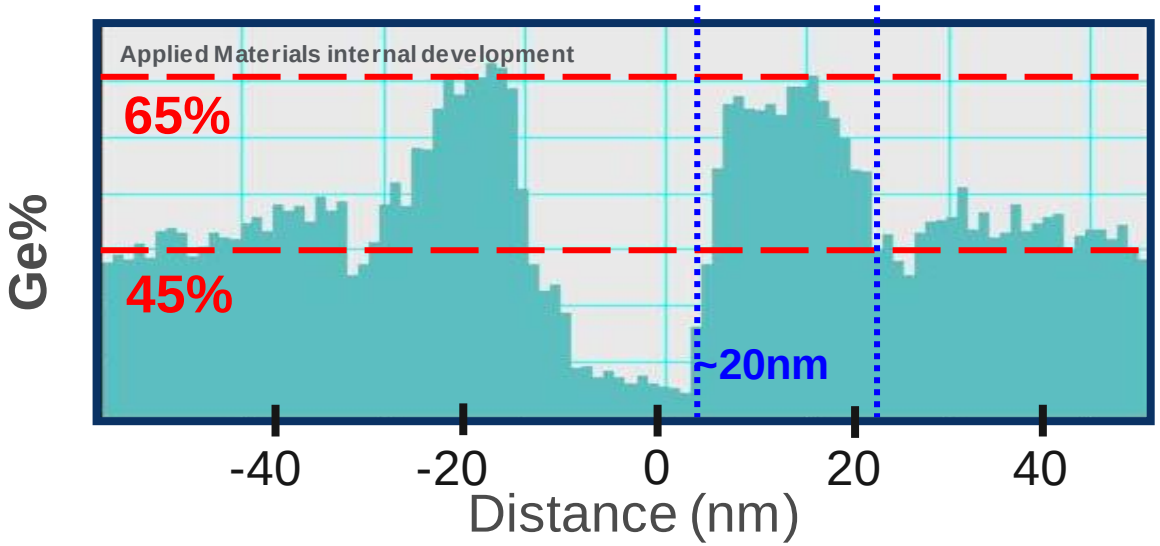


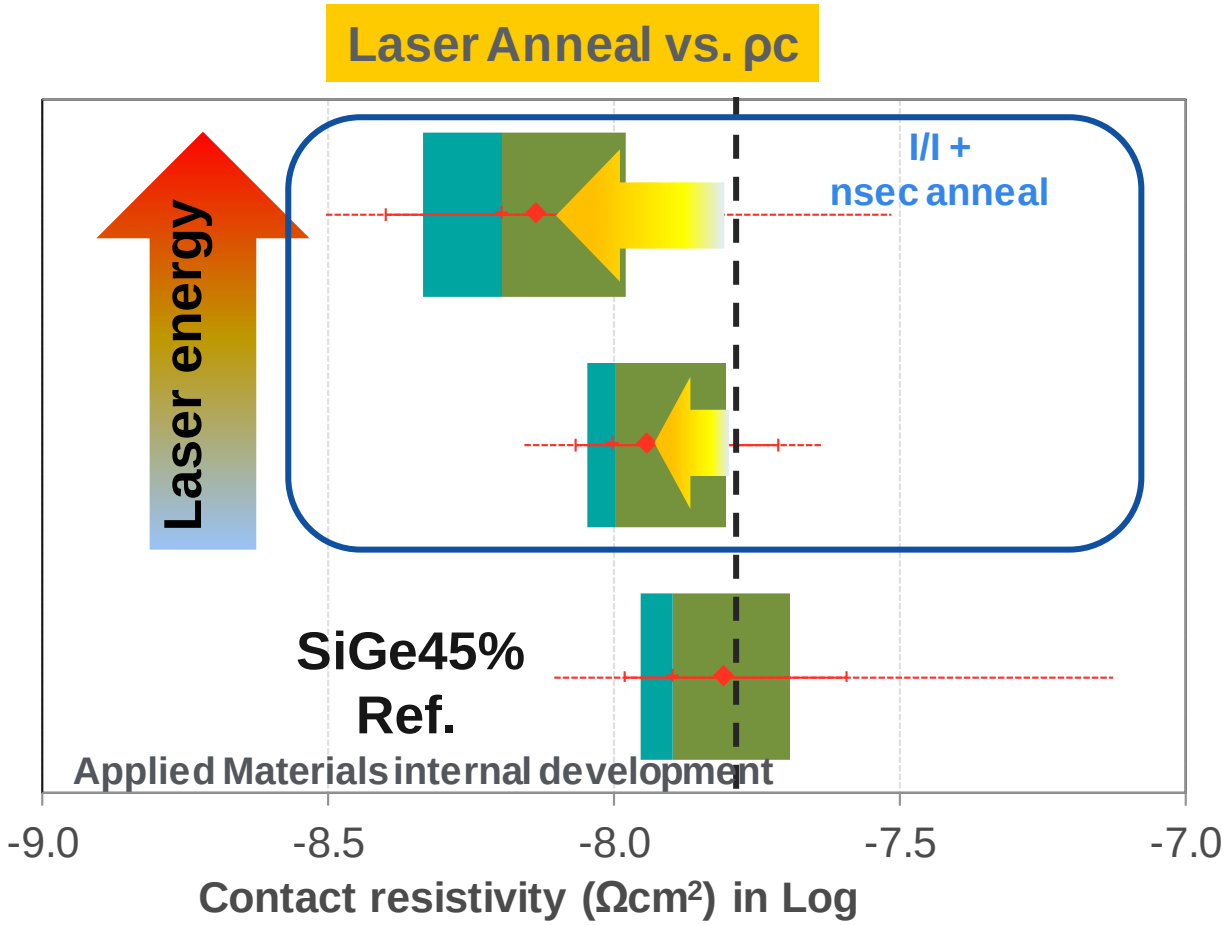
C.N.Ni et al., VLSI-TSA 2016

Ge is segregated towards SiGe surface with Implant + NLA

Ge Segregation by Nanosecond Laser Anneal





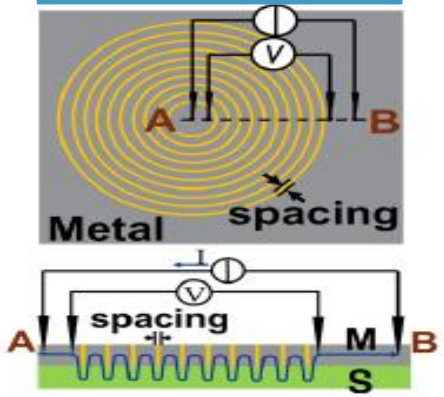


C.N.Ni et al., VLSI-TSA 2016

Localized Ge segregation by nsec laser anneal → 35% of ρc improvement

$Si_{0.3}Ge_{0.7}$:B Ultralow Contact Resistivity By Nanosecond Laser Anneal

Test Structure



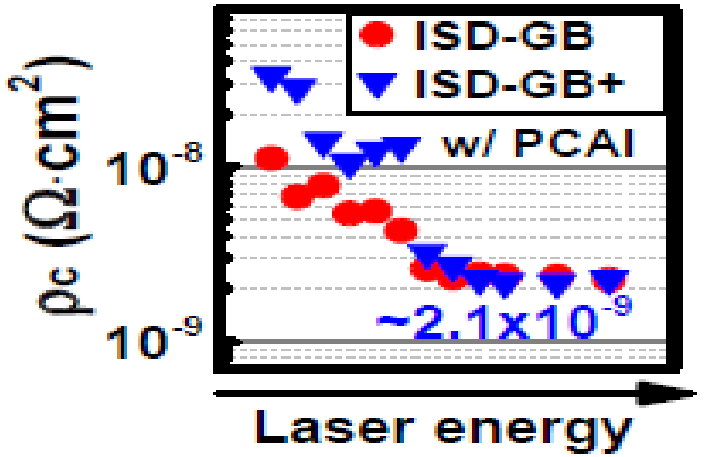
H.Yu et al., VLSI 2016

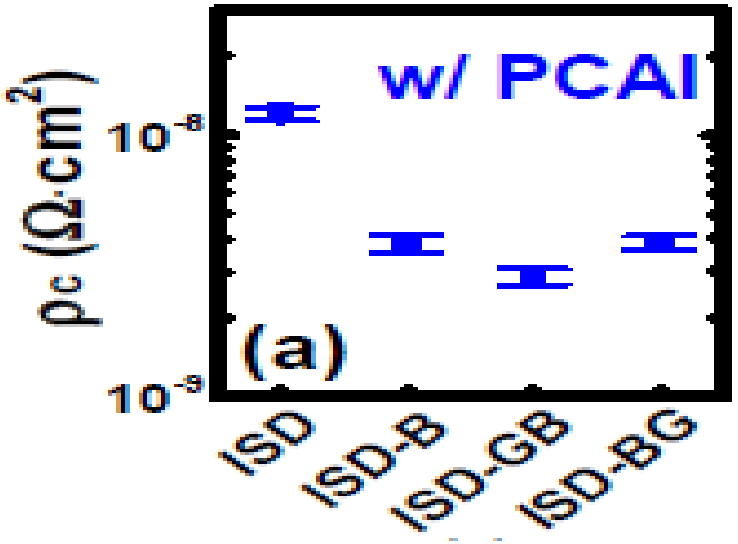
Process Flow

- 300mm lightly doped Si wafer
- n-well formation
- SiGe:B epitaxy
- B I/I & activation
- MR-CTLM patterning:Dielectric deposition, lithography, and etching (SiGe surface at the contact region exposed)
- PCAI with Ge I/I
- Ti/TiN deposition
- PMA with 1min N_2 RTP
- Cu barrier deposition
- Cu plating and CMP

Results

Sample ID	B I/I dose (cm^{-2})*
ISD	--
ISD-B	$3\times10^{15}+2\times10^{15}$
ISD-GB	$3\times10^{15}+2\times10^{15}$
ISD-BG	$3\times10^{15}+2\times10^{15}$
ISD-GB+	$6\times10^{15}+2\times10^{15}$

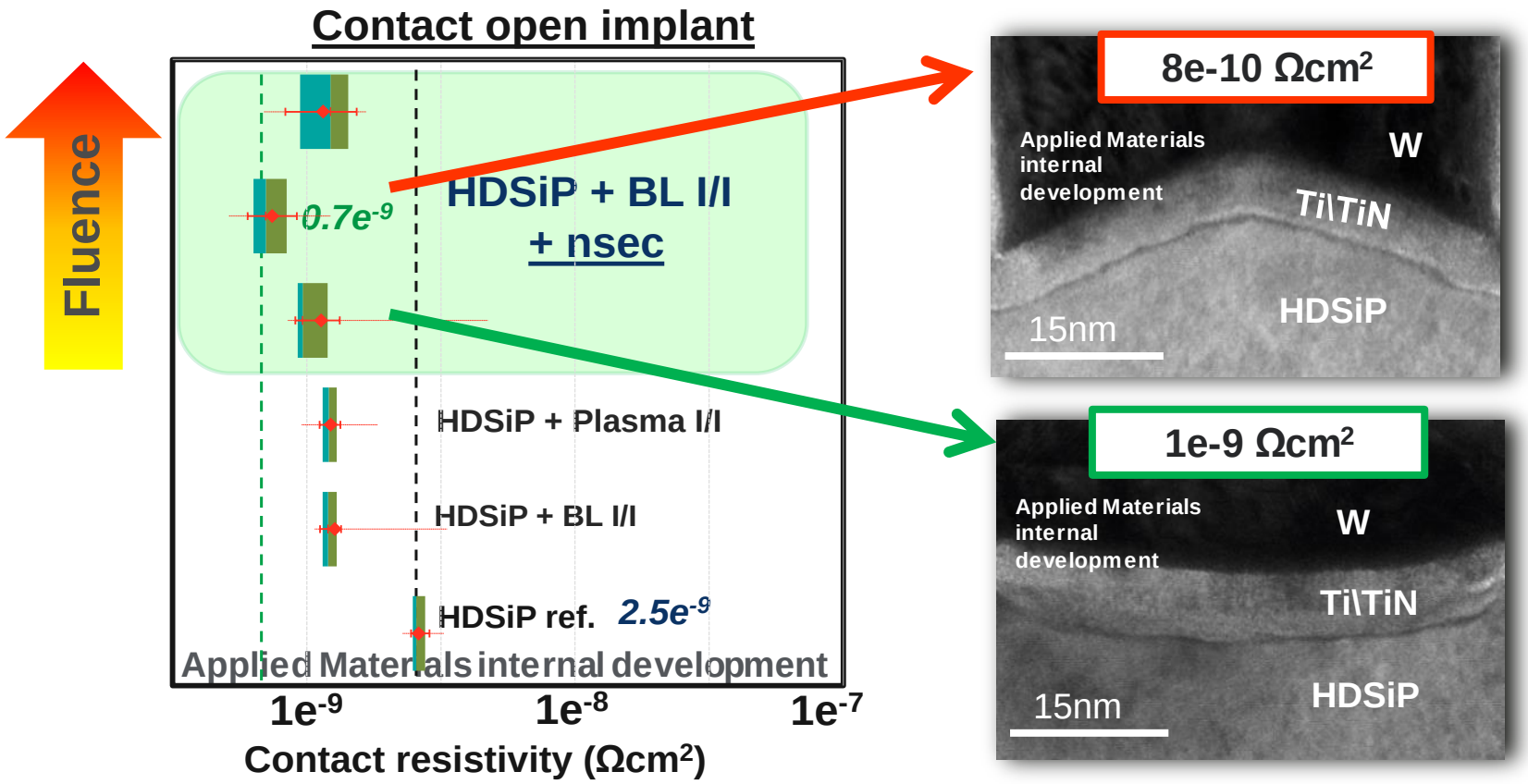




H.Yu et al., VLSI 2016

Optimization of Implant and nanosecond laser anneal resulted in ρc: ~2×10-9 Ω·cm²

Super-activation with Post Implant Nanosecond Anneal



C.N.Ni et al., VLSI 2016

Post implant nsec laser anneal brings NMOS to 1x10^{-9} Ωcm^2

Outline

- Motivation for Contact Resistivity (ρc) Reduction
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Summary

- **Implant and Anneal optimization is required for achieving low ρ_C**
  - Implant defect recovery is the key for low contact resistance
  - Plasma implant offers shallow/dopant-rich implanted surface and improved conformality

- **PMOS ρc:**
  - Ge-rich contact interface benefits to PMOS Rc, with 3e-9 Ωcm^2 achieved with pure Ge (B@1e20 at/cm^3)
  - nsec laser anneal after amorphization implant effectively segregates Ge towards SiGe surface

- **NMOS ρc:**
  - Pathways for further ρ_C reduction to < $1x10^{-9}$ Ωcm^2 and below is adding/optimizing post implant nsec laser anneal


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