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Moore's Law Continues into the 1x-nm Era

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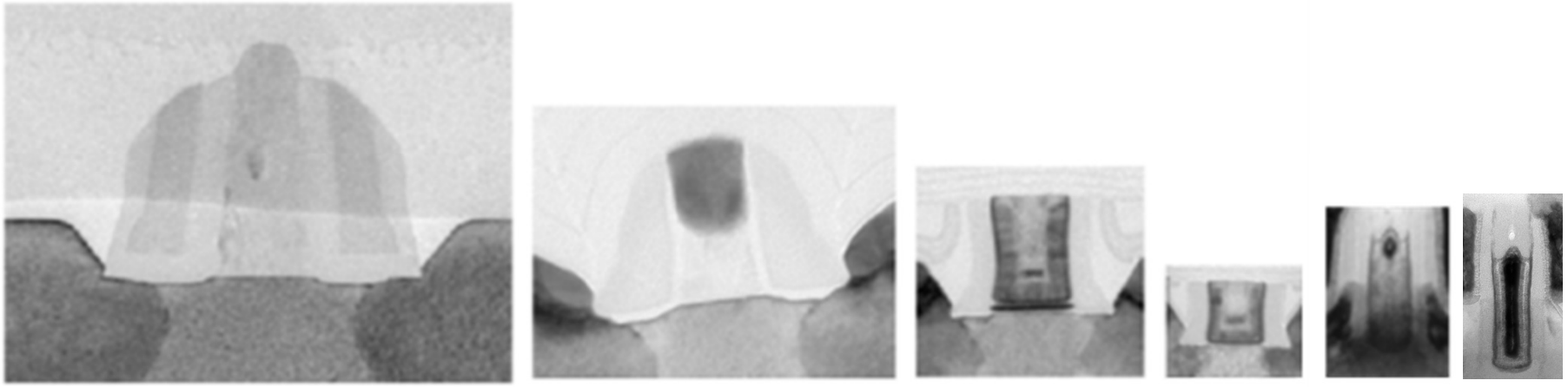
NCCAVS JTG User Group Meeting SemiconWest July 14, 2016

The Last Few Generations



Litho 248 nm → 193 nm dry → 193 nm wet → DP

Low-k dielectrics 1st gen → 2nd gen → 3rd gen →

Strained channels →

High-k, metal-gate →

FinFET

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Introduction

- Planar transistor high-k, metal-gate (HKMG) parts are in volume production down to the 20-nm generation, in gate-first and gate-last technologies
- HKMG tri-gate (finFET) devices are now also manufactured in high volume, in CPU and SoC formats
- Let's look at some!

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Qualcomm MDM9235 (TSMC 20 nm HPM HKMG Process)

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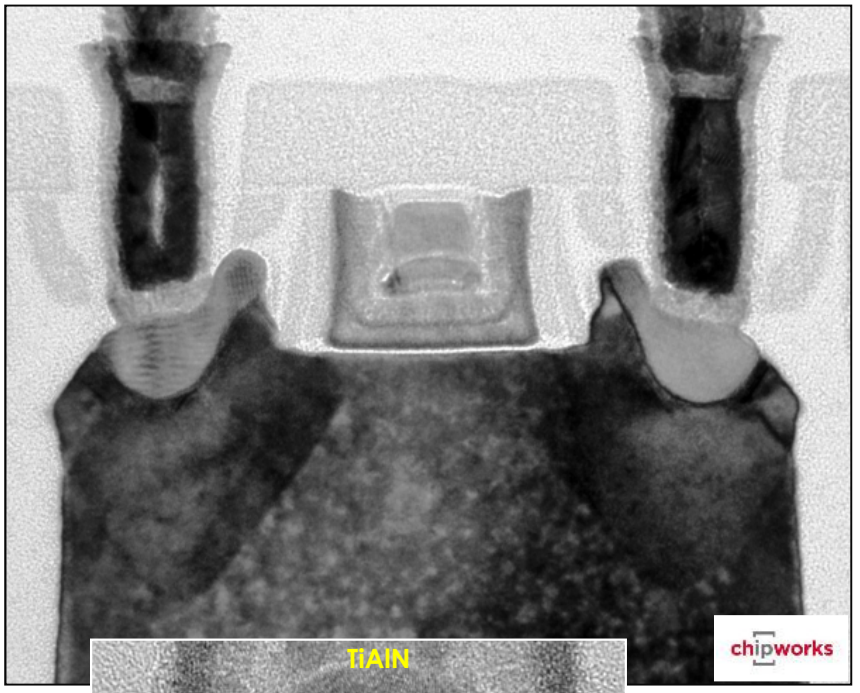
20HPM PMOS Transistors

- Second-generation HKMG process – hi-k formed after polySi removal (like Intel 32-nm)
- PMOS gate stack formed before NMOS
- Contacted gate pitch (CGP) ~90 nm
- Minimum observed gate length (MOL_g) ~28 nm,
- T_{ox} ~1.4 nm, t_{hi-k} ~1.3 nm – cf 28HP t_{ox} 1.4 nm, 28 HPM 1.5 nm, 28HPL 2.0 nm
- Work-function materials similar to 28-nm process – PMOS is TiN
- Raised source/drain epi with e-SiGe, graded -> ~40% Ge



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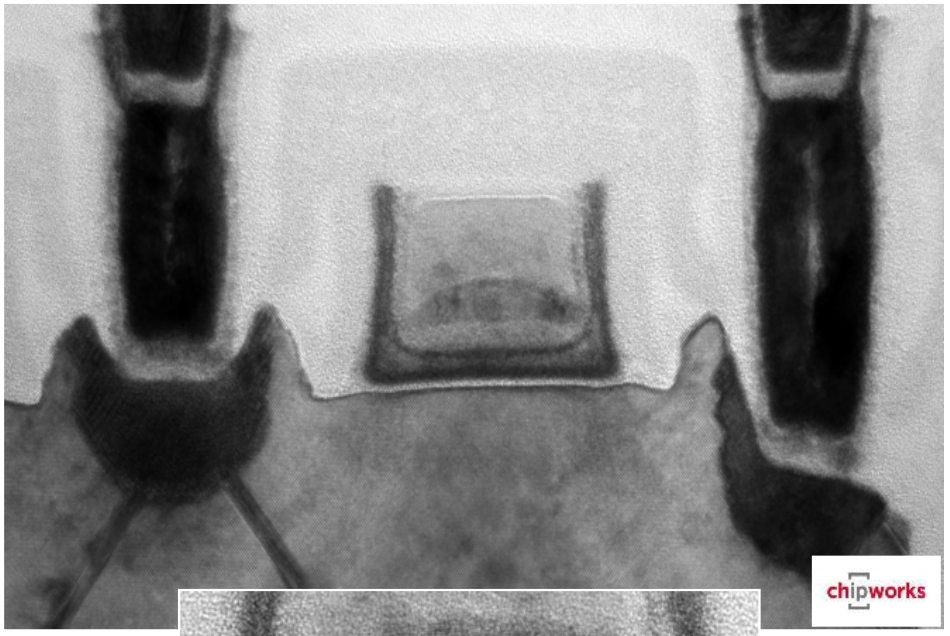
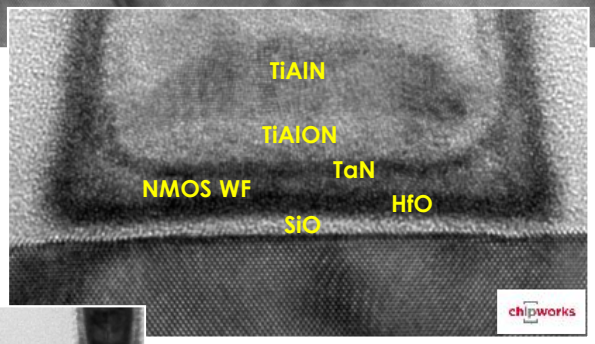
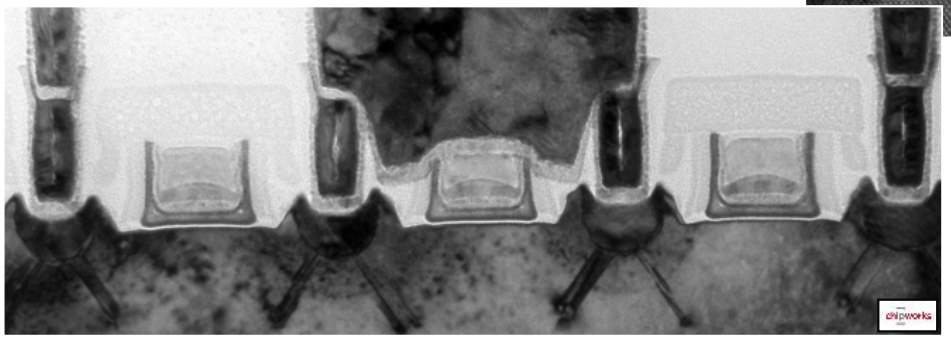
20HPM NMOS Transistors

- Minimum observed gate length 31 nm
- Raised source/drains, stacking faults for stress (like Intel 32-nm)
- TiAlN work-function material, similar to 28-nm process
- <110> channel
- AlCoCu gate fill with AlO cap







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Samsung Exynos 5430 (20 nm Gate-Last HKMG Process)

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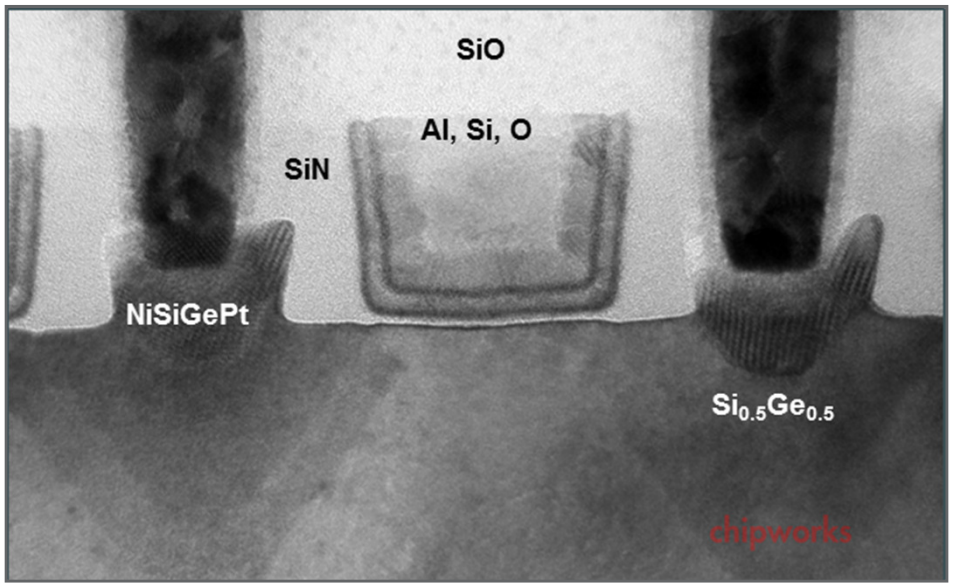
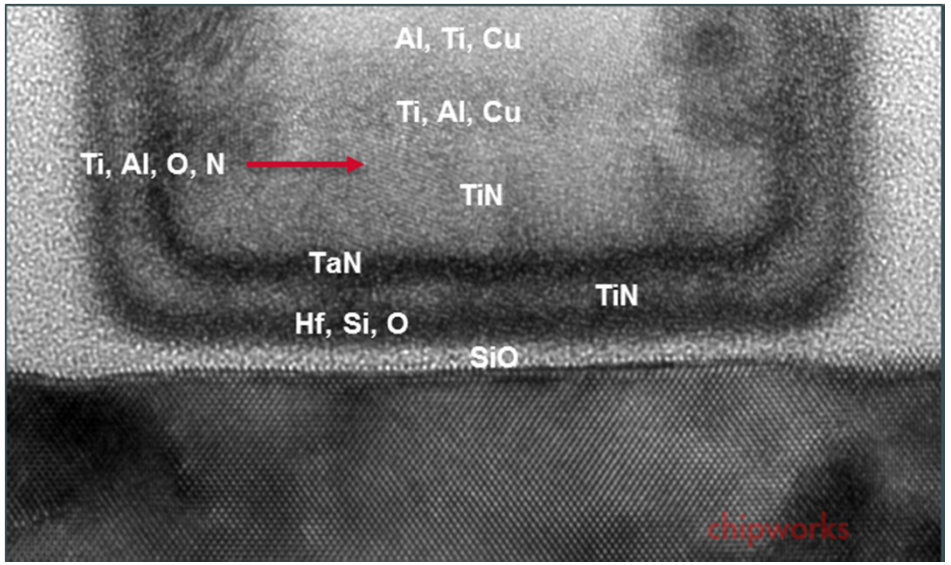
Samsung 20 nm PMOS Transistors

- Samsung's 1st generation gate-last, replacement gate HKMG process
  - High-k formed after polySi removal
- 193 nm immersion lithography
- PMOS e-SiGe graded to ~50%.
- T_{ox} ~1.7 nm, t_{hi-k} ~1.4 nm
- Work-function materials similar to Intel/TSMC processes – PMOS is TiN





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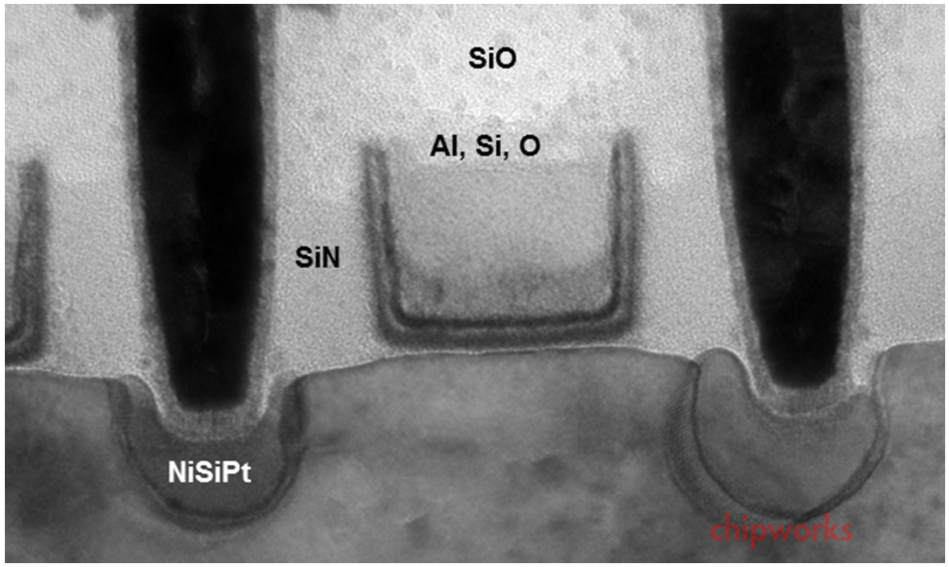
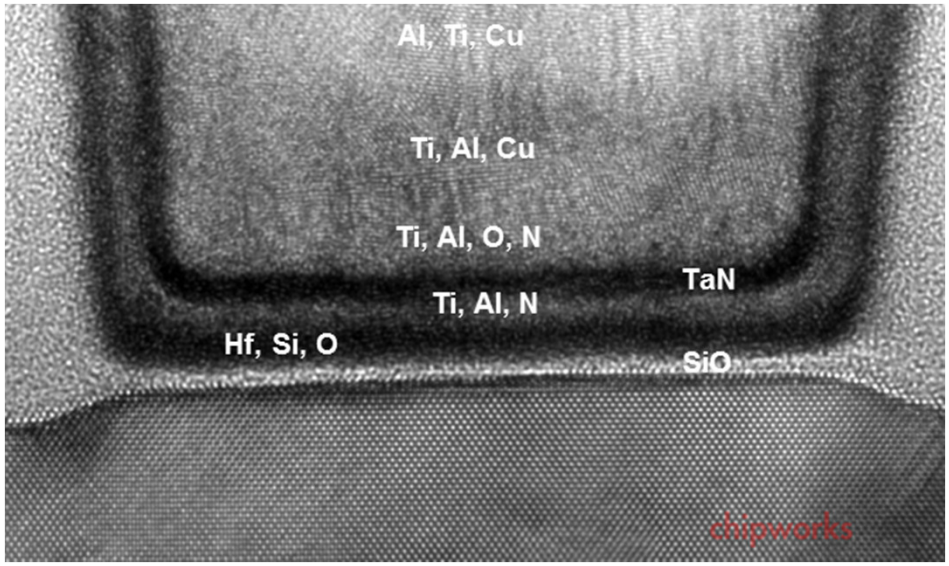
Samsung 20 nm NMOS Transistors

- Contacted logic gate pitch 90 nm
- Minimum metal pitch 80 nm
- Minimum observed gate length ~30 nm
- T_{ox} ~1.7 nm, t_{hi-k} ~1.0 nm
- Work-function materials similar to Intel/TSMC processes – NMOS is TiAlN





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IBM POWER 8 Server Processor (22 nm SOI Gate-First HKMG Process)

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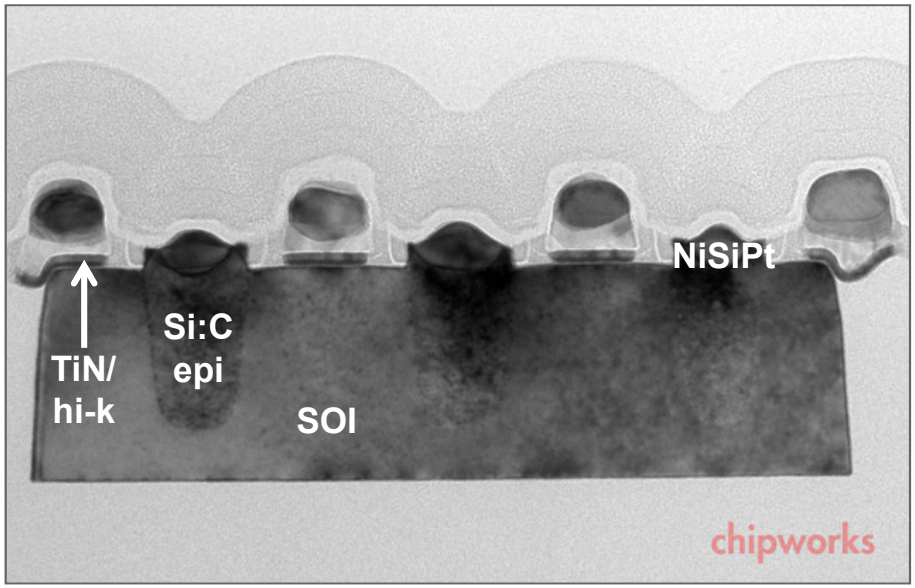
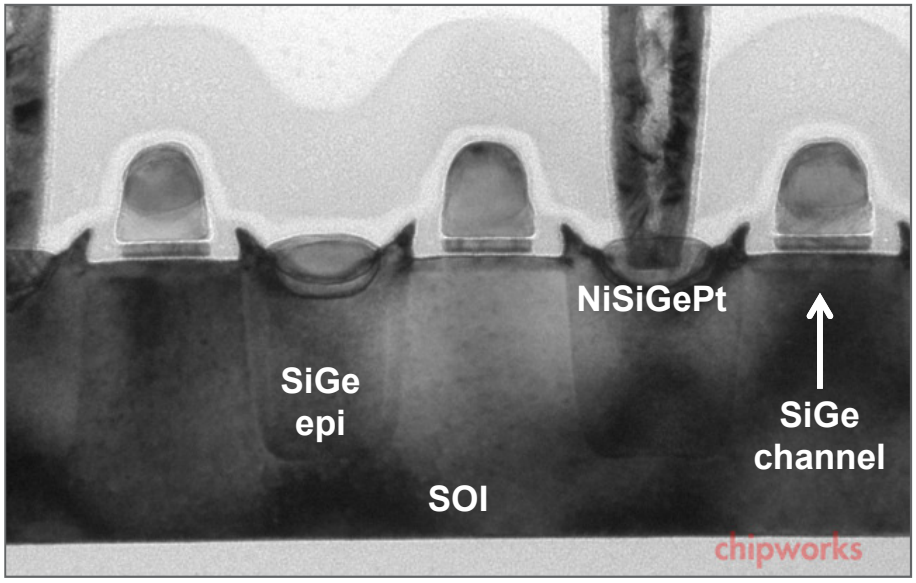
IBM/GF 22HP Transistors

- TiN metal layer under polysilicon gate, CGP ~98 nm, t_{ox} ~1.0 nm, t_{hi-k} ~1.3 nm
- SOI layer ~82 nm thick
- PMOS e-SiGe source/drain (S/D), Ge graded -> 30% Ge
- PMOS e-SiGe channel -> 25% Ge
- NMOS e-Si S/D tubs (claimed eSi:C[1,2]), also doped with 2% Ge (likely for stress relaxation or to control phosphorus out-diffusion)
- Aluminum on hafnium-based gate dielectric to adjust WF in PMOS, likely lanthanum for NMOS
- NiPt-silicided S/D and gate
- Raised S/D in both NMOS and PMOS
- Dual stress liner





[1] "22nm High-performance SOI technology featuring dual-embedded stressors, Epi-Plate High-K deep-trench embedded DRAM and self-aligned Via 15LM BEOL", Narasimha, S., et al., IEDM 2012.

[2] "Performance-optimized gate-first 22-nm SOI technology with embedded DRAM.", Freeman, G., et al. *IBM Journal of Research and Development* 59.1 (2015): 5-1.

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Analyzing finFETs – TEM sample artefacts

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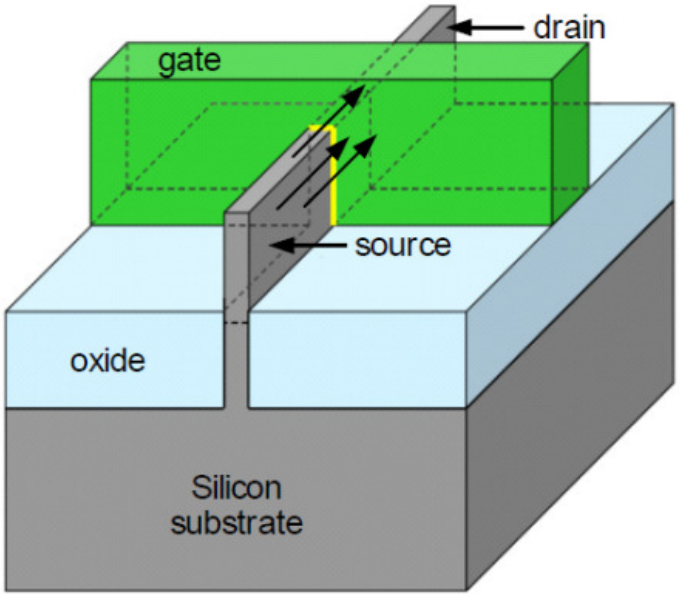
TEM Sample Artefacts



Intel tri-gate schematic

- TEM images *through* a thin sliver of sample material
- Typical TEM sample thickness 30 – 100 nm
- CGP → 70 nm, Lg ~20 - 30 nm, fin width 5 – 15 nm
- Almost inevitably get more than one feature in depth of sample

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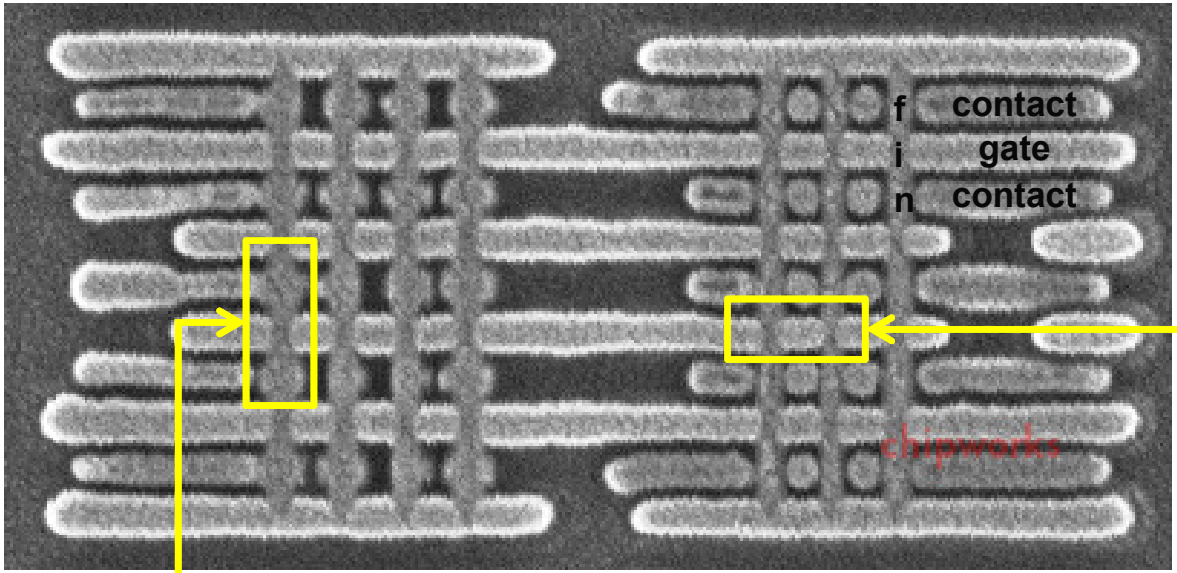
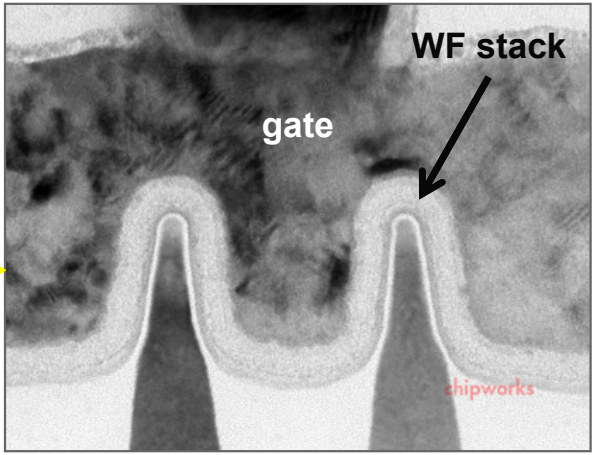
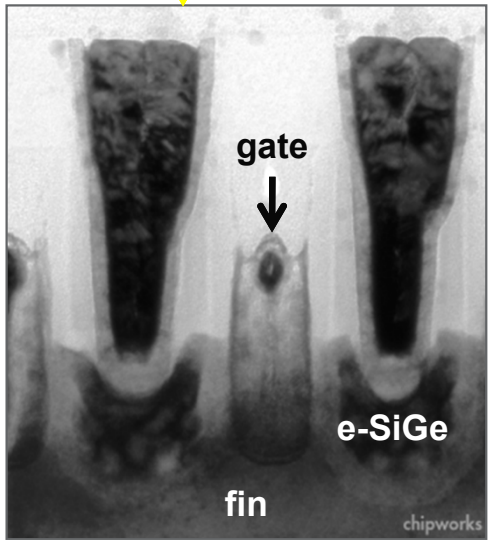
TEM Sample Artefacts

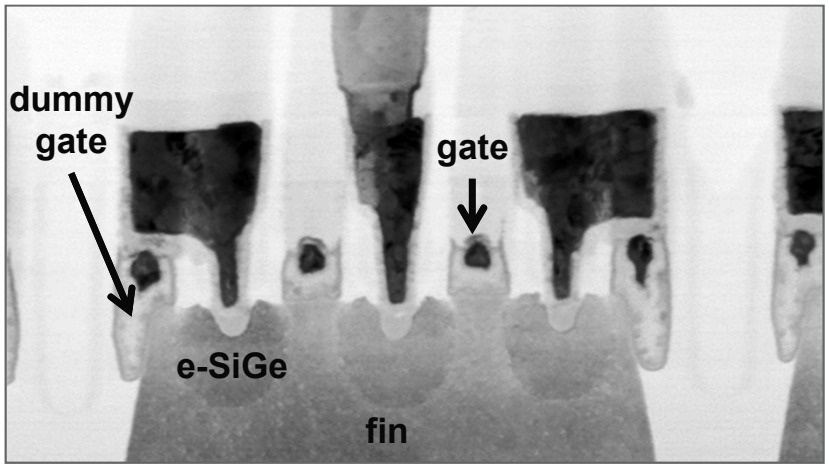
Intel 22 nm finFETs – plan view SEM image







10-nm thick PMOS sample



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Intel Broadwell (14 nm HKMG finFET Process)

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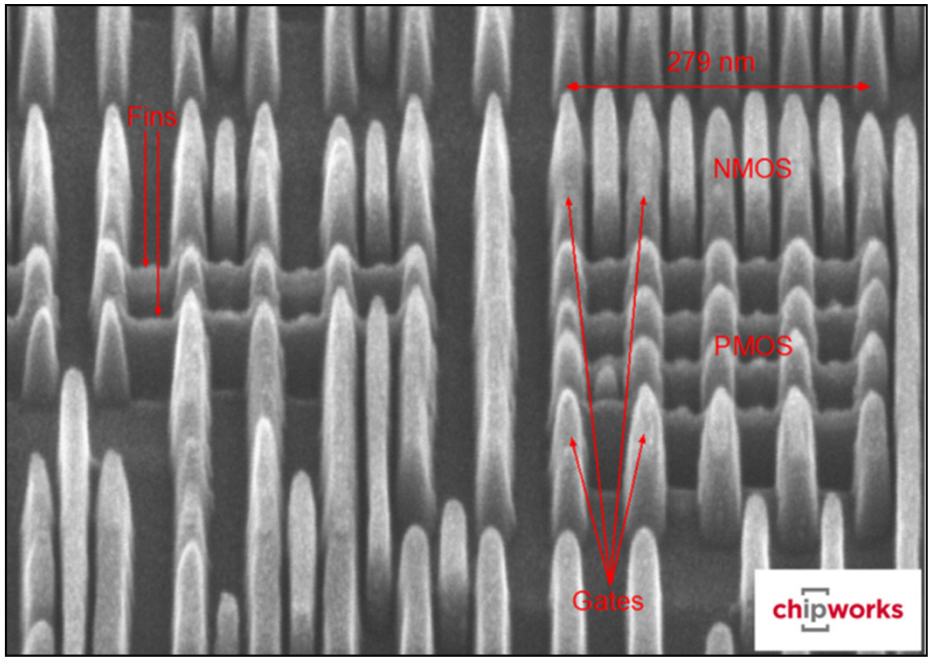
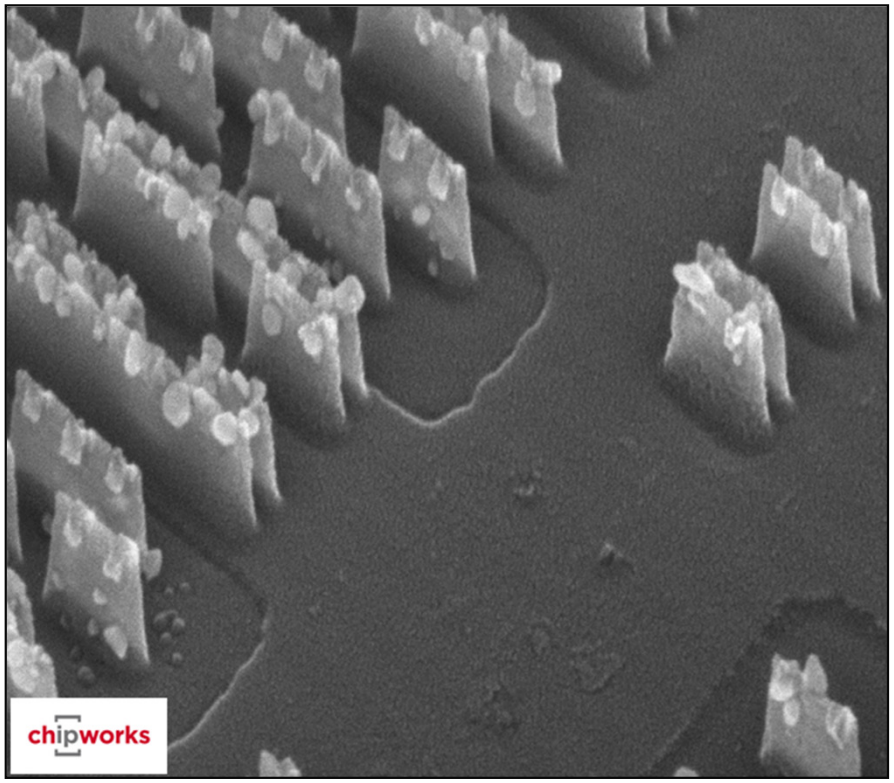
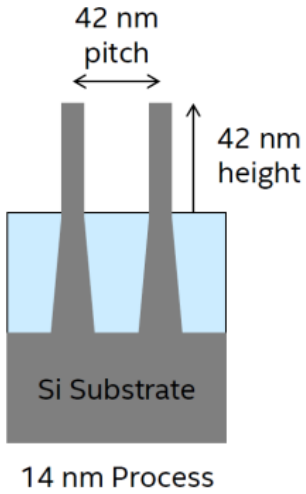
Intel 14-nm Broadwell



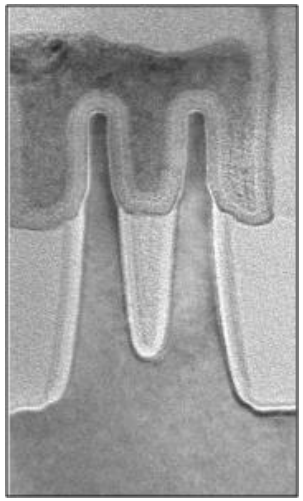
Etched back to STI



Etched back to substrate



14 nm Process



Source: Intel

- Contacted gate pitch ~70 nm
- Nominal fin pitch ~42 nm

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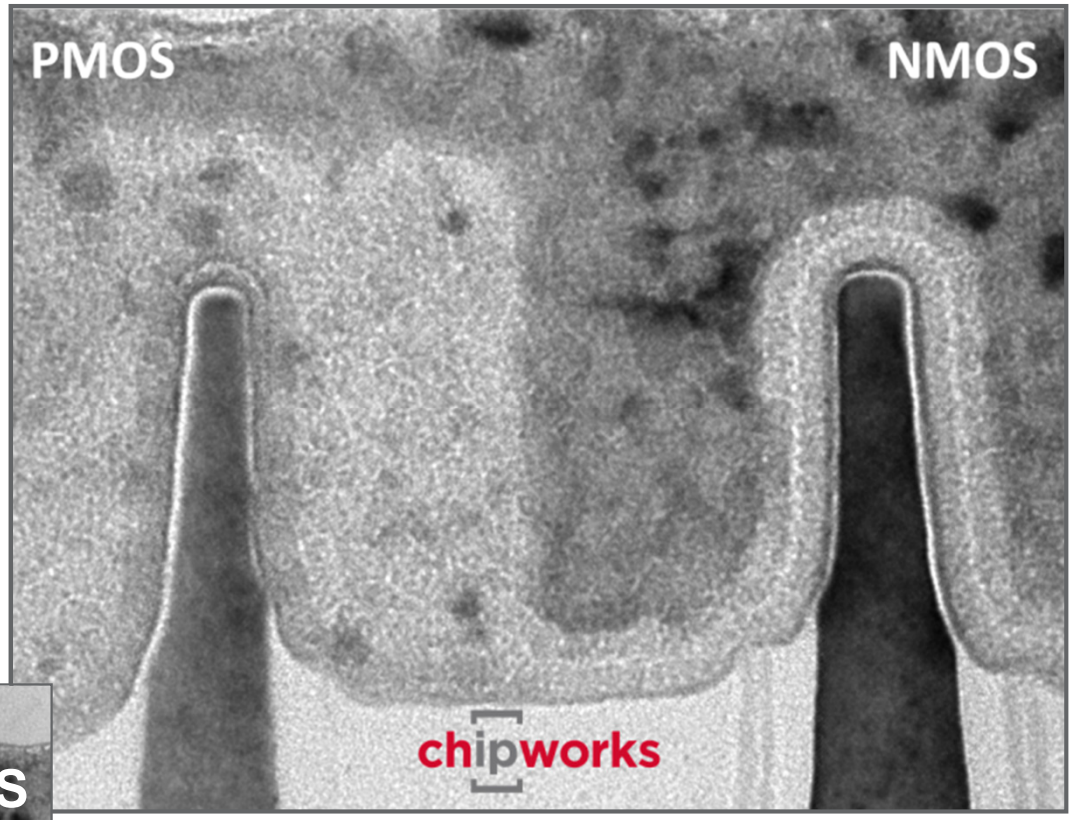
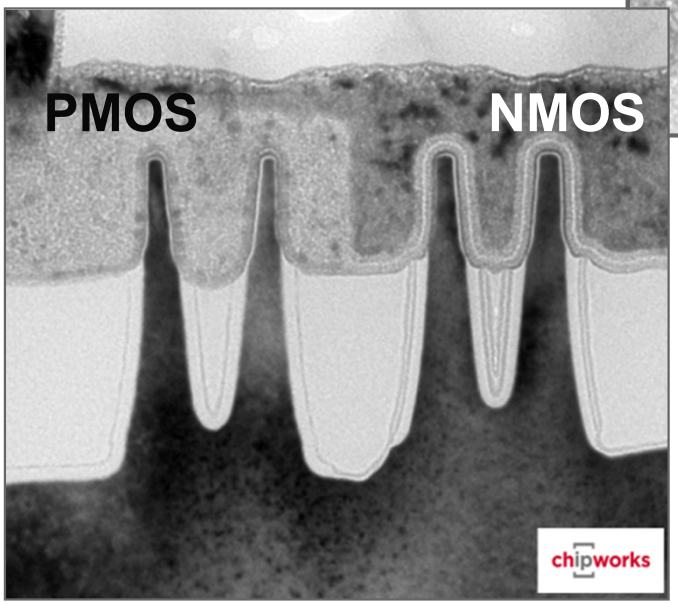
Intel 14-nm Broadwell

- Vertical fins! But still rounded fin tops.
- Multiple steps to achieve fin profiles after fin etch, fin width 7 – 11 nm
- Functional fin height ~37 – 40 nm, gate wrap-around ~85 nm, effective gate width for single-fin transistor.





- Asymmetric stress deforms fins
  - Leftmost fin leans left
  - Rightmost fin leans right

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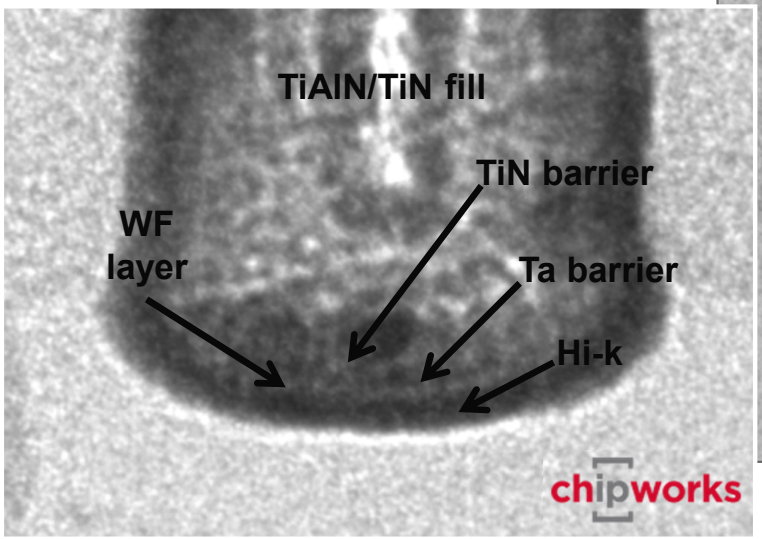
Intel 14-nm – PMOS Gates

- MOLg ~22 nm, PMOS gates formed first
- TiN WF material, t_{ox}, t_{hi-k} ~1.0 – 1.2 nm
- Epi SiGe in source-drains, isotropic cavity etch
- Gates back-etched and filled with dielectric, allows self-aligned contacts



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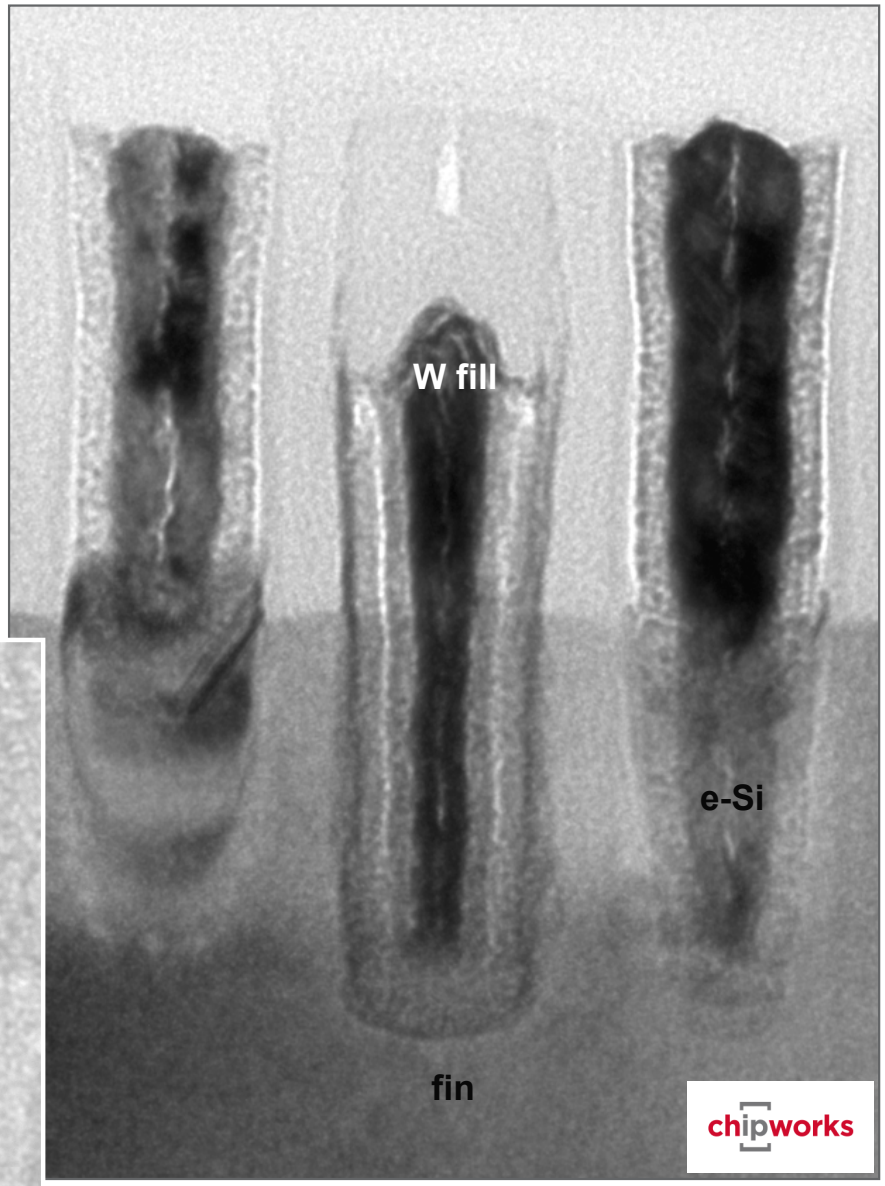
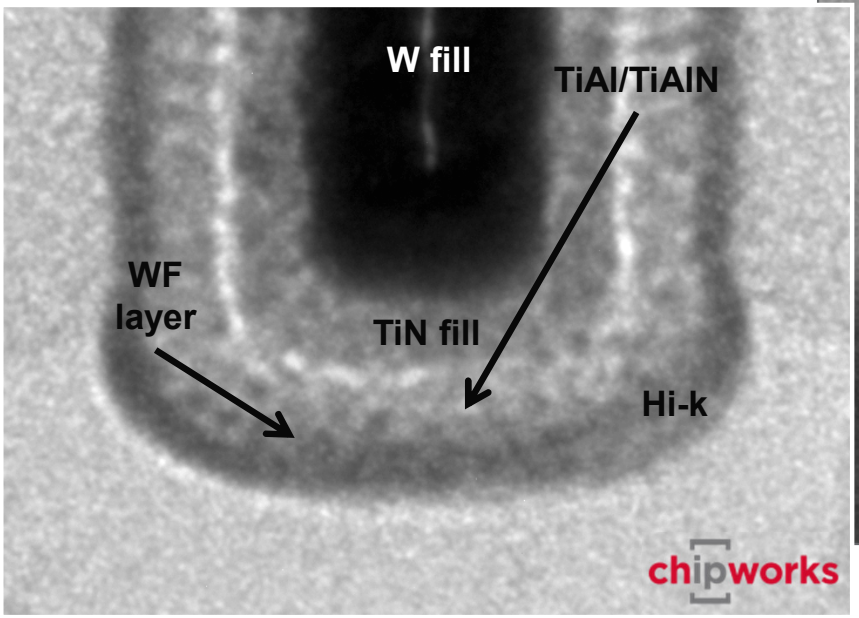
Intel 14-nm – NMOS Gates

- TiAlN WF material, t_{ox} ~1.1 nm, t_{hi-k} ~1.2 nm
- Epi SiGe in source-drains, isotropic cavity etch
- Ti silicide, not Ni
- Gates back-etched and filled with dielectric, allows self-aligned contacts





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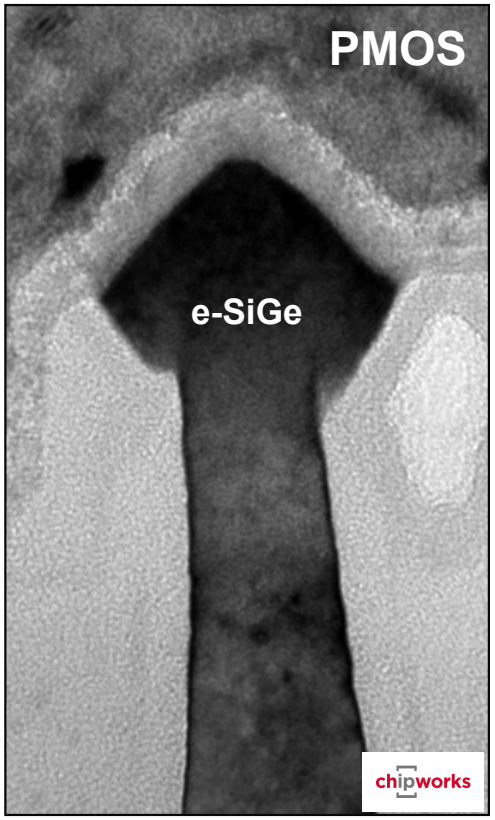
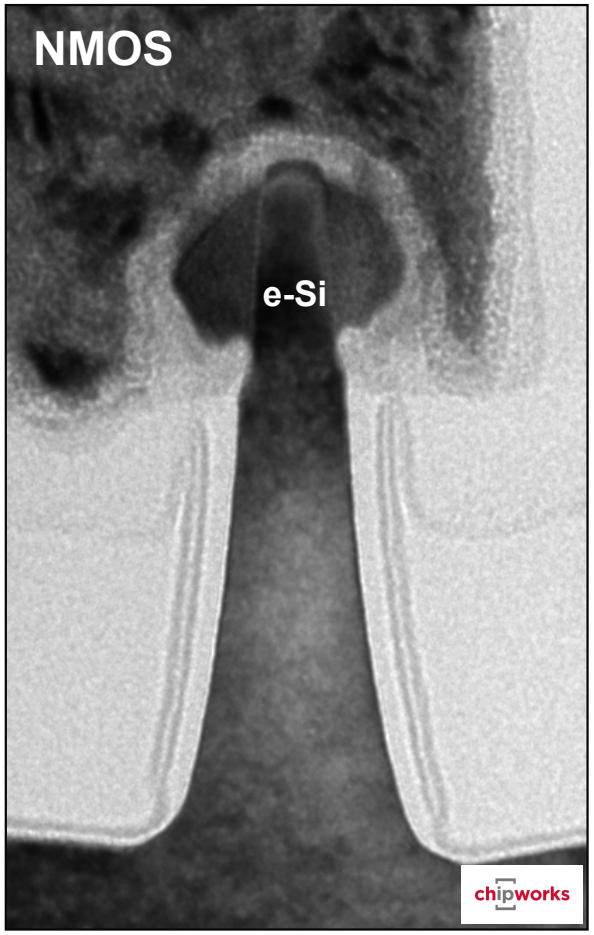
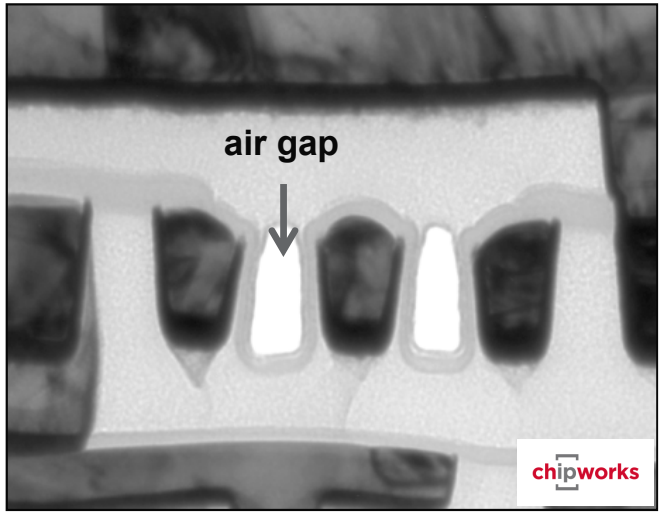
Intel 14-nm – Source/Drains

- PMOS epi-SiGe takes <111> planes as in 22-nm
- NMOS epi takes <111> planes at base
  - Cavity etch used
- SWS etched before S/D epi growth in PMOS and NMOS
- And.. here be airgaps!







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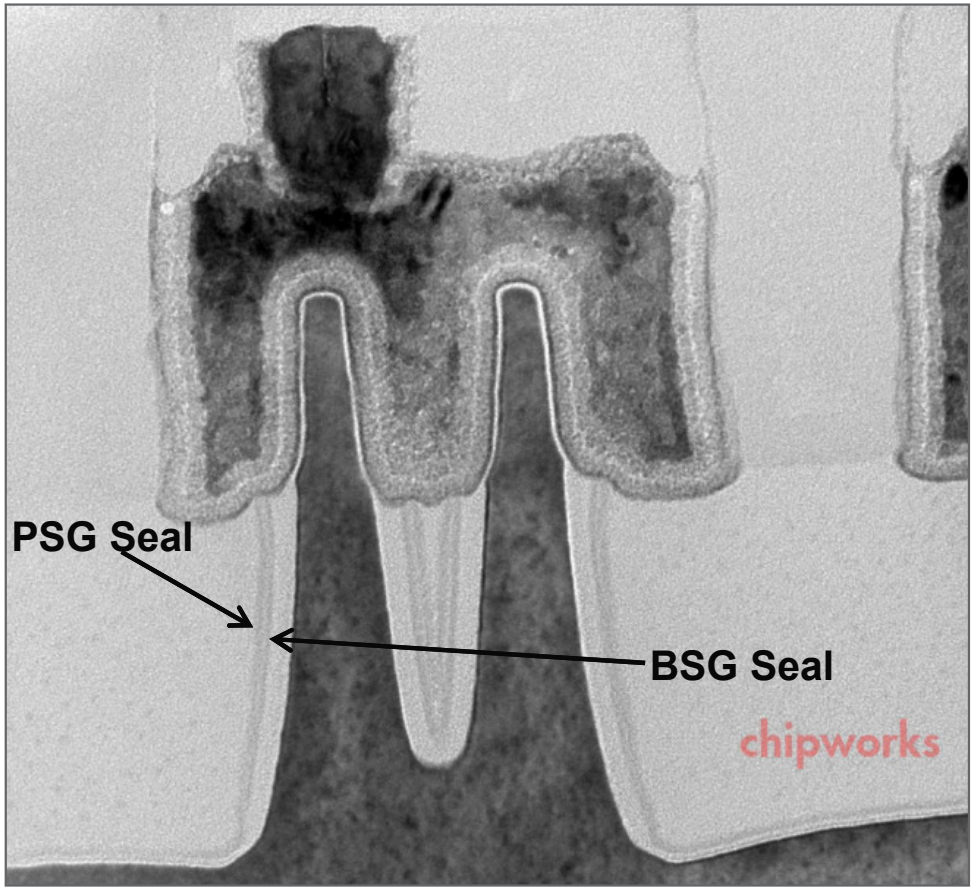
Intel Solid-Source Diffusion Punchstopper



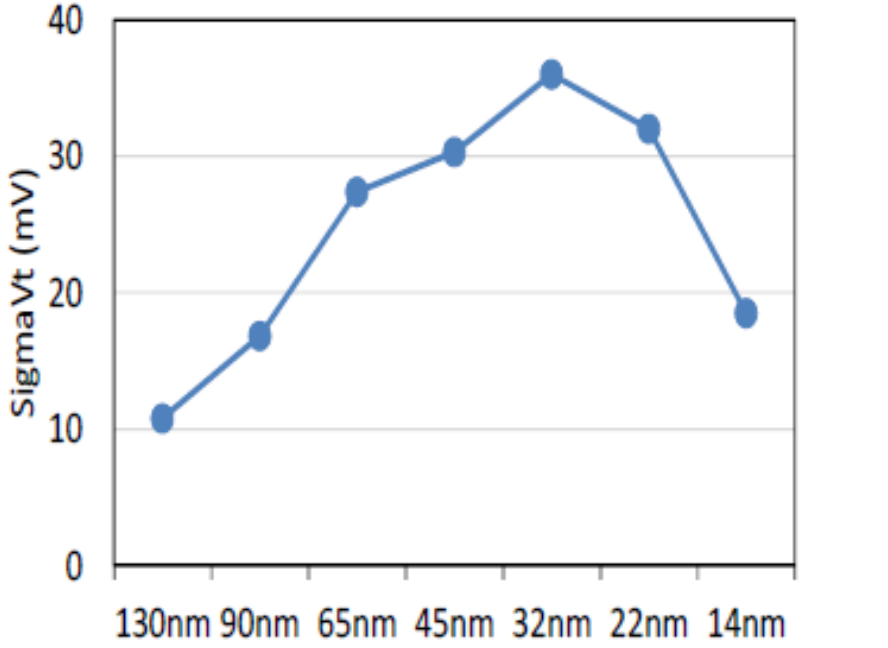


Figure 7: Random Varation Trend (σVt)

[3] Natarajan, et al. "A 14nm Logic Technology Featuring 2nd-Generation FinFET , Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 µm2 SRAM cell size", IEDM 2014

- Intel solved one of the biggest problems with bulk FinFETs, putting in a self-aligned punchstop
- Allows a bulk FinFET to be undoped, assuming multi-WF RMG
- Reduces random doping variation

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Intel 14 nm Atom "Cherrytrail" SoC

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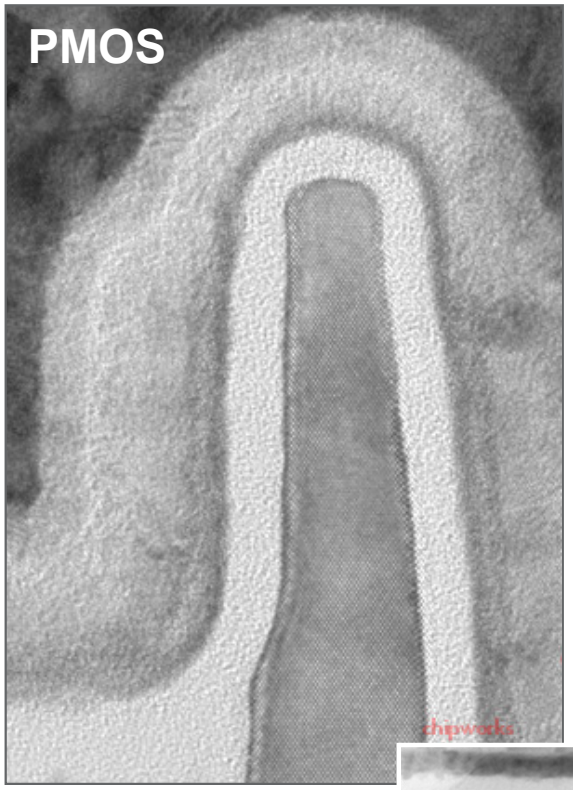
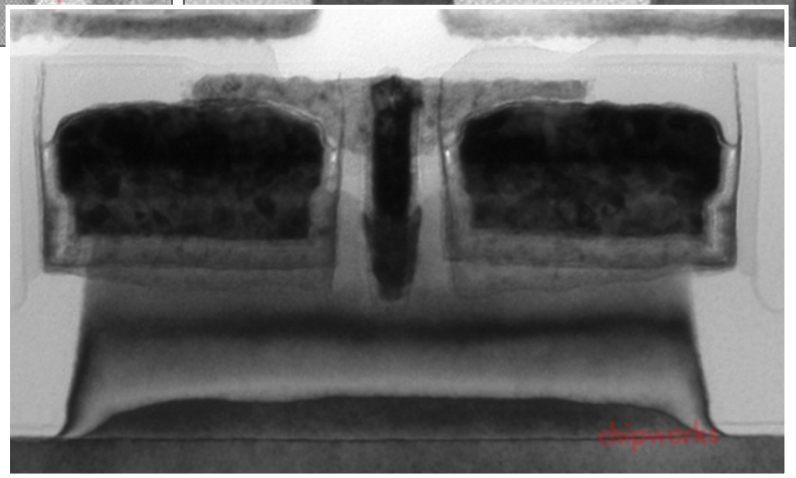
Intel 14 nm Atom "Cherrytrail" SoC

- Logic transistors same as Broadwell microprocessor
- HV MOS similar fins and 42 nm pitch with nearly vertical sidewalls and almost flat top as LV MOS.
- HV CGP ~220 nm, 150 nm gate length transistors
- Thicker t_{ox} (4.0 nm – 4.5 nm), same gate stack
- Merged SiGe epi and unmerged Si epi
- Similar passives to 22-nm SoC





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Samsung Exynos 7420 (14 nm Gate-Last HKMG FinFET Process)

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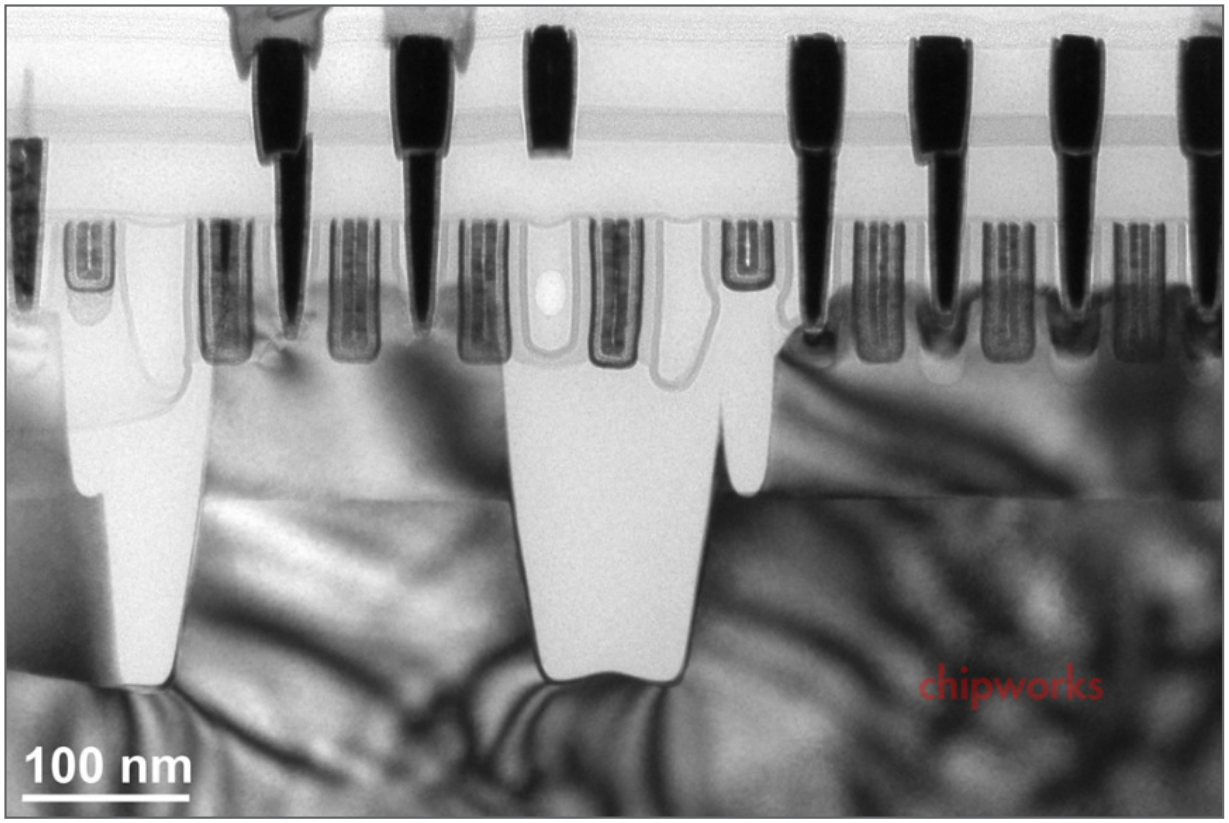
Samsung 14 nm finFETs



- First generation tri-gate transistors, 2nd generation RMG process
- Minimum fin pitch ~48 nm, SADP litho to define fins
- CGP ~78 nm, single patterning plus cut mask (limit for 193 nm immersion)
- Distinct fin isolation and well isolation

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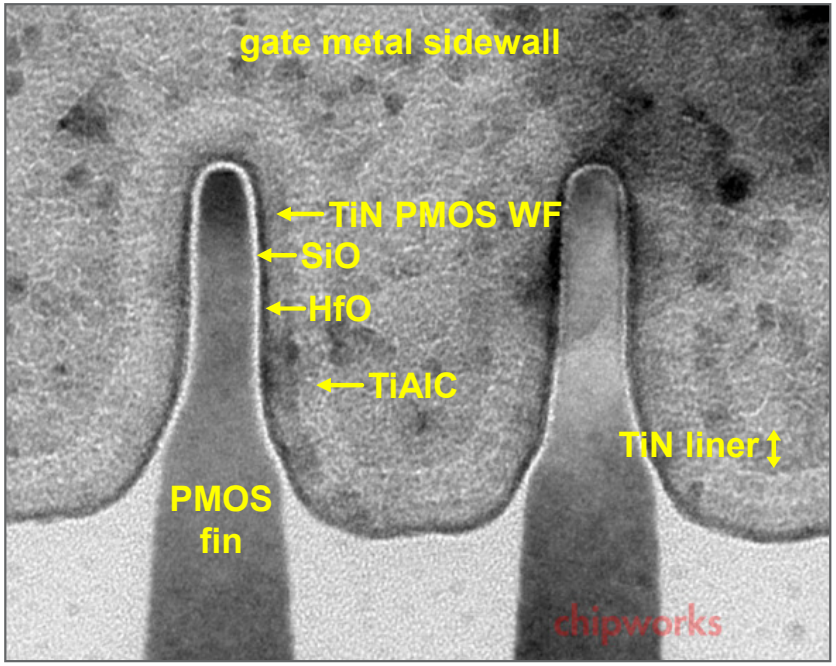
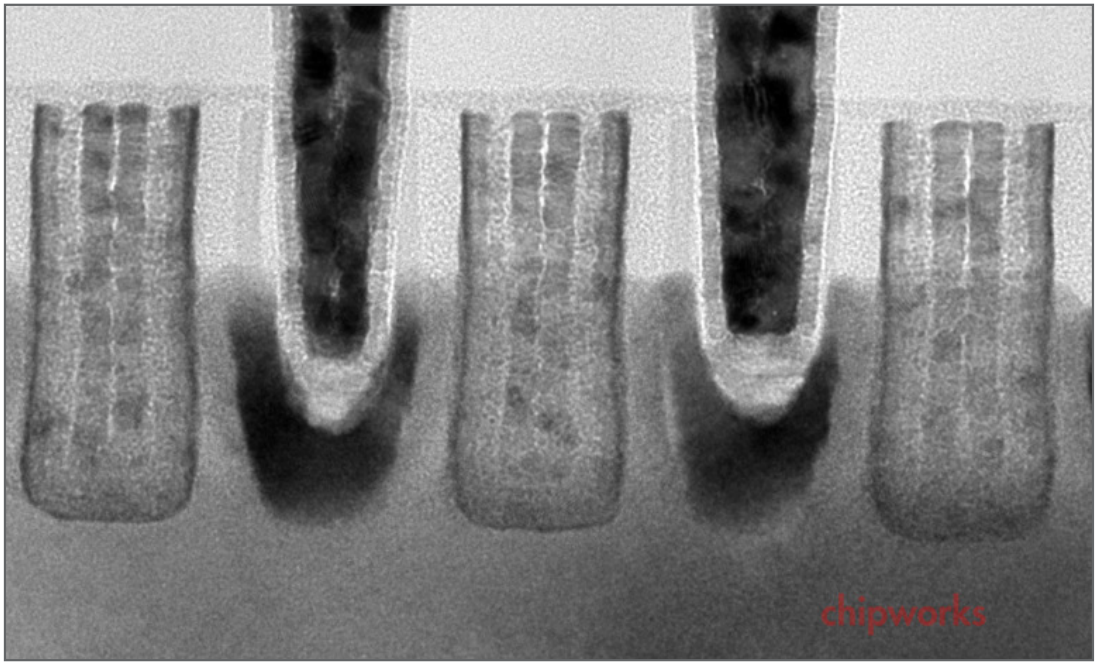
Samsung 14 nm PMOS Transistors





- MOL_g ~28 nm, gate width ~80 nm
- T_{ox} ~1.2 nm, t_{hi-k} ~1.3 nm
- Work-function materials similar to Intel/TSMC processes – PMOS is TiN
- E-SiGe for stress, -> 40% Ge

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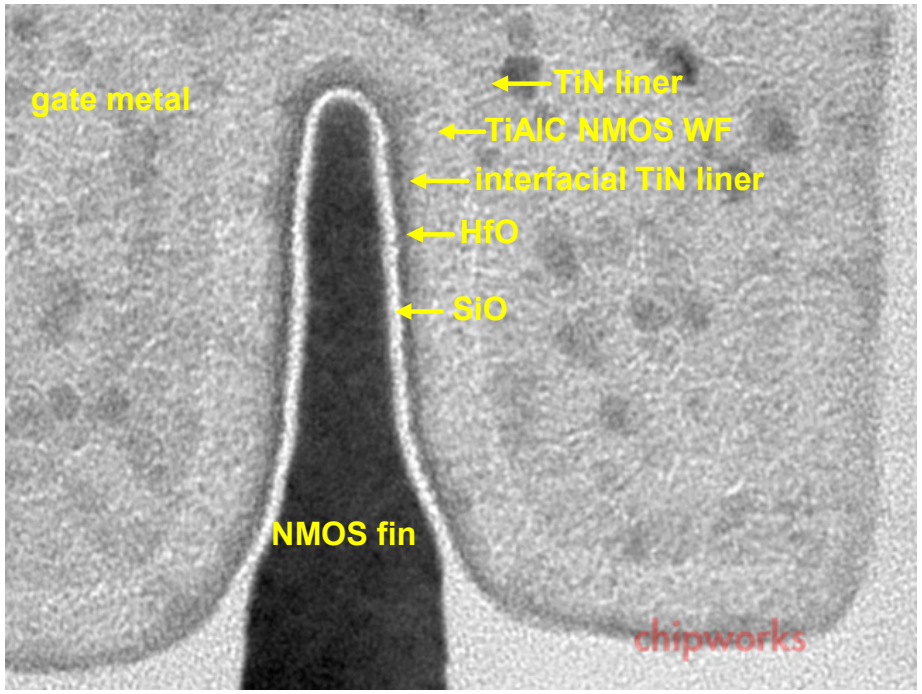
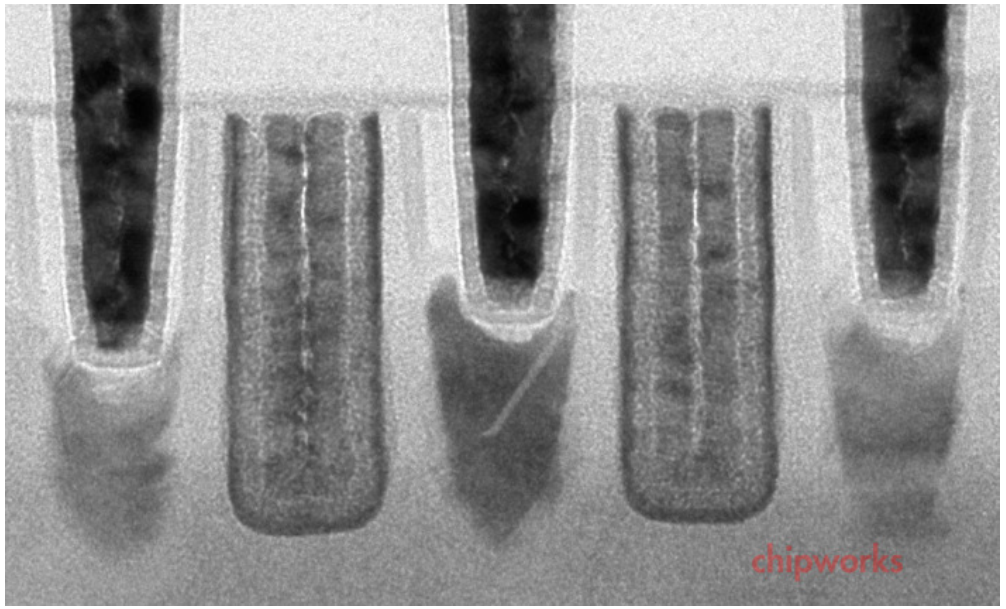
Samsung 14 nm NMOS Transistors





- MOL_g ~27 nm, gate width ~85 nm
- Fin width ~7 nm at half fin height
- Work-function materials similar to Intel/TSMC processes – NMOS is TiAl + TiN (with C from ALD)
- T_{ox} ~1.2 nm, $t_{hi\text{-}k}$ ~1.3 nm
- Si epi for NMOS

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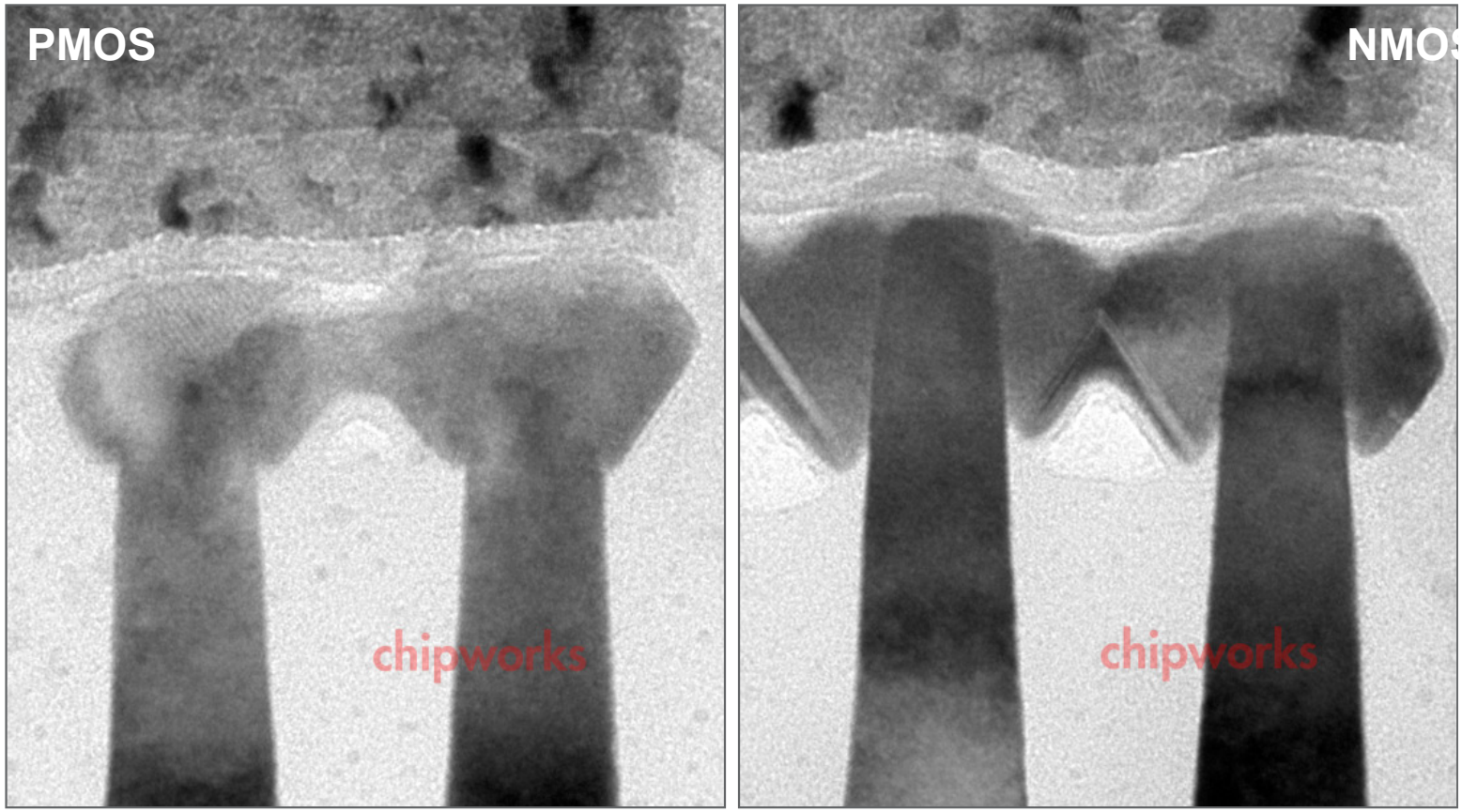
Samsung 14 nm Source/Drains



- Epi in both cases takes <111> planes, and merged, unlike Intel
- Ti silicidation
- Significant etching of the PMOS epi during the contact etch, dislocations in NMOS e-Si

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Apple APL1022 Application Processor (TSMC 16-nm FinFET HKMG Process)

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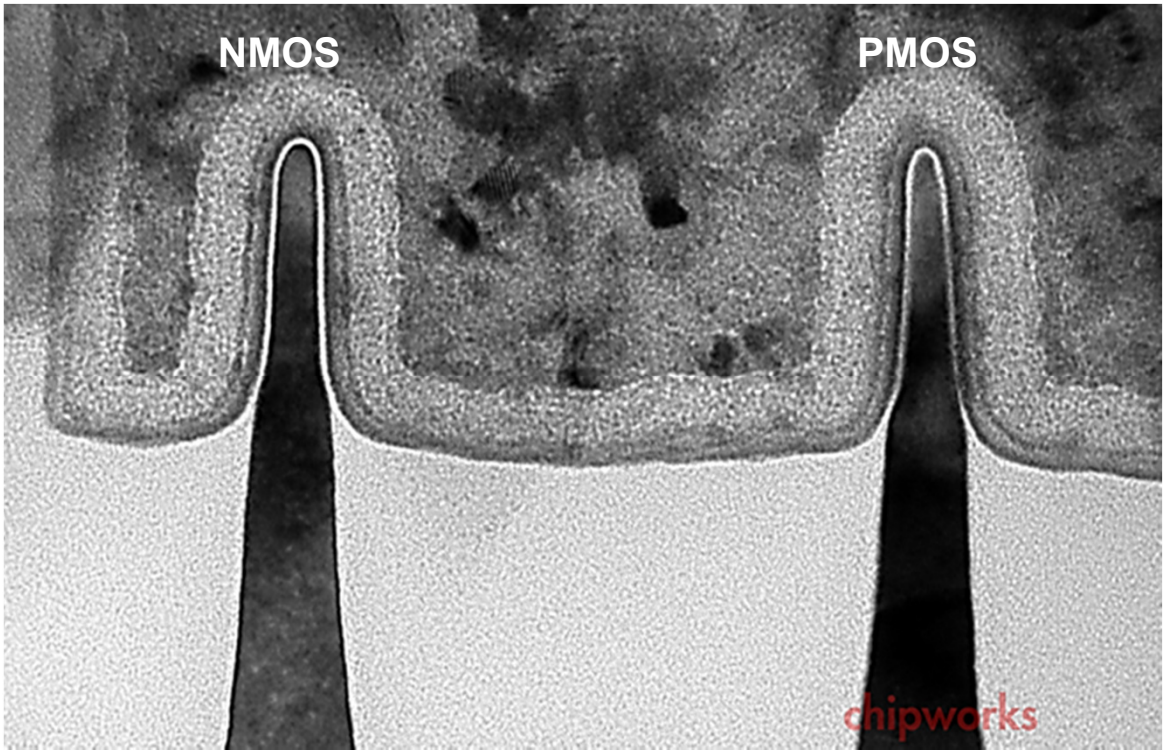
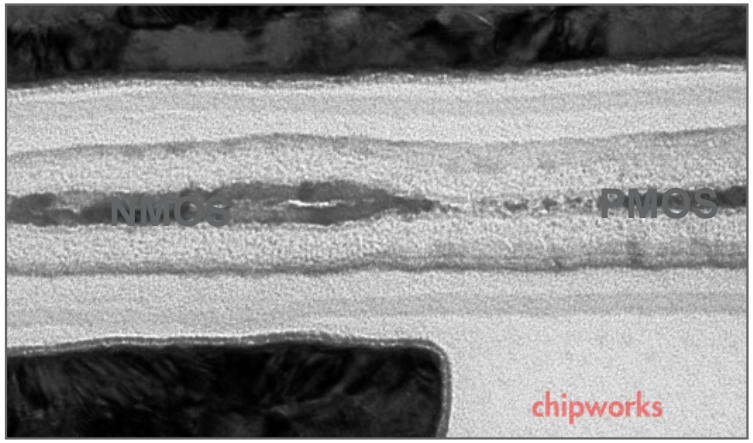
Apple APL1022 Application Processor





- First generation tri-gate transistors, 3rd generation RMG process
- Minimum fin pitch ~48 nm, CGP ~ 90 nm, SADP litho to define fins
- Functional gate height ~39 nm, gate width ~85 nm
- PMOS formed before NMOS; P + N WF layers in PMOS allows less room for W gate fill

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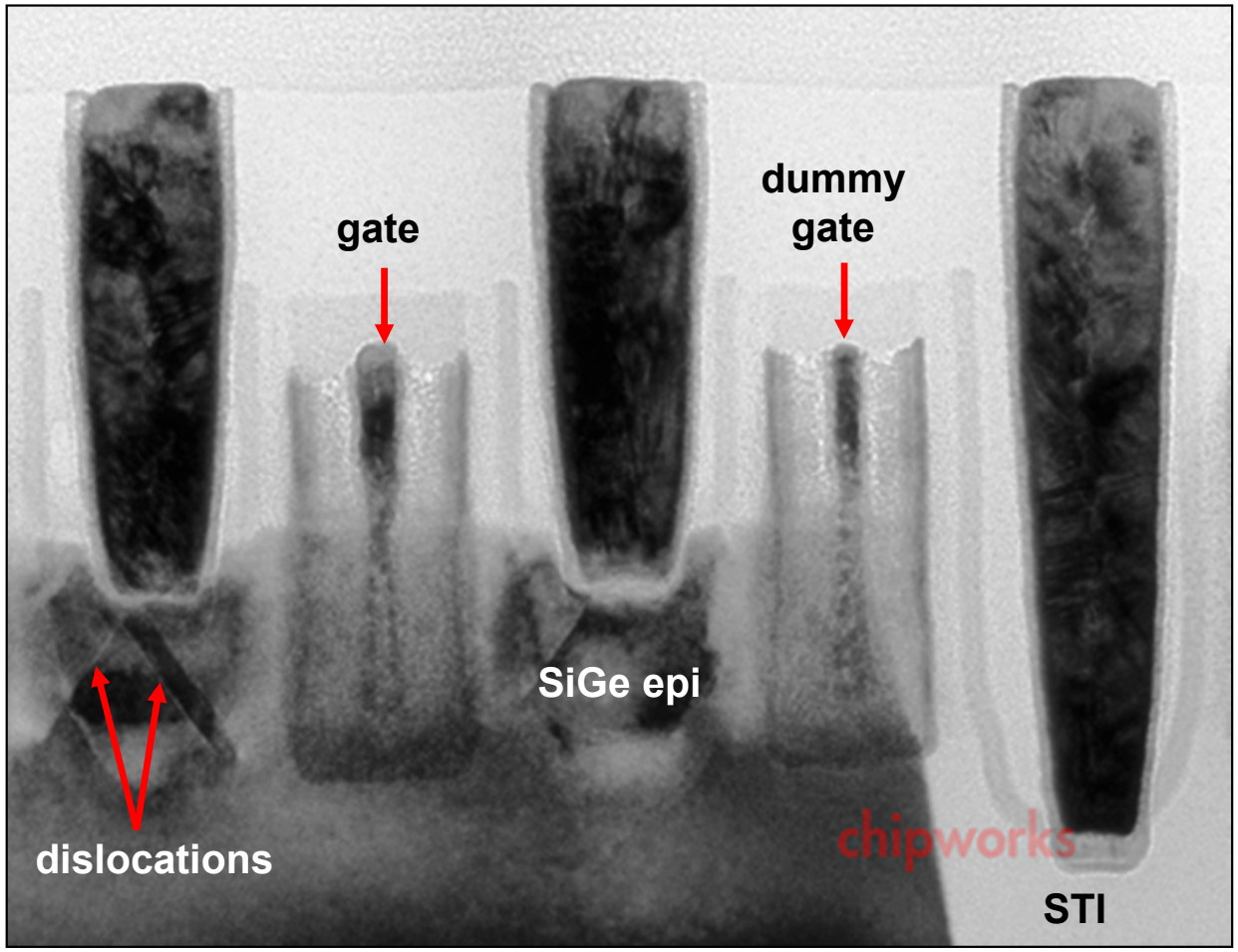
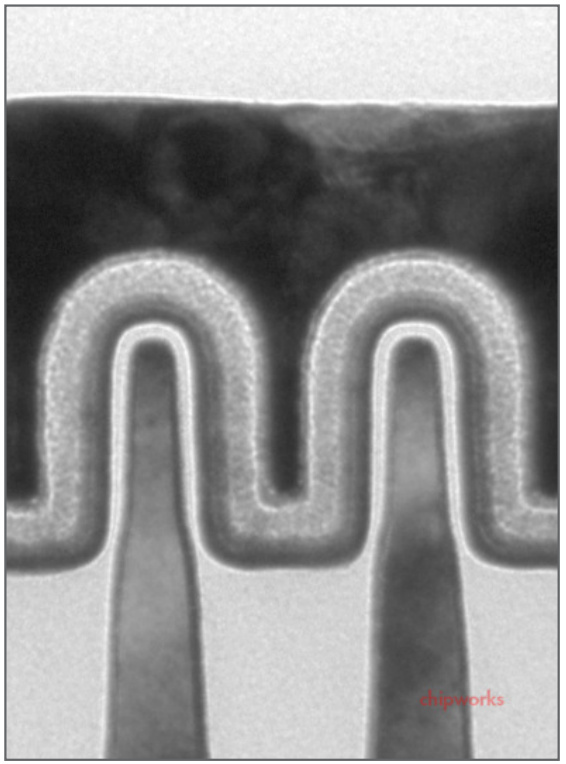
TSMC 16 nm PMOS Transistors





I/O transistor

- Gates back-etched, capped with SiN
- MOL_g ~30 nm, TiN WF layer, t_{ox}, $t_{hi\text{-}k}$ ~1.3 nm
- Cavity etch for source/drains, backfilled with SiGe epi
- ~4 nm t_{ox} in I/O transistors, longer gate lengths allow W fill

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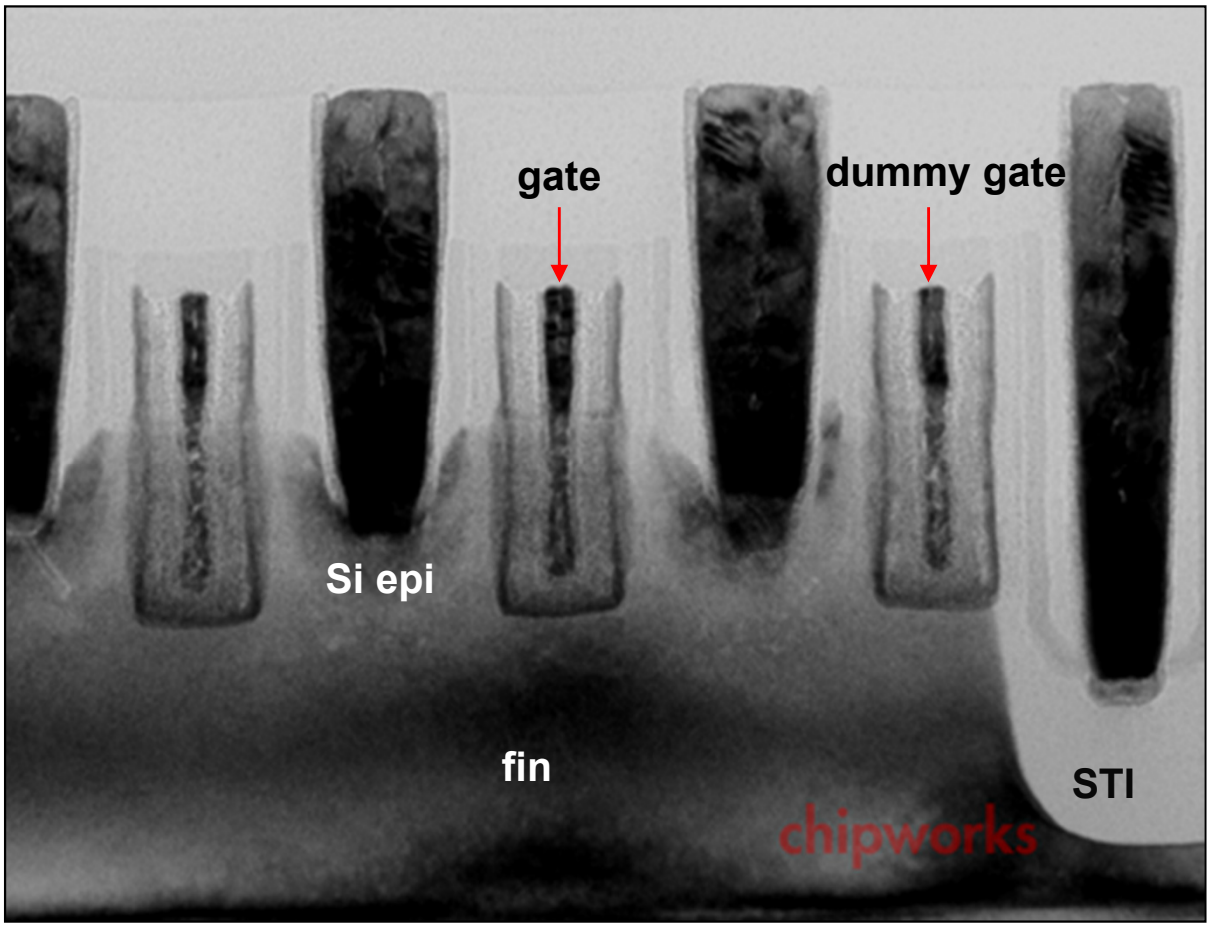
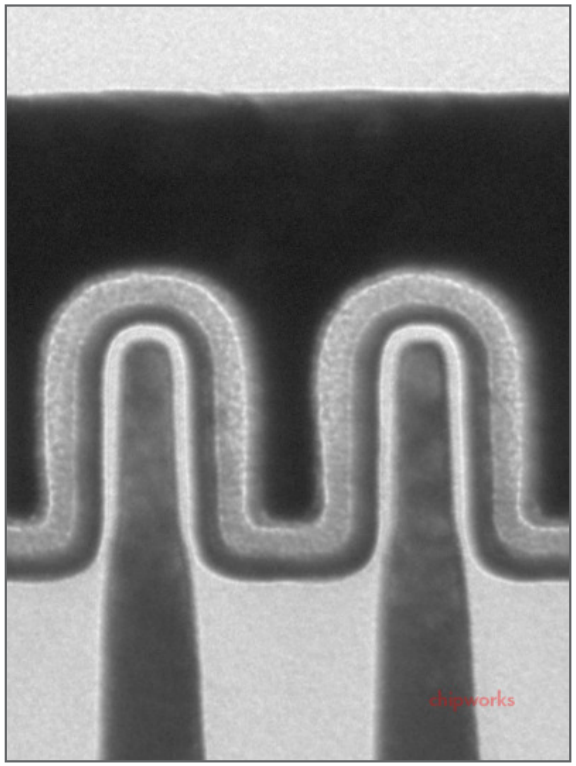
TSMC 16 nm NMOS Transistors





I/O transistor

- Gates back-etched, capped with SiN
- MOL_g ~30 nm, WF layer TiAlCOF, t_{ox}, $t_{hi\text{-}k}$ ~1.3 nm
- Cavity etch for source/drains, backfilled with Si epi
- ~3.5 nm t_{ox} in I/O transistors, longer gate lengths allow W fill

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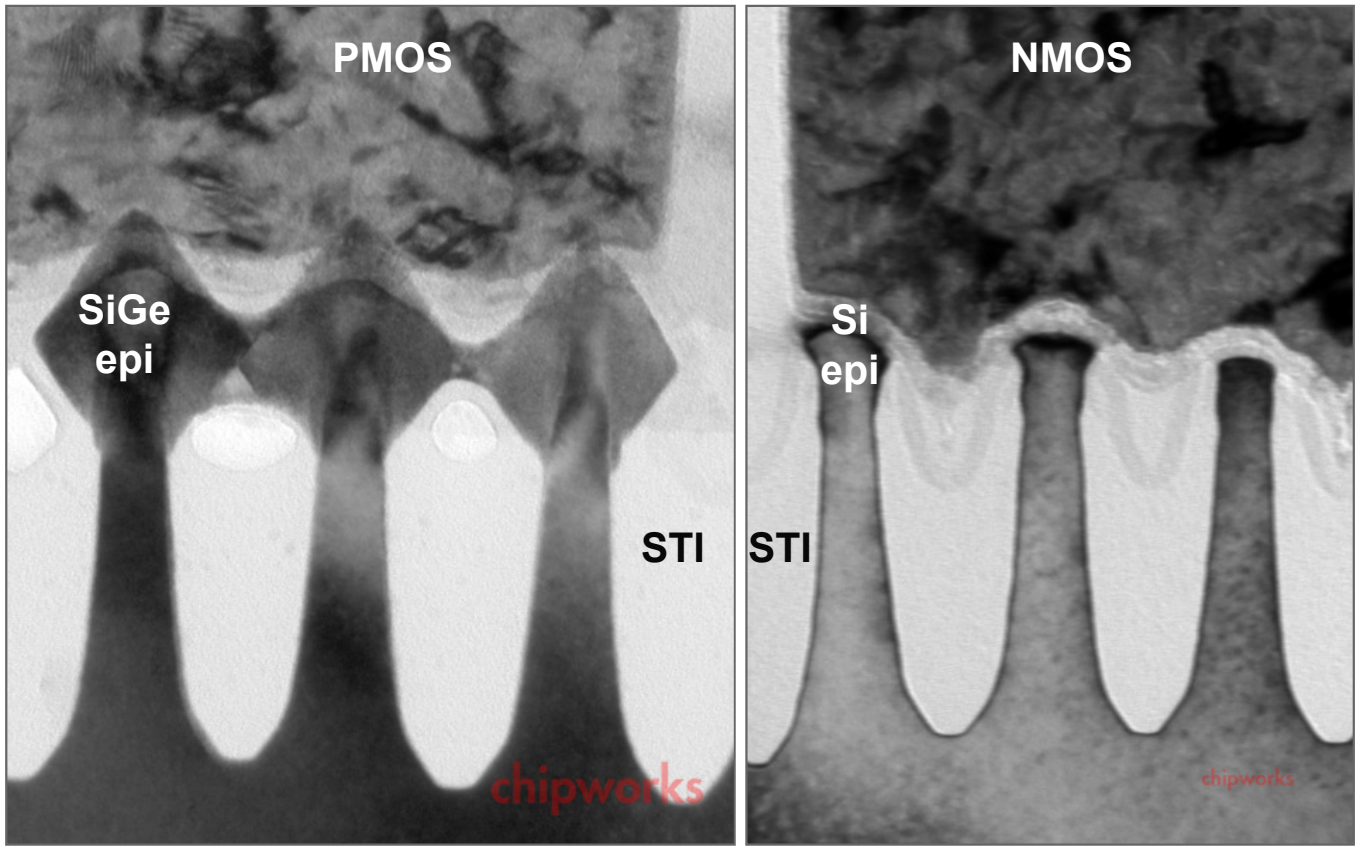
TSMC 16 nm Source/Drains



- PMOS e-SiGe has typical diamond shape, —> 55% Ge
- NMOS e-Si heavily gouged by contact etch
- Titanium used for silicidation

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Summary & Conclusions

- Definitely into the finFET era!
- Reviewed the last three 20/22-nm planar, 14/16 nm finFET transistors
- We see a large degree of commonality in the final devices
  - RMG gate dielectric high-k/oxide thicknesses all settled in the 1.0-1.3 nm range
  - Fin profiles and dimensions, and gate widths, are similar
- Detail differences in gate stacks and capping layers.
- Gate lengths/ fin pitch dependent on final performance
  - Foundries use L_g 28 – 30 nm, FP ~48 nm
  - Intel uses ~22 nm, FP ~42 nm
- Double patterning (SADP) now standard
- 10 nm in 2017?

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Acknowledgements

I would like to thank Chipworks' laboratory staff and process analysts for all the hard work of analyzing these complex devices. They did a great job!

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