Review of Key Papers From IWJT-2016 May 8-9, IEEE-PVSC 2016 June 6-10 & IEEE-VLSI Symposium 2016 June 14-16

Semicon/West 2016 WCJUG

July 14, 2016

John O. Borland

J.O.B. Technologies

Aiea, Hawaii

IWJT-2016

S3-8: Kingstone Semiconductor on FinFET Doping by ULE implant into Dielectric/Glass + Diffusion to Mimic PSG/BSG Doping

S4-4: SCREEN/Nissin on 10nm p+/ and n+/p Ge USJ with Flash Annealing

S3-2: Lam Research on Plasma Assisted Doping for 3-D Si-USJ

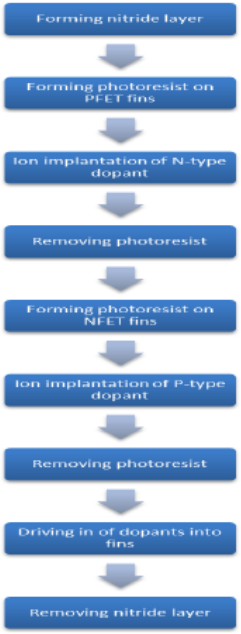
FinFET Doping with PSG/BSG Glass Mimic doping by Ultra Low Energy Ion Implantation

Jiong Chen, Junhua Hong, Jin Zhang, and Jeff Boeker

Kingstone Semiconductor Company, Ltd., 200 Niudun Road, Building 7, Shanghai, China 201203
john.chen@kingstonesemi.com

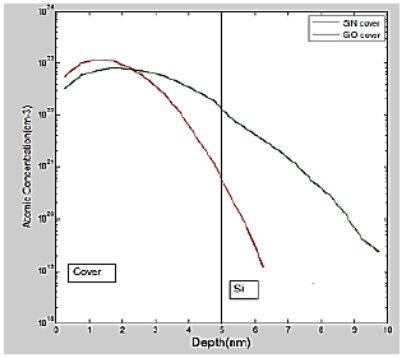
S3-8

Process flow for glass mimic doping

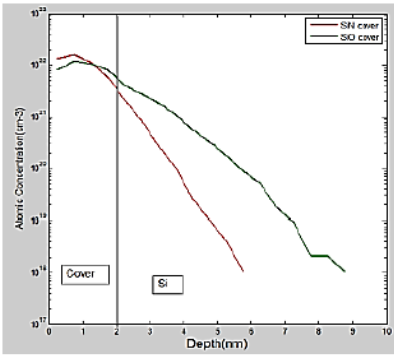


- Characteristics of glass mimic doping
  - Compatible with conventional ion beam implantation technique
  - Simplified process flow
  - No need for hard mask
  - Prevent amorphorization of fin

Simulation for the doses in dielectric layer and silicon fin



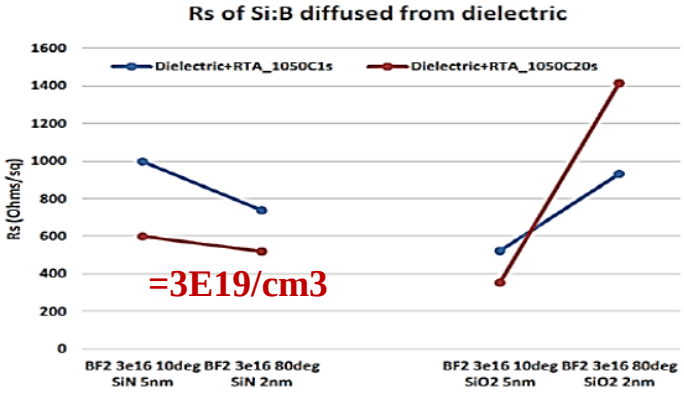
Top



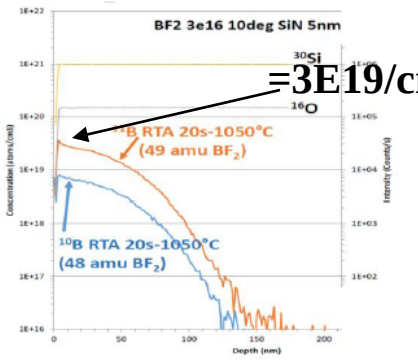
Sidewall

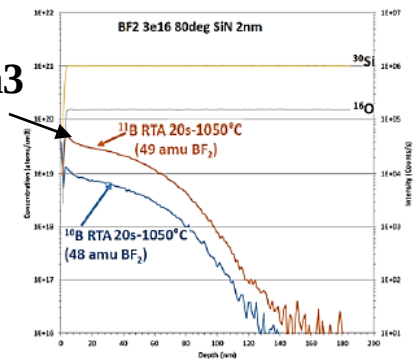
Location	Incident angle	Dielectric layer	Dose in dielectric (atoms/cm^2)	Dose in Si (atoms/cm^2)
Fin top	10°	5nm Si_3N_4	2.8E+16	1.7E+13
		5nm SiO_2	2.7E+16	1.1E+15
Sidewall	80°	2nm Si_3N_4	2.3E+15	2.7E+14
		2nm SiO_2	1.9E+15	9.6E+14

- The dopant concentration depends on the incident angle and the dielectric layer thickness. BF_2^+ at 1.3KeV, equivalent boron energy ~ 300eV

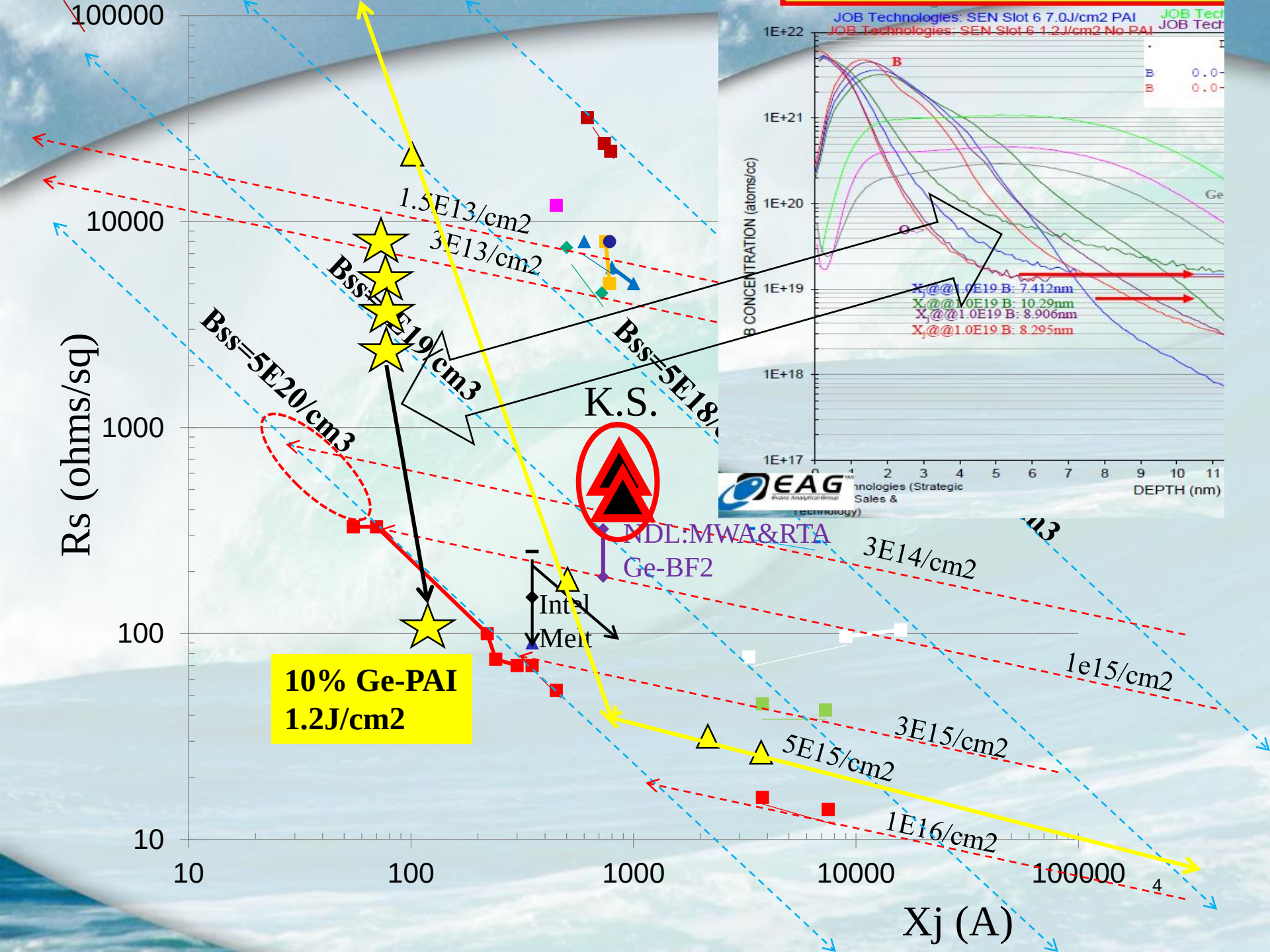


- The impact of dielectric layer material.
  - Similar Rs were obtained for fin top and sidewalls with the dielectric layer of SiN.
  - For SiO2, the Rs variation is large for fin top and sidewalls.

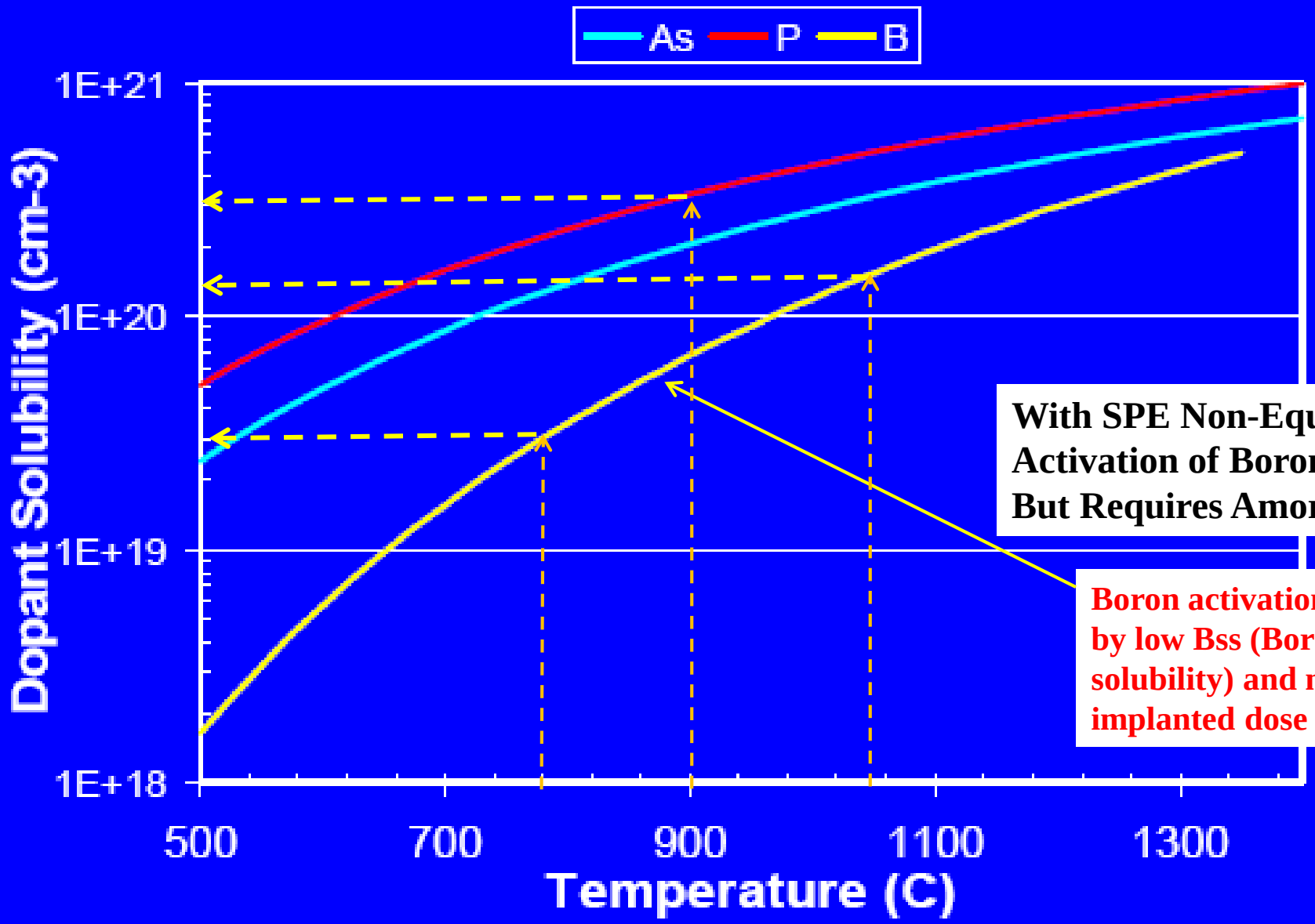




- The boron profiles for fin top and sidewalls are similar.
- The surface concentration of sidewall is higher than that of fin top, which is in accordance with Rs results.
- It can be further optimized by tuning incident angle and dielectric layer thickness


Rs (ohms/sq)
Xj (A)
100000
10000
1000
100
10
10
100
1000
10000
100000
1.5E13/cm2
3E13/cm2
Bss=1E19/cm3
Bss=5E20/cm3
Bss=5E18/
K.S.
NDL:MWA&RTA
Ge-BF2
Intel
Melt
3E14/cm2
1e15/cm2
3E15/cm2
5E15/cm2
1E16/cm2
10% Ge-PAI
1.2J/cm2
JOB Technologies: SEN Slot 6 7.0J/cm2 PAI
JOB Technologies: SEN Slot 6 1.2J/cm2 No PAI
B CONCENTRATION (atoms/cc)
1E+22
1E+21
1E+20
1E+19
1E+18
1E+17
B
Ge
O
Xj@@1.0E19 B: 7.412nm
Xj@@1.0E19 B: 10.29nm
Xj@@1.0E19 B: 8.906nm
Xj@@1.0E19 B: 8.295nm
DEPTH (nm)
EAG
Sales &

Solubility increases with Temp



With SPE Non-Equilibrium Activation of Boron >>Bss But Requires Amorphization!

Boron activation limited by low Bss (Boron solid solubility) and not by implanted dose

Kennel, Intel, IEEE/RTP 2006

10 nm-Deep n+/p and p+/n Ge Junctions with High Activation Formed by Ion Implantation and Flash Lamp Annealing (FLA)

H. Tanimura[1], H. Kawarazaki[1], K. Fuse[1], M. Abe[1], T. Yamada[1], Y. Ono[1], M. Furukawa[1], A. Ueda[1], Y. Ito[1], T. Aoyama[1], S. Kato[1], I. Kobayashi[1]
H. Onoda[2], Y. Nakashima[2], T. Nagayama[2], N. Hamamoto[2], S. Sakai[2]

[1]SCREEN Semiconductor Solutions Co., Ltd. 480-1 Takamiya-cho, Hikone, Shiga, 522-0292 Japan
[2] Nissin Ion Equipment Co., Ltd. 575 Kuze-Tonoshiro-cho, Minami-ku, Kyoto, 601-8205 Japan
Tel: +81-749-24-8460, E-mail: tanimura @prp.screeen.co.jp

S4-4

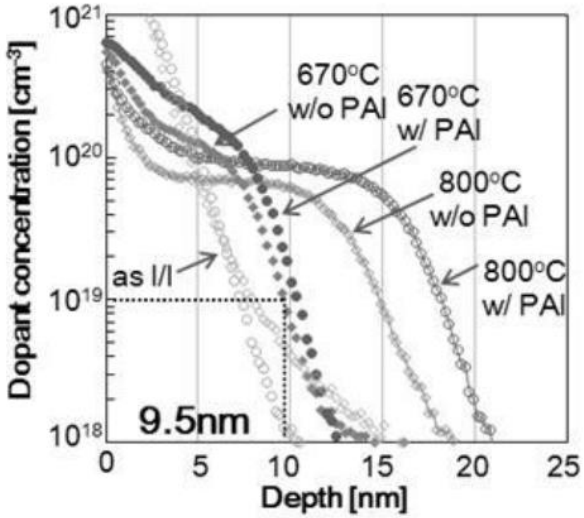


Fig. 2 SIMS profiles of P-doped samples. Shallow junctions below 10nm can be achieved.

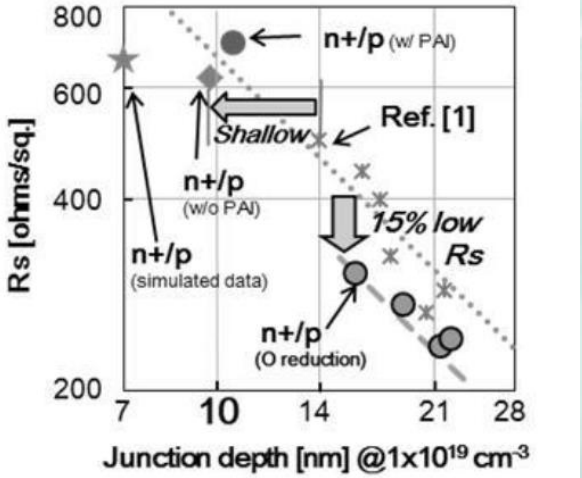


Fig. 4 Rs-Xj plots of n+/p junctions. 10nm depths can be obtained. By reducing knocked on oxygen, the activation level has been improved by a factor of 1.5.

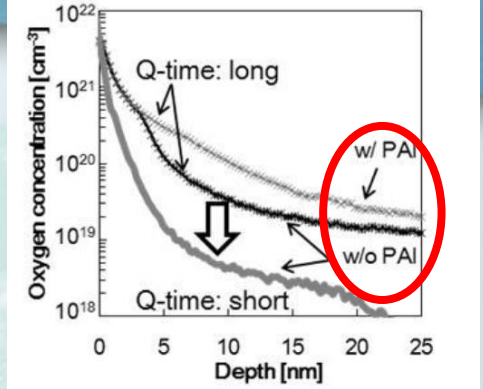


Fig. 6 SIMS profiles of oxygen. The sample with PAI has much more oxygen than the samples without PAI.

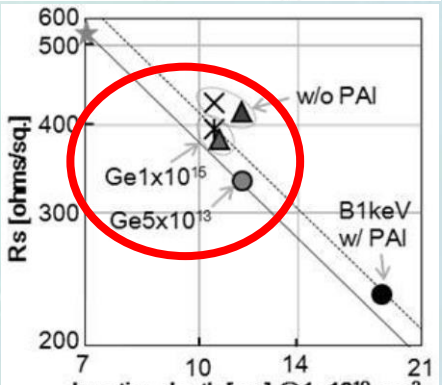


Fig. 11 Rs-Xj plots of p+/n junctions. The triangular symbols are for shorter pulses.

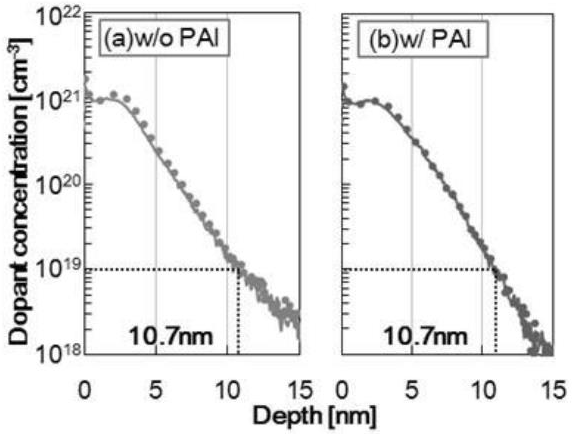


Fig. 8 SIMS profile of p+/n junctions. The dot plots and line plots are the profiles of pre- and post-annealed samples at 670 °C, respectively.

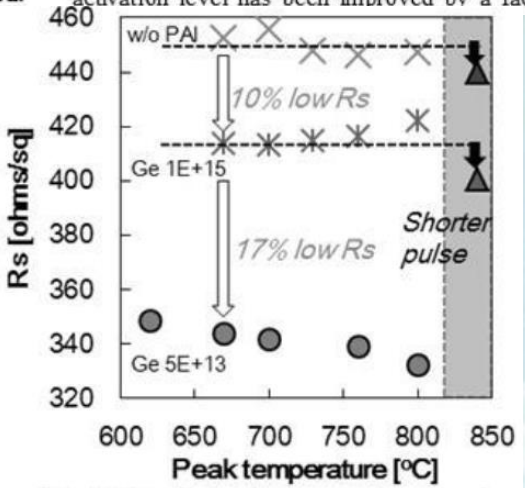


Fig. 10 The relationship between Rs and peak temperature.

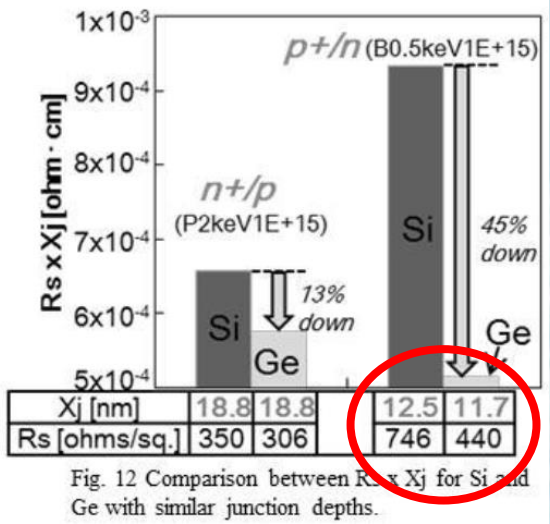
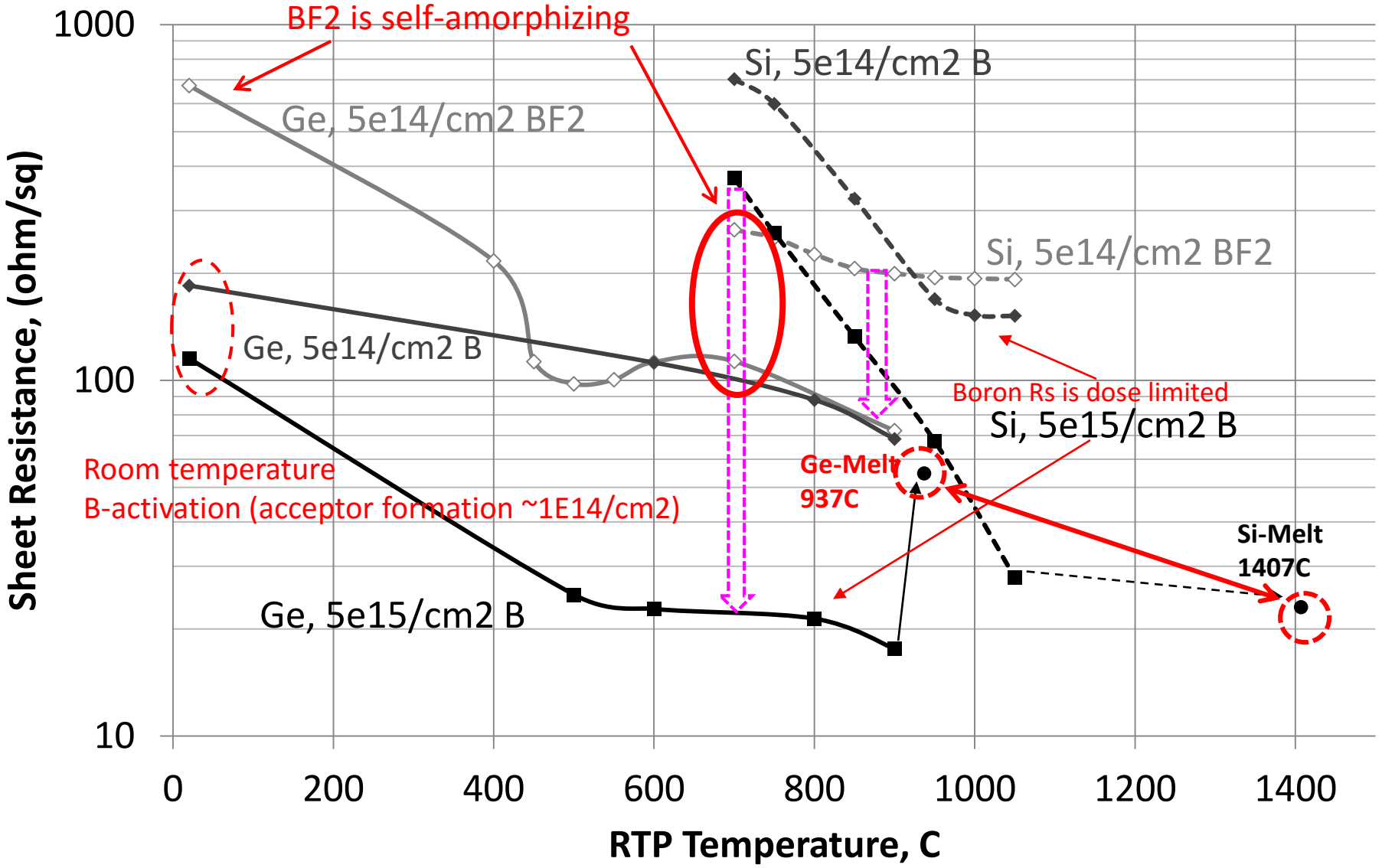
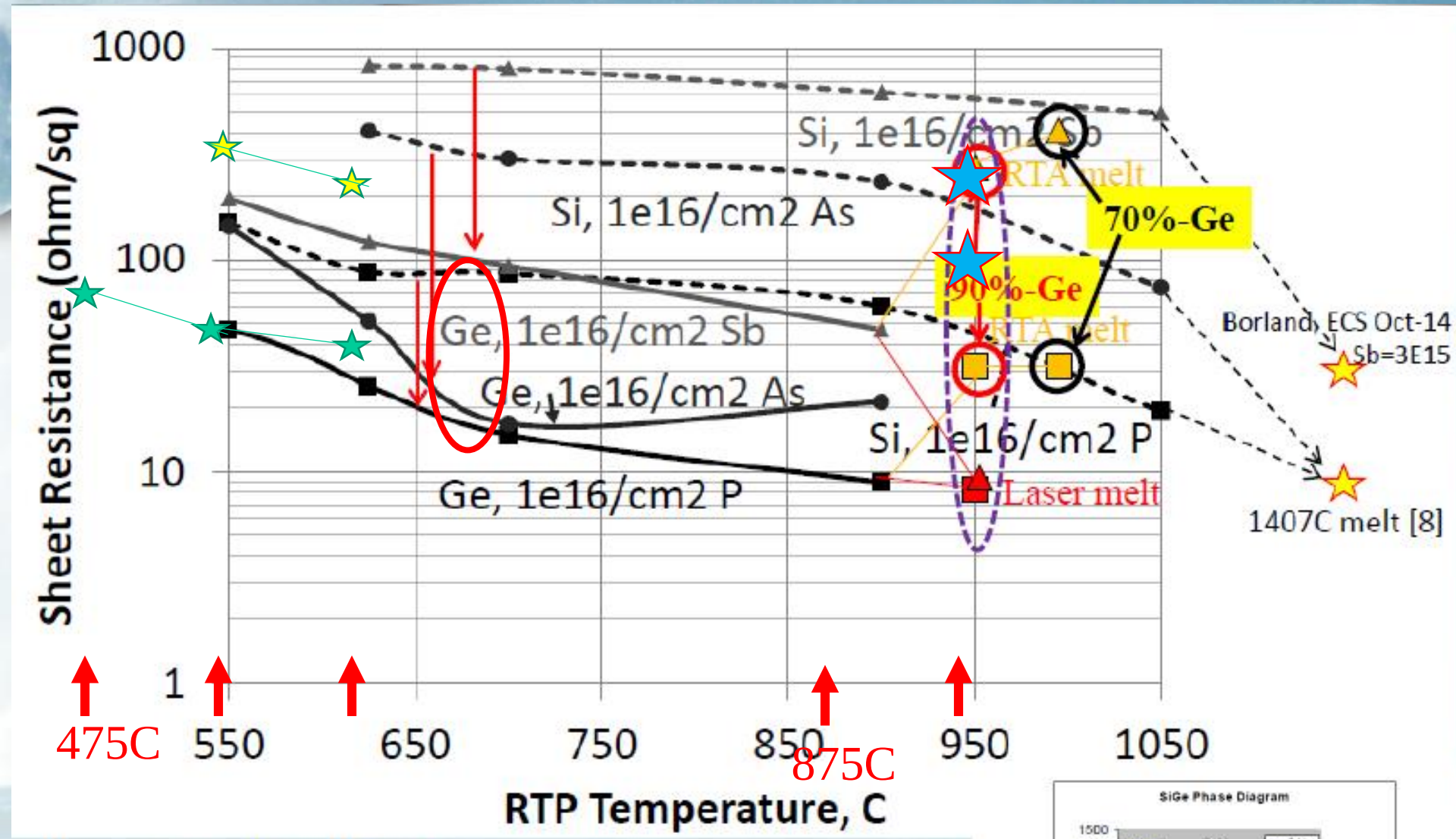


Fig. 12 Comparison between Rs x Xj for Si and Ge with similar junction depths.

Boron Activation in Si & Ge



Borland & Konkola, AIP, IIT-2014



Borland & Konkola, IIT-2014

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Technology)

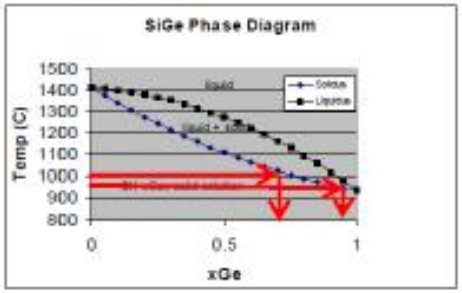


Figure 1. Binary phase diagram for Si-Ge. Note the continuous range of solid solutions for SiGe alloys, which form random solid solutions in a diamond cubic structure.

Ultra Shallow Junction (USJ) Formation Using Plasma assisted Doping on 3D Devices Structures

S3-2

YS Kim, YounGi Hong, and Ivan Berry

Lam Research Corp.

1650 Cushing pkwy, Fremont CA 94538, USA

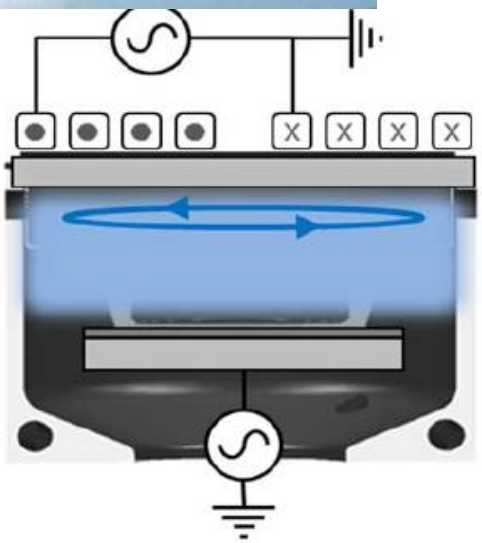
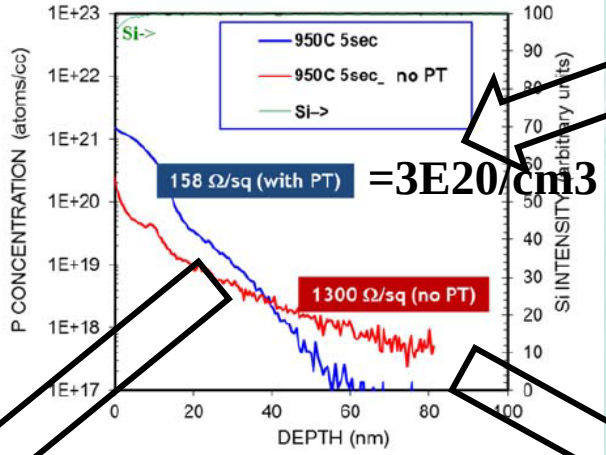


Figure 4: High density plasma sources to generate ion wafer uniformly is shown. Bias power at wafer level get enough ion energy to brings ions to wafer surface.



=3E20/cm3

Figure 7: Dopant profile in SIMS shows the difference of P level in Si for both with and without pre-treatment (PT) prior to PH_3 plasma doping process, respectively. ALD SiN layer was added for both samples after doping process without vacuum break, and annealed at 950C with RTP for Rs measurement.

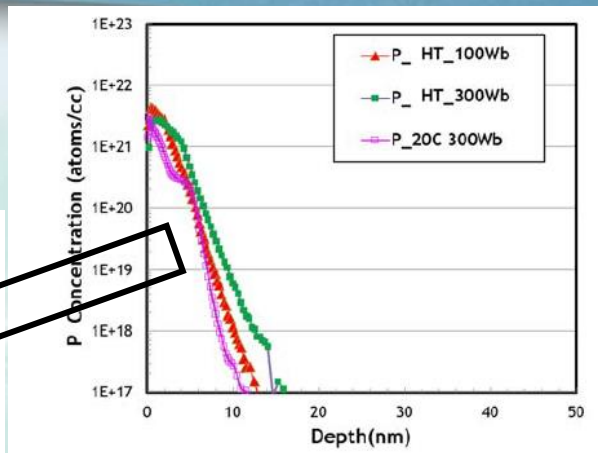


Figure 5: Plasma doping profile shows sharp transition on junction depth with two different wafer temperatures, room temperature and very high temperature(>150C), respectively.

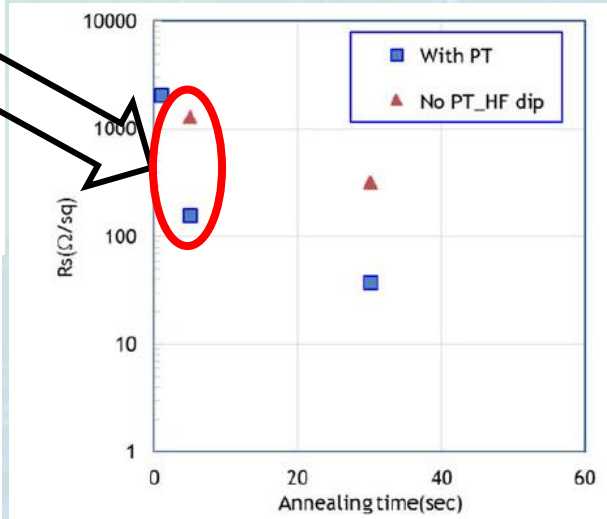


Figure 8: Rs measured by 4pt-pb with changing RTP annealing time. Lower Rs is seen with pre-treatment (PT) compared with the samples without PT.

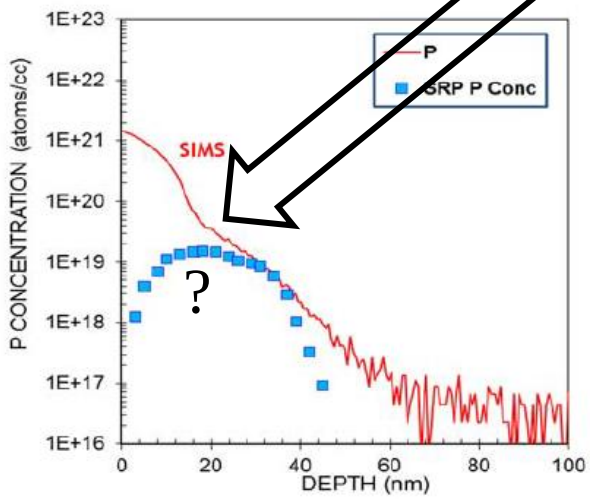


Figure 9: Dopant activation has been measured with SRP to compare with P level in SIMS.

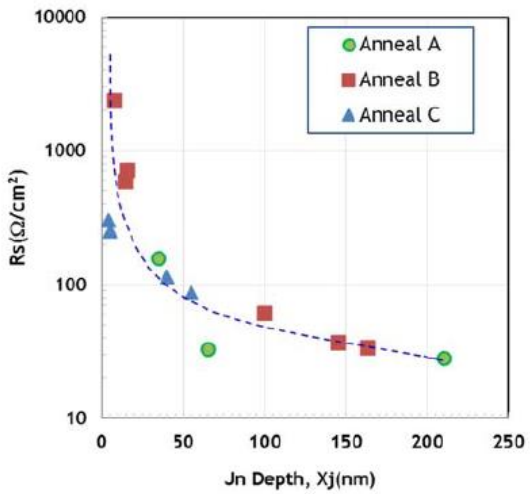
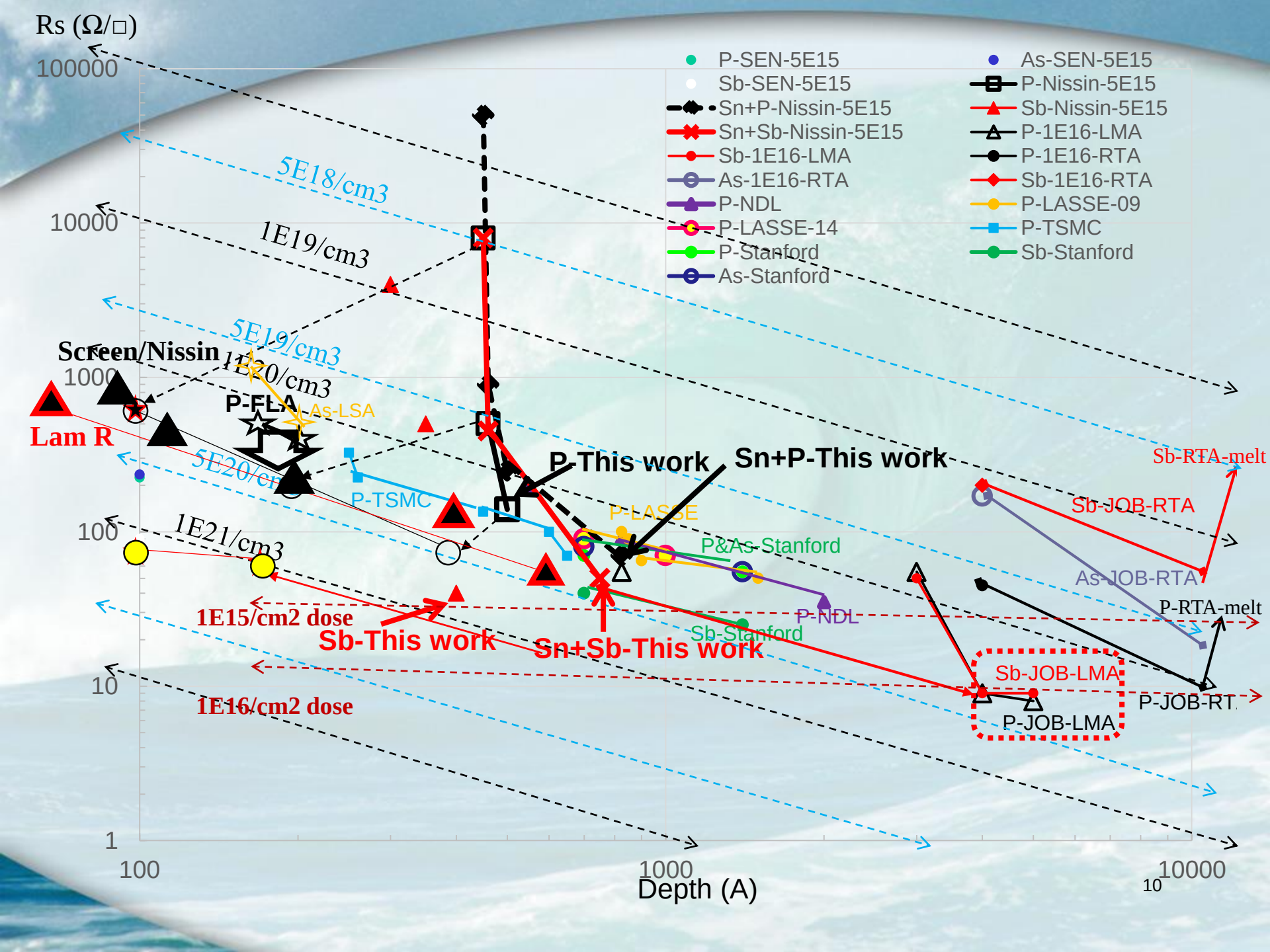


Figure 11: Various annealing techniques produces different performance on junction depth (X_j)


Rs (Ω/□)
100000
10000
1000
100
10
1
100
1000
10000
Depth (A)
5E18/cm3
1E19/cm3
5E19/cm3
1E20/cm3
5E20/cm3
1E21/cm3
P-SEN-5E15
Sb-SEN-5E15
Sn+P-Nissin-5E15
Sn+Sb-Nissin-5E15
Sb-1E16-LMA
As-1E16-RTA
P-NDL
P-LASSE-14
P-Stanford
As-Stanford
As-SEN-5E15
P-Nissin-5E15
Sb-Nissin-5E15
P-1E16-LMA
P-1E16-RTA
Sb-1E16-RTA
P-LASSE-09
P-TSMC
Sb-Stanford
Screen/Nissin
Lam R
P-FLA
As-LSA
P-TSMC
P-This work
Sn+P-This work
P-LASSE
P&As-Stanford
P-NDL
Sb-Stanford
1E15/cm2 dose
Sb-This work
Sn+Sb-This work
1E16/cm2 dose
Sb-RTA-melt
Sb-JOB-RTA
As-JOB-RTA
P-RTA-melt
Sb-JOB-LMA
P-JOB-RT
P-JOB-LMA

IEEE-PVSC 2016

Plasma Immersion Ion Implantation for Interdigitated Back Passivated Contact (IBPC) Solar Cells

David L. Young, William Nemeth, Vincenzo LaSalvia, Matthew R. Page, San Theingi, Matthew Young, Jeffery Aguiar, Benjamin G. Lee and Paul Stradins

National Renewable Energy Laboratory, Golden, CO, 80401, USA

ABSTRACT — **We present progress to develop low-cost interdigitated back contact solar cells with pc-Si/SiO_2/c-Si passivated contacts formed by plasma immersion ion implantation (PIII). PIII is a lower-cost implantation technique than traditional beam-line implantation due to its simpler design, lower operating costs, and ability to run high doses (1E14 – 1E18 cm^{-2}) at low ion energies (20 eV – 10 keV). These benefits make PIII ideal for high throughput production of patterned passivated contacts, where high-dose, low-energy implantations are made into thin (20 – 200 nm) a-Si layers instead of into the wafer itself. For this work symmetric passivated contact test structures grown on n-Cz wafers with PH_3 PIII doping gave implied open circuit voltage (iV_{oc}) values of 730 mV with J_o values of 2 fA/cm^2. Samples doped with B_2H_6 gave iV_{oc} values of 690 mV and J_o values of 24 fA/cm^2, outperforming BF_3 doping, which gave iV_{oc} values in the 660 - 680 mV range. Samples were further characterized by photoluminescence and SIMS depth profiles. Initial IBPC cell results are presented.**

Zero yielding IBPC solar cells, said beam-line was only 15.8% efficiency!

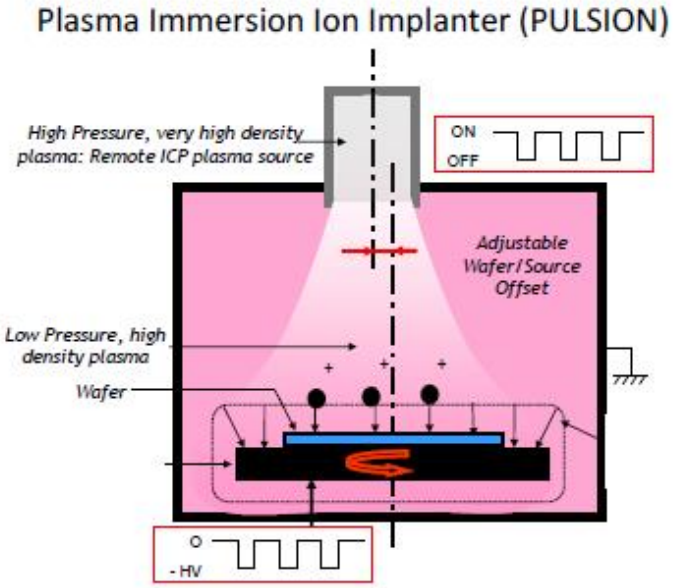


Fig. 1. Schematics for beam line (google image) and PIII implanters (IBS). (google images)

B Rs=1220Ω/□ =1E19/cm3

P Rs=152Ω/□ =8E19/cm3

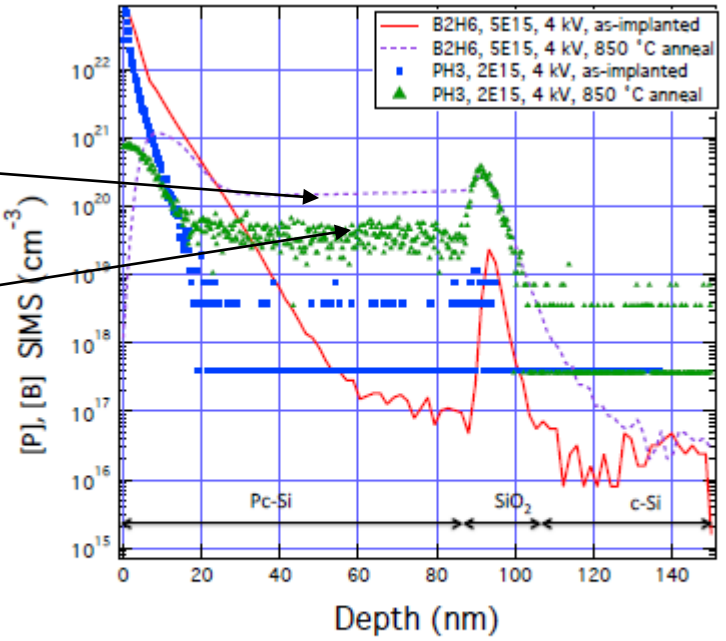


Fig. 2 SIMS depth profiles for PIII as-implanted and annealed samples. The legend indicates the implanted species, the dose (1/cm^2) and implant voltage.

Interdigitated Back Passivated Contact (IBPC) Solar Cells Formed by Ion Implantation

David L. Young, *Member, IEEE*, William Nemeth, Vincenzo LaSalvia, Robert Reedy, Stephanie Essig, Nicholas Bateman, and Paul Stradins

***Abstract*—We describe work toward an interdigitated back passivated contact (IBPC) solar cell formed by patterned ion-implanted passivated contacts. Formation of electron and hole passivated contacts to n-type Cz wafers using a thin SiO_2 layer and ion-implanted amorphous silicon (a-Si) is described. P and B were ion implanted into intrinsic a-Si films, forming symmetric and IBPC test structures. The recombination parameter J_0, as measured by a Sinton lifetime tester after thermal annealing, was $J_0 \sim 2.4$ fA/cm^2 for Si:P and $J_0 \sim 10$ fA/cm^2 for Si:B contacts. The contact resistivity for the passivated contacts was found to be 0.46 Ω·cm^2 for the n-type contact and 0.04 Ω·cm^2 for the p-type contact. The IBPC solar cell test structure gave 1-sun V_{oc} values of 682 mV and pFF = 80%. The benefits of the ion-implanted IBPC cell structure are discussed.**

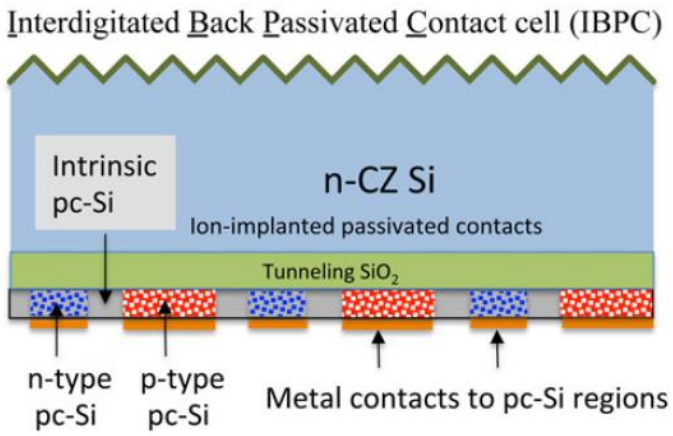


Fig. 1. Schematic of an IBPC solar cell formed by ion implantation.

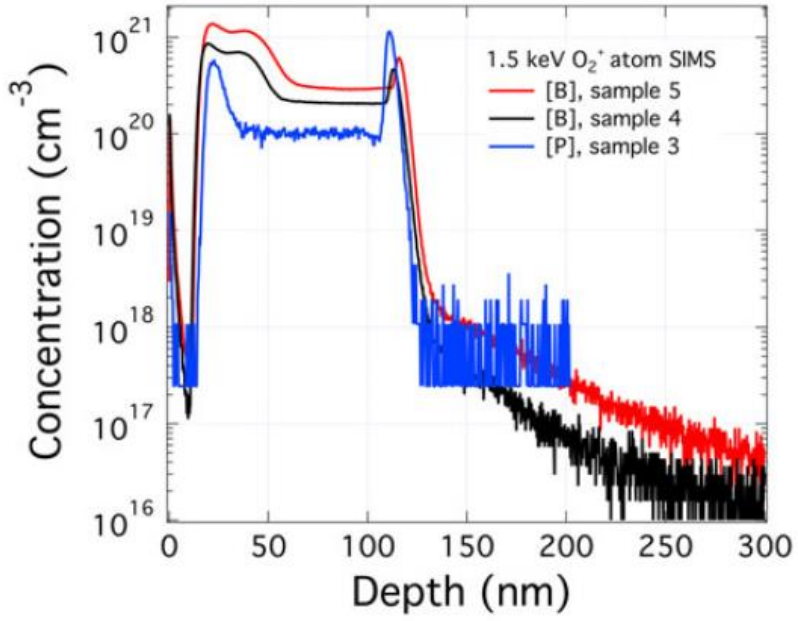


Fig. 3. Low-energy SIMS depth profiles for post-annealed samples 3–5.

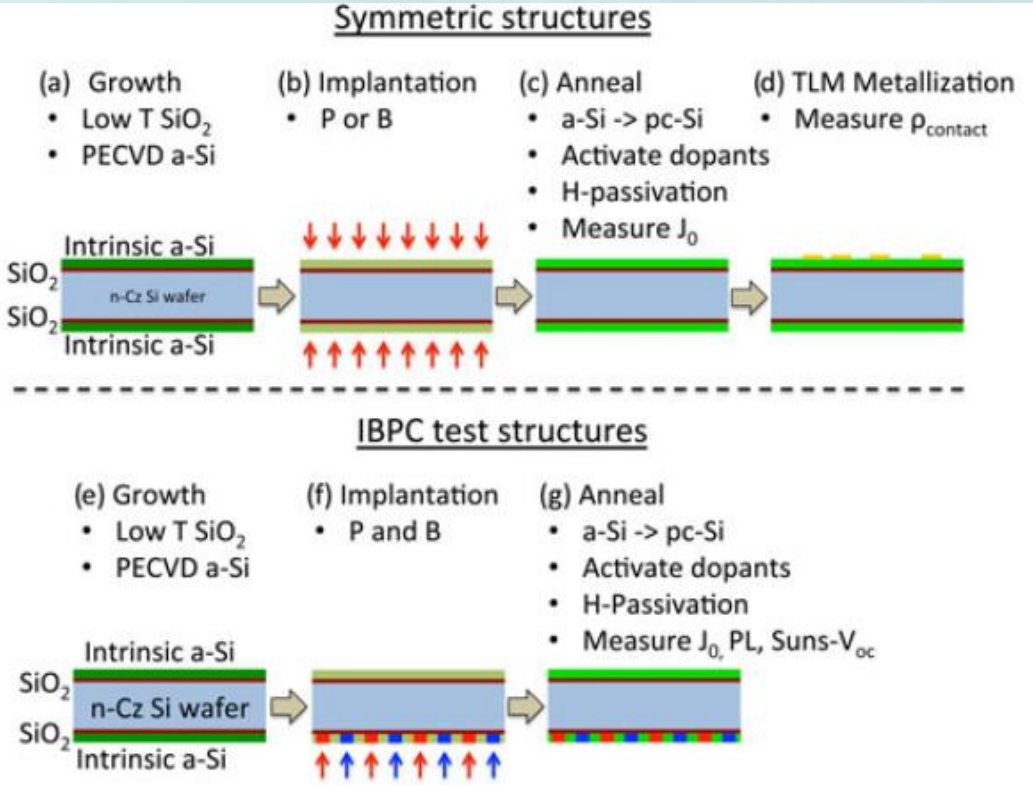
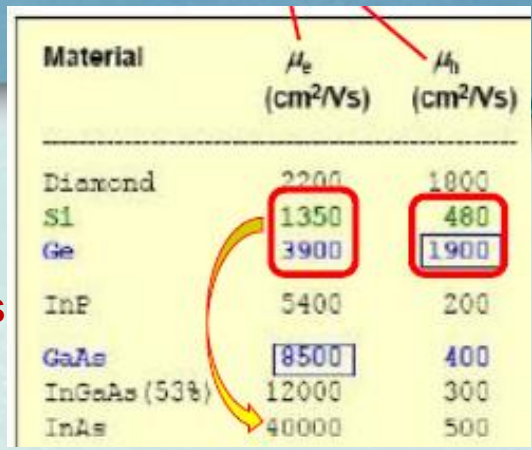


Fig. 2. Process flow for symmetric passivated contact test structures [(a)–(d)], and for an IBPC test structure [(e)–(g)].

VLSI Sym 2016



Paper 2.1: Samsung 10nm FinFET, μh=220cm2/V-s & μe=170cm2/V-s

Paper 2.2: IBM/GF 20% SiGe-channel 10nm pFinFET μh=+35%

Paper 2.3: TSMC InGaAs nFinFET μe=1731cm2/V-s

Paper 4.2: IMEC 14nm strained Ge FinFET Si μh=125cm2/V-s, r-Ge uh=240cm2/V-s and s-Ge uh=480cm2/V-s

Paper 4.3: IBM/GF/ST 40% SiGe FinFET μh=250 cm2/V-s

Paper 4.4: IBM 60% SiGe FinFET μh=325cm2/V-s

Paper 7.1: IMEC/AMAT/Samsung ultralow resistivity contacts (2.1E-9Ω-cm2)

Paper 7.3: AMAT 7nm node ultralow contact resistivity (<1.0E-9Ω-cm2)

Paper 7.4: GF/IBM canceled sub-2E-9Ω-cm2 contact resistivity

Paper 7.5: UMC/AMAT ultralow p+ SiGe contact resistivity (5.9E-9Ω-cm2)

Paper 9.1: TSMC 10nm FinFET

Paper 9.3: IBM 60% SiGe FinFET

Paper 13.1: CEA-LETI/ST +1.6GPa tensile strain 30% SiGe channel by STRASS

Paper 13.2: CEA-LETI/ST/IMEP/LAAS-CNRS FD-SOI with Low Temp SPE

Paper 15.1: IMEC GAA nanowire with EDS and S/D implantation

Paper 15.2: TSMC/Texas State InAs GAA

Paper 17.3: CEA-LETI/ST 3-D CoolCube

Paper 22.1: Renesas CMOS image sensor C-implant proximity gettering

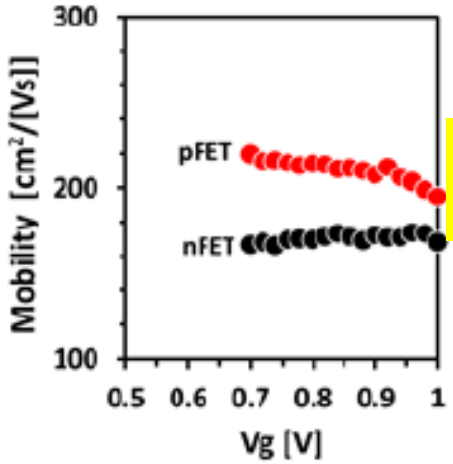
Si FinFET based 10nm Technology with Multi Vt Gate Stack for Low Power and High Performance Applications

H.-J. Cho, H.S. Oh, K.J. Nam, Y.H. Kim, K.H. Yeo, W.D. Kim, Y.S. Chung, Y.S. Nam, S.M. Kim, W.H. Kwon, M.J. Kang, I.R. Kim, H. Fukutome, C.W. Jeong, H.J. Shin, Y.S. Kim, D.W. Kim, S.H. Park, H.S. Oh, J.H. Jeong, S.B. Kim, D.W. Ha, J.H. Park, H.S. Rhee, S.J. Hyun, D.S. Shin, D.H. Kim, H.Y. Kim, S. Maeda, K.H. Lee, Y.H. Kim, M.C. Kim, Y.S. Koh, B. Yoon, K. Shin, N.I Lee, S.B. Kangh, K.H. Hwang, J.H. Lee, J.-H. Ku, S.W. Nam, S.M. Jung, H.K. Kang, J.S. Yoon, ES Jung

Semiconductor R&D Center, Samsung Electronics, San #16, Banweol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Korea,

Key module	10nm	14nm-2	14nm-1
Fin	3rd gen	2nd gen	1st gen
PC patterning	Mandrel	Single photo	
Epi growth	3rd gen	2nd gen	1st gen
Contact	Single	Trench	

Fig. 2 Process technology comparison between 10nm and 14nm technologies.



μh=220
μe=170

Fig. 6 Short channel mobility of pFET and nFET. The mobility of pFET is about 10% higher than that of nFET.

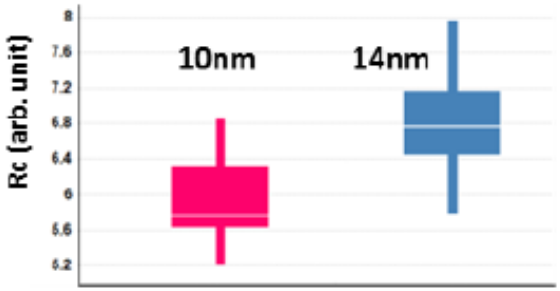


Fig. 3 pFET contact resistance (Rc) is reduced by 10% from 14nm to 10nm technology using contact process optimization.

10nm FinFET will stay with bulk Si-channels and eS/D-stressors. No SiGe channel.

Demonstration of a sub-0.03 um^2 High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node

Shien-Yang Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, C.H. Chang, V.S. Chang, K.H. Pan, C.H. Tsai, C.H. Yao, T. Miyashita, Y.K. Wu, K.C. Ting, C.H. Hsieh, R.F. Tsui, R. Chen, C.L. Yang, H.C. Chang, C.Y. Lee, K.S. Chen, Y. Ku, S. M. Jang

168, Park Ave. 2, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C., Email: shien-yang_wu@tsmc.com
Taiwan Semiconductor Manufacturing Company

Process Enablers

Advanced pitch-splitting patterning technique with 193nm immersion lithography is used to enable pitch scaling for critical layers. Fin width and profile are carefully optimized to maintain excellent short channel with scaled gate length to reduce parasitic capacitance between contact and gate. Raised source/drain with dual epitaxy process is optimized to mitigate source/drain (S/D) parasitic resistance. Enhanced contact process is developed to enlarge manufacturing margin.

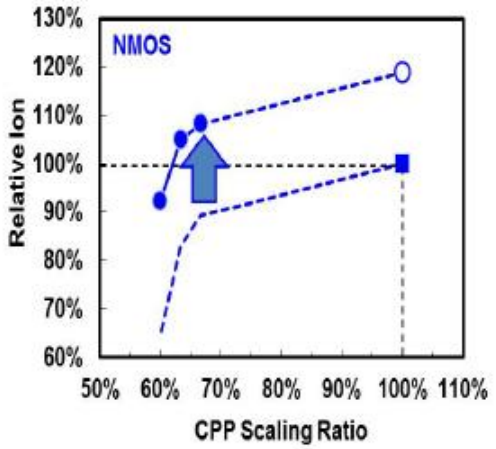


Fig.8 NMOS Ion boost with mobility enhancement and resistance reduction.

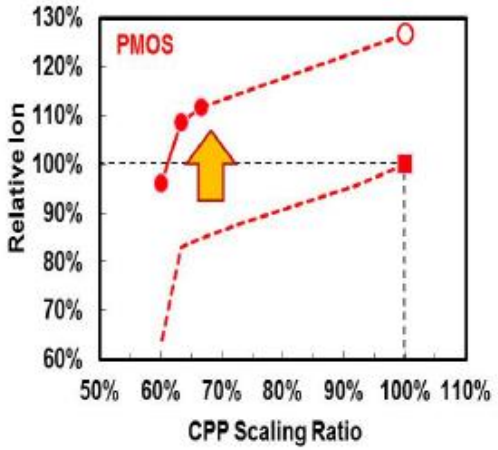


Fig.9 PMOS Ion boost with mobility enhancement and resistance reduction.

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FINFET Technology Featuring High Mobility SiGe Channel for 10nm and Beyond

D. Guo, G. Karve, G. Tsutsui, K-Y Lim*, R. Robison, T. Hook, R. Vega, D. Liu, S. Bedell, S. Mochizuki, F. Lie, K.Akarvardar*, M. Wang, R. Bao, S. Burns, V. Chan, K. Cheng, J. Demarest, J. Fronheiser*, P. Hashemi, J. Kelly, J. Li, N. Loubet, P. Montanini, B. Sahu*, M. Sankarapandian, S. Sieg, J. Sporre, J. Strane, R.Southwick, N. Tripathi*, R. Venigalla, J. Wang, K. Watanabe, C. W. Yeung, D. Gupta, B. Doris, N. Felix, A. Jacob*, H. Jagannathan, S. Kanakasabapathy, R. Mo, V. Narayanan, D. Sadana, P. Oldiges, J. Stathis, T. Yamashita, V. Paruchuri, M. Colburn, A. Knorr*, R. Divakaruni, H. Bu, M. Khare
IBM Semiconductor Technology Research, 257 Fuller Road, Albany, NY 12203, *GLOBALFOUNDRIES Inc.

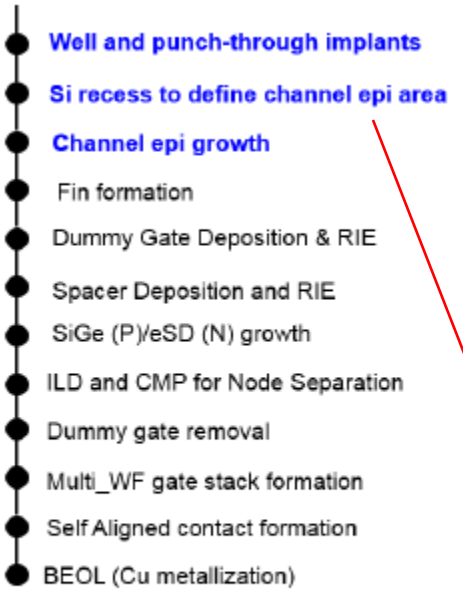


Fig. 1 10nm integration flow with optimized process steps for SiGe FIN.

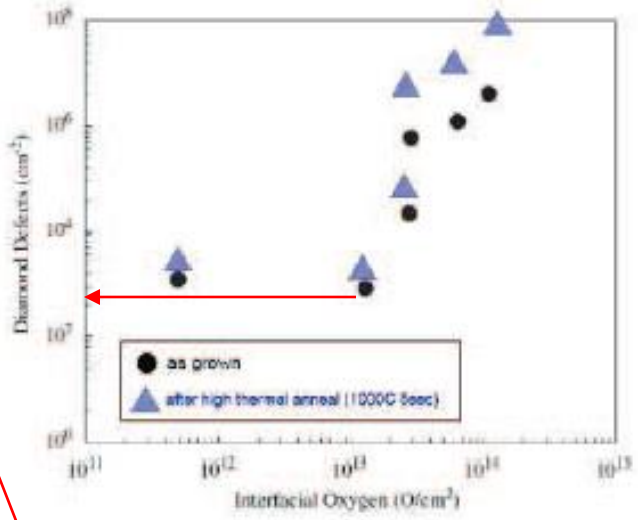


Fig. 3. The relationship between measured SiGe defects and the integrated oxygen concentration at the growth interface [6].

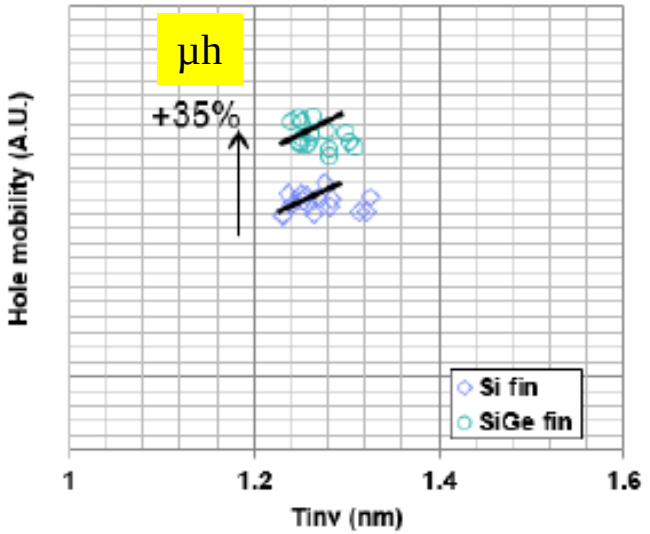
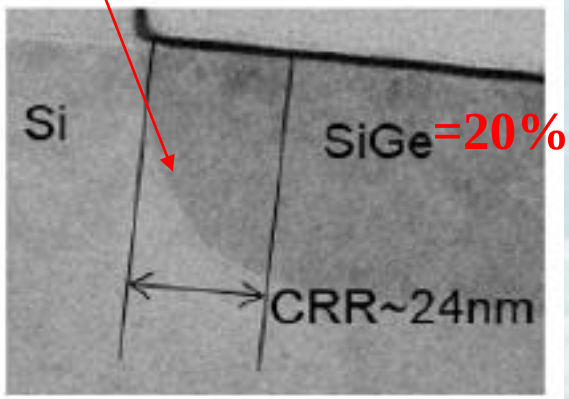


Fig. 8. At matched Tinv, SiGe fin with 20% Ge illustrates 35% hole mobility boost over Si FIN.



A 2nd Generation of 14/16nm-node compatible strained-Ge pFINFET with improved performance with respect to advanced Si-channel FinFETs

J. Mitard, L. Witters, Y. Sasaki, H. Arimura, A. Schulze, R. Loo, L.-Å. Ragnarsson, A. Hikavyy, D. Cott, T. Chiarella, S. Kubicek, H. Mertens, R. Ritzenthaler, C. Vrancken, P. Favia, H. Bender, N. Horiguchi, K. Barla, D. Mocuta, A. Mocuta, N. Collaert, A.V-Y. Thean

IMEC, Kapeldreef 75, 3001 Leuven, Belgium E-mail: Jerome.Mitard@imec.be

VLSI-2016
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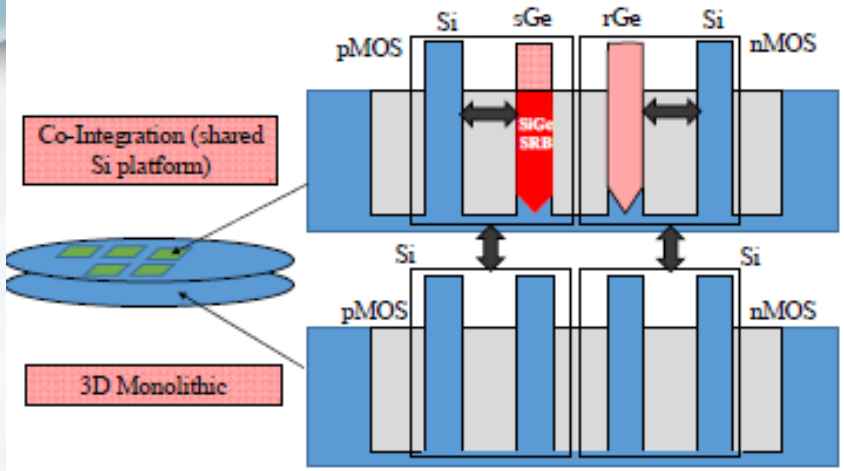


Fig.1: Two paths using high-mobility channel devices (here: strained Ge p or relaxed Ge n) co-integrated onto a Silicon platform is envisioned. The fin replacement process is also called STI-First approach as opposite to STI-Last where STI is etched into the high-mobility material (either locally or in 300mm wafers).

- Silicon SADP Fin Formation -11nm Wide Fins
- Si recess + in-situ relaxed Ph-doped SiGe70% + strained Ge deposition + STI Recess
- dummy gate deposition + patterning
- Boron Extension I/I + scaled SiN spacer
- Raised B-doped Germanium S/D SEG
- Boron HDD implantation + 500C 5' junc
- Epi Silicon + wet SiO_2 + HfO_2 + TiN + W
- Local Interconnect1 + Ti direct contact to S/D epi
- Local Interconnect2 to LI1 and RMG
- Via1 + Metal1 + passivation *Steps changed from [3]*

Fig.2: Detailed process flow leading to our 2nd generation strained Ge pFINFETs with 45nm Fin pitch, 110nm Contact Poly Pitch (CPP). Optimizations with respect to the first generation of devices [3] are highlighted.

Ge µh=1900cm2/V-s

Si-Fin µh=125
rGe-Fin µh=240
sGe-Fin µh=480

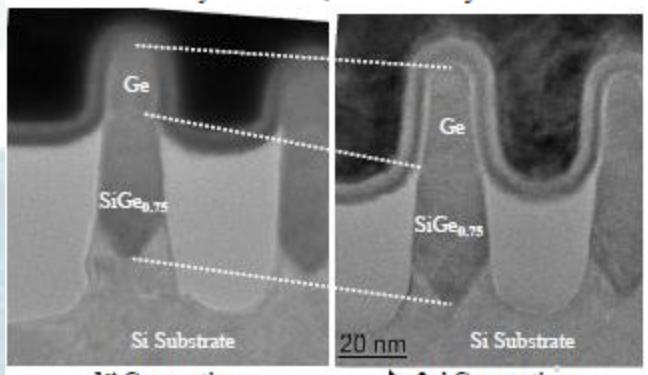


Fig.3: High resolution xTEM pictures from fully-processed transistors after fin module redevelopment. The devices considered in this analysis are 34nm-L_G devices to allow space for the xTEM preparation.

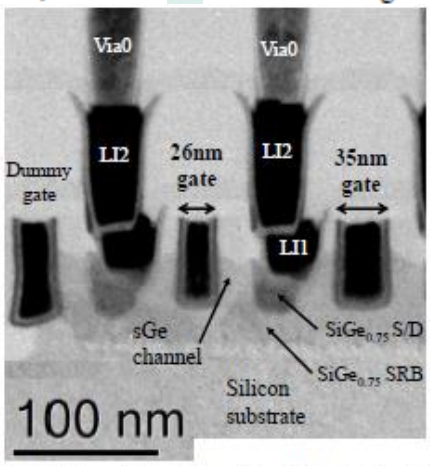
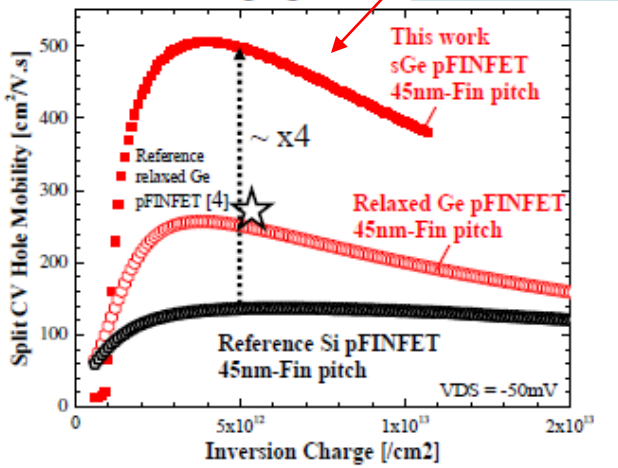


Fig.7: Gate cut along the ~10nm W_{FIN} strained Ge pFINFET (110nm CPP). 26nm dummy gate and 35nm active gates are shown.

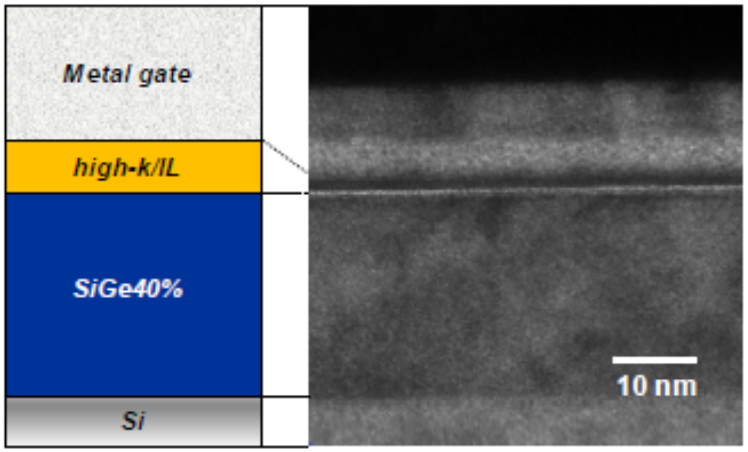


ig.9: Split CV mobility extractions carried out on our 45nm-Fin Pitch devices. High mobility is obtained after our gate stack developments confirming that the Ge is kept strained till the end of processing

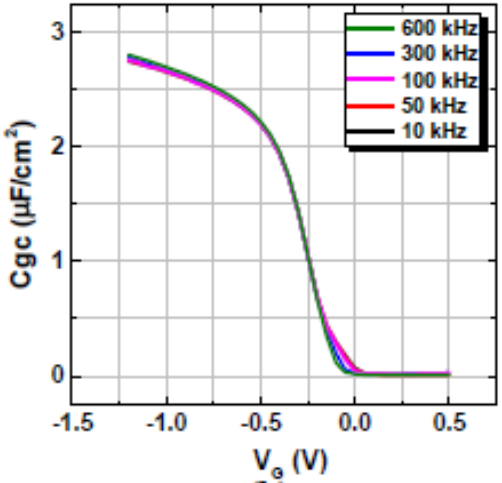
Selective GeO_x-Scavenging from Interfacial Layer on $Si_{1-x}Ge_x$ Channel for High Mobility $Si/Si_{1-x}Ge_x$ CMOS Application

C. H. Lee, H. Kim*, P. Jamison, R. G. Southwick III, S. Mochizuki, K. Watanabe, R. Bao, R. Galatage*, S. Guillaumet**, T. Ando, R. Pandey*, A. Konar*, B. Lherron**, J. Fronheiser*, S. Siddiqui*, H. Jagannathan, V. Paruchuri

IBM Research, *GLOBALFOUNDRIES Inc., **STMicroelectronics
257 Fuller Road, Suite 3100, Albany, NY 12203



(a)



(b)

Fig. 7 (a) Cross-sectional TEM image of gate stack showing MG/HK/IL/$Si_{0.6}Ge_{0.4}$ channel. The selective GeO_x-scavenging process was carried out right after the IL formation and there is no change of SiGe profile and surface roughness in the channel region. **(b)** Split-CV of $Si_{0.6}Ge_{0.4}$(100) pFET with GeO_x-free IL. A very small frequency dispersion in the depletion region indicates the low interface defects. (EOT ~0.9 nm)

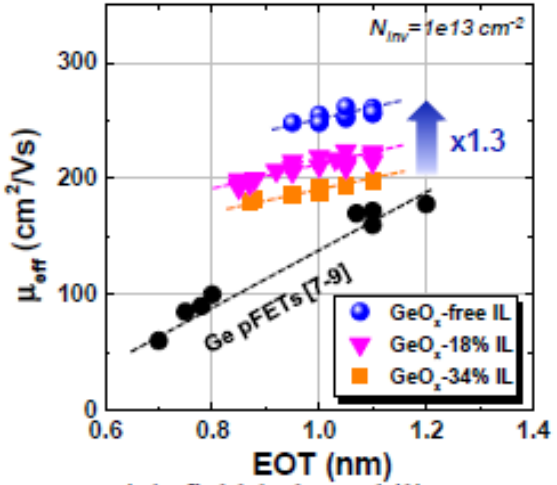


Fig. 10 High-field hole mobility vs. EOT in $Si_{0.6}Ge_{0.4}$(100) pFETs. Devices with GeO_x-free IL exhibit about 30% higher mobility than those with a $SiGeO_x$ (34%) IL. They also outperforms pure Ge pFETs [7-9].

40%-SiGe-Fin Hole mobility=250

Demonstration of Record SiGe Transconductance and Short-Channel Current Drive in High-Ge-Content SiGe PMOS FinFETs with Improved Junction and Scaled EOT

Pouya Hashemi, Kam-Leung Lee, Takashi Ando, Karthik Balakrishnan, John A. Ott, Syuranga Koswatta, Sebastian U. Engelmann, Dae-Gyu Park, Vijay Narayanan, Renee T. Mo and Effendi Leobandung
IBM Research, Thomas J. Watson Research Center, 1101 Kitchawan Rd., Yorktown Heights, NY 10598, USA.

- SGOI fabrication, fin patterning, 3D Ge condensation [7]
- Various scaled IL splits, HK/MG deposition and treatment, poly-Si deposition
- Gate hard mask, gate stack lithography/RIE
- Split for hot BF_2 I/I and splits for I/I-free: thick (~9-10nm) and thin (~5-6nm) spacers
- In-situ B-doped raised-S/D SiGe epitaxy
- S/D activation at 800°C for hot I/I split and up to 900°C for I/I-free splits
- Silicide offset spacer formation
- NiPt salicidation

Fig. 1 Process flow to fabricate HGC SiGe pMOS FinFETs, featuring a gate first HK/MG flow with various splits for EOT scaling and junction.

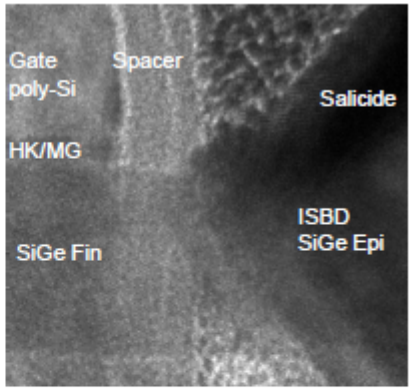


Fig. 2 High-resolution TEM image of a HGC SiGe fin under spacer for a device with junction formed by hot I/I. No crystalline defect was observed under the spacer, as confirmed from various images.

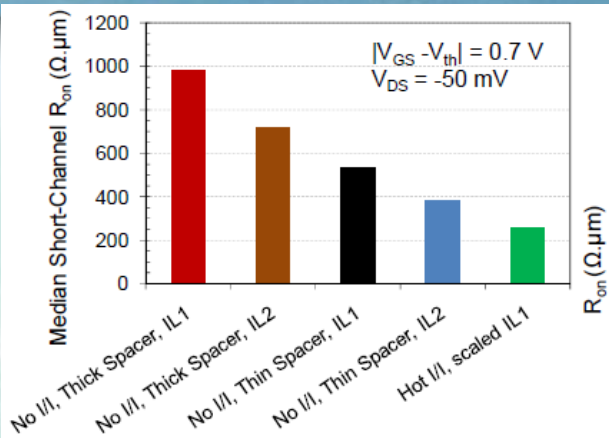
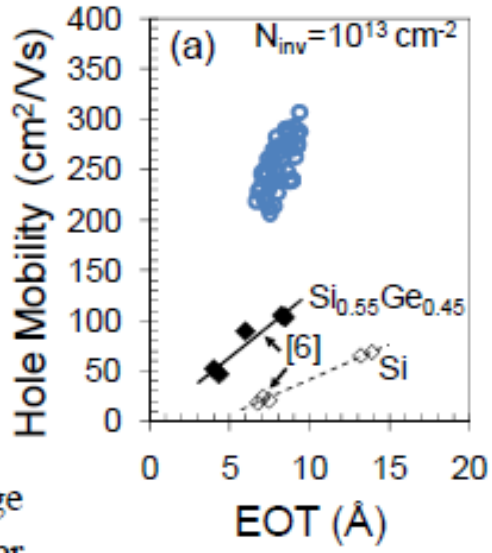
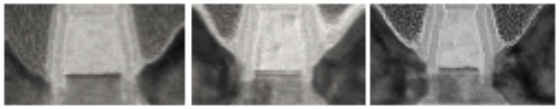


Fig. 5 Median short-channel R_{on} (L_G=30±10nm), measured at $|V_{GS}-V_{th}|$=0.7V and V_{DS}=-50mV, for various gate stack and splits, including I/I-free junctions with two spacer thicknesses and hot I/I. Higher V_{th} of IL1, which is also present under spacers, may lead to higher R_{ext} for an under-lapped I/I free device. By choosing IL2 under spacer, we are able to significantly reduce the R_{on} for I/I free devices.

60%-SiGe Fin Hole mobility=325



I-free process.



Junction	hot I/I	I/I -free	I/I -free
Physical L_G	37nm	33nm	25nm
SS at V_{DS}=-50mV	80mV/dec	75mV/dec	77mV/dec
SS at V_{DS}=-0.5V	80mV/dec	77mV/dec	86mV/dec
DIBL	57mV	24mV	40mV
V_{DD}	0.5V	0.5V	0.5V
I_{on} at fixed HP I_{off}	0.45mA/μm	0.45mA/μm	0.43mA/μm
I_{eff} at fixed HP I_{off}	0.210mA/μm	0.214mA/μm	0.187mA/μm

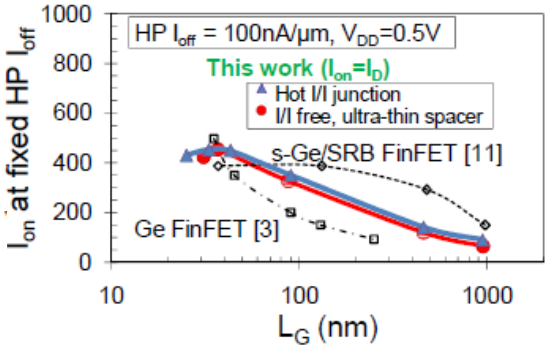


Fig. 14 I_{on} (=I_D) at target HP I_{off}=100nA/μm at V_{DD}=0.5V of HGC SiGe FinFETs of this work vs. physical L_G. Overlaid are the best FinFET data for bulk Ge [3] and s-Ge/SRB [11], with only reports available for source current. **At a fixed HP I_{off}=100nA/μm and V_{DD}=0.5V, we demonstrate the highest SiGe FinFET I_{on} and the highest PFET performance reported to date at L_G<35nm.**

Replacement High-K/Metal-Gate High-Ge-Content Strained SiGe FinFETs with High Hole Mobility and Excellent SS and Reliability at Aggressive EOT ~7Å and Scaled Dimensions Down to Sub-4nm Fin Widths

P. Hashemi, T. Ando, K. Balakrishnan, E. Cartier, M. Lofaro, J. A. Ott, J. Bruley, K.-L. Lee, S. Koswatta, S. Dawes, J. Rozen, A. Pyzyna, K. Chan, S. U. Engelmann, D.-G. Park, V. Narayanan, R. T. Mo and E. Leobandung
IBM Research, Thomas J. Watson Research Center, 1101 Kitchawan Rd., Yorktown Heights, NY 10598, USA.

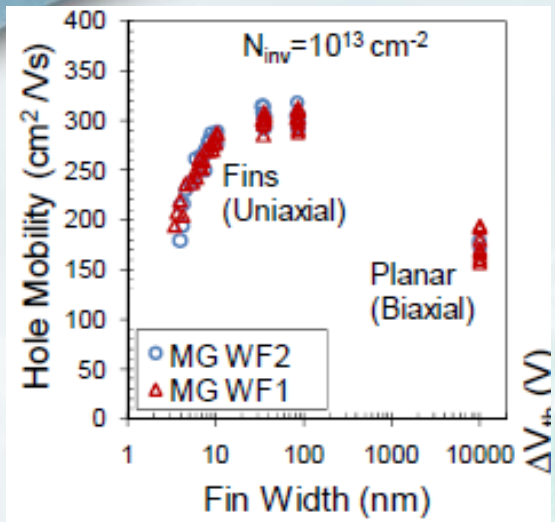


Fig. 12 Mobility vs. average W_{FIN} for a wide range of device widths, including planar, wide to sub-10nm-wide fins. μ_{eff} is nearly insensitive to the MG WF splits (WF2-WF1~70mV) and sharply decreases for narrow fins. Nevertheless, **we report a very high pFET μ_{eff}=235cm²/Vs at EOT~7Å for ultra-scaled fins with average W_{FIN}=4.6nm, which is very promising for 5nm-node.**

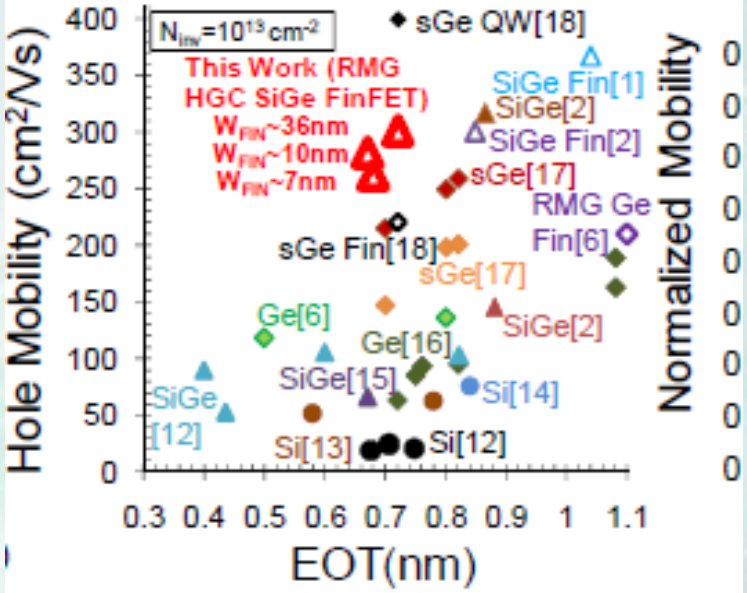


Fig. 15 Mobility benchmark for RMG HGC SiGe FinFETs of this work along with sub-1.1nm EOT data for Si (circles), SiGe (triangles) and Ge (diamonds) (close: planar, open : FinFETs); **Our data is over 5X higher than planar Si at EOT~0.7nm and outperforms state-of-the-art FinFETs at such EOT.**

60%-Ge
µh=220
µh=235

VLSI-2016 paper 9.3

Smart Solutions for Efficient Dual Strain Integration for Future FDSOI Generations

A. Bonnevialle[2,1,3], C. Le Royer[1], Y. Morand[2], S. Reboh[1], C. Plantier[1], N. Rambal[1], J.-P. Pédini[2], S. Kerdiles[1], P. Besson[1,2], J.-M. Hartmann[1], D. Marseilhan[1], B. Mathieu[1], R. Berthelon[1,2], M. Cassé[1], F. Andrieu[1], D. Rouchon[1], O. Weber[1], F. Bœuf[2], M. Haond[2], A. Claverie[3], M. Vinet[1]

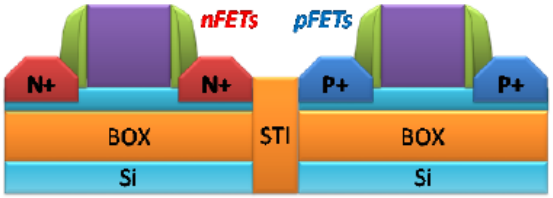
[1] *CEA, LETI*, Minatec Campus, F-38054 Grenoble, France;
[2] *STMicroelectronics*, 850 rue Jean Monnet, 38926 Crolles, France; [3] *CEMES-CNRS*, 29 rue J. Marvig, 31400 Toulouse France

Abstract

We present deep insights on the integration and physics of two new strain boosters for FDSOI CMOS. "STRASS" and "BOX creep" techniques (for tensily and compressively stressed channels, respectively) are for the first time integrated in a localized manner on a state-of-the-art 14nm FDSOI route. STRASS enables to achieve +1.6 GPa in SOI active regions (w.r.t. +1.3 GPa for thin BOX sSOI). BOX creep process leads to more than +10% in hole mobility and +6% in Ieff(Ioff) plots. The BOX creep efficiency is investigated with respect to device dimensions: the electrical data evolution matches the proposed mobility model based on 2D simulated stress profiles.

30% c-SiGe
STRASS: +1.6GPa tensile strain-Si→μ_e=+60%
BOX-Creep: μ_h=+10%

Dual localized strained channels for sub 14nm FDSOI:
tensile Si + compressive SiGe



FDSOI node	nFET channel	pFET channel
28nm	Si	Si
14nm	Si	compressive SiGe
sub 14nm	tensile Si >+1.5GPa	comp. SiGe <-2GPa
Strain boosters	STRASS, BOX creep	BOX creep, SAIPS

Fig.1: Schematics of advanced FDSOI CMOS, featuring highly strained Si and SiGe channels, with studied strain boosters for n/pFETs.

STRASS = Strained Si by Top Recrystallization of Amorphized SiGe on SOI

a) SiGe Epitaxy on SOI (relaxed Si)
b) Buried amorphization by ion implantation
c-d) Top-down recrystallization (anneal)
e) SiGe removal

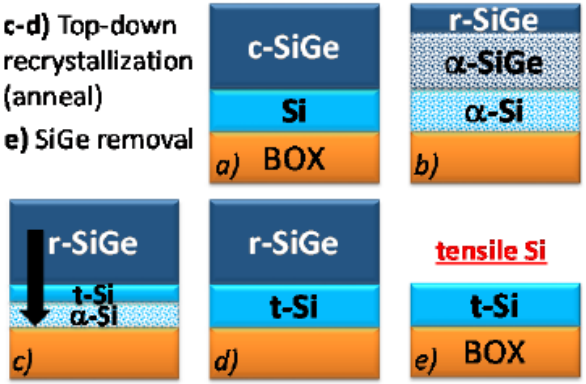


Fig.2: Schematics of the **STRASS** process to fabricate tensile Si on insulator. The top relaxed SiGe seed (b) imposes its lattice parameter to the Si film (c-d) [8,9].

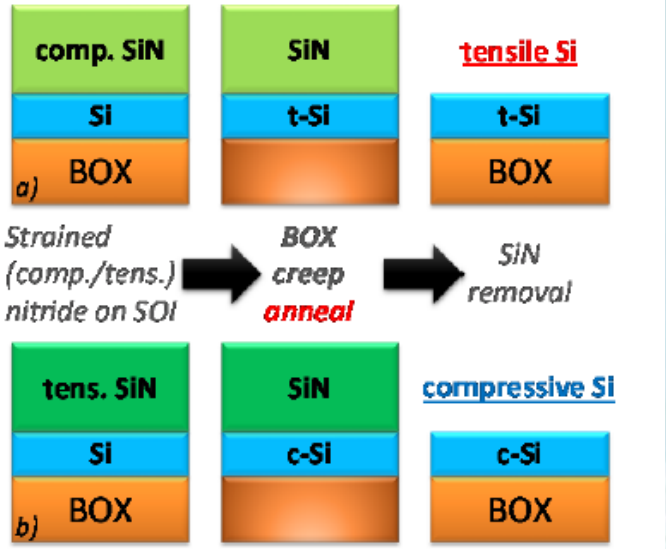


Fig.3: Principle of the **BOX creep** technique applied to the fabrication of a) tensile Si (+1.2 GPa demonstrated in [6]) and b) compressive Si, depending on the SiN stress.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

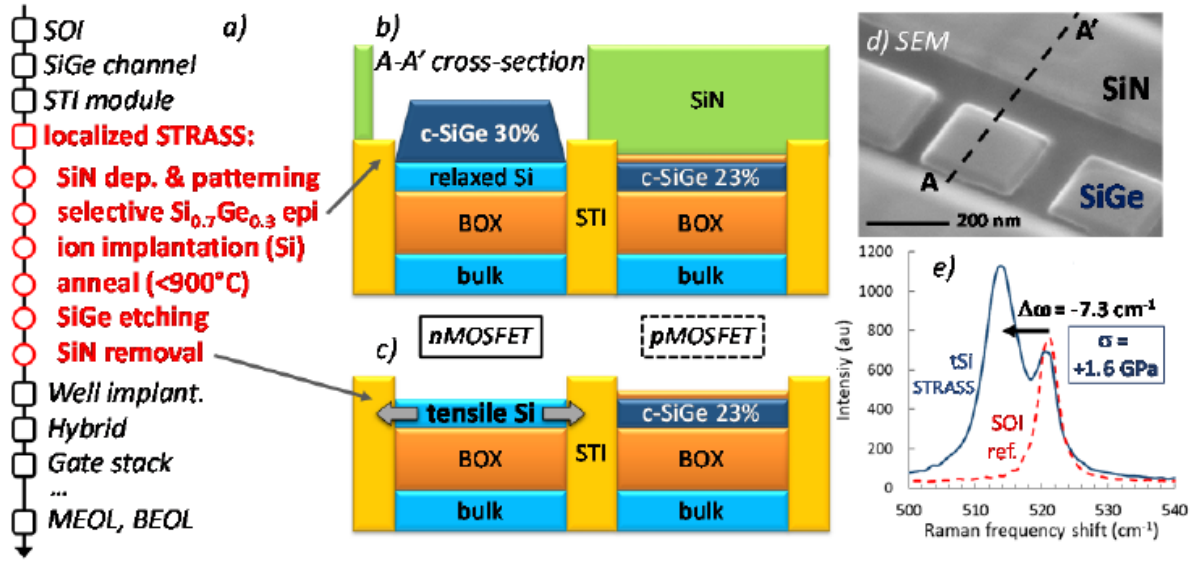
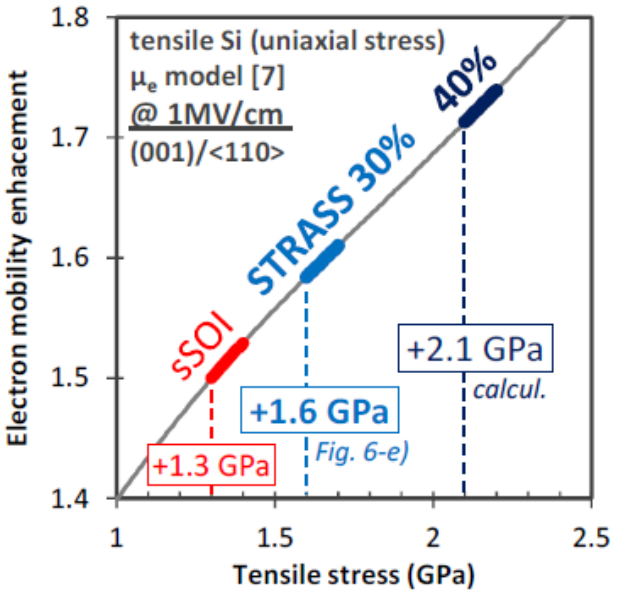


Fig.6: **STRASS** module integration for dual-strain FDSOI CMOS. a) Flow of the experiments, with n/p FETs schematics (b, c); d) Top view SEM picture after selective 40nm $Si_{0.7}Ge_{0.3}$ epitaxy (nFET); e) Tensile Stress in 1x4µm² SOI nFETs (after STRASS) by Raman spectroscopy: + **1.6 GPa** is demonstrated ($\Delta\omega_{Si} = \omega_{STRASS} - \omega_{ref} = -7.3\ cm^{-1}$).



ig.7: Electron mobility gains expected with TRASS technique. +1.6 GPa (exp. data ith SiGe 30%) for STRASS can be further nhanced with 40% Ge content.

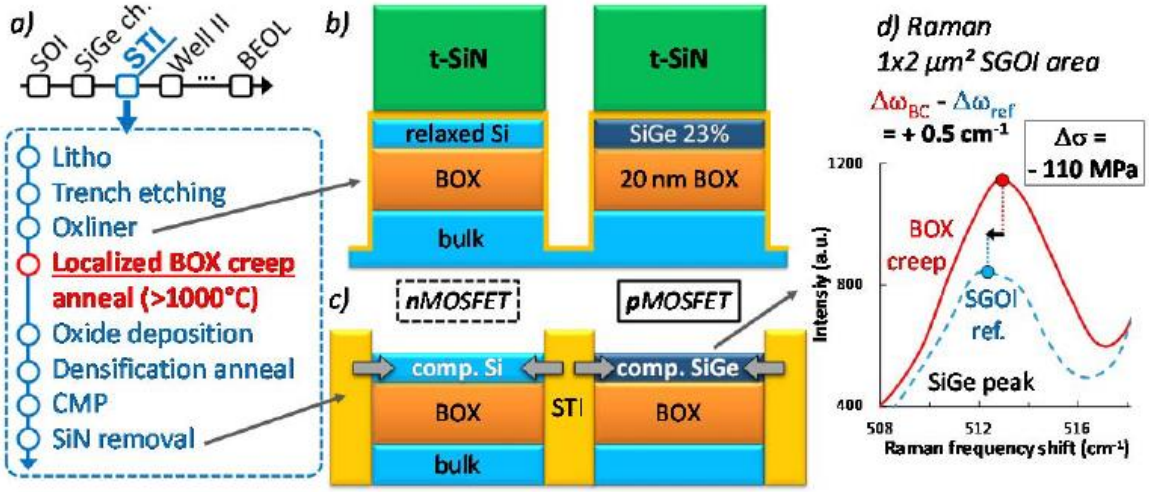


Fig.8: **BOX creep (BC)** module integration. a) Experiment flow, b-c) n/p FETs schematics, d) **-110 MPa** additional stress (Δσ) is evidenced in wide SGOI area by Raman spectroscopy.

High Performance CMOS FDSOI Devices activated at Low Temperature

L. Pasini[1,2,3], P. Batude[1], J. Lacord[1], M. Casse[1], B. Mathieu[1], B. Sklenard[1], F. Piegas Luce[1], J. Micout[1,3], A. Payet[1], F. Mazen[1], P. Besson[1], E. Ghegin[1,2], J. Borrel[1,2], R. Daubriac[4], L. Hutin[1], D. Blachier[1], D. Barge[2], S. Chhun[2], V. Mazzocchi[1], A. Cros[2], J-P. Barnes[1], Z. Saghi[1], V. Delaye[1], N. Rambal[1], V. Lapras[1], J. Mazurier[1], O. Weber[1], F. Andrieu[1], L. Brunet[1], C. Fenouillet-Beranger[1], Q. Rafhay[3], G. Ghibaudo[3], F. Cristiano[4], M. Haond[2], F. Boeuf[2] and M. Vinet[1]

[1]CEA- Leti, Minatec Grenoble, [2]STMicroelectronics Crolles, [3]IMEP-LAHC, Minatec Grenoble INP, [4]LAAS-CNRS, Toulouse FRANCE

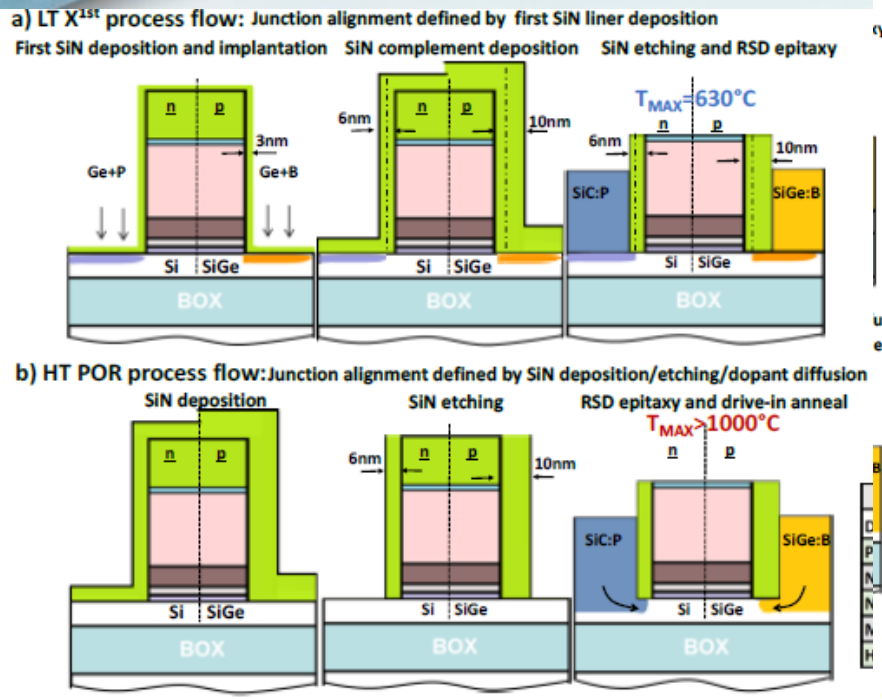
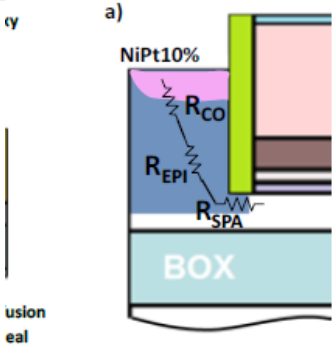


Fig.1: a) LT X[1st] integration process flow. Implantation through thin liner enables to place dopants at the channel entrance **b)** HT POR process flow. Dopants are activated by HT thermal anneal and driven by diffusion in the region below the spacer.



b)

	nMOS		pMOS		amorph. depth
Dose (at/cm³)	PAI (Ge)	P	PAI (Ge)	B	
POR	0	0	0	0	0
No Implant	0	0	0	0	0
No PAI	0	D2	0	D2	0
Medium PAI	D1	D2	D1	D2	~1nm
High PAI	2.4D1	D2	2.4D1	D2	~2nm

Fig.2: a) R_{ACCESS} main contributions: NiPt/Si contact resistance (R_{CO}), epitaxial region (R_{EPI}), region below the spacer (R_{SPA}) **b)** Devices split table.

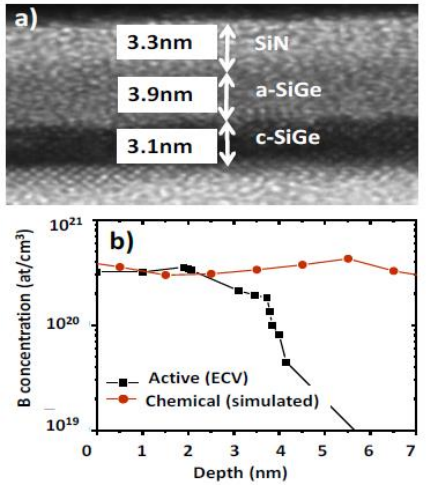


Fig.3: a) TEM micrograph showing a partial amorphization of the thin SiGe film. **b)** Active B concentration profile (ECV) obtained after 630°C annealing compared to total B. An activation level of $3x10^{20}$ at/cm³ is achieved.

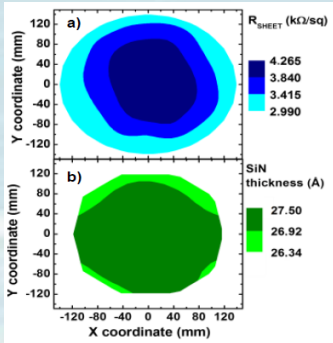


Fig.4: **a)** R_{SHEET} mapping on 300mm wafer of a 6nm SiGe film activated by SPE at 630°C. **b)** Thickness mapping of the thin SiN liner used to define the junction position in the X[1st] integration on 300mm wafer (Δ_{TH}<1Å).

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

VLSI-2016 paper 13.2

High performance $In_{0.53}Ga_{0.47}As$ FinFETs fabricated on 300 mm Si substrate

M. L. Huang, S. W. Chang, M. K. Chen, Y. Oniki, H. C. Chen, C. H. Lin, W. C. Lee, C. H. Lin, M. A. Khaderbad, K. Y. Lee, Z. C. Chen, P. Y. Tsai, L. T. Lin, M. H. Tsai, C. L. Hung, T. C. Huang, Y. C. Lin, Y.-C. Yeo, S. M. Jang, H. Y. Hwang, Howard C.-H. Wang, and Carlos H. Diaz
Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu 300, Taiwan

Process flow

- III-V epi. on 300mm Si
- Fin formation
- N^+-S/D
- HK deposition
- MG deposition
- S/D contact metal dep.
- Metallization

Fig. 1 Process flow for the InGaAs FinFET fabrication. Fin dimension was controlled by InGaAs epi-layer thickness and dry/wet etch conditions.

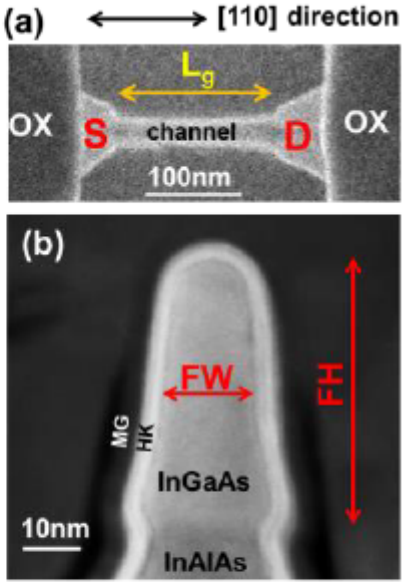


Fig. 2 (a) Top view SEM and (b) cross-sectional TEM images of the InGaAs FinFET.

InGaAs μe=12,000cm2/V-s

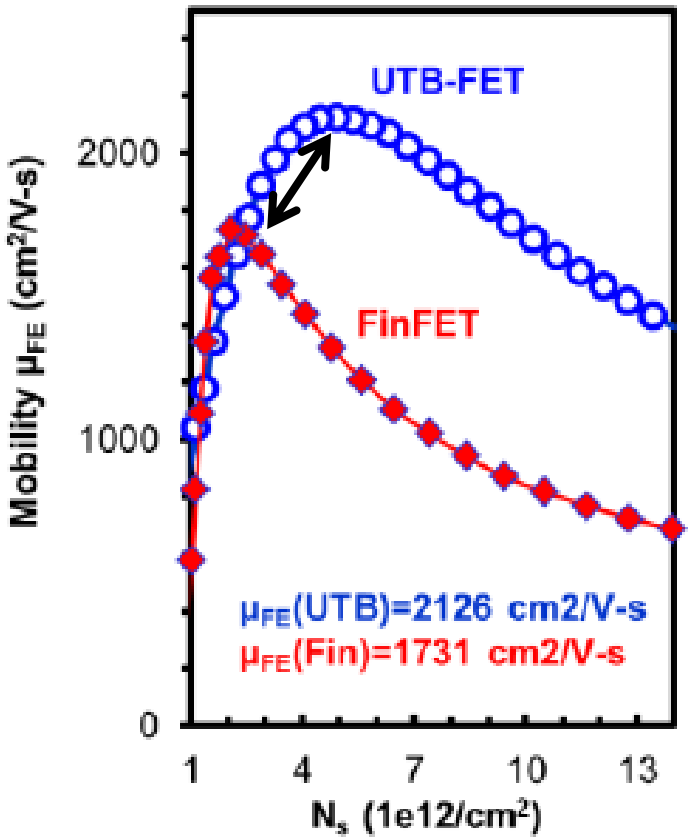


Fig. 13 Extracted field effect mobility (μ_{FE}) vs. N_s for UTB-, and Fin- FET.

Record mobility (μ_{eff} ~3100 cm^2/V-s) and reliability performance (V_{ov}~0.5V for 10yr operation) of $In_{0.53}Ga_{0.47}As$ MOS devices using improved surface preparation and a novel interfacial layer

A. Vais[1], A. Alian, L. Nyns, J. Franco, S. Sioncke, V. Putcha[1], H. Yu[1], Y. Mols, R. Rooyackers, D. Lin, J.W. Maes[2], Q. Xie[2], M. Givens[3], F. Tang[3], X. Jiang[3], A. Mocuta, N. Collaert, K. De Meyer[1], A. Thean
IMEC and also at [1]KULeuven; [2]ASM Belgium; [3]ASM America, Phoenix, AZ, USA. e-mail: Abhitosh.Vais@imec.be

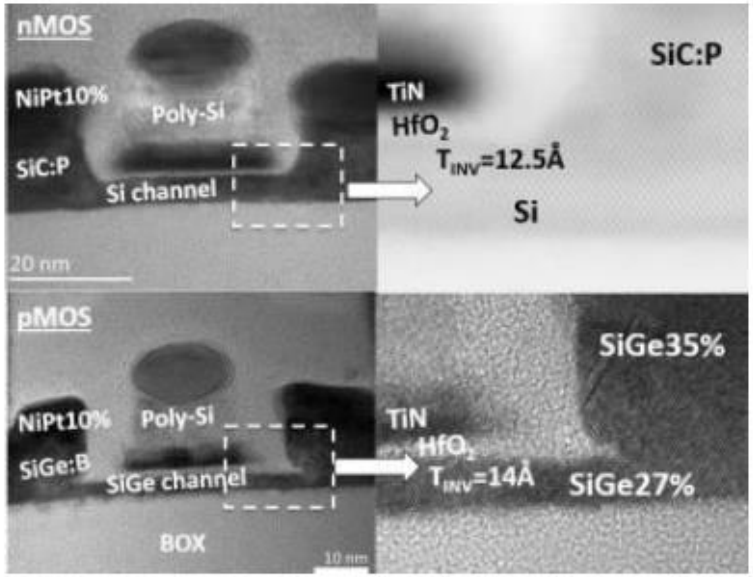


Fig.5: TEM micrographs of n & pMOS Medium PAI splits transistors fabricated with LT X^{1st} process. Good epitaxial growth quality on the implanted region is observed.

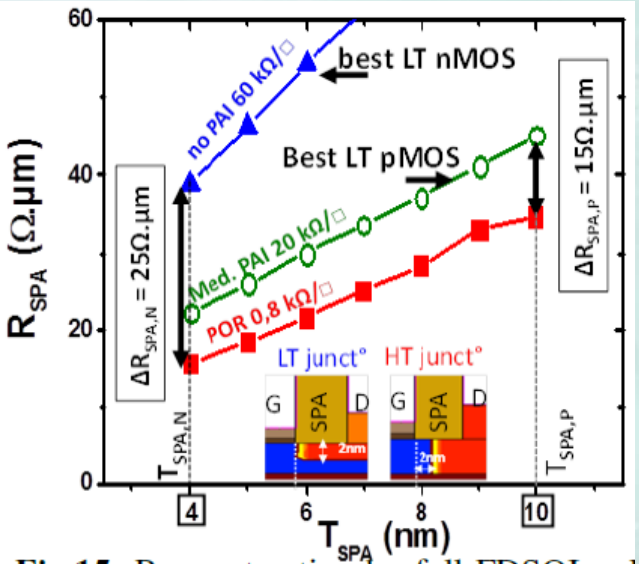


Fig.15: R_{SPA} extraction by full FDSOI device TCAD simulation (SDEVICE) as a function of the spacer thickness for various R_{SHEET} values. For both n&pFETs, the ΔR_{SPA} and ΔR_{CO} are consistent with the measured R_{ACCESS} difference between LT and POR splits.

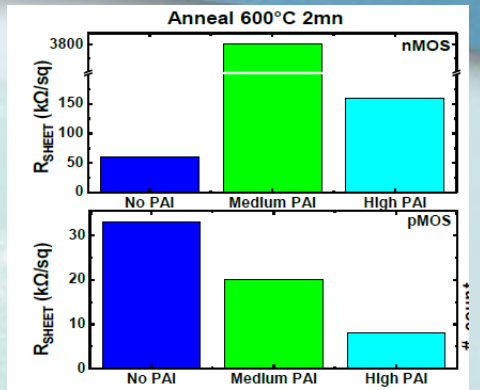


Fig. 13: R_{SHEET} measurements on a 6 nm Si film implanted with the conditions reported in Fig.2b. Expected evolution is observed for the pFET case, i.e. R_{SHEET} decreases with the amorphization depth. For n-type the values are not consistent with usual SPE activation levels.

μ_e=3100

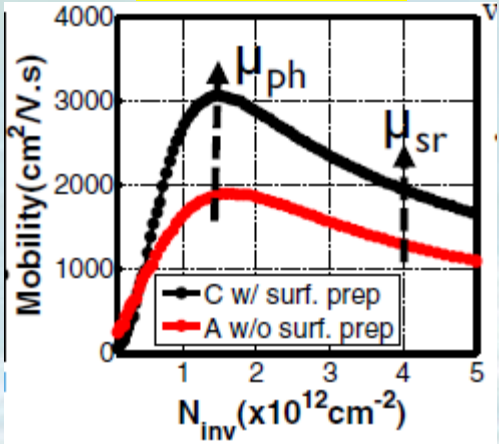


Fig. 11. A combined improvement in mobility, as a result of new IL and optimized processing

InAs Nanowire GAA n-MOSFETs with 12-15 nm Diameter

T. Vasen, P. Ramvall, A. Afzalian, C. Thelander[1], K.A. Dick[1], M. Holland, G. Doornbos, S.W. Wang, R. Oxland, G. Vellianitis, M.J.H. van Dal, B. Duriez, J.-R. Ramirez[2], R. Droopad[2], L.-E. Wernersson[1], L. Samuelson[1], T.-K. Chen[3], Y.-C. Yeo[3], and M. Passlack

TSMC, Kapeldreef 75, 3001 Leuven, Belgium; [1]Lund University, Lund, Sweden; [2]Texas State University, San Marcos TX, USA; [3]TSMC, Hsinchu, Taiwan 300-75 R.O.C.; Email: matthias_passlack@tsmc.com

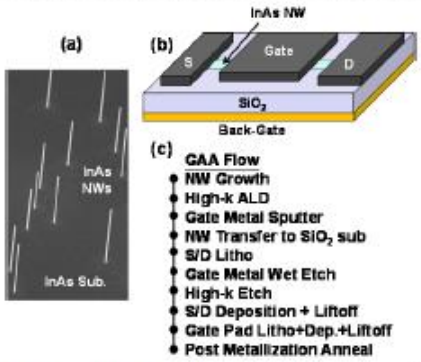


Fig. 1. (a) SEM image of as-grown InAs NWs, (b) schematic of completed device structure in lateral flow, and (c) gate all around (GAA) process steps.

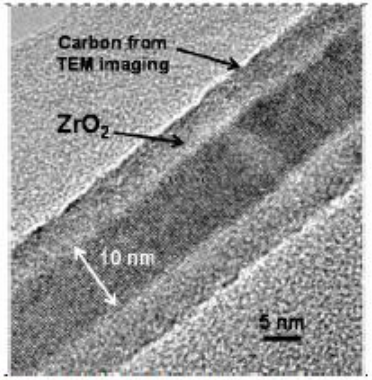


Fig. 2. HRTEM image along a NW with 4 nm ZrO_2 high-k and with d = 10 nm. The InAs crystal structure is wurtzite with no visible stacking faults.

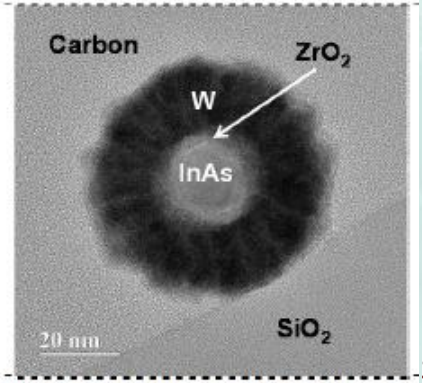


Fig. 3. TEM cross section image through the gate of the InAs NW GAA device with d = 15 nm, 3.5-4 nm ZrO_2 high-k and W gate metal.

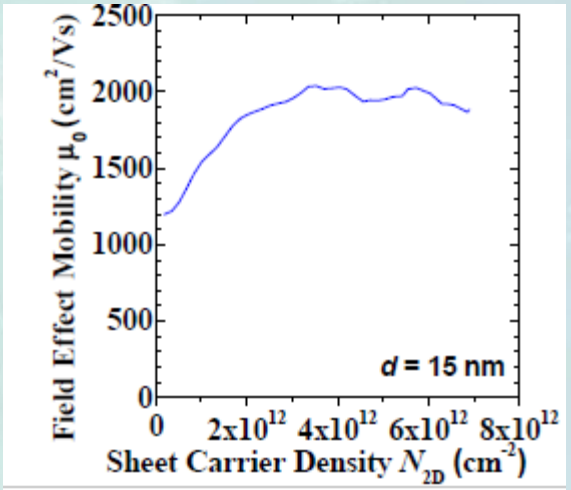
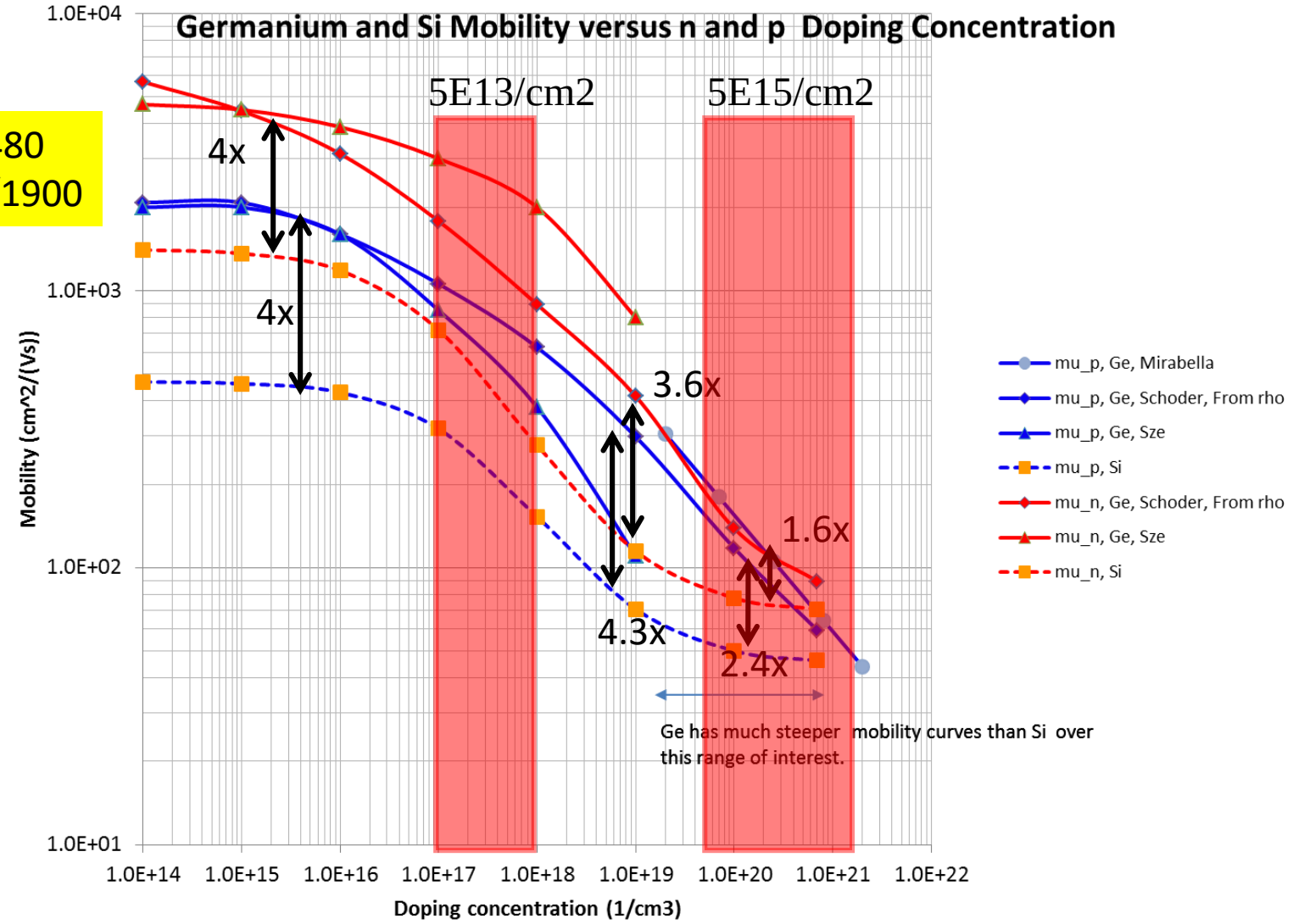


Fig. 13. Field-effect mobility μ_0 extracted from the measured linear transconductance at V_d = 0.05 V vs. equivalent sheet carrier density for the InAs NW device of Fig. 12. To compare with planar $N_{2D} \equiv N_{1D} / \pi d$ is plotted

InAs μ_e=2040

InAs μe should=40,000cm2/V-s

Si=1390/480
Ge=3900/1900



At 1E20/cm3 channel doping level Ge mobility only 2x of Si for electron and hole!

Ultralow-Resistivity CMOS Contact Scheme with Pre-Contact Amorphization Plus Ti (Germano-)Silicidation

H. Yu[1,2], M. Schaekers[1], A. Hikavyy[1], E. Rosseel[1], A. Peter[1], K. Hollar[3], F. A. Khaja[3], W. Aderhold[3], L. Date[3], A. J. Mayur[3], J.-G. Lee[4], K. M. Shin[5], B. Douhard[1], S. A. Chew[1], S. Demuynck[1], S. Kubicek[1], D. Kim[5], A. Mocuta[1], K. Barla[1], N. Horiguchi[1], N. Collaert[1], A.V.-Y. Thean[1], K. De Meyer[1,2]

[1]Imec, Kapeldreef 75, B-3001 Leuven, Belgium [2]Also at Katholieke Universiteit Leuven, Leuven, Belgium
[3]Applied Materials, Sunnyvale, USA [4]Samsung, Seoul, Korea [5]Samsung, assignee at imec, Leuven, Belgium

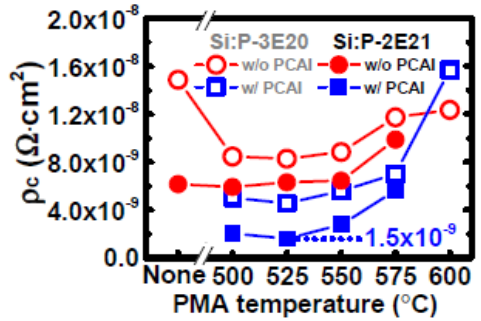


Fig. 1 ρ_c of Ti/Si:P or $TiSi_x$/Si:P as a function of PMA temperature [1]. $TiSi_x$ with PCAI has lower ρ_c. PCAI is with 3keV 6×10^{14} cm^{-2} Ge I/I. PMA window is 500-550°C 1min N_2 RTP.

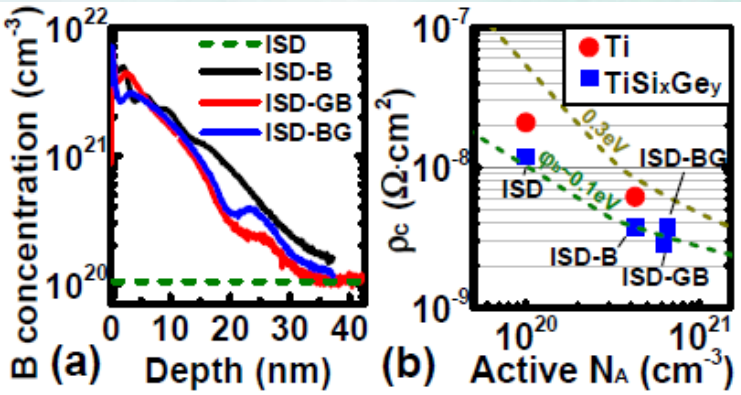


Fig. 10 (a) SIMS B profile; (b) summary of ρ_c-N_A on SiGe:B combining SIMS, Hall, and ρ_c results. Dash lines in (b) are simulated ρ_c-N_A curves with field emission theory [9].

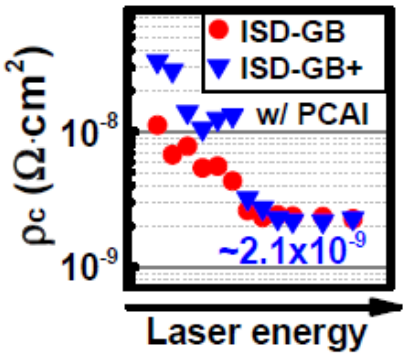


Fig. 11 ρ_c of Ti/SiGe:B on ISD-GB and ISD-GB+ with ns laser B activation. Samples are with PCAI and 500°C PMA.

- 300mm lightly doped Si wafer
- n-well formation
- SiGe:B epitaxy
- B I/I & activation
- MR-CTLM patterning:Dielectric deposition, lithography, and etching (SiGe surface at the contact region exposed)
- PCAI with Ge I/I
- Ti/TiN deposition
- PMA with 1min N_2 RTP
- Cu barrier deposition
- Cu plating and CMP

o Performed on only part of samples

Table I. SiGe:B samples defined by B doping methods.

Sample ID	B I/I dose (cm^{-2})*	Remark**
ISD	--	No extra B I/I
ISD-B	$3\times10^{15}+2\times10^{15}$	Extra B I/I
ISD-GB	$3\times10^{15}+2\times10^{15}$	Pre-B Ge AI
ISD-BG	$3\times10^{15}+2\times10^{15}$	Post-B Ge AI
ISD-GB+	$6\times10^{15}+2\times10^{15}$	Pre-B Ge AI

* Two-step B I/I: 1st with 2keV, and 2nd with 0.5keV
** Ge AI is with 10keV energy and 1×10^{15} cm^{-2} dose

Fig. 3 Process flow of MR-CTLM structure. Detailed B I/I conditions are in Table I. B I/I was followed by spike anneal or multi-pulse ns laser anneal for B activation. PCAI conditions are compared in Fig. 5.

SiP =2E21/cm^3 =2.1×10^{-9} Ω-cm^2
70%-SiGeB= 2.1×10^{-9} Ω-cm^2

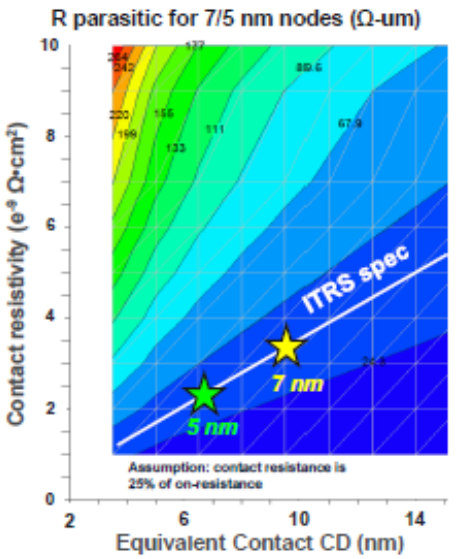
VLSI-2016 paper 7.1

Ultra-Low NMOS Contact Resistivity Using a Novel Plasma-Based DSS Implant and Laser Anneal for Post 7 nm Nodes

C.-N. Ni, K.V. Rao, F. Khaja, S. Sharma, S. Tang, J. J. Chen, K. E. Hollar, N. Breil, X. Li, M. Jin, C. Lazik, J. Lee
H. Maynard, N. Variam, A. J. Mayur, S. Kim, H. Chung, M. Chudzik, R. Hung, N. Yoshida, N. Kim
Applied Materials 3050 Bowers Avenue, Santa Clara, CA 95053, USA

VLSI-2016 paper 7.3

NMOS =1.2x10^{-9} Ω-cm^2 with msec DSA laser annealing
If nsec then <1x10^{-9} Ω-cm^2



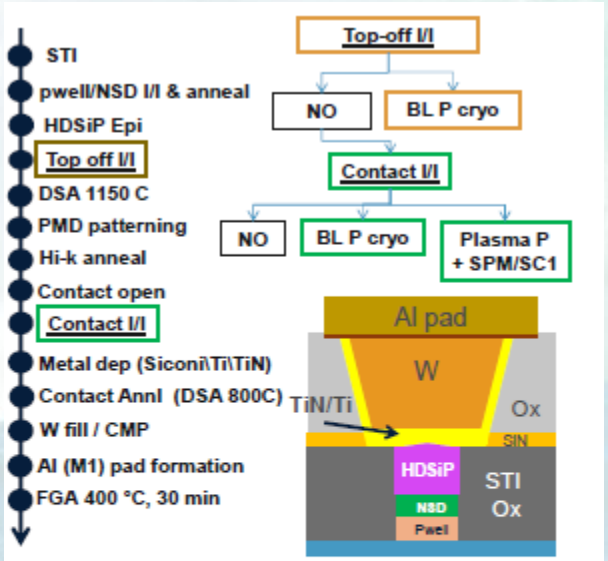


Figure 3. Process flow showing selective highly doped Si:P EPI with top-off or contact open implant. The inset is schematics of contact area

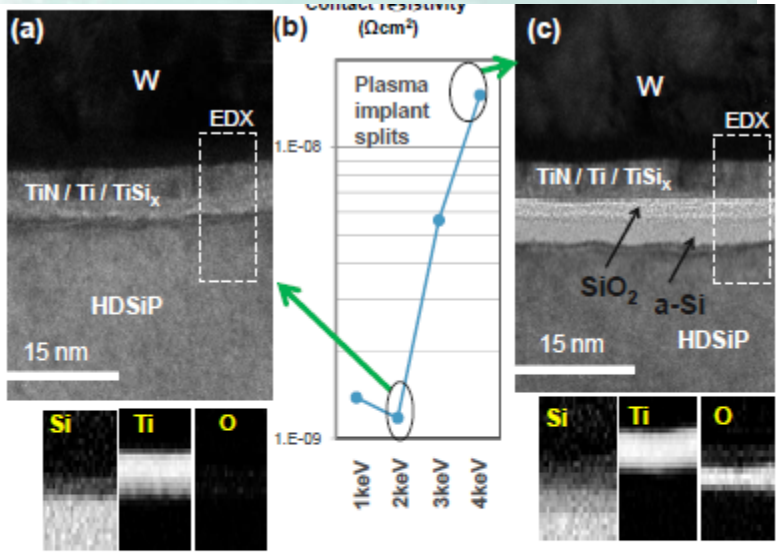


Figure 14. xTEM and EDX images from PLAD P 2keV and 4keV samples. Both a-Si layer and oxidation are seen at Ti/HDSiP interface of 4keV (higher Rc) sample.

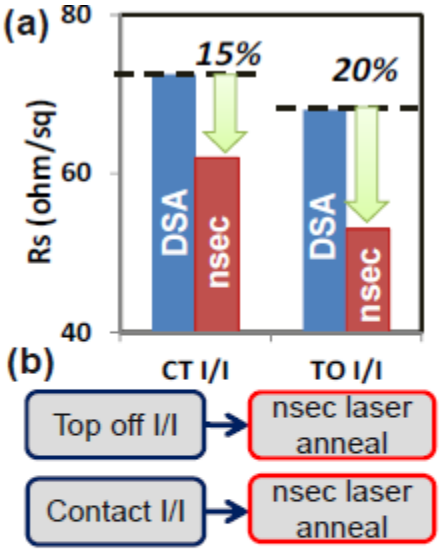


Figure 15. (a) Implanted /annealed HDSiP Rs are lower with nsec laser anneal than DSA. (b) Proposed new flow for NMOS low contact Rc

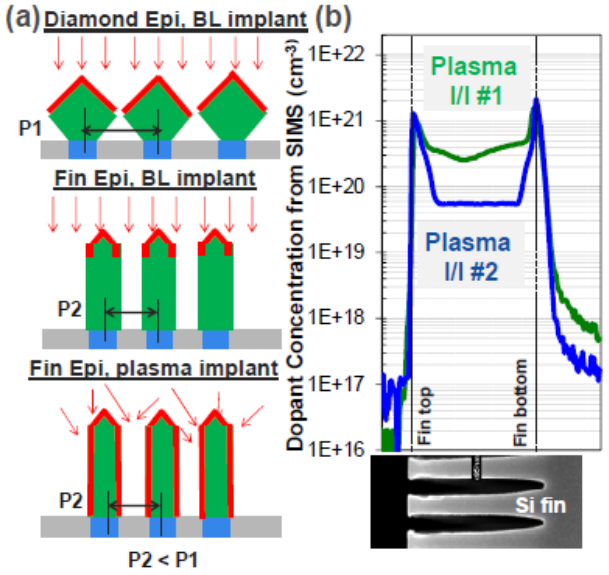


Figure 2. (a) Conformal implant for dopant boosting is needed for further fin scaling (b) SIMS plot showing good dopant conformality on Si fin

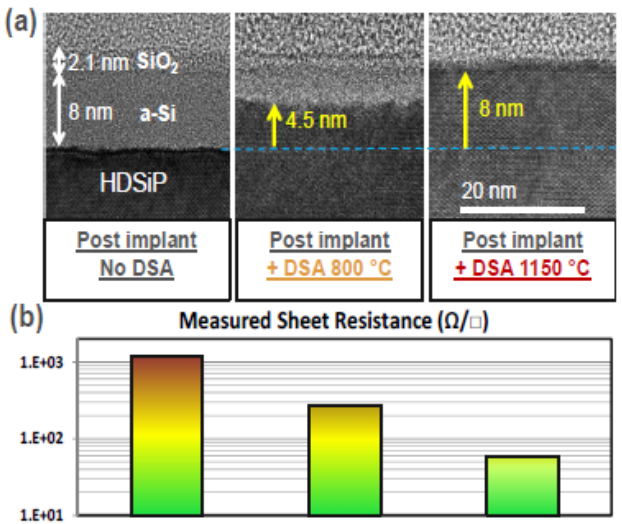


Figure 8. Epitaxial regrowth of HDSiP with laser anneal, with (a) cross-sectional TEM and (b) their corresponding sheet resistance.

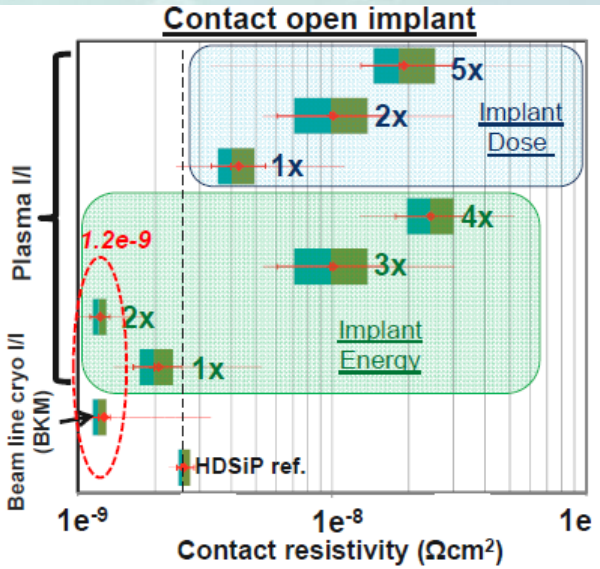


Figure 12. ρ_C of HD Si:P reference comparing to the ones with contact open implant energy and dose splits. Lowest Rc of $1.2e^{-9}$ Ωcm^2 is demonstrated. Post metal anneal is DSA 800 °C

VLSI Sym-2015 Paper 8-2 by Ni of **Applied** on "Ultra-Low Contact Resistivity with Highly Doped Si:P Contact for nMOSFET". This paper had similar results and message as reported last week at IWJT in Applied paper S4-1. Fig.1 shows the ITRS targets for contact resistivity at 10nm and 7nm nodes of 2-5E-9Ω-cm^2. Fig.2 shows the process flow and schematic of the doped contact structure to achieve low contact resistivity. Fig.5 shows the higher the in-situ doped epi dopant level the lower the contact resistivity going from P=7E19/cm^3 up to 2.5E21/cm^3 using DSA laser annealing to boost P-dopant activation. Using an additional P-Cryo top-off implant after S/D epi or contact opening with DSA annealing will further reduce resistivity as shown in Fig.10 with minimal strain relaxation as shown in Fig.11. So message is need to add more n+ S/D implants even with in-situ doped epi at 2E21/cm^3 doping level!

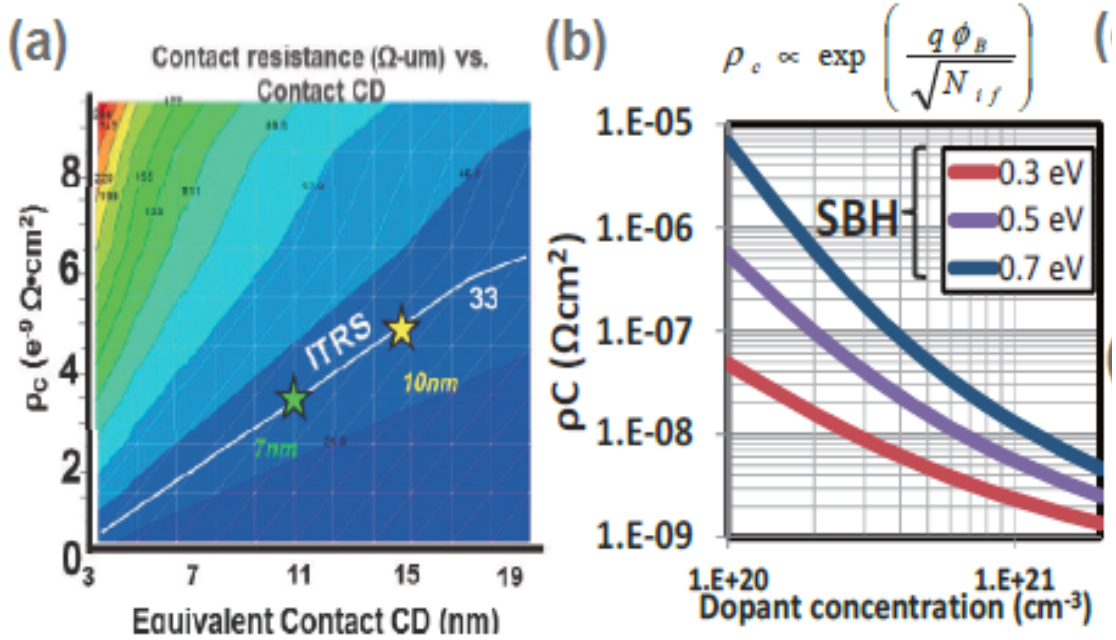


Figure 1. (a) ITRS predicted ρ_C of mid 1e^{-9} Ωcm^2 is required for 10/7-nm FinFET [1]. (b) Field-emission model simulates ρ_C as a function of SBH and n-dopant (c) Band alignment of Ti on n-Si. (d) Band alignment of Ti on highly doped Si:P showing reduced barrier thickness (δ)

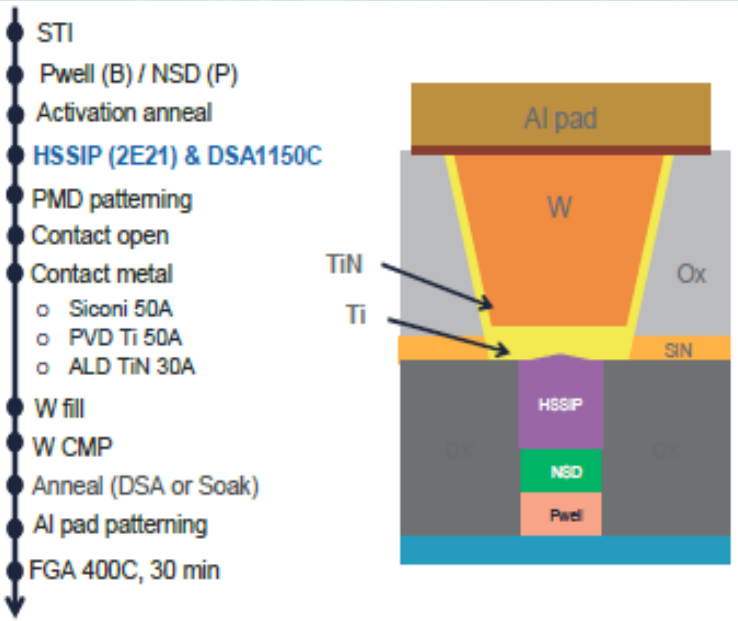


Figure 2. Detailed process flows showing selective highly doped Si:P EPI is processed prior to Ti/TiN contact metal deposition.

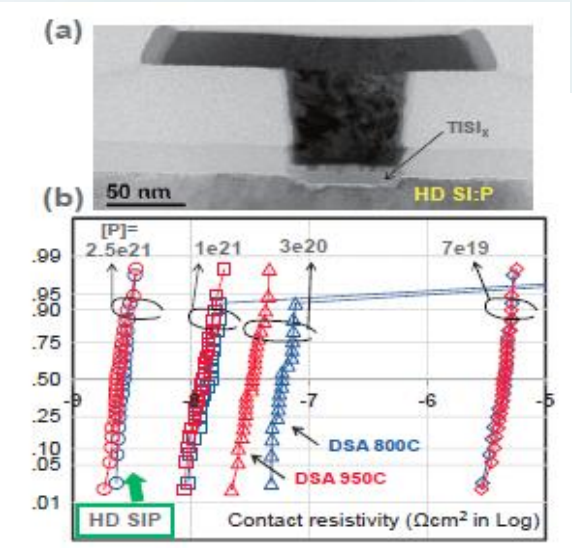


Figure 5. (a) TEM of kelvin contact test vehicle with Ti contacting on HD Si:P (b) ρ_C of Ti/Si:P contact as a function of n-dopant concentration.

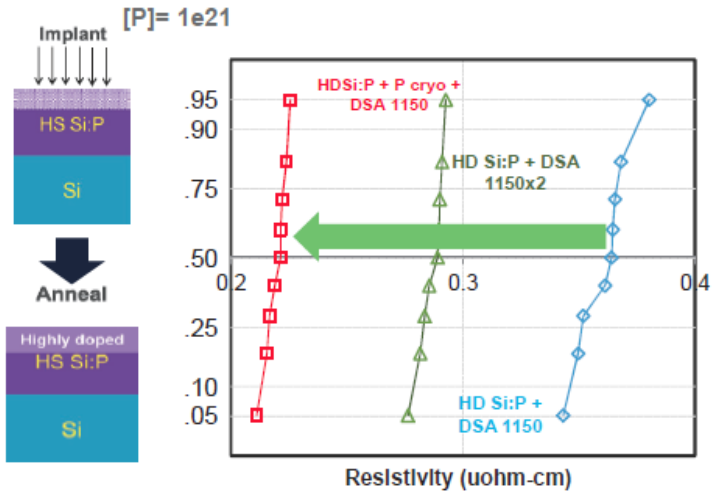


Figure 10. Sheet resistance measurement comparing pre- and post P cryo implant+anneal into HD Si:P. Rs improved with additional implant

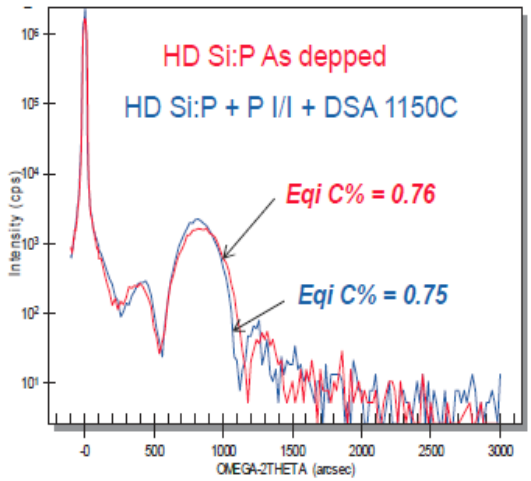


Figure 11. X-ray diffraction pattern shows no HD Si:P film relaxation after P implant and high temperature DSA anneal

Session 7: Contact Resistance Innovations for Sub-10nm Scaling

Sub-$2x10^{-9}$ Ω-cm^2 N- and P-Contact Resistivity with Si:P and Ge:Ga Metastable Alloys for FinFET CMOS Technology

GF and IBM Research

UTEK nsec LTA

Paper Withdrawn and Not Published!

Ultra low p-type SiGe contact resistance FinFETs with Ti silicide liner using cryogenic contact implantation amorphization and Solid-Phase Epitaxial Regrowth (SPER)

Y.R. Yang, N. Breil[1], C.Y. Yang, J. Hsieh, F. Chiang, B. Colombeau[1], B.N. Guo[2], K.H. Shim[2], N. Variam[2], G. Leung[1], J. Hebb[1], S. Sharma[1], C.N. Ni[1], J. Ren[1], J. Wen[1], J.H. Park[1], H. Chen[1], S. Chen[3], M. Hou[3], D. Tsai[3], J. Kuo[3], D. Liao[3], M. Chudzik[1], S.H. Lin, H.F Huang, N.H. Yang, J.F. Lin, C.T. Tsai, G.C. Hung, S.C. Hsu, O. Cheng, J.Y. Wu and T.R. Yew

United Microelectronics Corporation (UMC), Advanced Technology Development, No. 18, Nanke 2nd Rd, Tainan, Taiwan 74147

[1] – Applied Materials, 3050 Bowers Avenue, Santa Clara, CA 95053, USA

[2] – Applied Materials – Varian Semiconductor Equipment, 35 Dory Road, Gloucester, MA 01930, USA

[3] – Applied Materials Taiwan, Nanke 7th Rd, Tainan, Taiwan 741

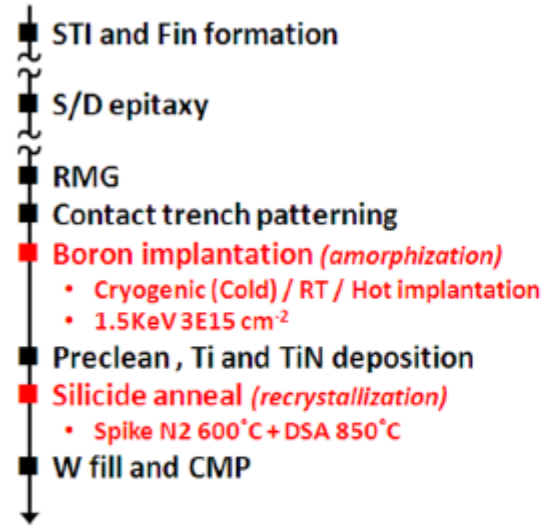


Fig.1: Process flow for the FinFET devices used in this experiment

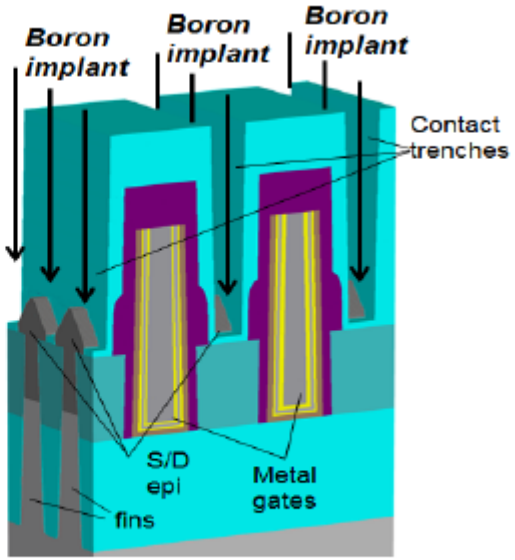


Fig.2: 3D schematic shows the boron implantation into contact trench.

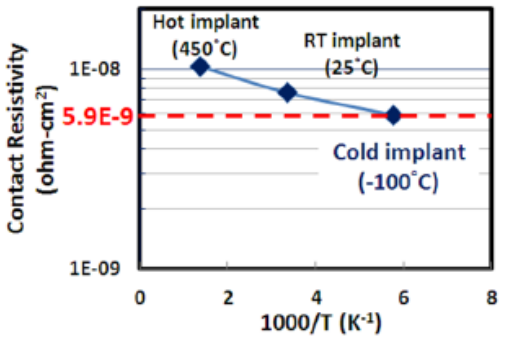


Fig.10: The contact resistivity vs. 1000/T plot shows an Arrhenius dependency. The best result for the cold implant demonstrates a record low contact resistivity of 5.9×10^{-9} ohm-cm^2.

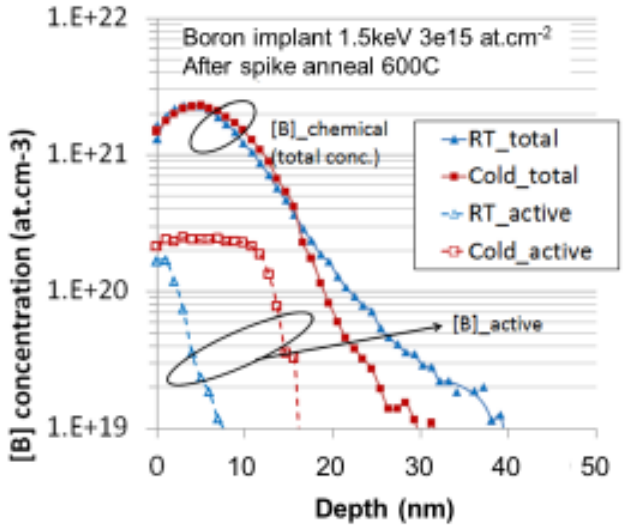


Fig.4: TCAD simulation showing comparable total boron concentration profiles for RT and cryogenic (cold) implants post anneals, and highlighting a significant activation improvement with cryogenic (cold) implant.

P-contact =5.9x10^{-9} Ω-cm^2

Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates

H. Mertens, R. Ritzenthaler, A. Hikavyy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel, T. Schram, K. Devriendt, D. Tsvetanova, H. Dekkers, S. Demuynck, A. Chasin, E. Van Besien, A. Dangol, S. Godny, B. Douhard, N. Bosman, O. Richard, J. Geypen, H. Bender, K. Barla, D. Mocuta, N. Horiguchi, A.V-Y Thean

- Starting material: Bulk Si wafer
- Ground plane I/I + anneal (a)
- SiGe/Si/SiGe/Si epitaxy (b)
- Spacer-defined fin patterning (SADP)
- Low-temperature STI filling (c)
- Dummy gate patterning
- Extension I/I + Spacer formation
- Embedded Si S/D epitaxy (d)
- HDD I/I + activation
- ILD0 deposition/CMP
- Dummy poly/oxide removal
- Si nanowire formation by SiGe etch (e)
- Gate dielectric (IL-SiO_2/HfO_2) dep.
- Work function (WF) metal deposition
- Fill metal (W) deposition/CMP (f)
- Contact formation + M1 BEOL

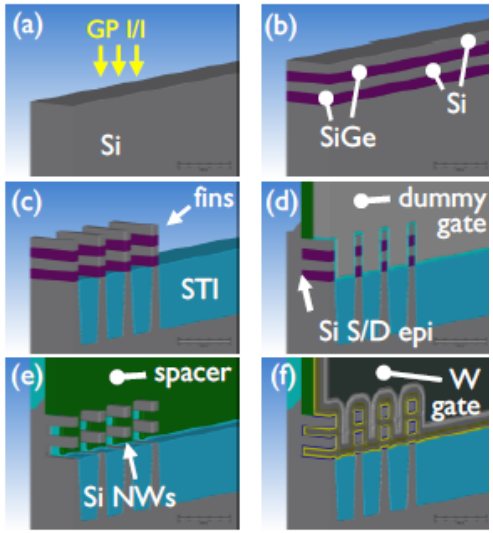


Fig. 1. Process flow for the fabrication of GAA Si NWFETs. **(a)** – **(f)** Coventor® images that illustrate the critical steps. The Ge concentration in the SiGe layers is 27%. The thickness of the SiGe and Si layers is ~10 nm.

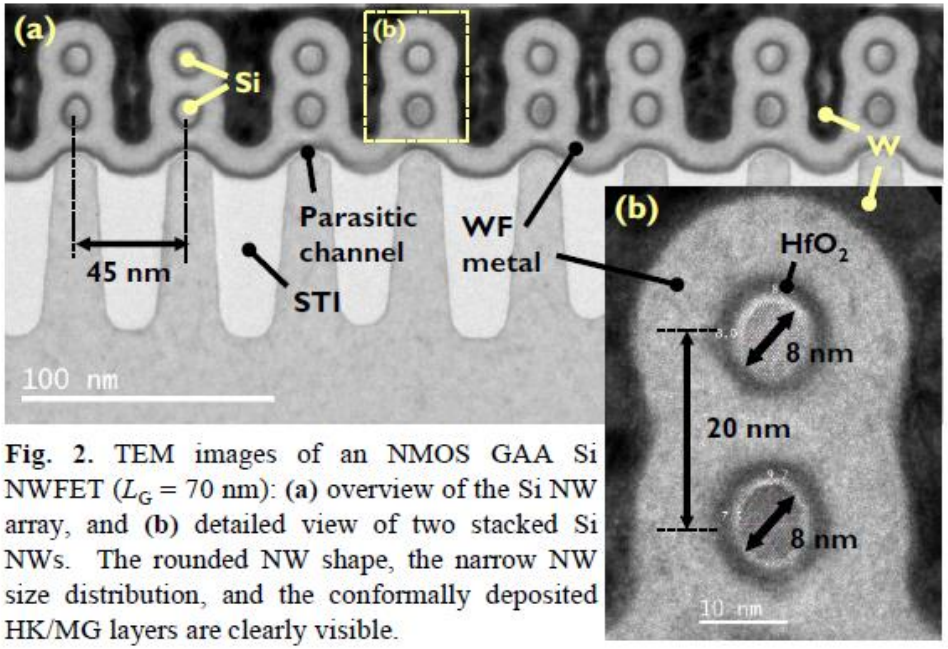


Fig. 2. TEM images of an NMOS GAA Si NWFET (L_G = 70 nm): **(a)** overview of the Si NW array, and **(b)** detailed view of two stacked Si NWs. The rounded NW shape, the narrow NW size distribution, and the conformally deposited HK/MG layers are clearly visible.

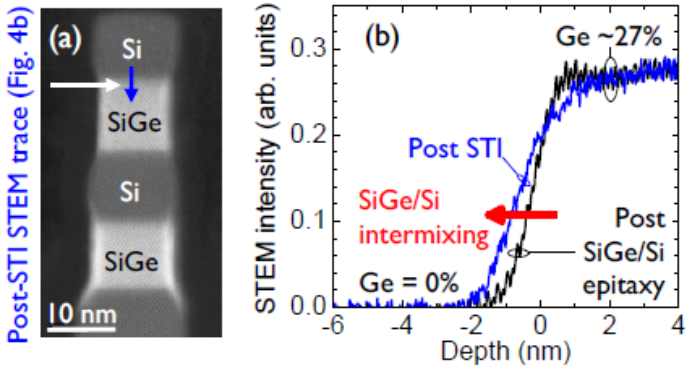


Fig. 4. **(a)** STEM image of a post-STI fin showing the SiGe and Si segments. **(b)** STEM intensity trace showing limited SiGe/Si intermixing by STI densification at 750 °C for 30 minutes. Junction activation spike annealing has low impact on SiGe/Si intermixing as well, which is attributed to short anneal duration.

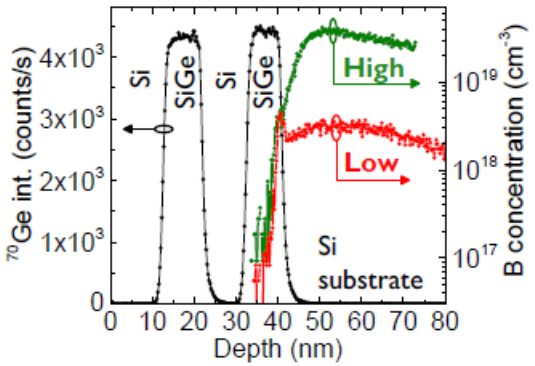


Fig. 5. SIMS profiles for Ge (left axis) and for NMOS GP doping (right axis) collected after SiGe/Si epi for two boron GP concentrations showing the steep profiles in the Si substrate below the SiGe/Si stack.

First demonstration of a CMOS over CMOS 3D VLSI CoolCube™ integration on 300mm wafers

L. Brunet[1], P. Batude[1], C. Fenouillet-Beranger[1], P. Besombes[1], L. Hortemel[1], F. Ponthenier[1], B. Previtali[1], C. Tabone[1], A.Royer[1], C. Agraffeil[1], C. Euvrard-Colnat[2], A. Seignard[1], C. Morales[1], F. Fournel[1],L. Benaissa[1], T. Signamarcheix[1], P. Besson[2], M. Jourdan[1], R. Kachtouli[1], V. Benevent[1], J.-M. Hartmann[1], C. Comboroure[2], N. Allouti[1], N. Posseme[1], C. Vizioz[1], C. Arvet[2], S. Barnola[1], S. Kerdiles[1], L. Baud[1], L. Pasini[1,2], C.-M. V. Lu[1,2], F. Deprat[1], A. Toffoli[1], G. Romano[2], C. Guedj[1], V. Delaye[1], F. Boeuf[1], O. Faynot[1] and M. Vinet[1]
[1]CEA, Leti, MINATEC Campus, [2]STMicroelectronics

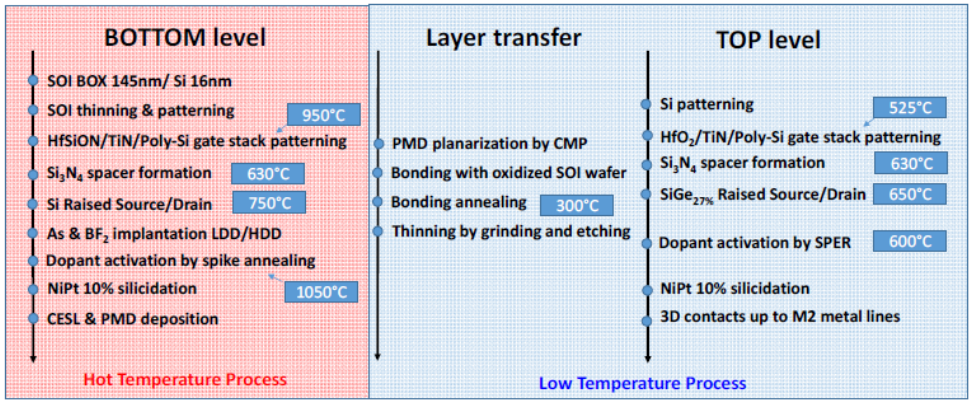


Fig.1: Process flow scheme of 3D CoolCube™ integration: bottom level realization at high temperature, layer transfer and realization of the top level at low thermal budget.

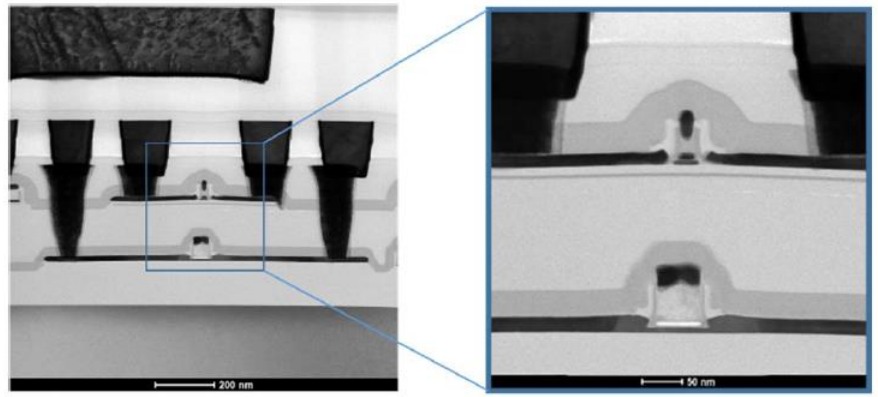


Fig.2: TEM cross-section of the 3D sequential structure up to M2 line. Nanometric top and bottom transistors alignment is observed.

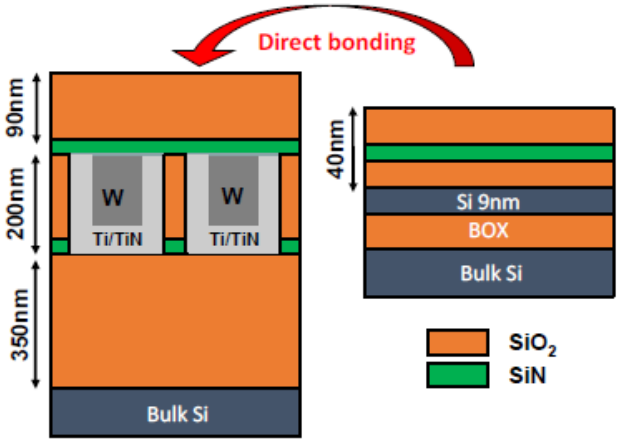


Fig.11: Description of the Si layer transfer above W metal 1 level. Ti/TiN diffusion barrier is used.

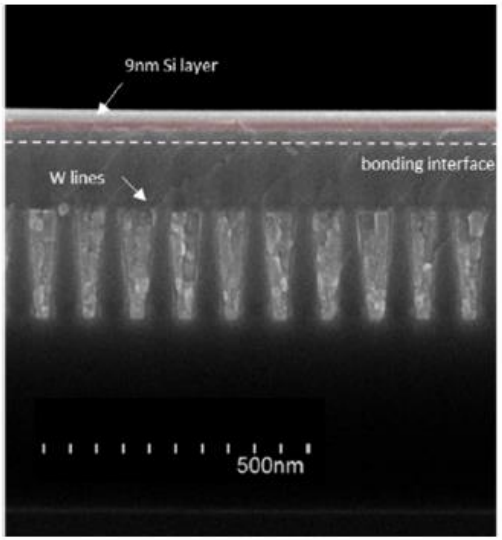


Fig.14: SEM cross-section of the bonded structure, with bottom W lines, after thinning. The 9nm Si layer is highlighted in red.

White Spots Reduction by Ultimate Proximity Metal Gettering at Carbon Complexes Formed underneath Contact Area in CMOS Image Sensors

Tadashi Yamaguchi, Tomohiro Yamashita, Takeshi Kamino*,
Yotaro Goto*, Takashi Kuroi*, and Masazumi Matsuura

Renesas Electronics Corp., 751 Horiguchi, Hitachinaka, Ibaraki Japan
tadashi.yamaguchi.pz@renesas.com
*Renesas Semiconductor Manufacturing Corp., 751 Horiguchi, Hitachinaka, Ibaraki Japan

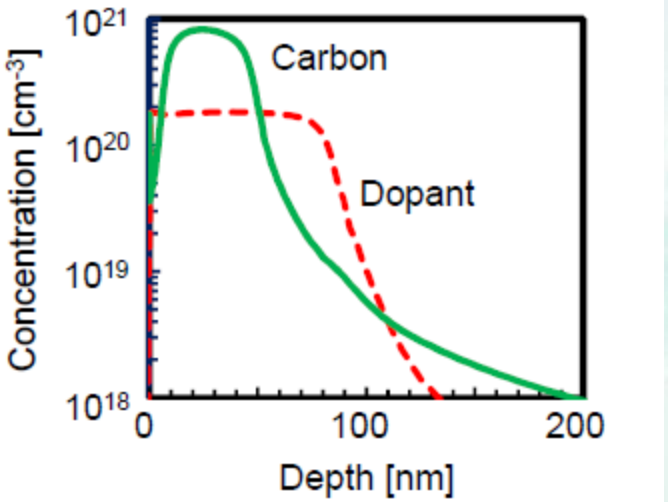


Fig. 9. Simulated carbon and dopant depth profiles after gettering site formation.

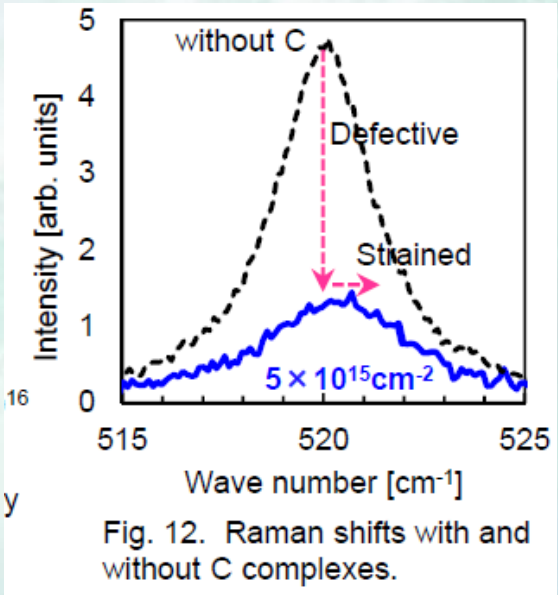


Fig. 12. Raman shifts with and without C complexes.

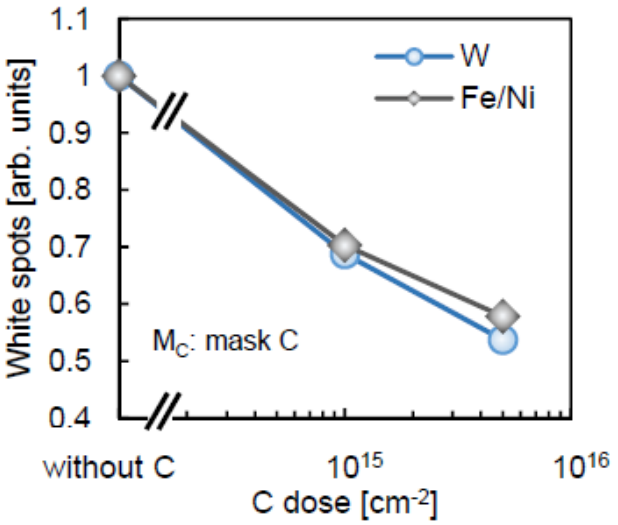


Fig. 10. White spots as a function of C dose.