

ion beam services the total ion implantation solution

PULSION® Plasma Implant Update

JULY 2015 – Semicon SFO



IBS PULSION[®]

A Differentiated Plasma Doping Technology for Advanced Device Manufacturing and High Productivity Applications



Agenda

- Advanced Technical Needs and Trends
- PULSION[™] Design Advantages and Validation
- Safety Validation
- New PULSION[™] Developments
 - Options
 - Marathon Performance
 - Manufacturability
 - Dose Calibration
 - 450mm
- Update On Applications and Species
 - FinFET
 - 3D Modeling Project
 - Hot As
 - FDSOI
 - III-V

Why Plasma Immersion Ion Implantation (PIII)?

New technology requirements

- Lower Energy
- Higher Dose
 - Material modification
 - 3D structures



- No risk of high energy contamination
- Simultaneous implantation of the whole wafer
 - No scanning required
- Ultra Low Energy (down to eV)
- High implantation current even at low energies
- 3D doping



PULSION ® - Dual Region Chamber Design



PULSION[®] schematic: unique features enabling high performance process

PULSION® Configurations

PULSION nano	PULSION nano Auto-loading	PULSION HP					
Manual loading 1 chamber	Auto loading 1-2 chambers	Auto loading 1-4 chambers					
Labs	Device qualification	Production					
+ Substrate heating (up to 500°C on chuck)							

PULSION™ Overview

- **Plasma Immersion Ion Implantation**
 - 100V to 10kV (20kV option)
 - 1e14 /cm² to 1e18/cm² Dose
 - 200 or 300mm
 - Up To 4 Chambers
 - Up To 6 Gas Lines/Chamber
 - In-situ Dosimetry
 - Available Species
 - Gas Precursor
 - Liquid Precursor
 - Passivation/ Outgassing Chamber
 - High Temp Implant Option (up to 450° C)





PULSION[®] - Available Species

- Current Species Used
 - B (BF3, B2H6)
 - P (PH3)
 - As (AsH3)
 - C (CH4, CF4)
 - N (N2)
 - O (O2)
 - F (several)
 - Si (SiH4, SiF4)
 - S (SF6)
 - H (H2)
 - Не
 - Ge (GeH4, GeF4, under study)
 - Al





Safety

- Customer Concerns Regarding As Outgassing
 - As < detectable limits with normal PULSION configuration</p>
 - Past experience with other PIII systems drove OG chamber
 - Also used for Passivation applications and others.....
- S2/S8 Certification Complete
- Fab Interlock interfaces complete and verified





Technical Advantages From Unique PULSION™ Design



PULSION[®] Key Technical Advantages

- Small volume, remote plasma source
 - De-coupling of plasma source and process chamber
 - Tunable etching/deposition ratio
 - Excellent conformal doping of 3D/Fin structures
 - no erosion and residual damage
 - Very low gas consumption and exhaust
 - Lower acquisition and installation costs
 - Best choice for low energy and/or high dose applications
 - Versatility for Materials Modification
- More process parameter tuning options than BL or other Plasma tools
 - Multiple controls of ion behavior

PULSION® Key Productivity & Cost Advantages

- Throughput 2 to 4 times higher than BL
 - ~50% footprint area of BL tools
 - High Dose/Low Energy Applications
- Low (2 to 10 sccm) gas consumption
- Cost per wafer is <50% of BL cost
- Lower Installation Costs (on board gas distribution)
- PULSION is the GREEN Plasma Doping Solution







Dosimetry

In PIII at low energy, retained dose of doping species can't be precisely measured by a simple current integration (even using a Faraday cup system), calibration is needed.

• Dose calibration examples for BF3







Doping Uniformity (300 mm wafers)

USJ Application

BF₃ 1 kV 1E15/cm²

(implant depth 10nm @ 1E19/cm3)



RTA Anneal

 R_s uniformity : 0.98% (1 σ)

DRAM Poly Gate Counter-Doping

BF₃ 6.5kV 7E16 cm⁻²

HF strip before anneal

1000C, 10 sec anneal



R_s uniformity : 0.8% (1 σ) Dose uniformity : 0.73% (1 σ) Depth uniformity : 1.86% (1 σ)



Uniformity & Repeatability (300 mm wafers)

USJ Application

BF₃, 1 kV, 1E15 cm⁻²

RTA Anneal



Reproducibility

Uniformity $(1\sigma) < 1\%$ Repeatability $(1\sigma) = 1.6\%$

DRAM Poly Gate Counter-Doping

BF₃, 6.5 kV, 7E16 cm⁻²

HF strip before anneal

1000C, 10 sec anneal

Mean Rs	Uniformity		
(0)	(70,10)		
162.55	0.828		
161.19	0.780		
160.17	0.787		
157.96	0.777		
158.66	0.840		

Uniformity $(1\sigma) < 1\%$ Repeatability $(1\sigma) = 1.16\%$



SIMS Profiles: Voltage Response for BF₃

- Implant depth control proportional to wafer voltage
- USJ depths below 10nm can be achieved by reducing the wafer voltage



Control of Si Etching with F containing species

HRTEM : Implanted (BF₃ 4kV, 1.5E16 atoms/cm²) / Unimplanted Samples



SIMS Profile of Arsenic USJ with Flash Anneal

6

AsH₃, 0.3 kV, 2E14 cm⁻² 1200C flash anneal As depth at 1E18 cm⁻³ is 7 nm



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Effect of PM and Species Change

Implant time (Implant current) stability (BF3 recipe)



• Minimized impact of PM or species change on implant current and implant time



Tool Conditioning after PM for BF₃

BF₃ sheet resistance and non uniformity (BF₃ 5kV 4E15/cm² + RTA 1050° C)



- 25 to 50 wafers are needed to condition the tool after PM (total dose of 1.2E17/cm²)
- Non uniformity : 1 to 2 %
- Wafer to wafer reproducibility after 35 wafers : 1.5%



Tool Conditioning after PM for AsH₃

AsH₃ sheet resistance and non uniformity (AsH₃ 4kV 4E15/cm² + RTA 1050°C)



- 10 to 25 wafers are needed to condition the tool after PM (total dose of 1.2E17/cm²)
- Non uniformity improves to < 2% after 25 wafers
- Wafer to wafer reproducibility after 12 wafers : 1.2 %





Particles

G Handling :

- Front side : < 1 adder @ 65 nm</p>
- Backside :
 - 700 to 1000 adders @ > 120 nm demonstrated

G Argon implant :

• Front side particle : Ar 1kV 1E15/cm² and 1E16/cm²

	Ar 1 kV 1 ^E 15 /cm ²			Ar 1	l kV 1 ^E 16 /	cm²
size	> 65nm	> 80nm	> 120nm	> 65nm	> 80nm	> 120nm
adders	6	5	3	7	6	5





450 mm Scalaibility



450 mm PULSION[®] Scalability

PULSION® advantages for 450 mm :

- Implant time is independent from the surface
- Doping efficiency proven on the technology which will be installed on 450 mm (FinFET doping, material modification, memories)



Roadmap for 450 mm :

- Phase 1 : demonstrate scalability : target < 4% non homogeneity
- Phase 2 : final design : < 1% non homogeneity ٠

450 mm PULSION[®] Scalability

BF3 6kV implant on n-type 450 mm wafers Dose and implant depth uniformity meseared by CAMECA LEXES => Less than 4% non uniformity demonstrated

450 mm wafer dose non-uniformity 450 mm wafer thickness non-uniformity 47 points mapping 32 points mapping Wafer B Wafer B 8 Dose (x 1e15 at/om2 84.00 43.00 82.00 81.00 4.02 80.00 3.96 19.00 3.90 78.00 3.64 77.00 3.78 76.00 3.72 75.00 3.66 B average thickness: 79.59 nm B average dose: 3.80e15 at/cm2 Non-uniformity: 3.59% Non-uniformity : 3.91%



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Compatibility with CMOS devices





PULSION® General Performance: fully CMOS compatible

• Compatibility with resist



No resist damages

• Compatibility with standard resist strip processes used for beam line implantation



PCOR-SIMS depth profiles of n-type wafers plasma doped with BF₃ 6kV 5E16/cm²

No dose loss or excessive oxidation after plasma strip resist process





PULSION® General Performance: metal contamination

G Ar implantation : Measurement by VPD-ICPMS



Frontside Ar 1kV 1E15 at/cm²



PULSION[®] General Performances : fully CMOS compatible

- Customer need:
 - Similar doping results than beamline implantation
 - <u>No process flow modification</u>
 - Higher throughput and performances
- Typical application
 - S/D for CMOS devices

• PULSION benefits

- LDD Doping of 120 nm CMOS Devices
 - High throughput
 - Die consumption below spec, comparable to beamline implant
 - Relative yields comparable to or better than beamline implant



USJ applications

- Application on SOI transistor : collaboration with CEA LETI, IIT2012
 - Less amorphization than beam line for equivalent implant depth
 - As efficient as beam line on electrical characteristics of devices
 - Only solution for FD-SOI where < 300 eV implantation is needed



With courtesi of CEA LETI



FINFET DOPING



FinFET BF₃ Doping using PULSION[®] : conformal doping



S. Felch et al. (Sematech, CNSE, IBS), IWJT11

- Conformal doping of as-implanted sample
 - White regions on top of fins, along sidewalls, and between fins are B-doped, not B deposition on surfaces of fins.
 - Equal thicknesses of all regions. No dimensional fin changes.
- Entire fin is light-colored after PMOS source/drain anneal
 - Anneal caused B to diffuse toward center of fin



FinFET BF₃ Doping using PULSION® : defects

- HRTEM image of BF₃, 0.5 kV, 1E15 cm⁻² implant
- Thickness of amorphous layer ~2 nm (SiO2)
 - Thin enough to leave crystalline Si region in interior of 16nm node fin and enable complete regrowth of fin Si





FinFET AsH₃ Doping using PULSION[®]

FinFET doping requirements for < 10 nm nodes

- Ultra shallow junction (< 5 nm)
- Conformal doping
- No Fin erosion
- High retained dose
- Perfect crystal recovery after activation annealing

Tested on the following structure :


FinFET AsH₃ Doping using PULSION®



FinFET AsH₃ Doping using PULSION[®]

1E+21

As (at /cm3) 05+31

1E+19

1E+18 0

10

20

30

depth (nm)

40

50

60



Very good conformality, Efficiency of SiO2 cap layer to avoid dose loss





No Fin etching Perfect cristal regrowth



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FinFET AsH₃ Doping using PULSION[®]

Main results :

Sample	SIMS (center)		EDX (center)	
	Dose Top / Sidewall (at/cm ²)	Conformality	Dose Top / Sidewall (at/cm ²)	Conformality
Slot 4 (as implanted)	8.9E14 / 8.0E14	90 %	7.8E14 / 7.0E14	90 %
Slot 5 (annealed)	2.1E15 / 2.1E15	100 %	1.5E15 / 1.5E15	100 %

SIMS uses integral deconvolution to calculate As dose at fin top and fin sidewall.

EDX dose is calculated by the integral of the EDX profiles

Very good and coherent conformality were measured

FinFET AsH₃ Doping using PULSION®

SSRM: (wider structures on the same wafers)



Good conformality of active carriers on FIN structures

FinFET AsH₃ Doping using PULSION®

Main results : LEXES dose non uniformity and dose loss

As implanted



Good non uniformity of PULSION implantation on Fin structured wafers (Non unif < 3%) After SiO₂ cap dep. / annealing / SiO₂ cap etching



Dose loss (50%) and non uniformity (Non unif = 15%) During SiO₂ cap deposition

During annealing





After cap etching

SiO₂ cap layer deposition, annealing and cap etching processes are the main sources of dose loss and non uniformity

FinFET AsH₃ Doping Using PULSION®

Summary :

- AsH₃ PULSION[®] implantation shows a very good conformality on FIN structures
- No Fin erosion nor crystal defect after annealing was observed
- SiO₂ cap layer is effective to avoid dose loss during annealing and allow high dose retention in silicon.
- SiO₂ cap layer deposition and etching as well as RTA processes must be well controlled not to degrade the good non-uniformity obtained after implantation



3D PULSION Modeling

Approach n° 1 (very simple) : use of SRIM to implant through a gas layer



Example for AsH3 plasma : implantation of As at 500 eV through 1 mm of As gas

Pressure : P1



A - Target Depth - Interview of the second s

- Scattering of transmitted ions
- Recoil atoms due to colisions



3D Modeling

Some tendencies (AsH3) : Transmitted ions





Low energy + high pressure



Scattering of transmitted ions -Angle distribution (3D implant) -Energy distribution



conformal implantation (and deposition)

3D Modeling

Some tendencies (AsH3) : Recoil atoms 500V, P2



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HOT IMPLANTATION



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PULSION® PIII Implanter



Schematic of PULSION[®] with high temp chuck option

- Heated chuck with realtime feedback loop to compensate heating by plasma and implant.
- Up to 500° C



Hot Implantation

Advanced device requirements for Ion Implantation :

- FinFET : 3D conformal shallow doping + no amorphization of the FIN for good crystal regrowth
- FD-SOI : shallow doping + no amorphization of the Si-Top film to allow crystal Epi regrowth and Epi layer deposition (elevated S/D)
- III-V, SiGe, SiC, Diamond, or other exotic and thermally unstable semiconductor : need to reduce defects during implant to limit thermal budget of post implant annealing
- 3D integration : Need to reduce thermal budget for activation and crystal recovery after implantation

PIII + hot implantation

= PULSION[®] with high temp. option

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L. A. Marqués et al., J. Appl. Phys. 111, 034302 (2012)





High Temp Implant Summary

- Up to 500° C Plasma Immersion Ion Implantation is now available on PULSION[®] and has been qualified using AsH₃ plasma
- High temperature PIII implant allows drastic reduction of the thickness of amorphous layer after Arsenic implantation, even at high dose.
- Hot implantation induces 10% deeper profile (also observed on beam line) due to enhanced diffusion of interstitials and vacancies during implant and channeling.
- Partial activation is observed after high temperature implantation even at 300° C, but after annealing sheet resistance does not depend on implant temperature if the as-implanted retained dose is the same.
- No big differences are observed between 400° C and 500° C implantations.



Application for FINFET doping and FD-SOI is under study (Places2Be European project)



Experiment 1 : AsH₃ 10 kV high dose

For the same as-implanted retained dose (~ 1.2 E16 /cm²)



- After implant :
 - High temp implant are ~ 10% deeper
 - Same "channeling" tail for samples implanted at high temp.
- After annealing :
 - no big difference in profile above 1E19/cm³
 - below 1E19/cm³ the tail increases with implant temperature



Experiment 1 : AsH₃ 10 kV high dose

TEM images and thickness measurement of the amorphous layer on as implanted samples as a function of implant temperature







 Important reduction of the amorphous layer thickness is observed when implanting above 400° C

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Experiment 1 : AsH₃ 10 kV high dose



- Partial activation is observed just after implantation when implanting at high temperature
- No significant change of the sheet resistance after annealing
 ~ (240 +/-10) Ω/sq regardless of implantation temperature
- Possible to make high dose As implantation (~ 1.2 E16 /cm²) on 30 nm with only 9 nm amorphous layer (without affecting final sheet resistance)



Experiment 2 : AsH₃ 10 kV lower dose (2^E15/cm²)

TEM on as implanted wafers

(20 nm implant depth)

500°C RT 12.8nm 3.1nm 5 nm 278149.00144 278149.003#10 Center-X-Section TE130306003 Center-X-Section TL130308003 has it / address w/r limit / Room T° 500°C Amorphous layer thickness 3.1 nm 12.8 nm (as implanted)

Drastic reduction of the amorphous layer thickness



Experiment 3 : AsH₃ 1 kV 2^E15/cm²

TEM on as implanted wafers

(7 nm implant depth)

500°C RT ~2nm 278149.003#11 Snm 276149.003#5 Center-X-Section Center-X-Section TL150508003 11130308003 500°C Room T^o Amorphous layer thickness 2 nm 0 nm (as implanted)

- Suppression of the amorphous layer
- Some remaining defects are visible





FDSOI



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III-V DOPING



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III-V (InGaAs) doping

Challenges for III-V doping :

- Very sensitive to implant defects
- Limited thermal budget allowed for post-implant annealing
- USJ and 3D doping needed

Study using PULSION® doping:

- Test of different Silicon containing plasmas
- Test of different plasma and implant conditions





III-V (InGaAs) doping



- Si PULSION[®] doping results in significantly shallower junction depth and higher dopant incorporation compared to ion-implantation and in-situ doping technique (MBE)
- High dependency of Rsq and mobility on Si precursors and process conditions





CMOS imager – BSI back side doping

Passivated layer by implant and laser annealing:

- Minimize recombination of electron-hole pairs at the backside surface
 - Reflect photo-electrons back to photodiodes to increase charge collection efficiency
- Minimize dark current created by residual implant damage after anneal
 - Reduce number of hot pixels
- Temperature rise from anneal must be <400° C at metal levels (--> laser anneal)

PULSIONTM Advantages:

 Shallower implant profile keeps all dopants and defects into melted area: few residual defects, and lower dark current (leakage)
 Ultra-low implant energy with zero high-energy contamination: minimize dead layer
 Lower energies available while keeping higher throughput







Pulsion + Laser annealing

Applications :

-Doping processes for backside applications (**Cmos imagers**, thin substrates, sensors, power devices, security...)

-Doping processes for advanced materials (SiC, III-V, SiGe...)

-Develop doping processes for advanced microelectronics (32-22nm nodes)



Example : SIMS profile of a CMOS BSI doping PULSION BF_3 + laser anneal



CMOS Imager Application : BSI

- Application to CMOS imager (BSI) : IBS / Customer A
 - PULSION Boron implantation
 - Laser anneal



Normalized results from customer feedback

Dark current reduction : 30%

This is due to the fact that the implant depth is ultra shallow and that PIII creates less defects than beam line

=> All the Implant defects are suppressed by the laser annealing



CMOS imager - **STI** trench doping

STI doping requirements:

- Shallow, conformal doping around STI (Shallow Trench Isolation)
- Screen defective sidewalls and edges of STI from depletion region of photodiode
- Frontside CMOS imager application

PULSIONTM Advantages:

 Conformal doping with single wafer placement
 "Dual or Quad implants" and similar beamline techniques are not effective
 Higher dose capability for dark current improvement, while keeping high throughput



Real Devices Conformal doping along STI



CMOS Imager Application : DTI Trench doping

• Application to CMOS imager (DTI) : IBS / STM



Test structures: 20/1 form factor

Uniform doping on the trench walls demonstrated Possibility to adjust doping concentration along the wall

Atemox European R&D project



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CMOS Imager Doping Summary

- PULSION is an efficient solution for Boron USJ doping before laser anneal for BSI Application
- PULSION can do uniform and conformal trench doping for DTI application (20:1 form factor)







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Poly doping for Cool Mos Application

Studied application (with 2 different customers in Europe)

- Poly doping for Cool Mos Application (Boron and Phosphorus)
- Super junction for Cool Mos (low dose, 3D with high aspect ratio)
- SFET plug contact doping (3D trench doping)
- IGBT : backside doping / trench doping



Collector



Conformal doping of $60 \mu m$ wide/200 μm deep silicon trench







Experiment - Silicidation Improvement (NiSi)



- Improved thermal stability and lower sheet resistance on all PULSION® implanted samples
- No differences between the conditions used : very stable process



Thermal stability : Sheet resistance measurement



DS

JÜLICH

- Enhanced of sheet resistance and thermal stability after CF₄ PULSION[®]
- Suppression of surface agglomerates
- Improvement Si / NiSi Interface and NiSi thickness uniformity

Haitao Zhang¹, Julian Duchaine² at al. : IITC MAM 2015 : Improved NiSi contacts on Si by CF4 Plasma Immersion Ion Implantation for 16nm node MOSFETs



Shotcky Barrier Height and Contact resistance



Improved NiSi contacts on Si by CF4 Plasma Immersion Ion Implantation for 16nm node MOSFETs

Vth Tuning for metal gate

G Al implantation using TMA :

- In progress
- First demos have been done with 2 customers
 Up to 130 mV Vth shift observed








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