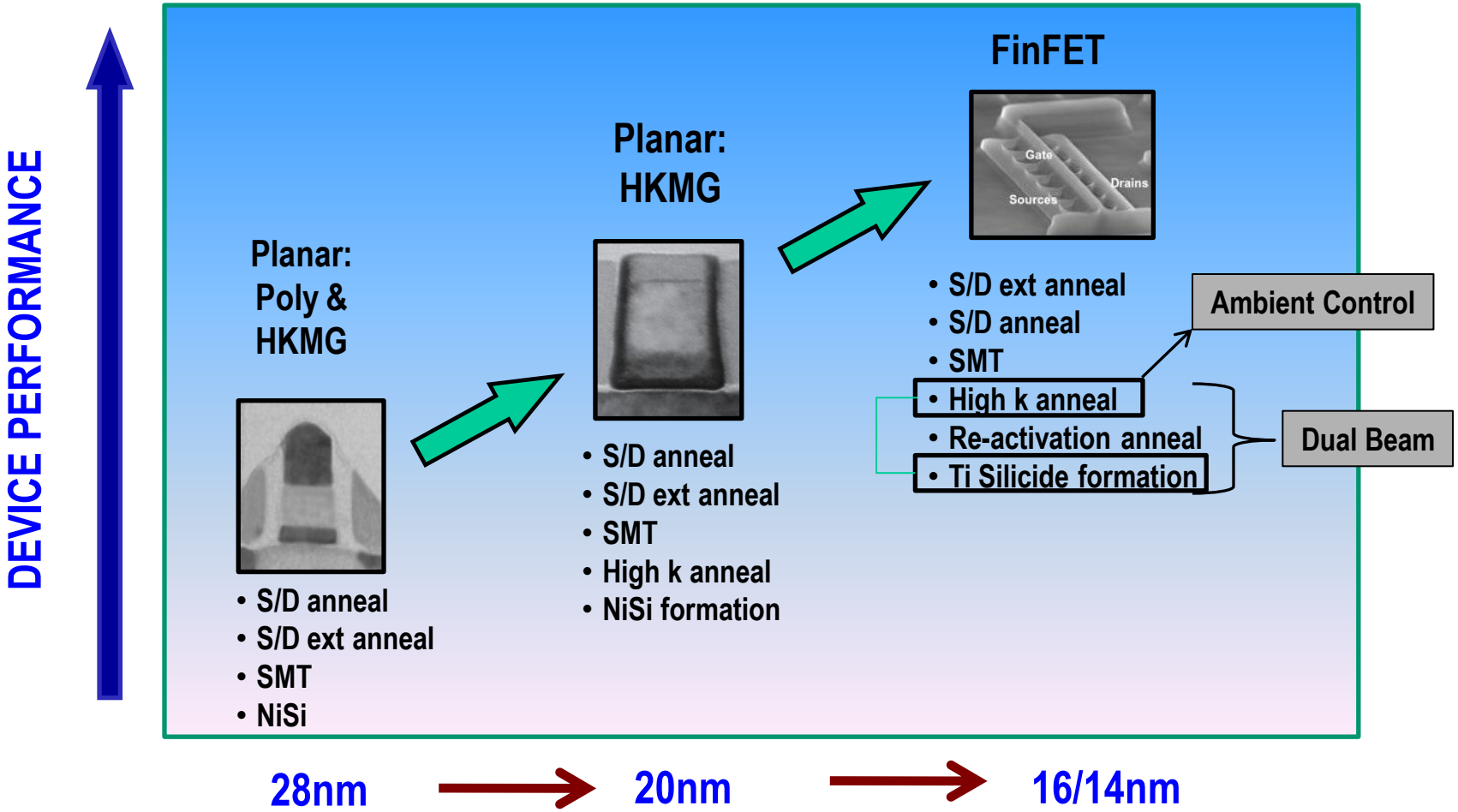
Process Uniformity Improvements for LSA Millisecond Annealing in the FinFET era

Jim McWhirter, Ph.D.

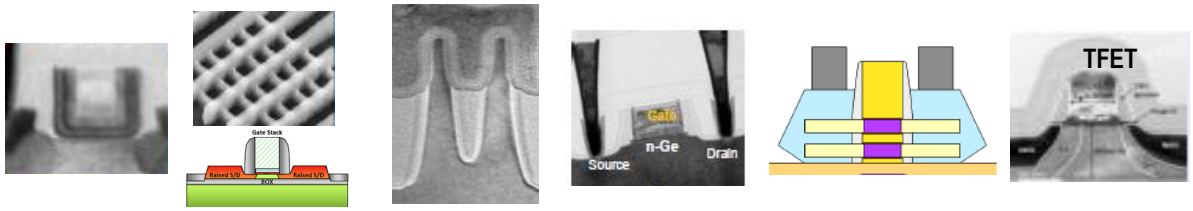
July 16, 2015

LSA Logic Processes vs. Device Node



Decreasing thermal budget and new materials leads to new applications for LSA, and drives trend towards dual-beam and ambient control configurations.

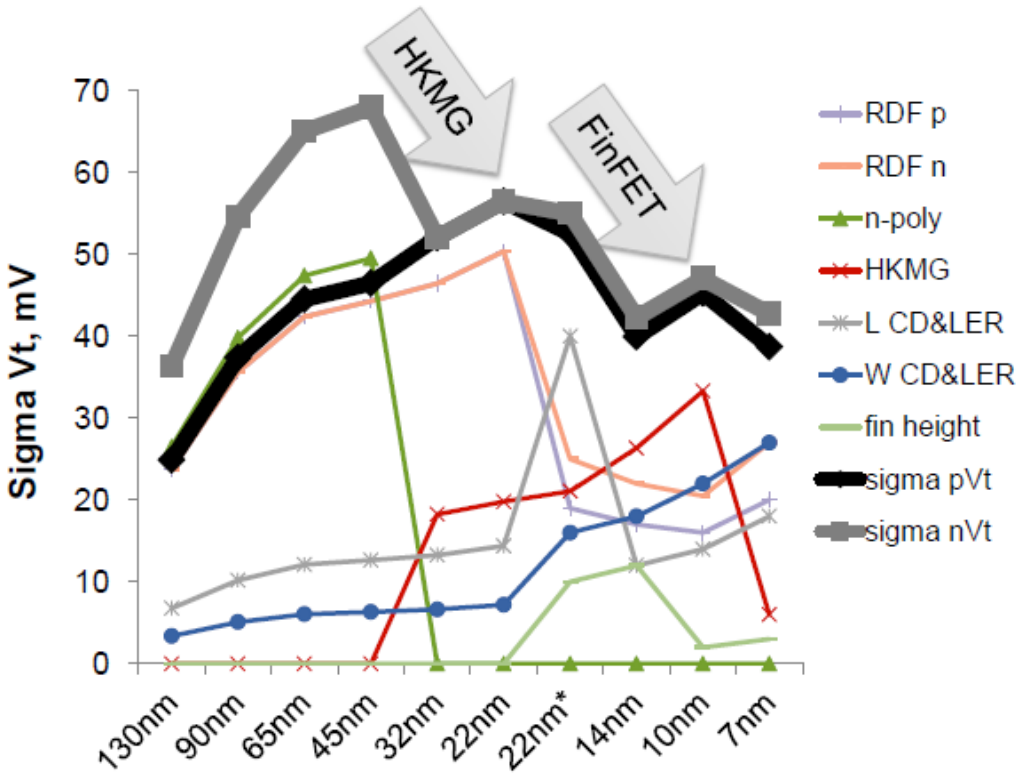
Advanced Logic Device Scaling Trend



	28nm	20nm	14nm	10nm	7nm	5nm	3nm
Device Structure	Planar						
		FinFET					
					Stacked Nanowire		
New Material	SiGe						
				Ge			
					III-V		

- **Device structures approach atomic scales → precise process control more critical**

Example: Power Reduction ($V_{dd} \rightarrow \sigma_{Vt}$)



The data is for the L_{min} W_{min} transistor

*Synopsis: WMED'13

Solid State TECHNOLOGY
Insights for Electronics Manufacturing

Jan '14

FinFET evolution for the 7nm and 5nm CMOS technology nodes

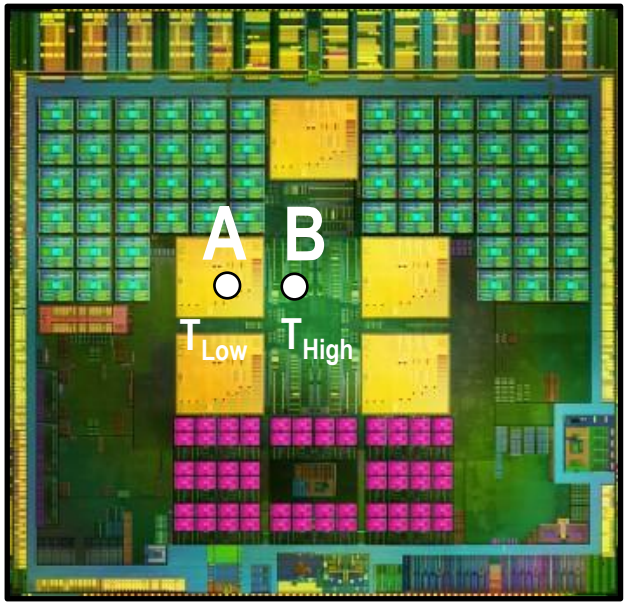
AARON THEAN, *imec, Leuven, Belgium*

"With a goal to reduce close to 50% of the supply voltage (Vdd<0.5-0.6V) relative to today's most advanced microprocessors in production, ***significant improvements of transistor short-channel electrostatics as well as performance are sought***."

- **Roadmap puts pressure on all processes to reduce critical device parameter variations**
- **MSA thermal anneal process variation must improve to advance the roadmap.**

Within Die Uniformity & Parametric Yield

System-on-a-Chip



Device A gets colder during anneal
Device B gets hotter during anneal

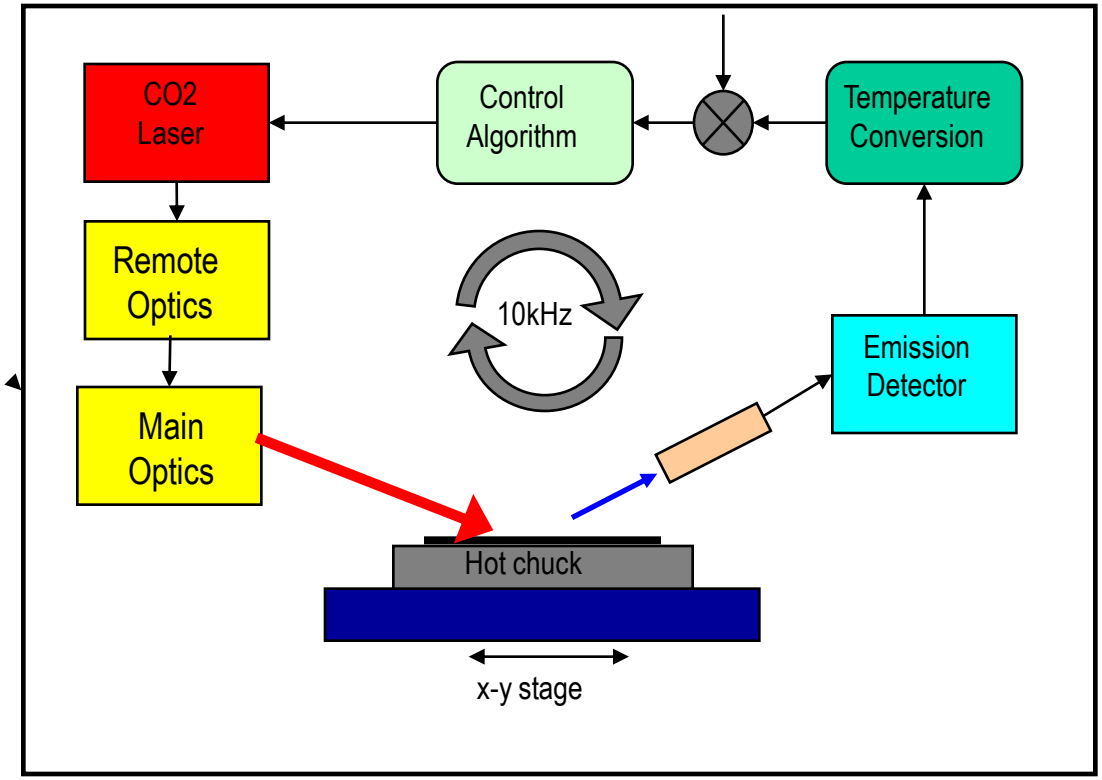
Device Performance Mismatch!

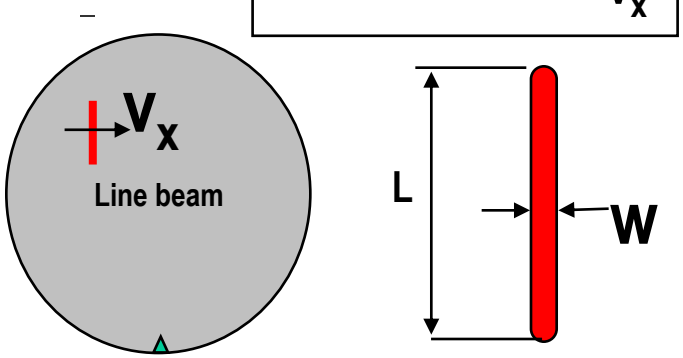
- Variations in pattern density lead to local variations in the absorbed radiation during RTP or millisecond anneal
- This can lead to local variations in peak temperature, and variations in performance of devices which are supposed to be matched.
  - E.g., SRAM cell inverters, Poly-resistor matching for mixed-signal
- Thermal process uniformity within-die is critical.

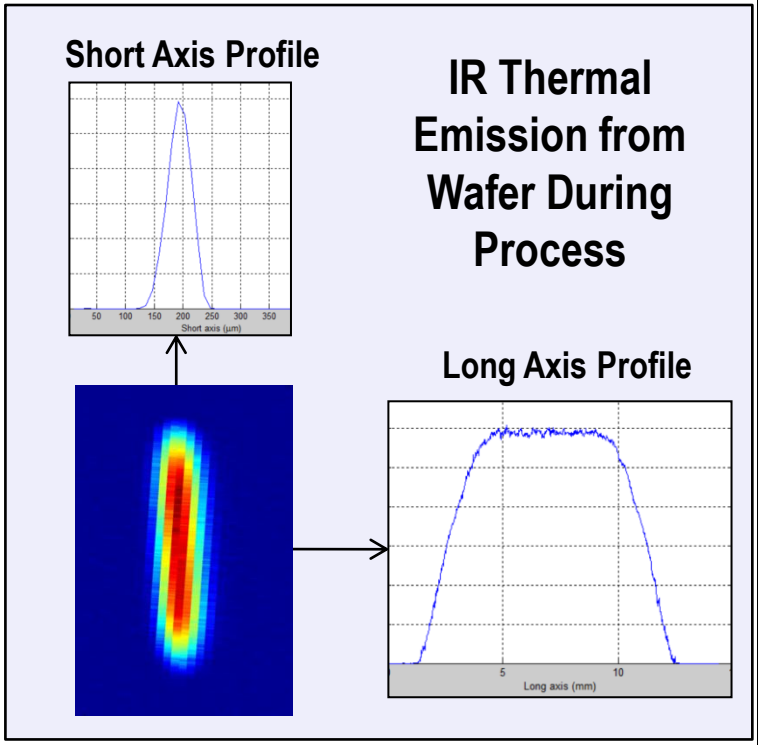
Pattern loading effects during millisecond annealing or RTP can cause device performance mismatch within the die → parametric yield loss and degraded circuit speed

LSA101/201 Overview

$$\text{Dwell time} = \frac{w}{v_x}$$





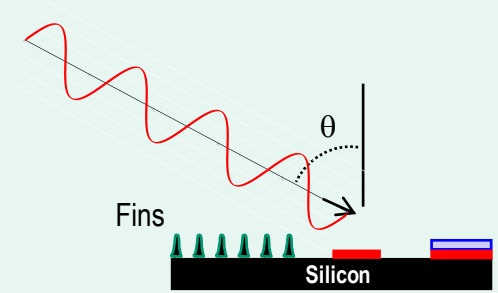


Key Attributes

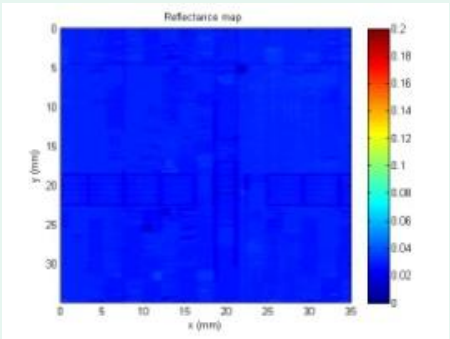
- Within Die Uniformity
  - CO2 Laser: $\lambda \sim 10$um
  - P-polarized, Brewster's angle
- Within-Wafer Uniformity.
  - Real time temperature control.

Pattern Loading Effects in Millisecond Annealing: Equipment Solution (LSA)

LSA



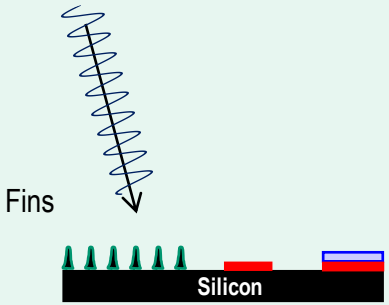
- Long λ
- Brewsters Angle
- No shadowing or light trapping by Fins



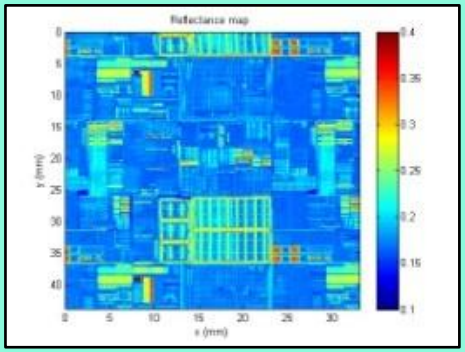
Measured reflectance map

ΔT ~ 10°C

Flash Anneal / Diode Laser



- Short λ
- Near normal incidence
- Can have light trapping by Fins



Measured reflectance map

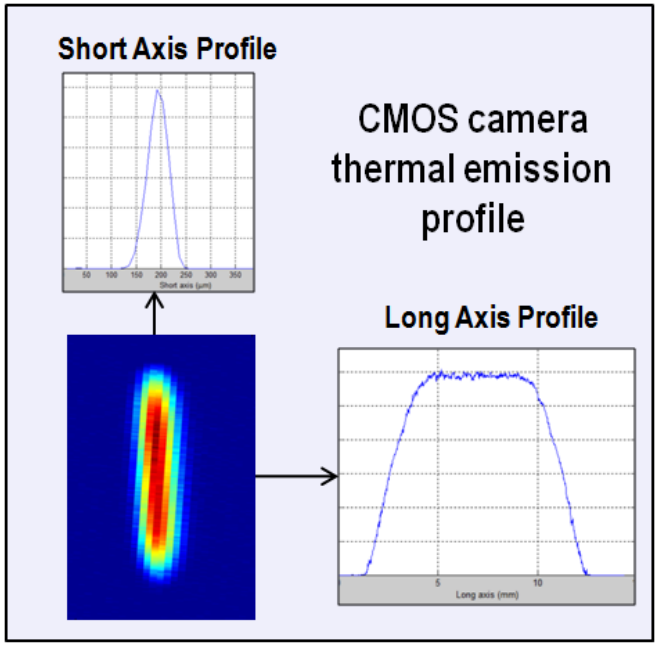
ΔT > 100°C

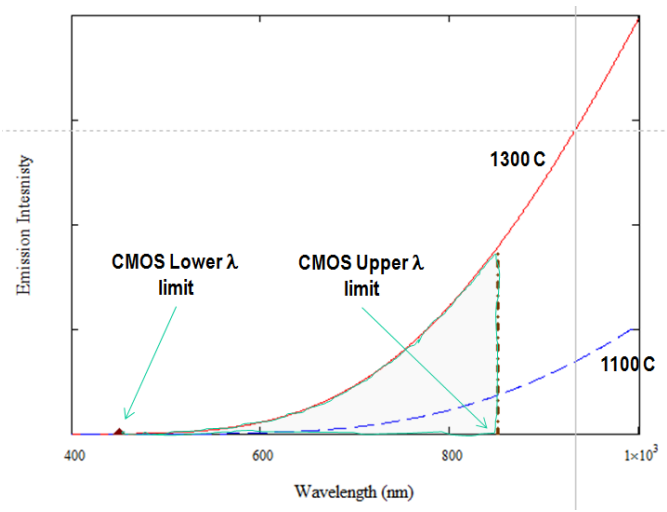
LSA provides an equipment solution for PLE in millisecond annealing

Process Uniformity Improvements for LSA

- **Existing LSA process uniformity has been sufficient through the 14nm node.**
- **In response to roadmap trends for ≤10nm, Ultratech embarked on a project to improve the LSA process uniformity.**
- **We will report here on the results of this work.**
- **The project culminated in a combination of hardware/system design modifications/additions:**
  - **New optics**
    - For profile shape control.
    - Three new optical components, replacing existing optics.
  - **New feedback control system**
    - “Emission Profile Control”, EPC
    - Dynamic (in-process real time) control of process profile.
- **These components are fully field-upgradable on the LSA101/201 family of laser annealing systems.**

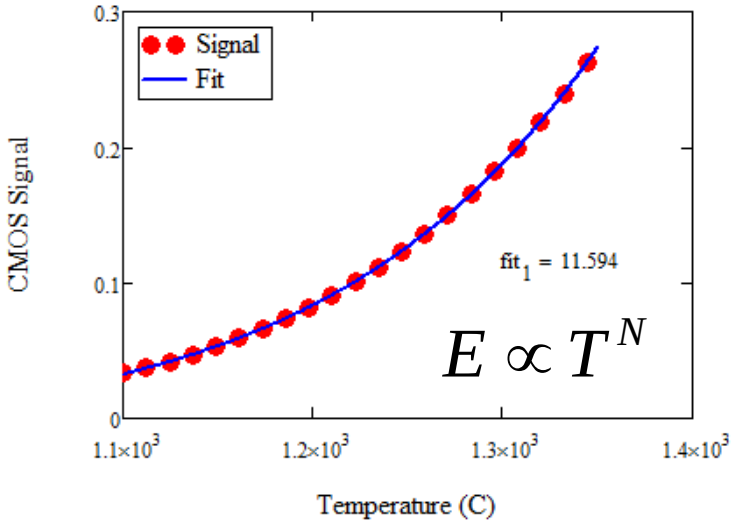
Interpreting Emission Profile Data





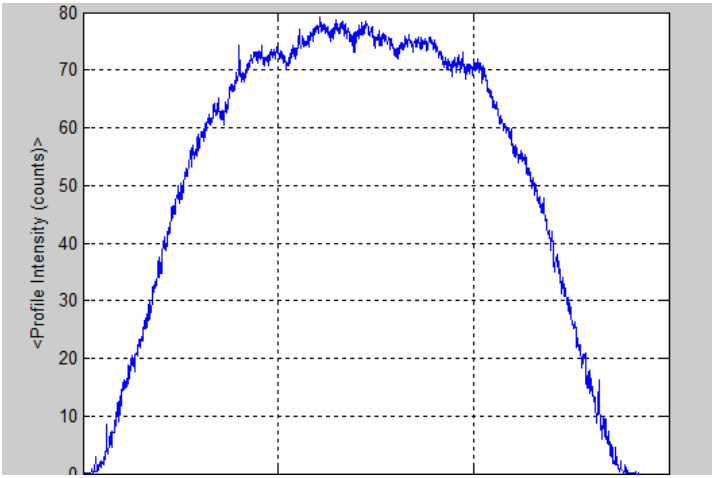
Emission signal (E) captured by CMOS cameral is very sensitive to temperature (T).

$$\frac{\Delta T}{T} = \frac{1}{N}\frac{\Delta E}{E}, \quad and\ N \approx 12$$

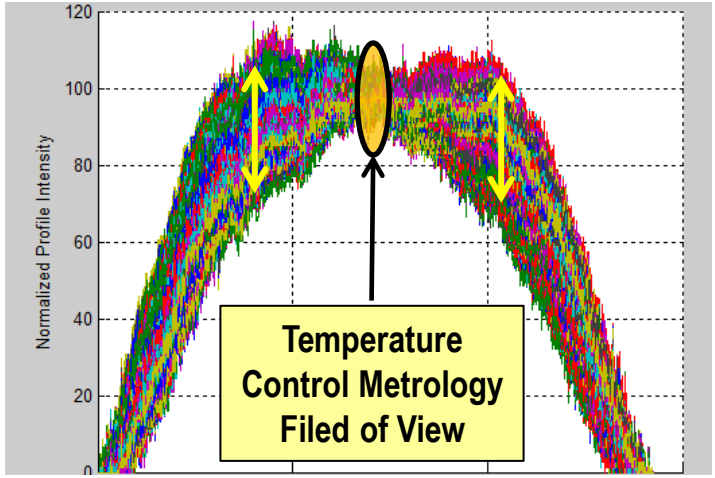


Process Beam Stability

Average emission profile



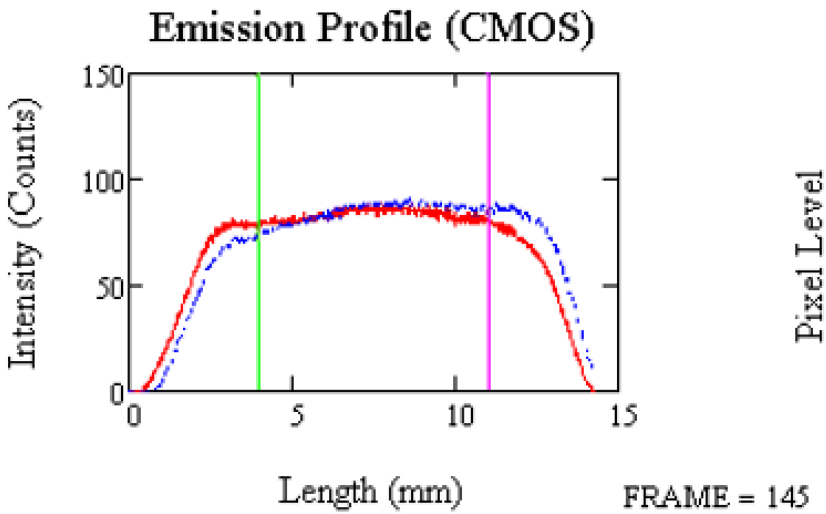
Overlay of frame-by-frame emission profiles

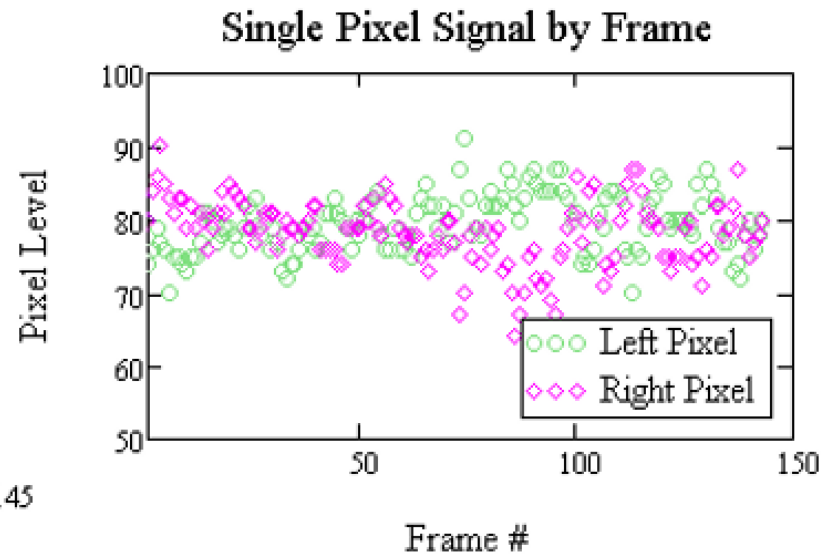


- **Process beam is well-controlled by temperature feedback system at center**
- **Edges of beam have larger variation.**
  - **Use of 50% overlap helps average this out.**
- **Goal: Improve whole-beam stability**
  - **Improved process uniformity**
  - **Enable higher throughput operation (larger step)**

$$\frac{\Delta T}{T} = \frac{1}{N}\frac{\Delta E}{E}, \quad and\ N \approx 12$$

Beam Stability: Cross-Stripe Correlation

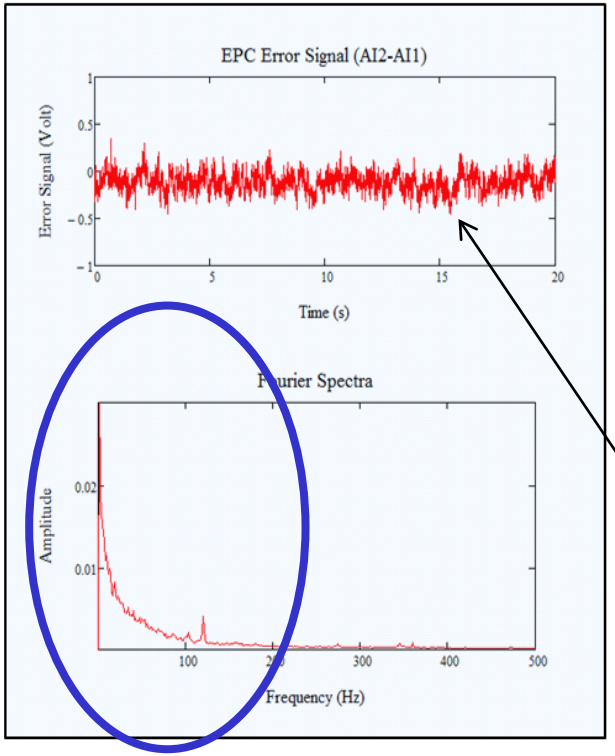




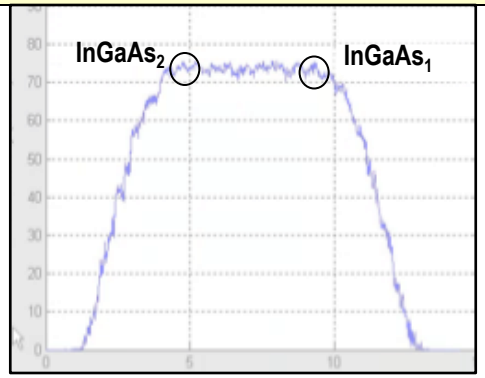
- **Analysis shows that opposite sides of profile are statistically "anti correlated"**
  - **Variation on left and right are random, but not statistically independent.**
  - **This realization led to "Emission Profile Control (EPC)" concept.**

EPC Feedback System Performance

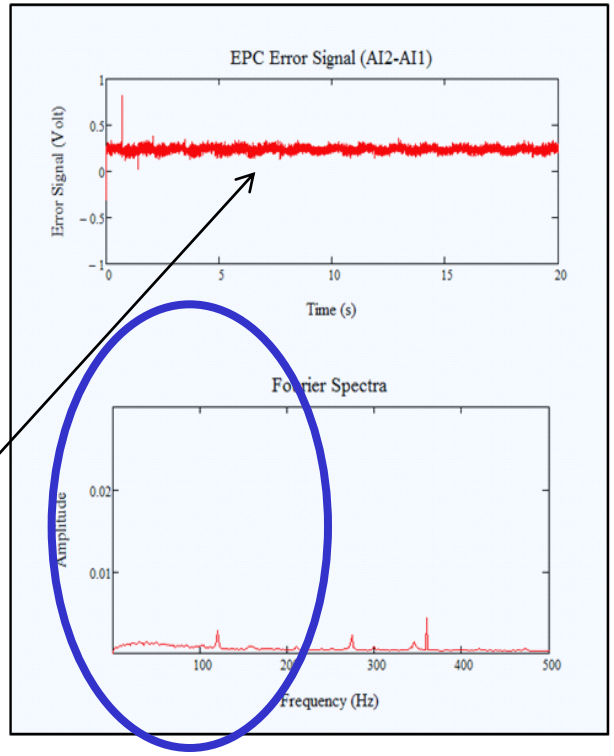
EPC Error Signal Open Loop



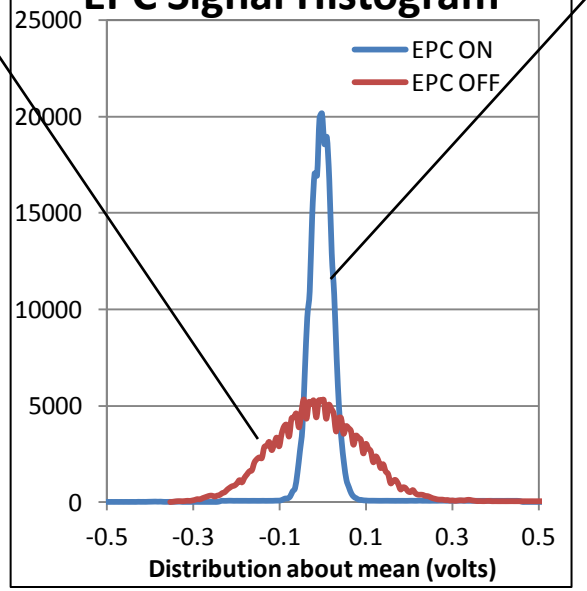
EPC Signal = $InGaAs_2 - InGaAs_1$



EPC Error Signal Closed Loop



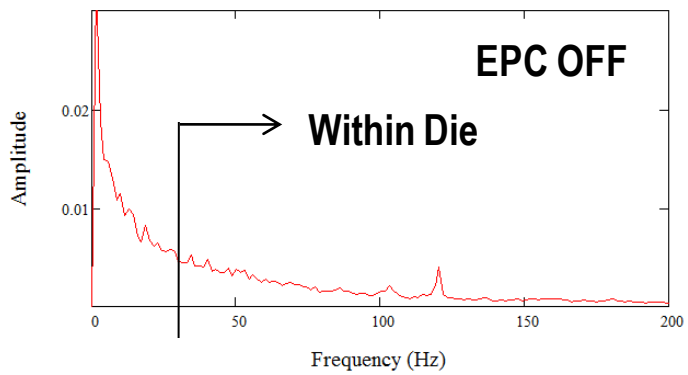
EPC Signal Histogram

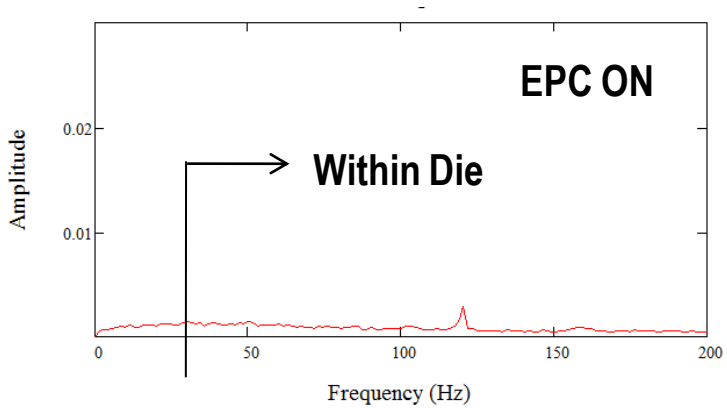


Die Scale Uniformity

- Beam variation in time/frequency domain translate to thermal process variation in distance/spatial-frequency on the wafer.
  - Based on stage speed.
- EPC system significantly improves within-die profile stability.

Frequency Spectra of Beam Stability (Slope)



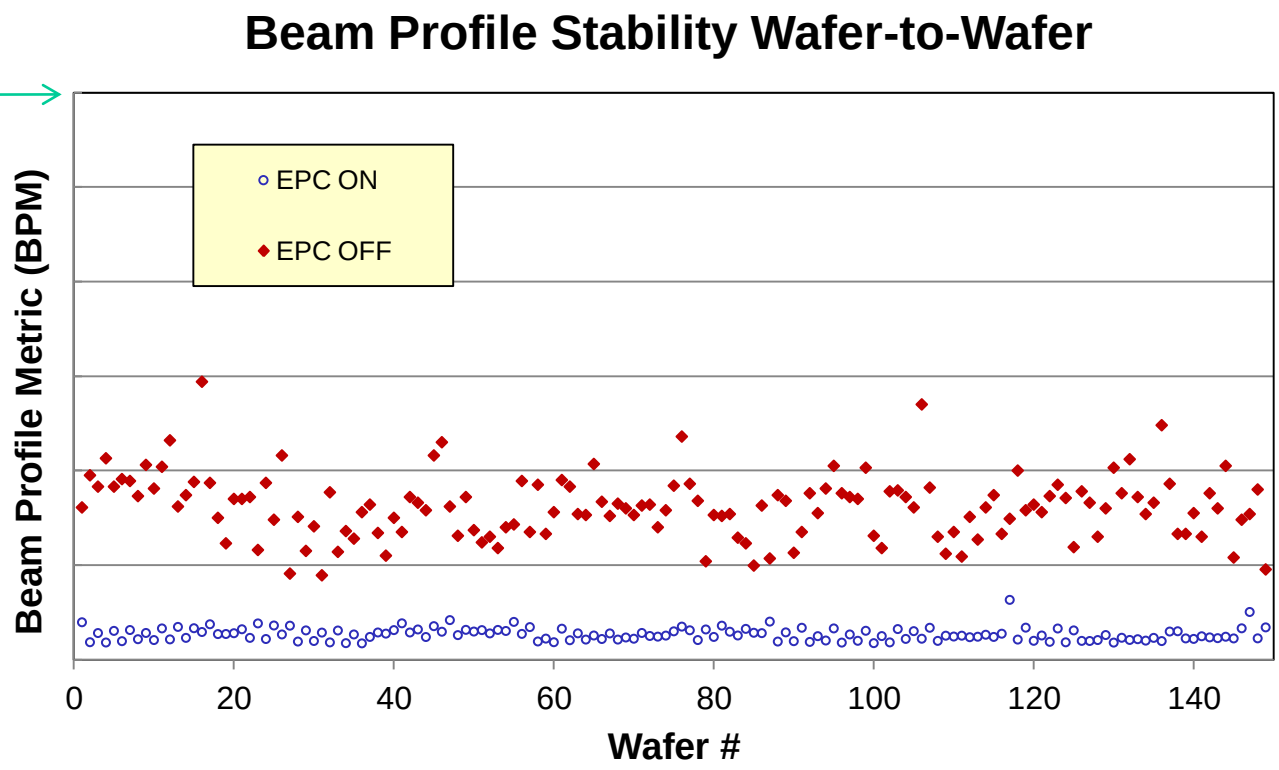


Emission Profile Control: Profile Stability

28nm Process Control Limit

Beam Profile Metric (BPM)

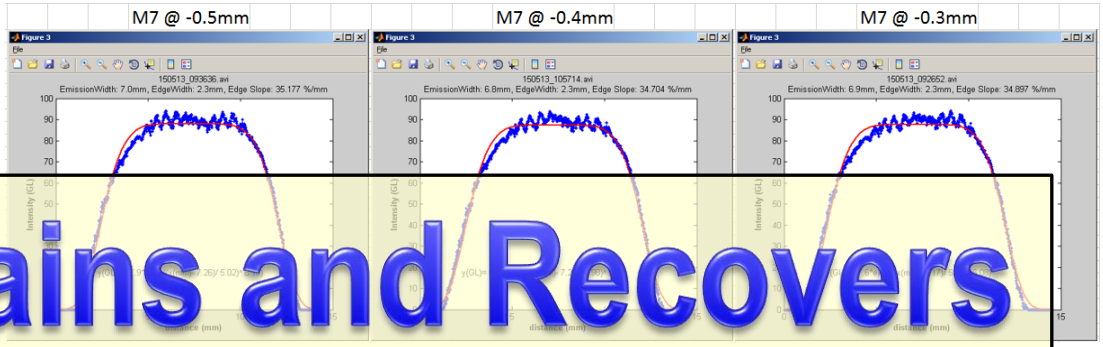
- Compares profile to stored reference.
- Numerical algorithm returns a number representing degree of match.
- Zero = perfect match (lower number is better)



- Emission Profile Control (EPC) improves process profile stability by >5x
- Enables maintaining or improving C_{pk} with tighter process windows

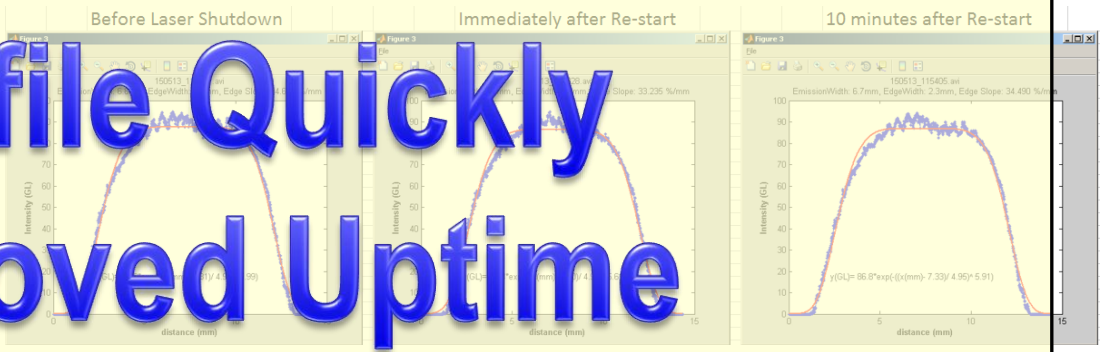
Major System Events: Profile Stability With EPC

- Alignment motor moved on purpose – EPC corrects.

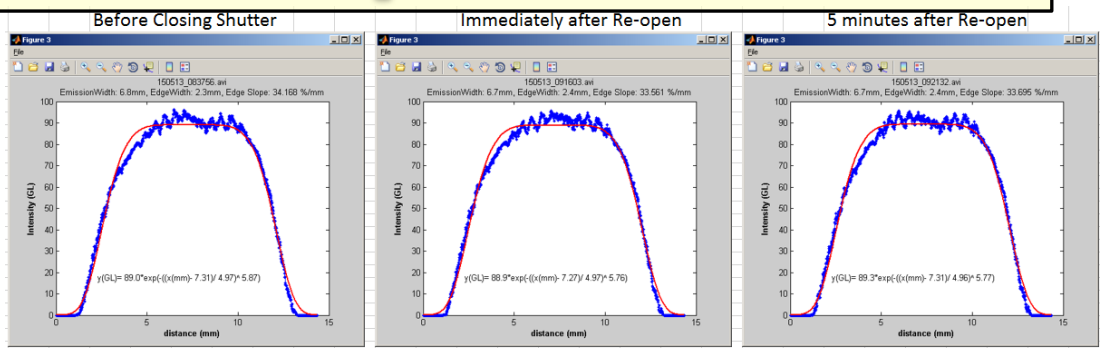


EPC Maintains and Recovers Profile Quickly Improved Uptime

- Profile recovery immediately after gas change – EPC maitains profile during laser warm-up



- Laser shutter closed, optics cooled, then opened.
- EPC maintains profile as optics regain thermal equilibrium.

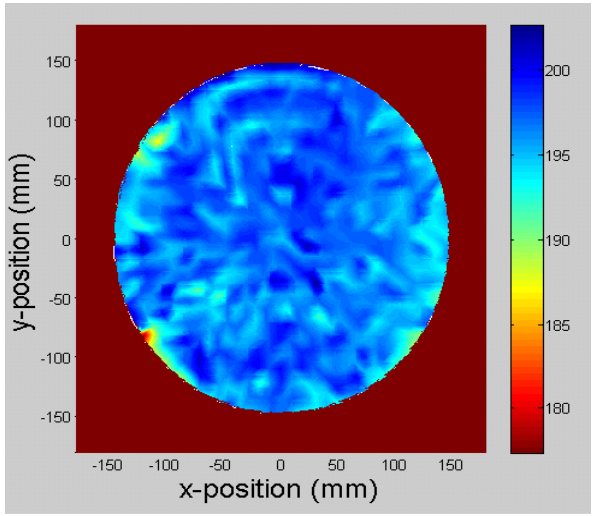


Process Uniformity Results

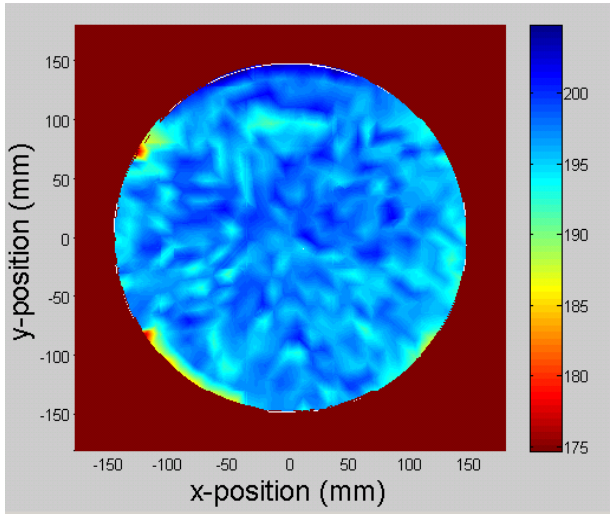
- **Process uniformity results based on Rs measurements from post-annealed wafer.**
- **Implant Conditions**
  - **Substrate 20-40 ohm-cm**
  - **B Implant**
    - 2.0E15/cm^2
    - 5keV

Whole Wafer Process Uniformity

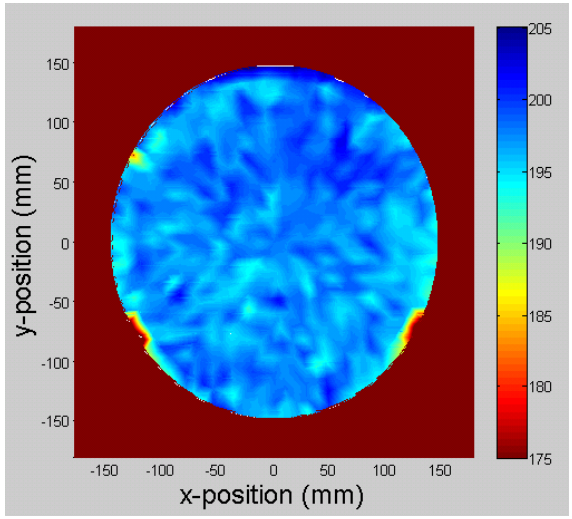
Day 1



Day 2



Day 3



Day	Center	Whole Wafer (3mm MEE)
1	1.0%	1.2%
2	1.0%	1.5%
3	0.9%	1.7%

2x Improvement in whole wafer process uniformity.

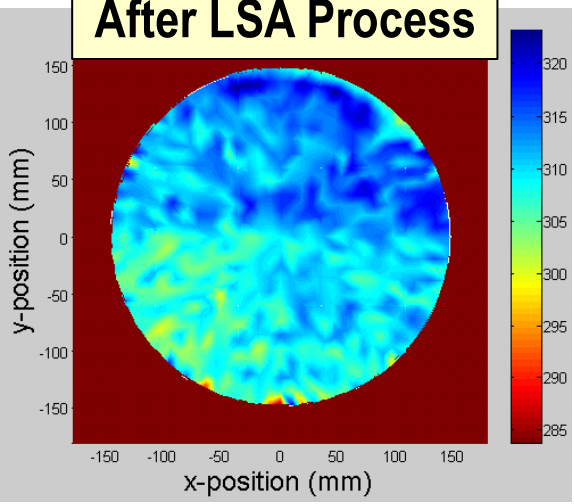
Implant Non-Uniformity

- With recent uniformity improvements, LSA process uniformity is achieving measur4ed Rs results ~1% 1-sigma uniformity.
- Implant uniformity of ~tenths of a percent are now noticeable in post-LSA Rs results.

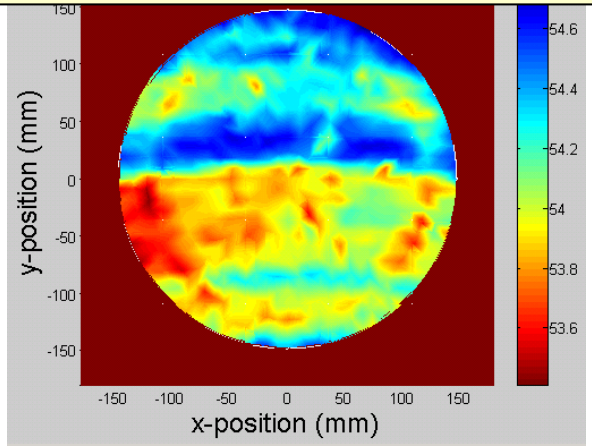
$$\sigma_{RS} = \sqrt{\sigma_{LSA}^2 + \sigma_{implant}^2}$$

- Example shown here
  - Measured σ_{RS} = 1.3%
  - $\sigma_{implant}$ = 0.5% (soak anneal measurement)
  - σ_{LSA}=1.2%
- Benchmark:
  - σ_{RS} = 1%
  - $\sigma_{implant}$ = 0.3%
  - Then σ_{LSA} is 0.95%

After LSA Process

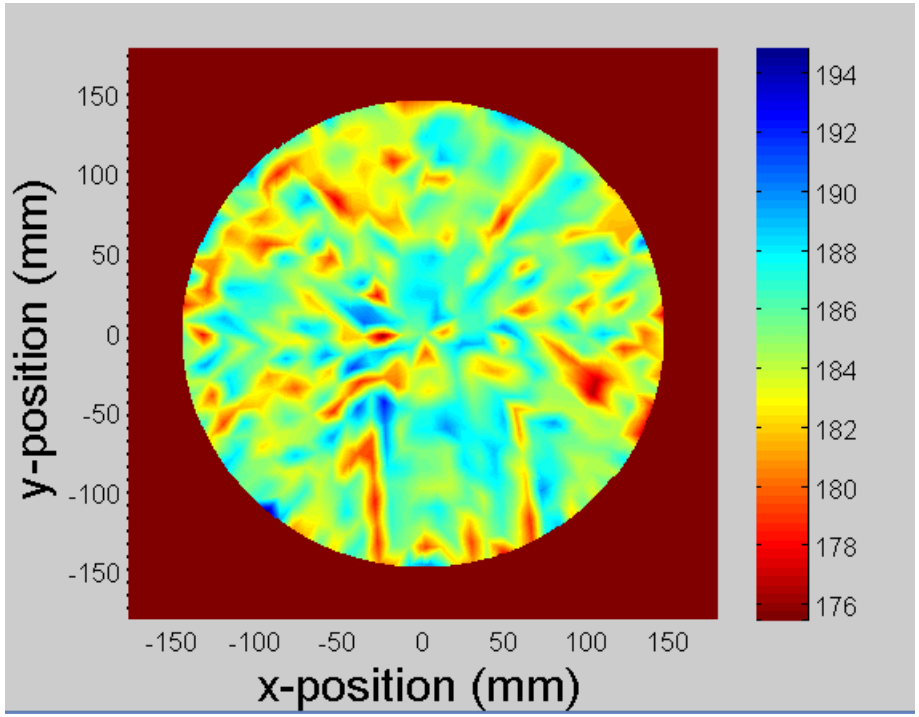


Soak Anneal (same implant lot)

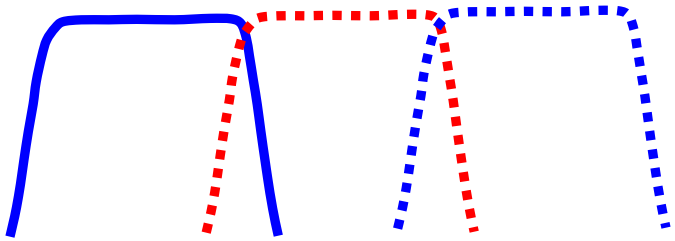


High Throughput Process

- **Uniformity:**
  - **1.48% Center,**
  - **1.53% 3mm MEE.**



- **With improvements in profile stability, processing is possible at maximum step size condition.**



  - **Stable beam reduces need for the averaging effect from 50% step size.**
- **Results shown here exceed current uniformity specification, but with 43% increase in wafer throughput!**

Summary

- **Semiconductor roadmap demands ongoing improvements to reduce process variability.**
  - **Front-end thermal processes are at the critical path.**
- **LSA plays a critical role in today's and tomorrow's FinFETs through multiple applications**
- **Recent developments have generated 2x improvement in LSA process uniformity performance.**
  - **Process uniformity approaching 1% level.**
    - Implant uniformity becomes a consideration when interpreting results.
  - **Improvements work with dual-beam as well as single beam configuration.**
  - **Enables higher throughput operation with no sacrifice in performance.**
  - **Side-benefit is improved stability and recovery of process beam after tool-down events.**
    - Improved uptime
  - **Hardware components are upgradeable on existing LSA101/201 systems.**