P, Sb and Sn Ion Implantation with Laser Melt-LPC (Liquid Phase Crystallization) For High Activation n+ Ultra-Shallow Junction in Ge Epilayer and Surface Strain-Ge Formation For Mobility Enhancement

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Semicon/West July 16, 2015 www.job-technologies.com

# • Introduction

- Device Roadmap to High Mobility Channels at 7/10nm Node
- Issues with Ge n+ USJ Formation & High Dopant Activation
- Strain-Ge High Mobility Channel Material
- Experimentation
  - 70nm Ge-epi/SiGe-buffer/Si P(100) wafer
  - P, Sb and Sn Implantation
  - 308nm Eximer Laser Annealing
- Results
  - Rs Dopant Activation
  - SIMS Dopant Profiles
  - XRD Strain-Ge Analysis
  - Differential Hall Mobility Depth Profiles

#### 20,000,000 IC End-Use Markets (\$B) and Growth Rates 2014=\$336B 30% 18,000,000 Standard PCs Cellphones \$58.1 \$64.3 Share of 2013 IC Sales (Est) 25% 16,000,000 20% Wearables Number Of Devices In Use (In Thousands) 15% 14,000,000 Automotive Smart TVs Tablets \$19.9 10% Servers Wireless \$14.7 \$14.0 Networks Digital 12,000,000 Set Top Box Game \$8.6 5% TVs \$6.0 Medical Consoles \$13.1 \$3.8 \$3.8 0% 10,000,000 0% -5% 5% 10% 15% 20% 2012-2017 CAGR Source: IC Insights **Internet Of Things** 8,000,000 We are here 6,000,000 2014 total smartphone sales were 1.24B units. **Tablets** Q4/14=367.5B smartphones =69% of cell phone sells! 4,000,000 Q1/15=71.7B PC/tablets Smartphones 2,000,000 **Personal Computers** (Desktop And Notebook) 0

#### **Global Internet Device Installed Base Forecast**

2004 2005 2006 2007 2008 2009 2010 2011 2012 2013E 2014E 2015E 2016E 2017E 2018E

Smart Watch User Case	40LP	28SLP	FinFet	FD	FD+FBB
Power @ ISO Freq	1	0.71	0.39	0.33	0.23
Freq. @ ISO power	1	1.56	2.80	2.55	2.97
mW/Day (active and static)	334	238.6	131.2	109.7	76.3
Battery Life (Days)	4.55	6.37	11.58	13.85	19.91
Battery Life ISO	1	1.4	2.5	3.0	4.4

~5x battery life increase from 4 to ~20 days



Rated and Actual Energy Use and Battery Energy Storage for Conventional Smart Phones

gure 1. Average power draw constraint as a function of etime and battery size

Pr	roduct Name	Mfg. Standby	Vendor reported Run Time	Actual Run Time * <sup>1</sup>	Installed Battery
1	HTC	406 h	5h 20	2 ~ 3.5 h	Li-Ion
	Dream		minutes		1150 mAh
2	Google Nexus One	290 h	7h	3.5 ~ 5.5 h	Li-Ion 1400 mAh
3	Apple IPhone 5	225 h	8h	3~5h	Li-Po 1440 mAh (5.45 Wh)
4	Samsung Galaxy 5	375 h	6.45 h	2.5 ~ 4.5 h	1200 mAh
5	Nokia Lumen 1520	32 days	24 h	9 ~ 10.8h	3400mAh * <sup>2</sup>
(	Motorola Droid	>	48 hrs		

Morris Chan chairman of TSMC wants 1 week cell phone battery life so need low leakage devices!



Figure 16. Key electronic parameters for major semiconductors. Note the improved mobility for Ge vs Si, along with the degraded bandgap (47).

#### \*2016: >50%SiGe→100%Ge-FinFET at **10nm** \*2018: Nano-wire at 5nm (Si, SiGe and Ge)



Low Parasitics

Variability sources for Vmin < 0.5V

Conclusion

#### Transistor Structure for 10nm and 7nm nodes



### **100nm Ge Thermal Surface Loss at 600C**



Fig. 4. SIMS profiles of ion-implanted boron in the Ge wafer with/without an SiO<sub>2</sub> cap layer as a function of temperature.

Oh & Campbell, Univ of Texas, J. Electronic Mats., vol.33, no.4, p. 364, 2004.

6

7/15/2015

# Anneals appear to have caused Ge loss

Assuming repeatable anneal conditions....

#### Following High Temp Anneals Only:

- 700 °C loss is 33%
- 900 °C loss is 50%

Very low temperature anneal (375 °C) prior to high temp. anneal greatly mitigates Ge loss.

#### Following Very Low Temp Anneals (375 °C) + High Temp Anneal:

- 700 °C loss is 7%
- 900 °C loss is ~ 0%

# **Random RBS channel**



375C then 900C anneal shows no Ge loss 900C alone shows 50% Ge loss





SRP for P-implant and co-implant in 1um Ge-epi wafers after 625°C RTA annealing

SRP for P-implant and co-implant in 1um Ge-epi wafers after 900°C RTA annealing



for SiGe alloys, which form random solid solutions in a diamond cubic structure.

IEDM-2012 Paper 23.3: YJ Lee of NDL on "Full Low Temperature Microwave Processed Ge CMOS Achieving Diffusion-Less Junction and Ultrathin 7.5nm Ni Mono-Germanide".

10<sup>10</sup>

100

Depth (nm)

50 100 Depth (nm)

150

15

 $10^{22}$ 

Concentration (cm<sup>-3</sup>

 $10^{18}$ 

as-imp

(a) P

50

RTA 600 °C 60sec

RTA 600 °C 10sec

MWA 390 °C



100

Depth (nm)

150

200

50

Fig. 3 SIMS and SRP profiles of (a) P and (b)  $BF_2$  at  $1 \times 10^{15}$  cm<sup>-2</sup> in (100) Ge. The P distribution after MWA is identical to as-implanted, but not after RTA. All boron distribution profiles are close to as-implanted. The insets show the activated levels of P and B by SRP are  $2 \times 10^{19}$  cm<sup>-3</sup> and  $7.5 \times 10^{19}$  cm<sup>-3</sup>.

200

### **DIFFUSION & ACTIVATION ANALYSIS**



Phos 180 160 140 Rs (Ohm/sq) 120 12 J/cm<sup>2</sup> 2×11J/cm 100 Sheet resistance 2×12 J/cm<sup>2</sup> 13 J/cm 80 14 J/cm<sup>2</sup> 155 J/cm<sup>2</sup> 60 40 P annealing 20 **15Ω/**□ max solid solubility [1] 0 0 25 50 75 100 125 150 175 Xj (nm) at 1E18 at/cm3

Submelt: no modification of SIMS profile
 Melt < 1.4 J/cm<sup>2</sup>: no diffusion at 1×10<sup>18</sup>cm<sup>-3</sup>
 Abruptness : from 28 to 8 nm/dec

LTA vs RTP: reduced Rs at same Xj depth
 Extracted Nact = 1.2×10<sup>20</sup>cm<sup>-3</sup> with 1.3 J/cm<sup>2</sup>
 Energy >1.3 J/cm<sup>2</sup> :100% dose activated
 No positive contribution of multi pulse laser

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[1] F. A. Trumbore, Elec. Soc., 205-233 (1959)

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Mazzocchi et al., IEEE-RTP 2009

### Thareja et al., Stanford, IEDM-2010 ref 11



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Fig. 13 : Reduction in ps as laser fluence is increased from 0.3 - 0.5 J-cm<sup>-2</sup>. Sb provides the lowest pe

### Rs results: Slot 11 (P) and Slot 13 (Sb)



- Rs decrease with laser-annealing energy.
  - Reach saturation at high energy

Rs (Ohms/sq)	Slot 11	Slot 13	
Edge	741.53	538.49	
No-anneal	701.77	494.59	
Substrate	100.72	85.21	

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# Trumble, Bell Labs, 1959



7/15/2015





Marketing, Sales & Technology)

950℃では、SiGe層からの信号有るが非常にブロード(濃度分布?)。

# Localized/Selective Ge & SiGe Formation By Liquid Phase Epitaxy (LPE) Using Ge+B Plasma Ion Implantation And Laser Melt Anealing

**IWJT June 6, 2013** 

JOB Technology, Micron, Innovavent, Excico, KLA-Tencor, CNSE, EAG & UCLA

Ge 3keV (~7nm) at 1E16/cm2 & 1E17/cm2 B2H6 500V (~7nm) at 4E15/cm2 & 4E16/cm2

Ge+B Plasma Implanted Wafers Provided by Micron Laser Melt Annealing Provided by Innovavent & Excico



Laser Power Level (J/cm2)







Borland et al., IWJT-2013

Liquid Phase Epitaxy (LPE) Formation of Localized High Quality/Mobility Ge & SiGe by High Dose Ge-Implantation with Laser Melt Annealing for 10nm and 7nm Node

#### Oct 6, 2014 ECS Conference on SiGe & Ge Technology

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<sup>6</sup>EAG, East Windsor, New Jersey
<sup>7</sup>University of Florida, Gainsville, FL
<sup>8</sup>Active Layer Parametrics, LA, CA



Laser Power Level (J/cm2)



J.O.B. Technologies (Strategic Marketing, Sales & Technology)



Borland et al., ECS Oct 2014

## IEDM-2013 Stanford/Synopsys paper: 4%GeSnchannel for pMOS & 100%Ge-channel nMOS

3.0E+

1.1E+

-1.2E+

-1,4E+

1.5E+

1,7E+

ST

Stress-XX [

1.5E+

1.1E+

9.0E

7.0E+4

ST

SRB

SRB



Fig. 3 MOSFET fabrication process flow (a) Fin, SiGeSn SRB patterning (b) STI formation (c) Poly gate definition (d) Spacer formation and S/D recess (e) In-situ doped S/D epitaxial re-growth, (f) Gate last high-k metal gate. In-situ doped S/D epitaxial re-growth, (f) Gate last high-k metal gate. In-situ doped S/D epitaxial re-growth, (f) Gate last high-k metal gate. In-situ doped S/D epitaxial re-growth, (f) Gate last high-k metal gate. In-situ doped S/D epitaxial re-growth, (f) Gate last high-k metal gate.



Fig. 4 (a, b) PMOS and NMOS devices (gate stack, spacers, contacts omitted) fabricated using '7nm' design rules. PMOS: GeSn (4% Sn) channel, *in-situ* doped GeSn (8% Sn) S/D. NMOS: Ge channel, *in-situ* doped Si<sub>0.3</sub>Ge<sub>0.7</sub> S/D (c, d) Longitudinal stress distribution ( $\sigma_{xx}$ ) for PMOS and NMOS. Other components of stress were found to be less than 10% of  $\sigma_{xx}$ 



Fig. 12 Different options for tuning the channel stress: (a) Si content in NMOS S/D stressor, Sn content in PMOS S/D stressor (b) Lattice constant of the common SRB. Channel material kept invariant: GeSn (4% Sn) (PMOS) and Ge (NMOS), '7nm' design rules.

7/15/2015

- Outline Introduction
- **Experimentation** 
  - 70nm Ge-epi/SiGe-buffer/Si P(100) wafer

110

-73

-110

-147

- P, Sb and Sn Implantation at 5E15/cm2
  - P=4keV, Sb=11keV & Sn=10keV
  - P, Sn+P, Sb and Sn+Sb
- 308nm Excimer Laser Annealing 0.6-1.6J/cm2 147

0.6 07

-147 -110 -73

## Results

- SIMS Dopant Prof 36
- XRD Strain-Ge Ar •
- Summary

J.O.B. Technologies (Strategic Marketing, Sales & **Technology**)



110

147

Sn+Sb

36

Sb

-36

sor.



31

# Half-Wafer Sn-Implant 5E15/cm2 Full Wafer P or Sb 5E15/cm2 Implant



# Half-Wafer Sn-Implant 5E15/cm2



## µ-uniformity mapping (µMap)





TWU increase with laser-annealing energy



Laser annealing Energy (J/cm<sup>2</sup>)

w/ Si

lo Sn



TWU increase with laser-annealing energy

**IWJT-2015 Paper S5-2** by Nishimura of **Univ of Tokyo** on "Recent Progress of Junction Technology for Germanium CMOS". In Fig.4 below they used Raman analysis to quantify implant annealing damage recovery from the P=30keV/3E15 implant in to Ge-Cz wafers. They commented that even after high temperature annealing at 850°C the Raman Ge peak did not recover to the reference Ge-Cz wafer level concluding there still remains some residual implant damage. Fig.5 shows the effects of P implant dose from 1E13/cm<sup>2</sup> to 3E15/cm<sup>2</sup> on resistivity and FWHM Raman Ge-peak with 600°C 5 min SPC (solid phase crystallization) annealing and the critical P-implant dose is <2E14/cm<sup>2</sup> to be defect free after annealing.



Fig. 4 (a) Typical Ge Raman peaks (around 300 cm<sup>-1</sup>) before and after P ion implantation with a dose of  $3 \times 10^{15}$  /cm<sup>2</sup> and thermal annealing. (b) Annealing temperature dependence on crystallinity recovery of Ge. Although the annealing temperature was increased up to 850°C, still crystallinity is still worse than that of initial Ge substrate.

Fig. 5 (a) Resistivity and FWHM of Raman peak of P implanted GeOI as a function of implantation dose. Above 3  $\times 10^{14}$  /cm<sup>2</sup>, FWHM of Raman peak is increased and reduction of resistivity is saturated. (b) Correlation between resistivity and FWHM of Raman peak. By solid phase diffusion with phosphorous silicate glass (PSG), further reduction of resistivity is achieved without increasing FWHM of Raman peak.

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### Summary





Borland & Konkola, AIP, IIT-2014



















Laser Anneal Power (J/cm2)



# Trumble, Bell Labs, 1959



7/15/2015









# **Bulk Trends – Mobility**







See large variation in reported Ge electron & hole mobilities reported in the literature!

# • Introduction

- Experimentation
- Results
- Summary:
  - Laser-LPC (Liquid Phase Crystallization) critical to achieve controlled n+ USJ down to sub-10nm with high dopant activation without diffusion.
  - Best reported Ge n+ USJ activation level of 1E21/cm3 at 10nm is for Sb implant with laser-LPC
  - Best reported Ge n+ USJ activation level of 3-5E20/cm3 at 10-40nm is for P implant with laser-LPC.
  - Sn implant can be engineered to:
    - Improve Electron Mobility by 2x and uniform depth with Sb implant n+ doping
    - Is neutral to degrade Electron Mobility by 3x with P implant n+ doping.

 Next try Sn implant for Ge p+ USJ Hole Mobility Enhancement (B, BF2, B18, In, Ga)