Leading Edge Silicon Devices

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Chipworks
Outline

- Intel finFETs
  - 22 nm Xeon 1230 & Baytrail
  - 14 nm Broadwell
- TSMC 20 nm planar (Qualcomm MDM9235)
- Samsung 20 nm planar (Exynos 5430) & 14 nm finFET (Exynos 7420)
- IBM 22 nm planar SOI (Power8)
Intel’s Finfet Evolution – from 22-nm to 14-nm Process (+ Variants)
FinFETs – Fin Details

- NMOS/PMOS fins similar
- Top radius ~ 2.5 nm
- Functional fin width 5 – 15 nm top/bottom
- Gate width ~70 nm
- <110> channel direction
FinFETs – PMOS Gates

- Minimum gate length observed ~ 25 nm
- Epi SiGe in PMOS source-drains, isotropic cavity etch
- Ti silicide, not Ni
- Gates back-etched and filled with dielectric, allows self-aligned contacts
FinFETs – PMOS Gate

- Similar gate stack to 32-nm, 45-nm generations
- TiN work-function metal, ~1 nm Hf-based hi-k, ~1 nm SiO
- Gate fill changed from Ti-Al to tungsten/TiN
FinFETs – PMOS Source/Drains

- ~50% SiGe, defects in epi growth on some fins
- E-SiGe appears to penetrate slightly under gate
- Epi lateral growth limited by sidewall spacer (SWS)
PMOS Source/Drains EDS Maps

- Clearly shows Ti silicide in epi
FinFETs – NMOS Gates

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FinFETs – NMOS Source/Drains

- ‘Mushroom’ profile epi, no facets
- SWS nitride left on fin sides
- Epi lateral growth limited by SWS
**NMOS Source/Drains EDS Maps**

- Clearly shows Ti silicide in epi
- P diffusion can be seen
Intel 22 nm Atom “Baytrail” SoC
Intel 22 nm SoC HV Transistors

- Similar gate stack to logic transistors, longer gate, thicker $T_{ox}$
Intel 22 nm SoC Source/Drains

- Modified epi compared with Xeon device – shorter cycles?
Intel 22-nm Summary

- First example of a tri-gate/finFET part in high-volume commercial production
- Gate work-function materials are similar to those used for the previous 45- and 32-nm generations
- Embedded SiGe is still used as a PMOS stressor
- Gate fill has changed from TiAl to tungsten
- Al-doped copper is used for electromigration improvement
- Effective k-value of the dielectric has been reduced to help minimize intermetal parasitic capacitances
- Integrated MIM capacitors in CPU, SoC parts
- Passives introduced in SoC process
- Embedded DRAM available
Intel 14 nm Broadwell
Intel 14-nm Broadwell

- Contacted gate pitch ~70 nm
- Nominal fin pitch ~42 nm
Intel 14-nm Broadwell

- Vertical fins! But still rounded fin tops.
- PMOS gates formed first
- W fill in NMOS
- Multiple steps to achieve fin profiles after fin etch

- Asymmetric stress deforms fins
  - Leftmost fin leans left
  - Rightmost fin leans right
Intel 14-nm – PMOS Gates

- Minimum gate length observed ~22 nm
- TiN work-function metal
- Epi SiGe in PMOS source-drains, isotropic cavity etch
- Gates back-etched and filled with dielectric, allows self-aligned contacts
Intel 14-nm – NMOS Gates

- TiAlN work-function metal
- SWS etched before S/D epi growth
- Ti silicide, not Ni
Intel 14-nm – Source/Drains

- PMOS epi-SiGe takes<br>  <111> planes as in 22-nm
- NMOS epi takes <111> planes at base
  - Cavity etch used
- SWS etched before S/D epi growth in PMOS and NMOS
- And.. here be airgaps!
Intel 14-nm – Fin Distortion

- Visible micro-loading and double patterning effects

Before STI densification fins are vertical

STI densification severely deforms the fins. Later, at STI etch, they partially recover.

Qualcomm MDM9235 (20 nm HPM HKMG Process)
20HPM PMOS Transistors

- Second-generation HKMG process – hi-k formed after polySi removal (like Intel 32-nm)
- PMOS gate stack formed before NMOS
- Minimum observed gate length 28 nm
- Work-function materials similar to 28-nm process – PMOS is TiN
- Raised source/drain epi with e-SiGe, graded -> ~40% Ge
20HPM NMOS Transistors

- Minimum observed gate length 31 nm
- Raised source/drains, stacking faults for stress (like Intel 32-nm)
- TiAlN work-function material, similar to 28-nm process
- <110> channel
- AlCoCu gate fill with AlO cap
Samsung Exynos 5430
(20 nm Gate-Last HKMG Process)
Samsung 20 nm PMOS Transistors

- This is Samsung’s 1st generation gate-last, replacement gate HKMG process
  - High-k formed after polySi removal
- 193 nm immersion lithography was used for critical layers
- 10 metals including one level of Al, nine levels of Cu. Mn-doped Cu metallization was used in the lower Cu levels.
- PMOS e-SiGe graded to ~50%.
- Work-function materials similar to Intel/TSMC process – PMOS is TiN
Samsung 20 nm NMOS Transistors

- Contacted logic gate pitch 90 nm
- Minimum metal pitch 80 nm
- Minimum observed gate length ~30 nm
- Work-function materials similar to Intel/TSMC process – NMOS is TiAlN
Samsung Exynos 7420 (14 nm FinFET Process)
Samsung 14 nm FinFETs

- 1\textsuperscript{st} generation finFET transistors, 2\textsuperscript{nd} generation RMG process
- 48 nm fin pitch, gate pitch ~78 nm
- No self-aligned contacts, Ti silicide
Samsung 14 nm FinFETs

- TiN PMOS WF material, TiAlC NMOS WF material
- Functional fin height ~38 nm, fin width ~8 nm at half height
- Minimum gate length ~27 nm, gate width ~80 nm
Samsung 14 nm FinFET Source/Drains

- PMOS epi not consistently merged, location dependent
- NMOS epi is consistently merged, location independent
- PMOS Ge graded -> ~40%
Samsung 14 nm FinFET Source/Drains

- Isotropic cavity etch, ~50 nm deep
IBM POWER 8 Server Processor (22 nm SOI Gate-First HKMG Process)
IBM 22HP Transistors

- PMOS e-SiGe source/drain (S/D), Ge graded $\rightarrow$ 30% Ge
- PMOS e-SiGe channel $\rightarrow$ 25% Ge
- NMOS e-Si S/D tubs (claimed eSi:C$^{[7, 8]}$), also doped with 2% Ge (likely for stress relaxation or to control phosphorus out-diffusion)
- Aluminum on hafnium oxide gate dielectric to adjust WF in PMOS gate dielectric layer
- TiN layer under silicided polysilicon gate
- NiPt-silicided S/D and gate
- Raised S/D in both NMOS and PMOS
- Dual stress liner


Where do we go from here?

Source: imec

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<th>Node</th>
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Source: Synopsys

− Intel 14 nm
− Samsung 14 nm
Where do we go from here?

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**Strained SiGe: Combination Champion (7 nm)**

My guess:
- Si FinFETs at 10 nm (possibly SiGe for HP)
- Si -> SiGe at 7 nm
- RMG at 10 nm, but 7?
- The clock will slow down – 10 in 2017, 7 in 2020?
Summary

- A look at Intel’s finFET evolution
- TSMC’s 20-nm transistors
- Samsung 20-nm planar and 14-nm finFET transistors
- IBM 22-nm transistors
- The future?
Acknowledgements

I would like to thank Chipworks’ laboratory staff and process analysts for all the hard work of analyzing these complex devices. They did a great job!