Laser Spike Annealing for sub-20nm Logic Devices

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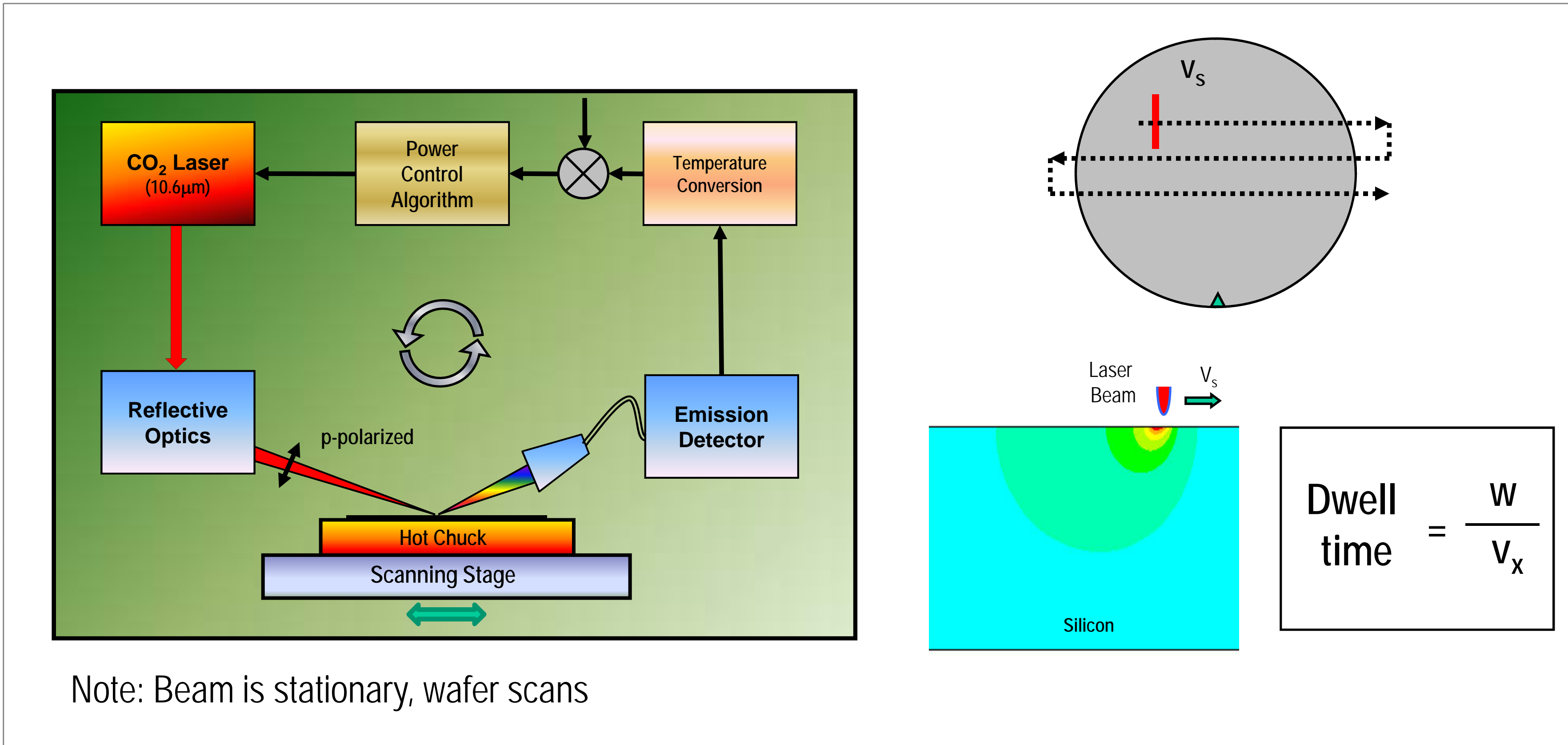
Outline

- Introduction
- Pattern Loading Effects
- LSA Applications
    - Dopant Activation
    - Ti silicide
- Summary

LSA Overview



Key Attributes

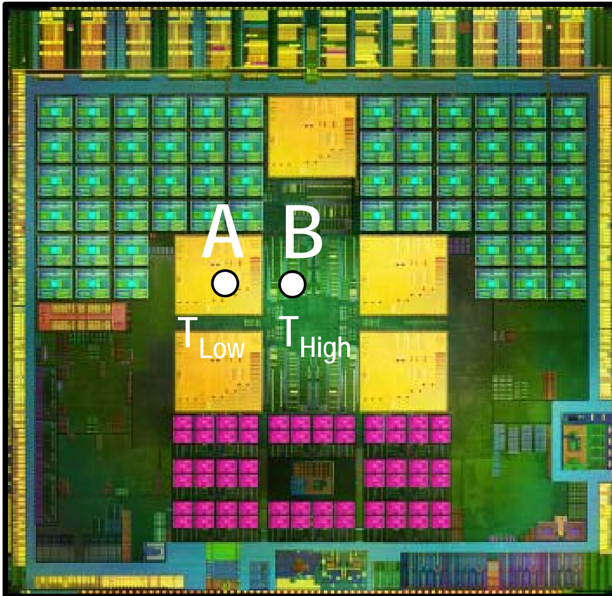
Within-die Uniformity
- CO2 Laser: λ ~ 10um
- P-polarized, brewster angle

Within-wafer & Wafer-to-wafer
- Temperature feedback control

Pattern Loading Effects

Pattern Effects and Parametric Yield

System-on-a-Chip



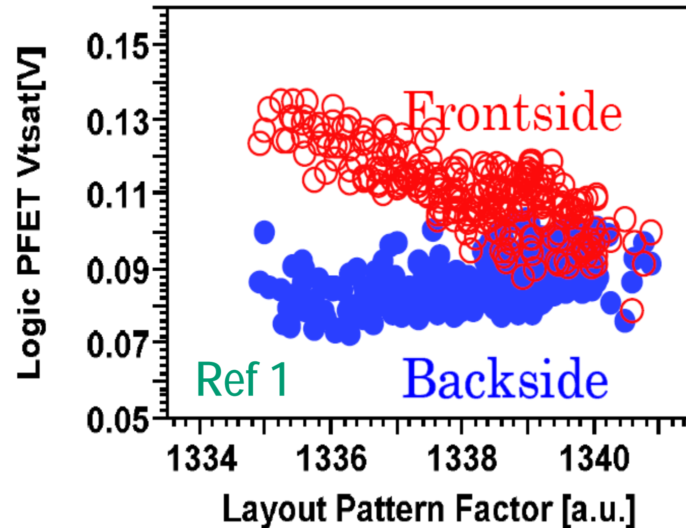
Device A gets colder during anneal
Device B gets hotter during anneal

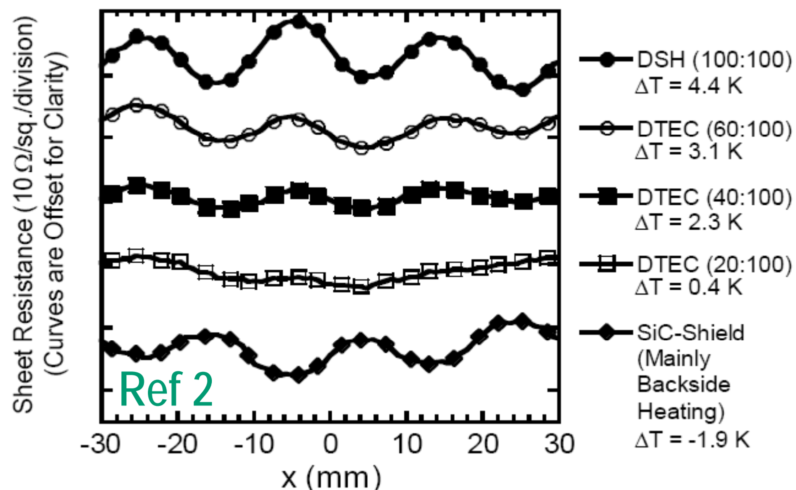
Device Performance Mismatch!

- Variations in pattern density lead to local variations in the absorbed radiation during RTP or millisecond anneal
- This can lead to local variations in peak temperature, and variations in performance of devices which are supposed to be matched

Pattern loading effects during millisecond annealing or RTP can cause device performance mismatch within the die → parametric yield loss and degraded circuit speed

Pattern Loading Effects in RTP: Equipment Solution





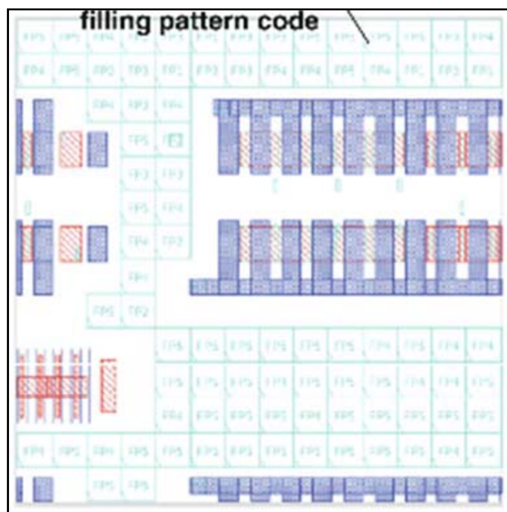
Highlights

- Lots of recent work on how to change RTP equipment solutions to suppress pattern effects: backside heating[1] or Differential Thermal Energy Control[2]
- These approaches are being implemented in Fabs for critical processes at advanced nodes
- Current implementations for "dummification" are not adequate for critical processes

1. X. Yu et al, IEDM 2012
2. P. Timans et al., IWJT 2014

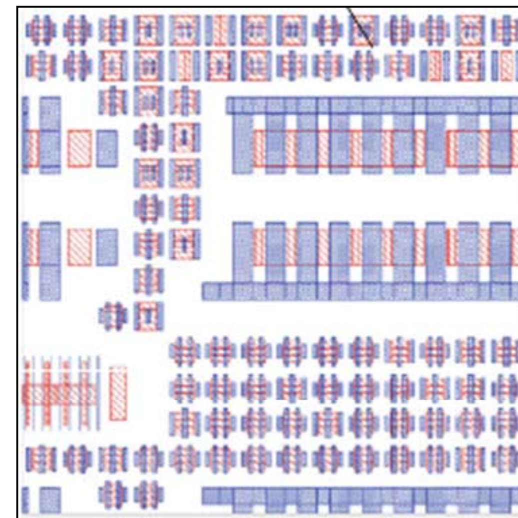
Pattern Effects in MSA: Layout Design Solution

Pre-dummification



$\Delta T > 100^oC$ (typical)

Post-dummification



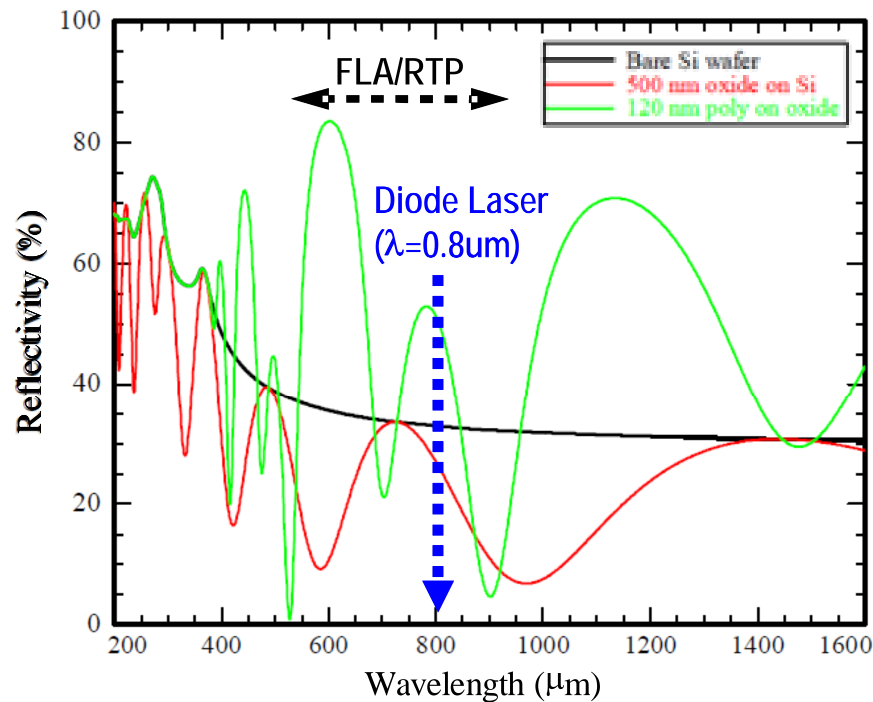
Simulation showed "$\Delta T < 50^oC$"

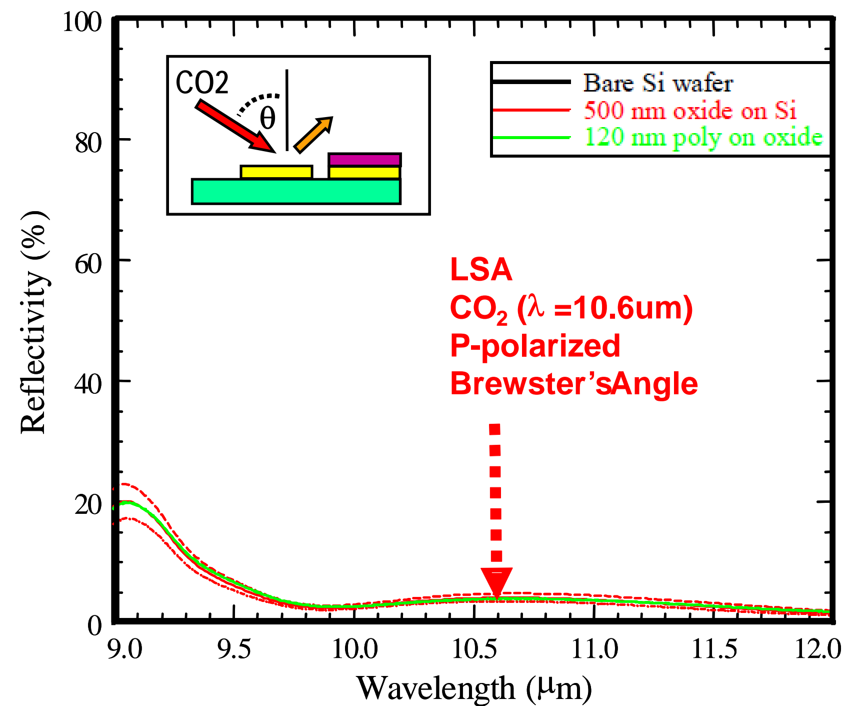
SC Lin et al., "Using genetic algorithm to optimize the dummy filling problem of the flash lamp anneal process in semiconductor manufacturing", J. Intell. Man. (2012)

- **Difficult to reduce to acceptable levels due to short heat diffusion length (~100um)**
- **Difficult to make design rules to cover all layouts in a foundry environment**

Pattern Loading Effects: Thin Film Interference

PLE: DL > FLA >> LSA

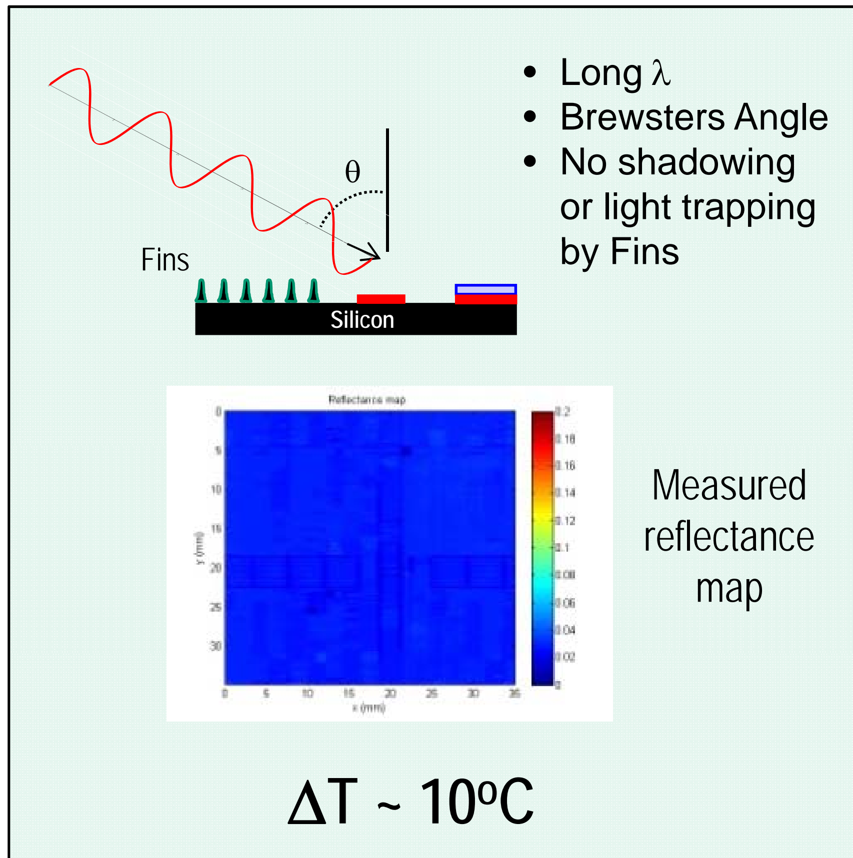




- PLE caused by thin film interference variations → severe at short λ
- Long λ+p-pol+Brewster's angle make LSA insensitive to device film variations

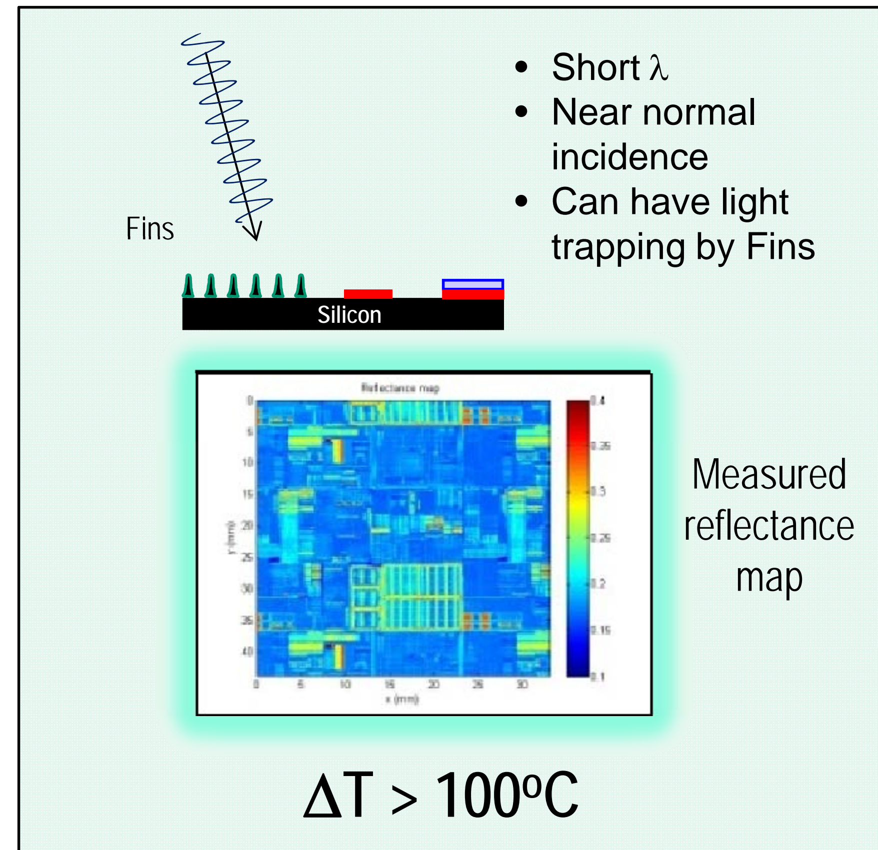
Pattern Loading Effects in Millisecond Annealing: Equipment Solution (LSA)

LSA



- Long λ
- Brewsters Angle
- No shadowing or light trapping by Fins

Flash Anneal / Diode Laser

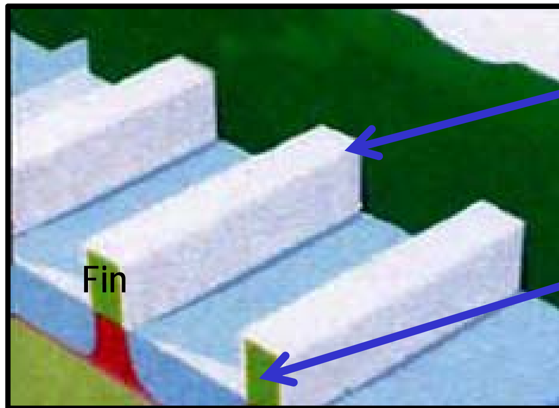


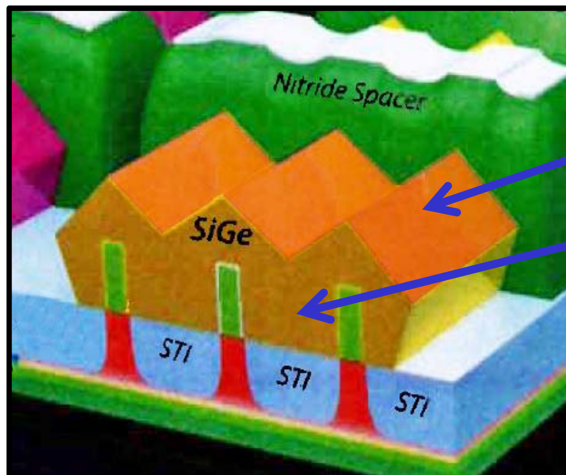
- Short λ
- Near normal incidence
- Can have light trapping by Fins

LSA provides an equipment solution for PLE in millisecond annealing

Applications

LSA Applications for 14/10nm FinFET Devices





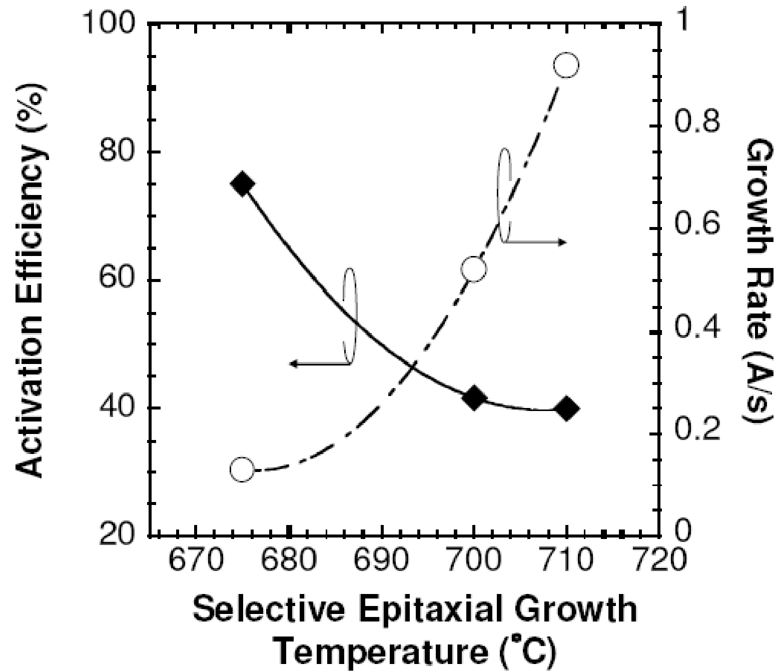
Device Applications

- Source/Drain extension annealing
- Deep Source/Drain annealing
- Hi-k anneal
- Dopant re-activation
- Ti Silicide

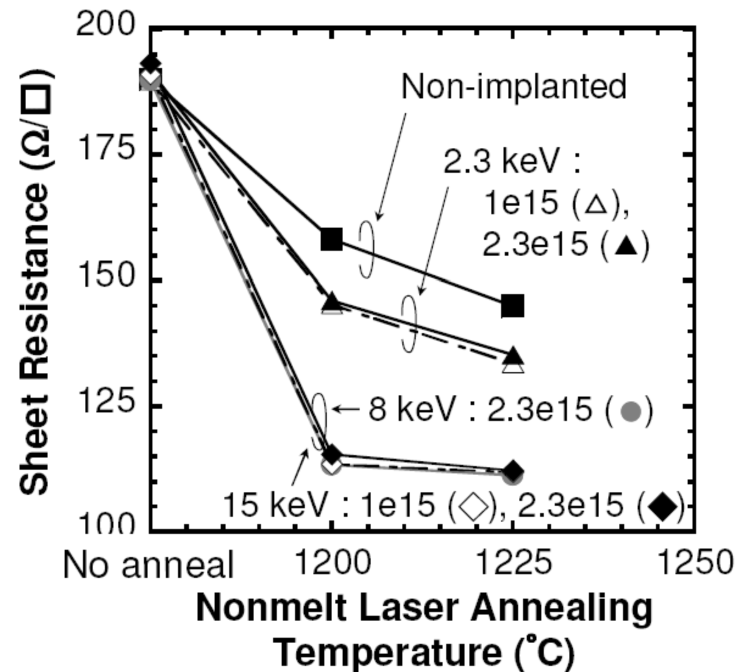
LSA enables device performance improvements and leakage reduction for FinFETs

Source/Drain (epi) Activation

Post-dep properties of Si:P Epi [1]



Post-LSA properties of Si:P Epi [1]



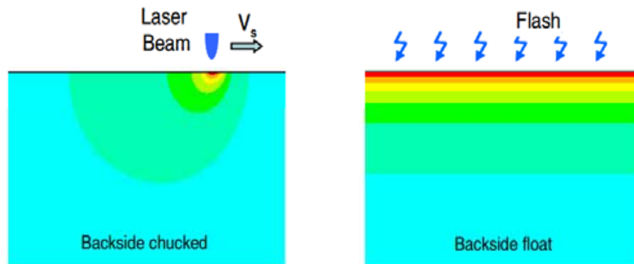
- As-deposited activation efficiency is low
- Trade-off between growth rate and activation

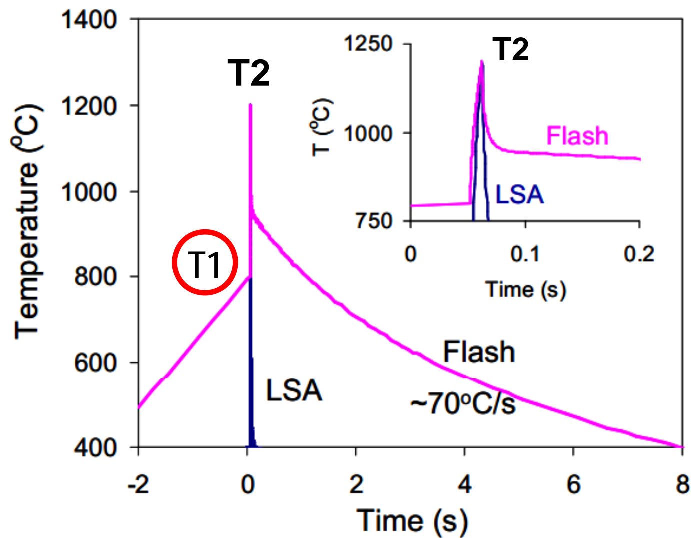
- Activation greatly improves with LSA
- Further improvement with cryogenic a-Si + LSA

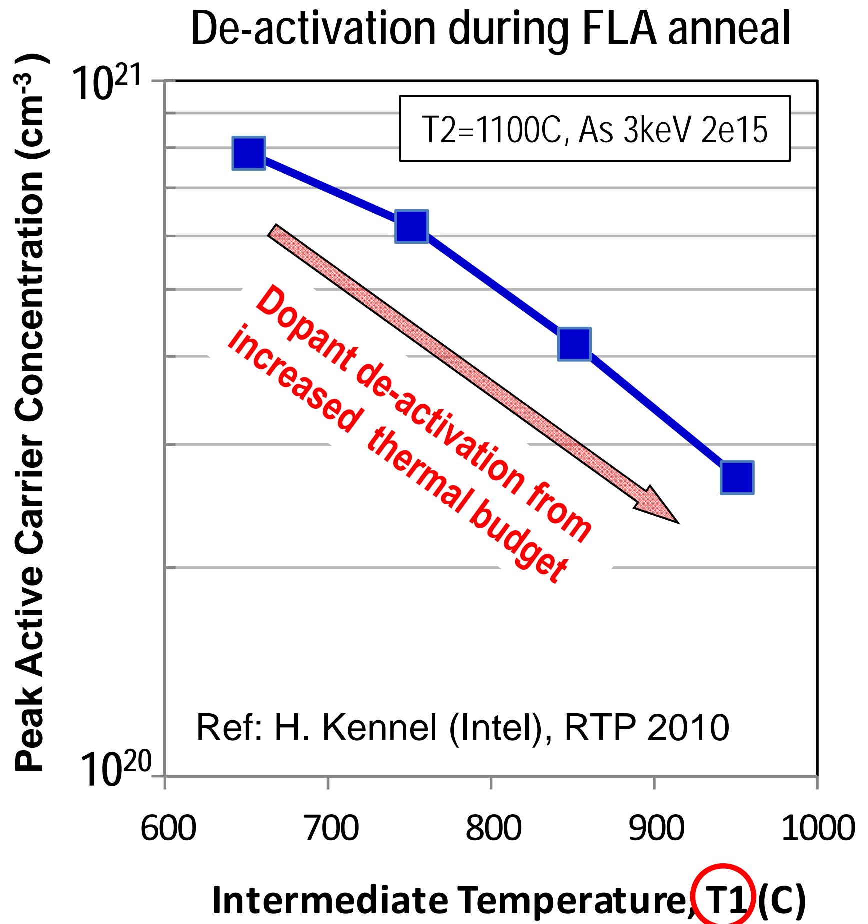
LSA improves activation and device performance by S/D activation in FinFETs[2]

Sources: 1.Itokawa et al., IWJT 2012, 2.Yamashita et al, VLSI 2011

Thermal Profiles of LSA vs. Flash Anneal

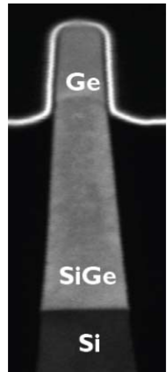




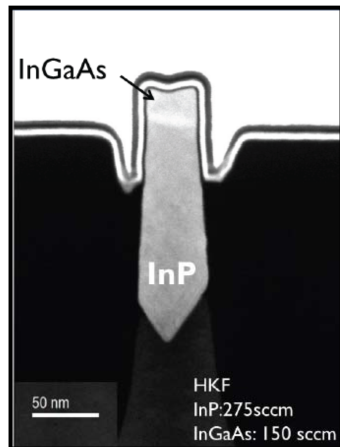


- LSA is a true low thermal budget anneal with no dopant de-activation
- Extra thermal budget of FLA can cause dopant de-activation → slower devices

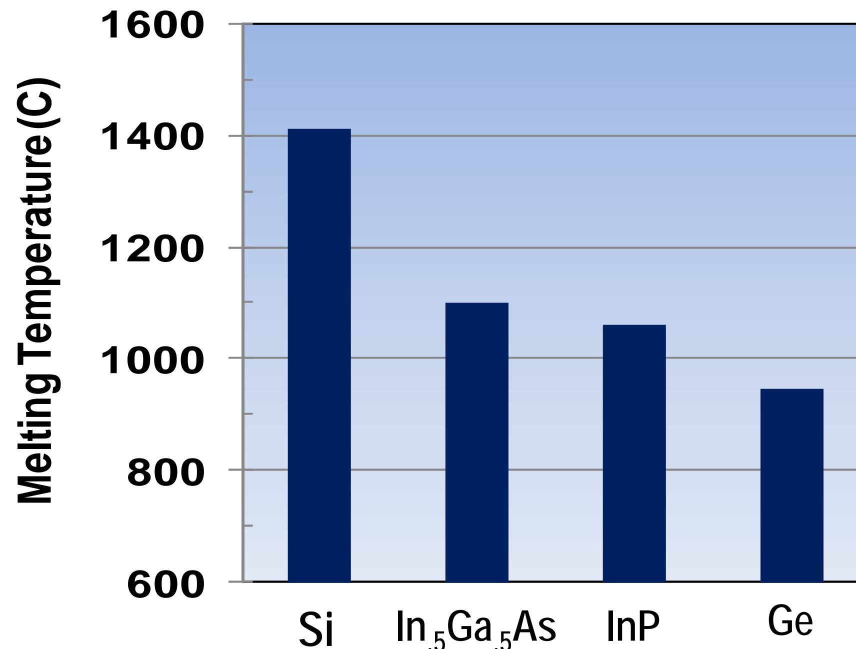
New Channel Materials



7nm pFET



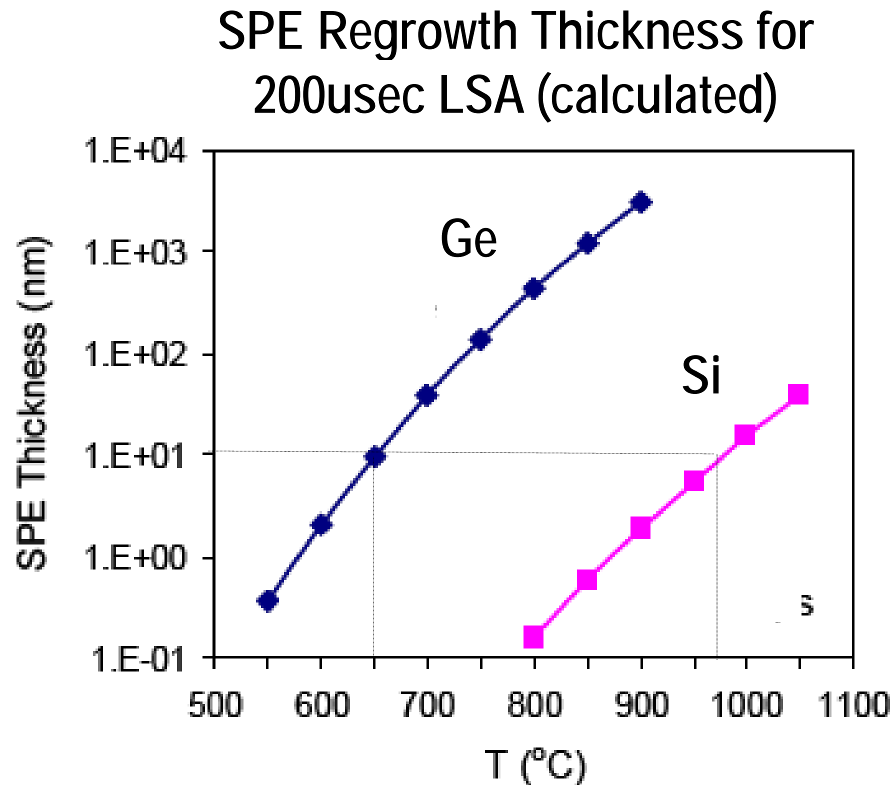
7nm nFET



A. Steegen, Imec Technology Forum, Semicon 2014

- **New channel materials will suffer damage at much lower thermal budgets than Si**
- **Low thermal budget of LSA compatible with new channel materials**

Arsenic Activation and Diffusion in Ge



Highlights

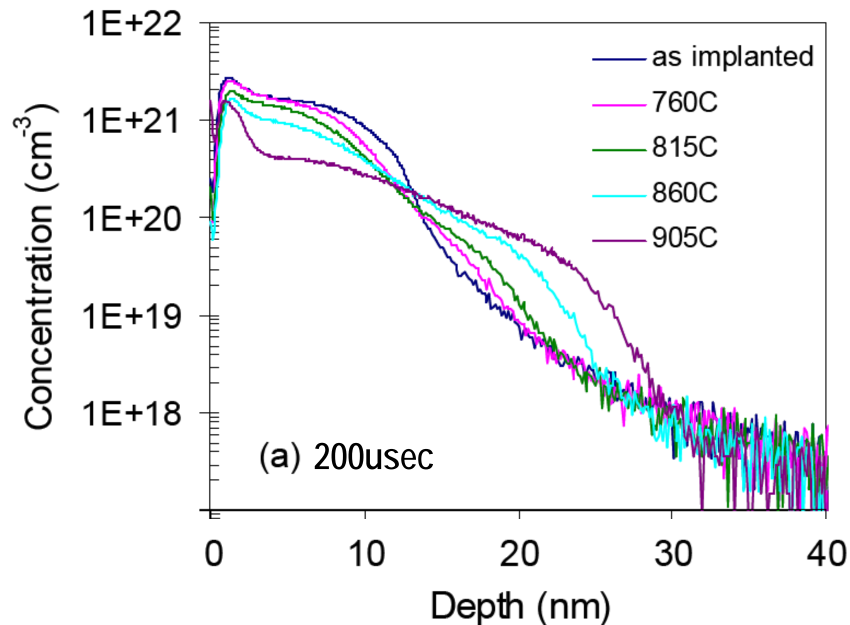
- Ge substrates* implanted with As 5keV 2e15 (creates ~10nm self amorphizing layer)
- Since SPE happens in Ge at much lower temperatures than Si, use low chuck temperatures to reduce thermal budget**
- Splits:
  - Peak temperature: 600 to 900C
  - Dwell time: 200 and 800usec
  - Chuck temperature: RT and 200C

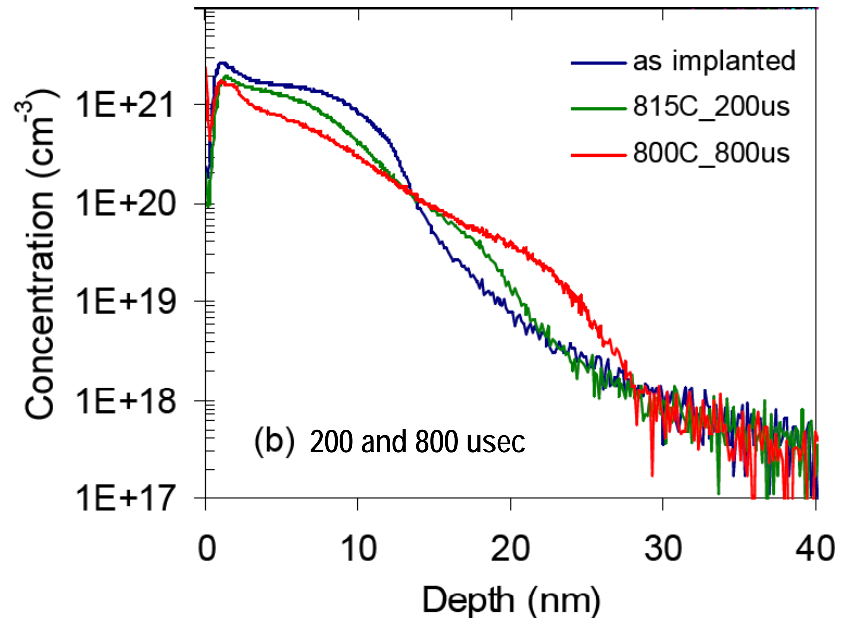
*Note: Substrates were Ga doped to ~ 6e17cm-2

** A higher SPE temperature typically results in higher activation

* Y. Wang et al., IWJT 2014

Arsenic Activation in Ge: Results



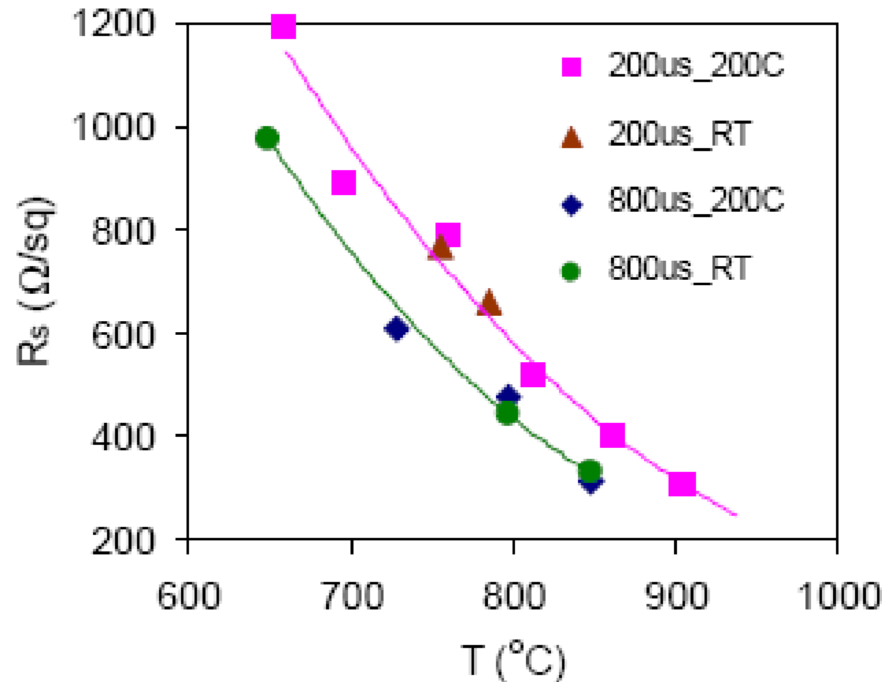


- Significant diffusion starts above 760C at 200usec
- Significantly more diffusion at 800usec than 200usec

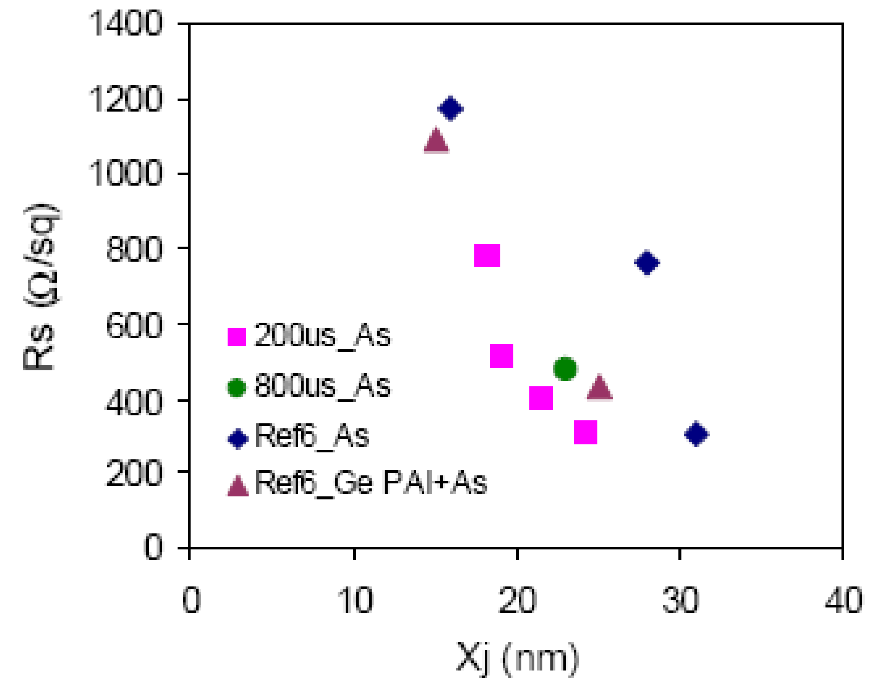
* Y. Wang et al., IWJT 2014

Arsenic Activation in Ge: Results (cont'd)

Rs vs. Temperature



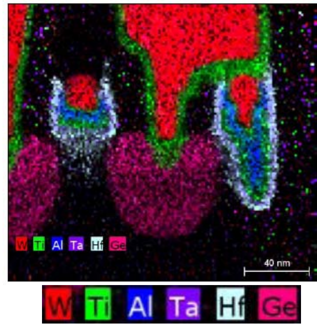
Rs vs. Xj



- **Significant Rs reduction at 800usec due to extra diffusion**
- **Chuck temperature RT vs. 200C did not make significant difference**

* Y. Wang et al., IWJT 2014

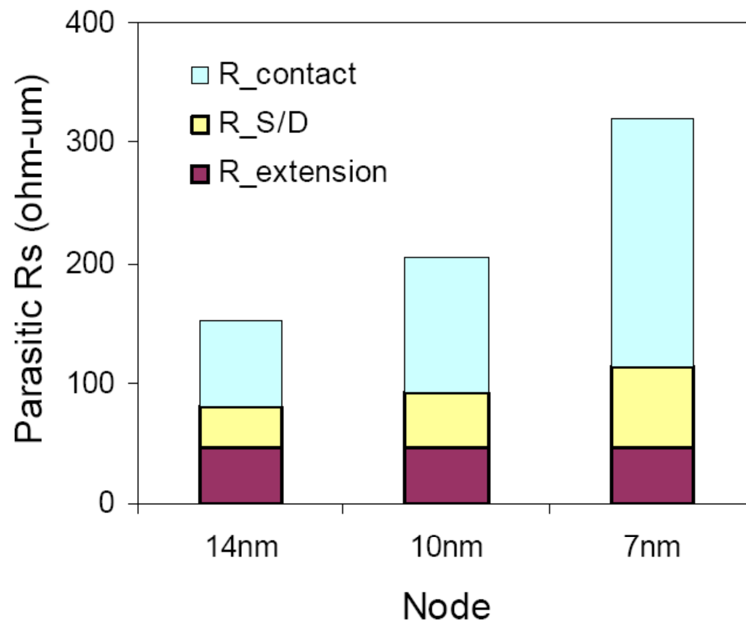
LSA for Titanium Silicide



Schottky barrier height

$$\rho_c \propto \exp\left(\frac{\phi_B}{\sqrt{N_D}}\right)$$

Dopant concentration

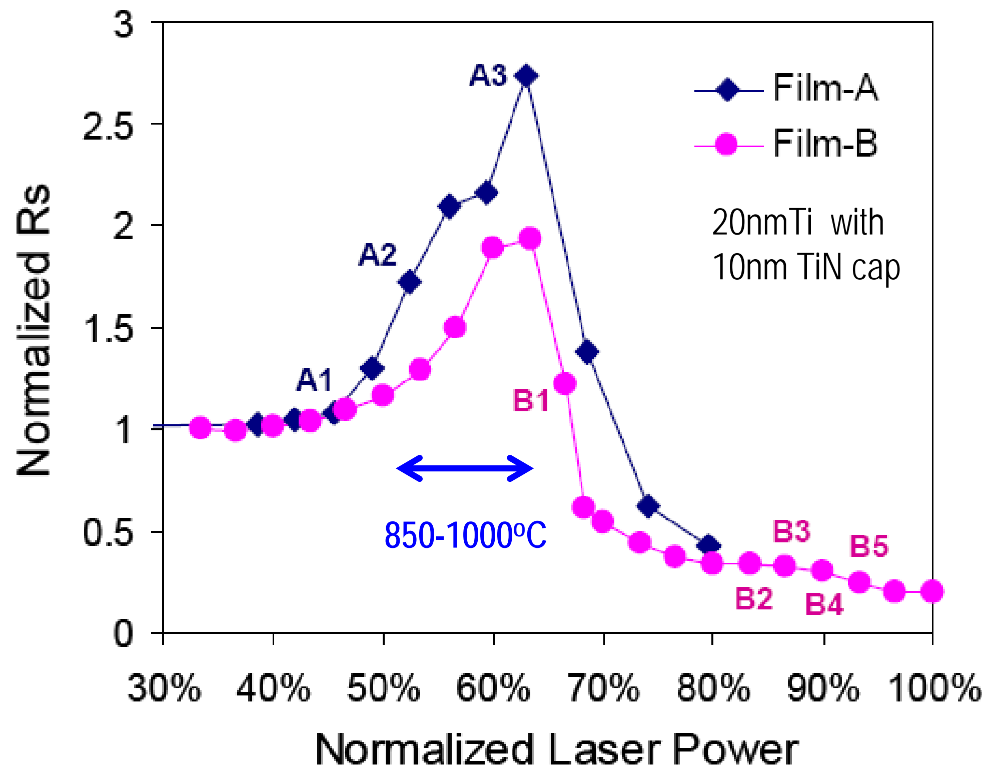


<u>Advantages of LSA for Ti silicide</u>

- Higher temperature than RTA → lower contact resistance
- Minimal interdiffusion of gate stack layers
- Process control
  - Minimal pattern effects
  - Closed loop temperature control
  - Becomes critical for Ti silicide where process window is smaller than Ni silicide

Refs: D. James, AVS JTG Semicon West (2013) and C. Sohn et al.," IEEE Trans. Elec. Dev., Apr. 2013.

LSA for Ti silicide: Phase Transformation Study

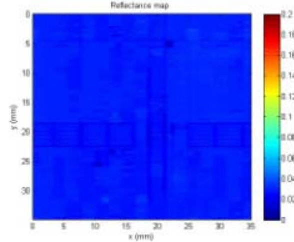


- Phases detected by XRD:
  - A1: Ti
  - A2: Ti, Ti_5Si_3
  - A3: Ti_5Si_3, possible Ti_5Si_4 or TiSi
  - B2/B3: $TiSi_2$ (C40)
  - B4/B5: $TiSi_2$ (C54)
- Examples of ϕ_B (G. Ottaviani et al, Phys. Rev. Lett., 1980):
  - $TiSi_2$: 0.6V
  - TiSi: 0.5V
  - NiSi: 0.67V

- Low Rs not required → Low Rc is the goal (low ϕ_B)
- No need to anneal at temperatures greater than ~1000C, where gate stack could be compromised

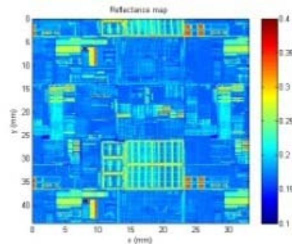
Pattern Loading Effects (PLE) For Silicides

Measured reflectance: LSA (10.6um)



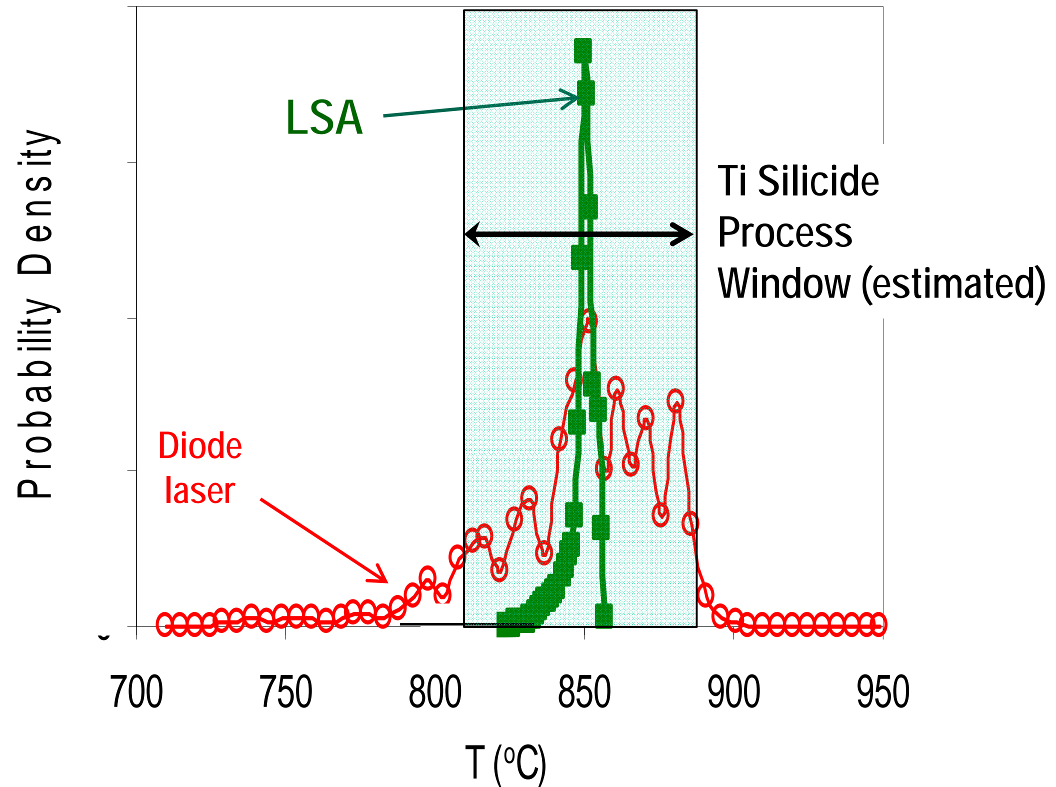
ΔT ~ 10C

Measured reflectance: Diode Laser (0.8um)



ΔT > 100C

Within-die temperature distribution: Simulated from measured reflectance maps



- Severe PLE of diode laser could impact yield for Ti silicide (PLE >100C)
- PLE of LSA is well within the process window (PLE~10C)

Summary

- Long-wavelength LSA provides an equipment-design solution for pattern loading effects in millisecond annealing
- LSA plays a critical role in reducing series resistance and leakage in today's FinFETs through multiple applications
- As sub-10nm devices migrate to new channel materials, low thermal budget annealing approaches such as LSA will be become more critical