Material Engineering for 7nm FinFETs

Victor Moroz

July 10, JTG Semicon West 2014,
San Francisco

Outline

- Introduction
- Group IV FinFETs
- III-V FinFETs
- Summary

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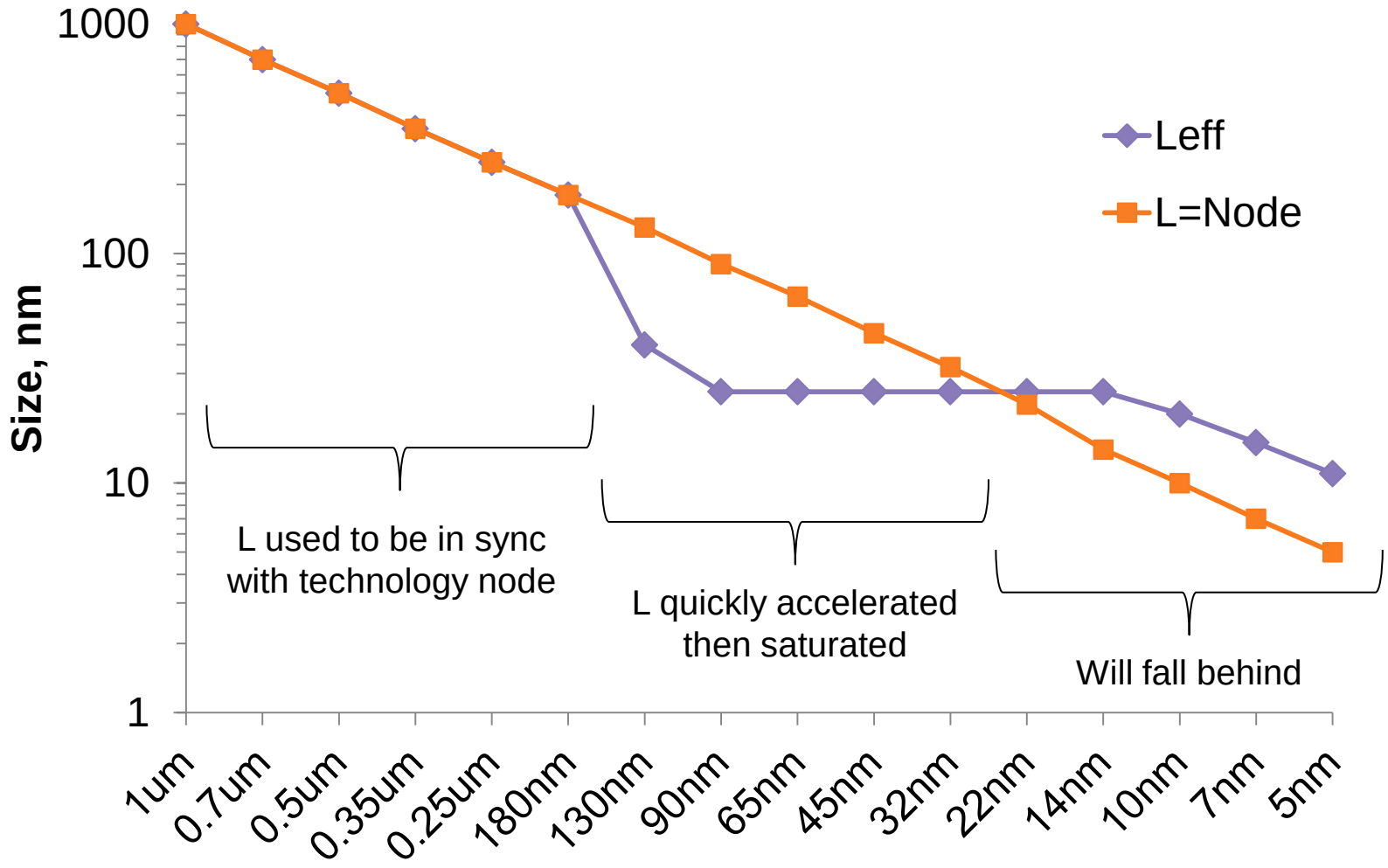
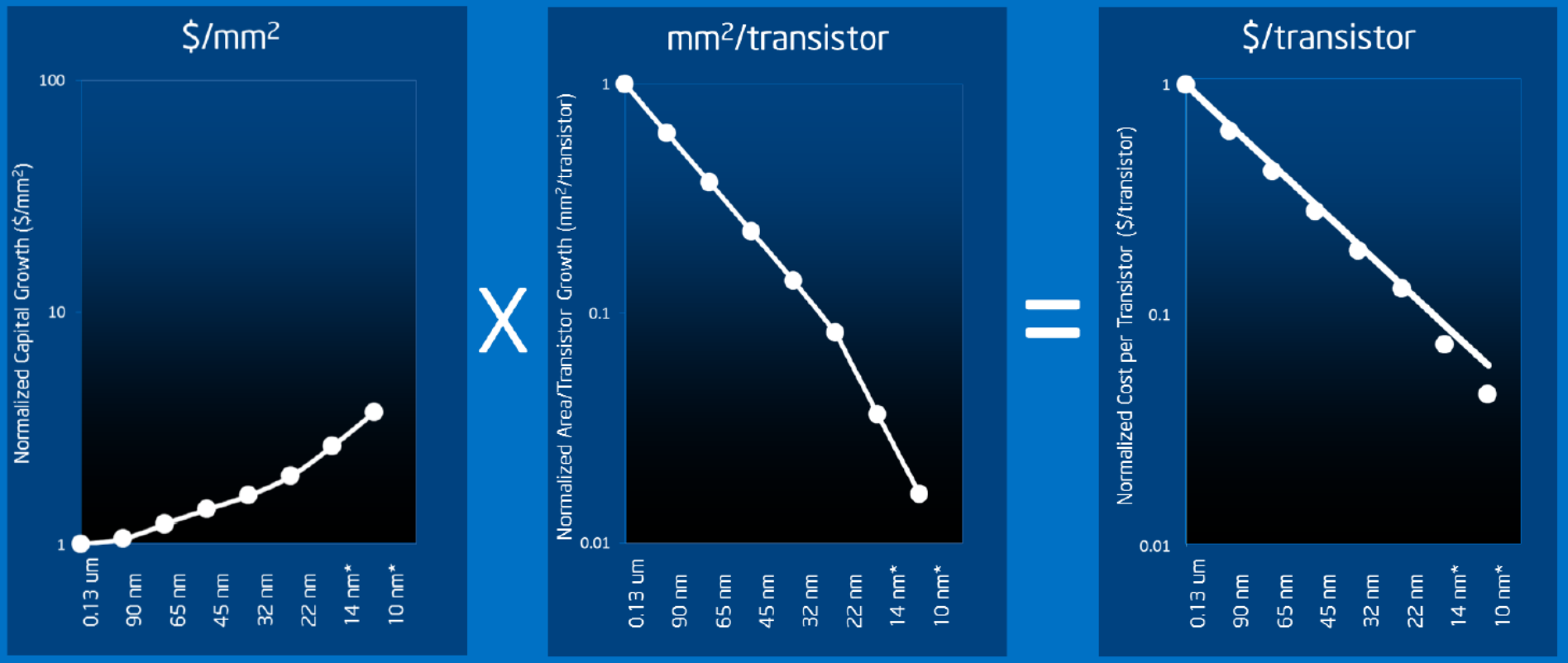
Evolution of Transistor Scaling



Intel Investor Meeting, Nov. 21, 2013

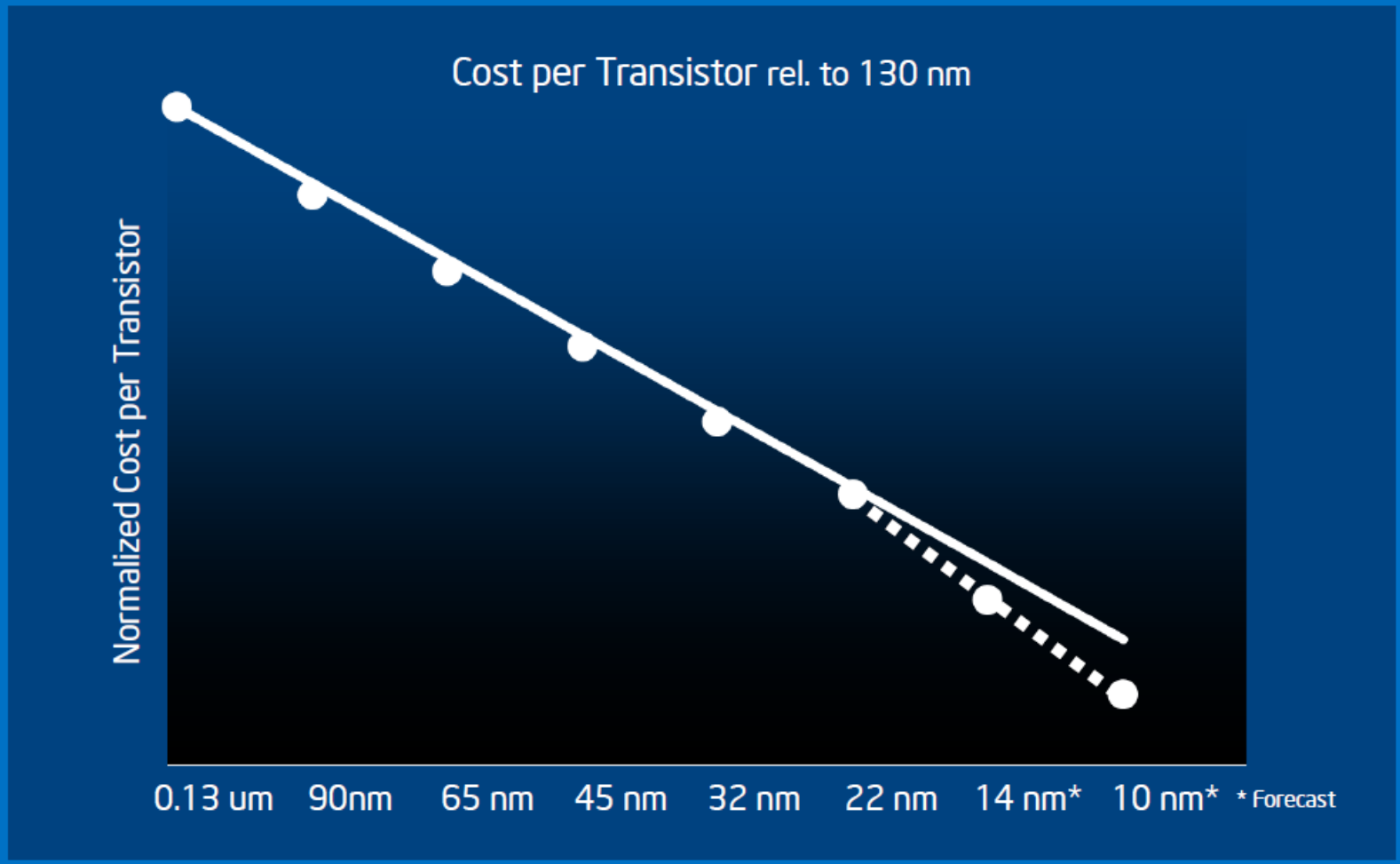
Density Improvements Offset Wafer Cost Trends



Source: Intel

* Forecast

Density Scaling ~~Continues~~ Cost Improvement Accelerates



Source: Intel

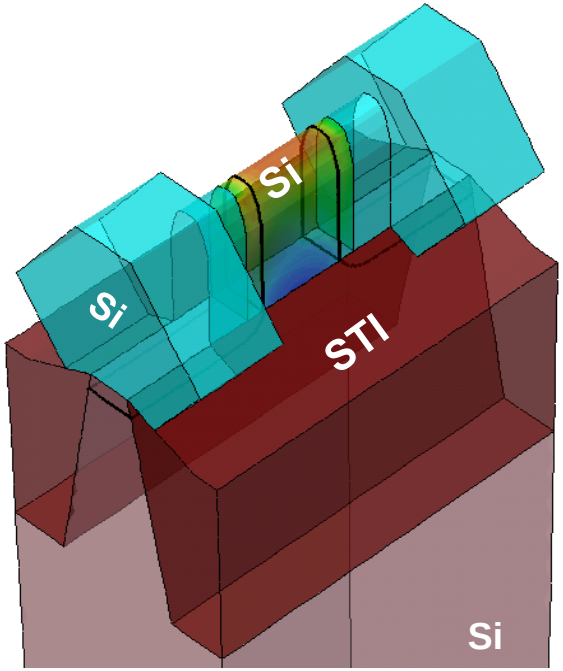
Expected Design Rules

Node	Gate pitch	L	Spa-cer	Fin width	Fin height	Fin pitch	Contact size	EOT
10	63	20	11	8	32	34	21	0.85
7	44	15	7	6	30	24	15	0.8

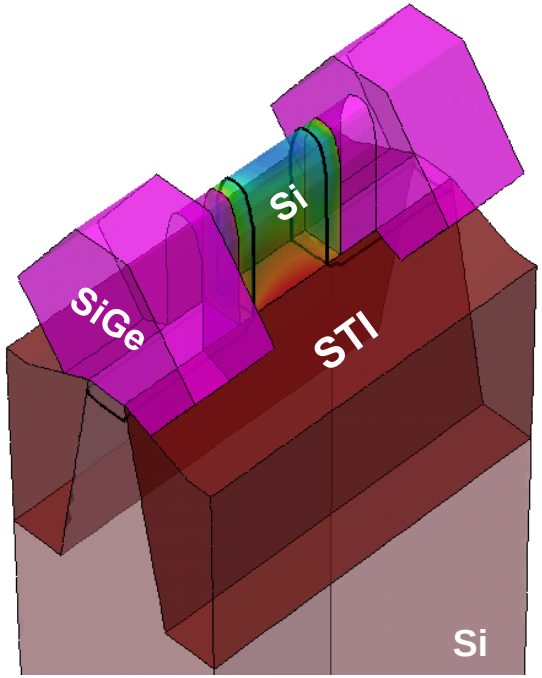
All sizes are in nm

Stress Engineering at 14 nm Node

NMOS: Low Stress

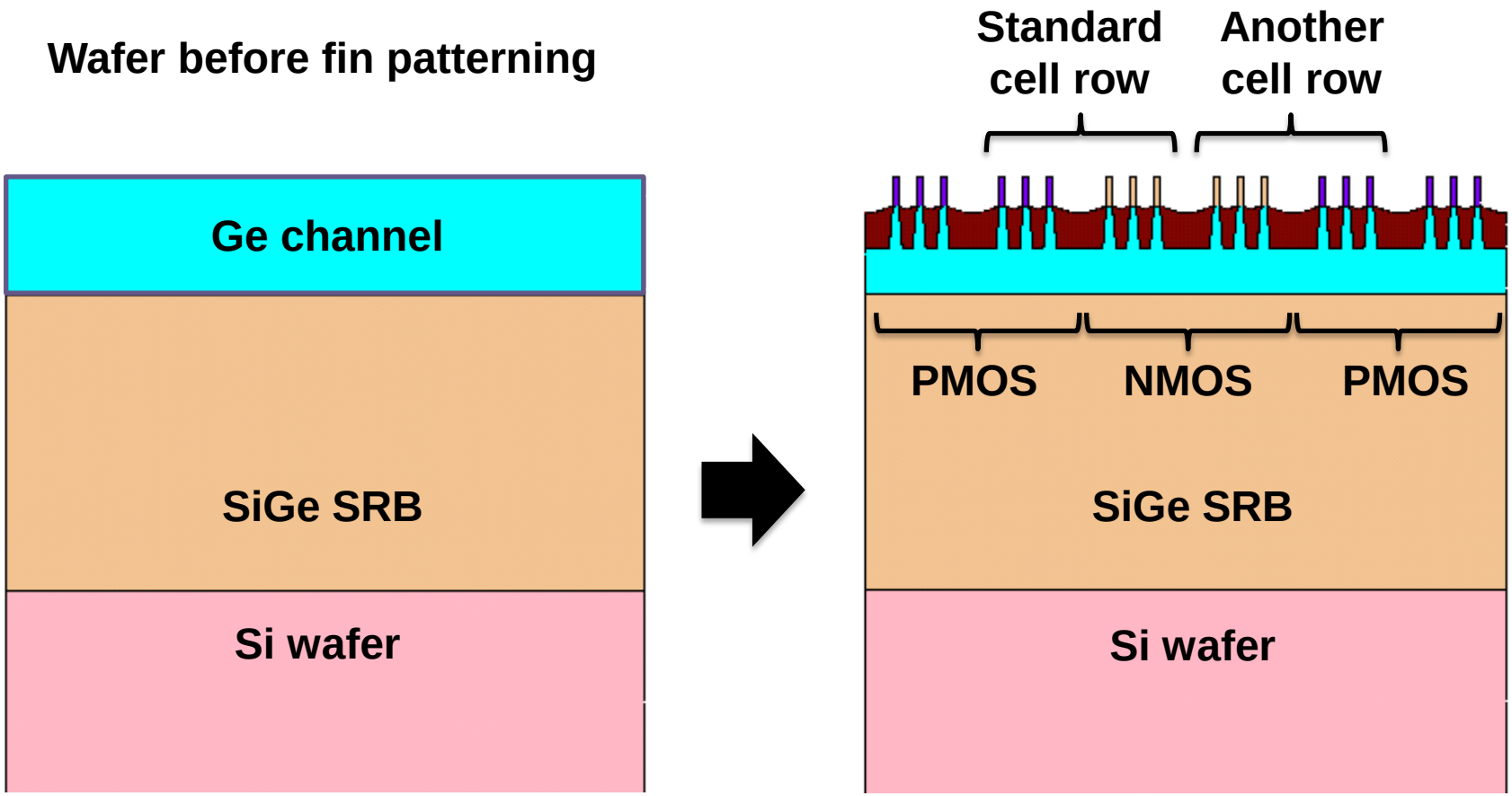


PMOS: High Stress



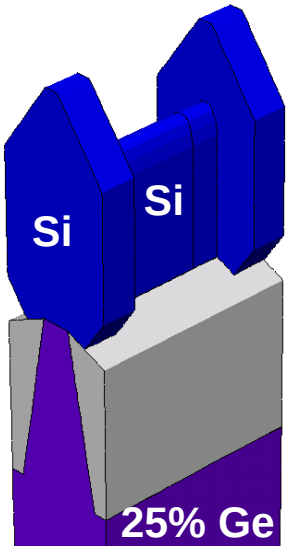
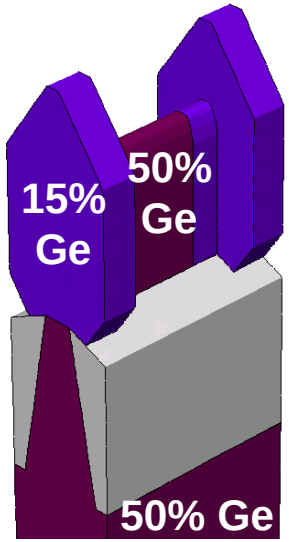
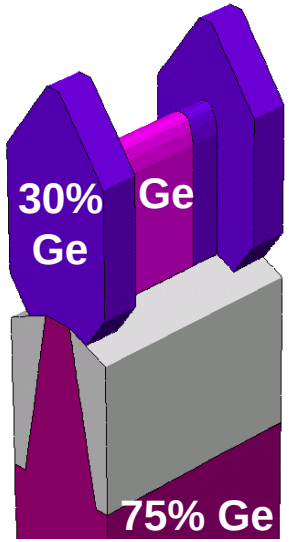
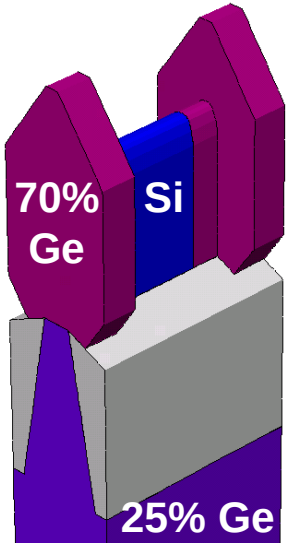
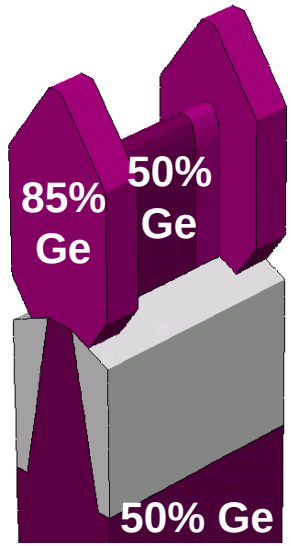
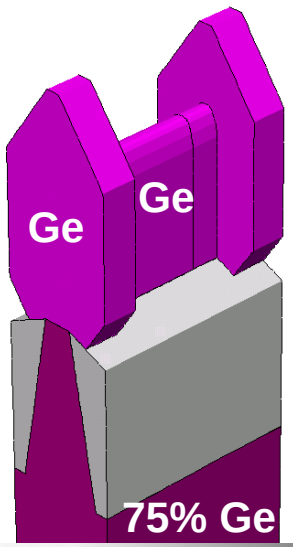
- Main stress source is SiGe PMOS source/drain epitaxy

Common SRB Epi for NMOS & PMOS

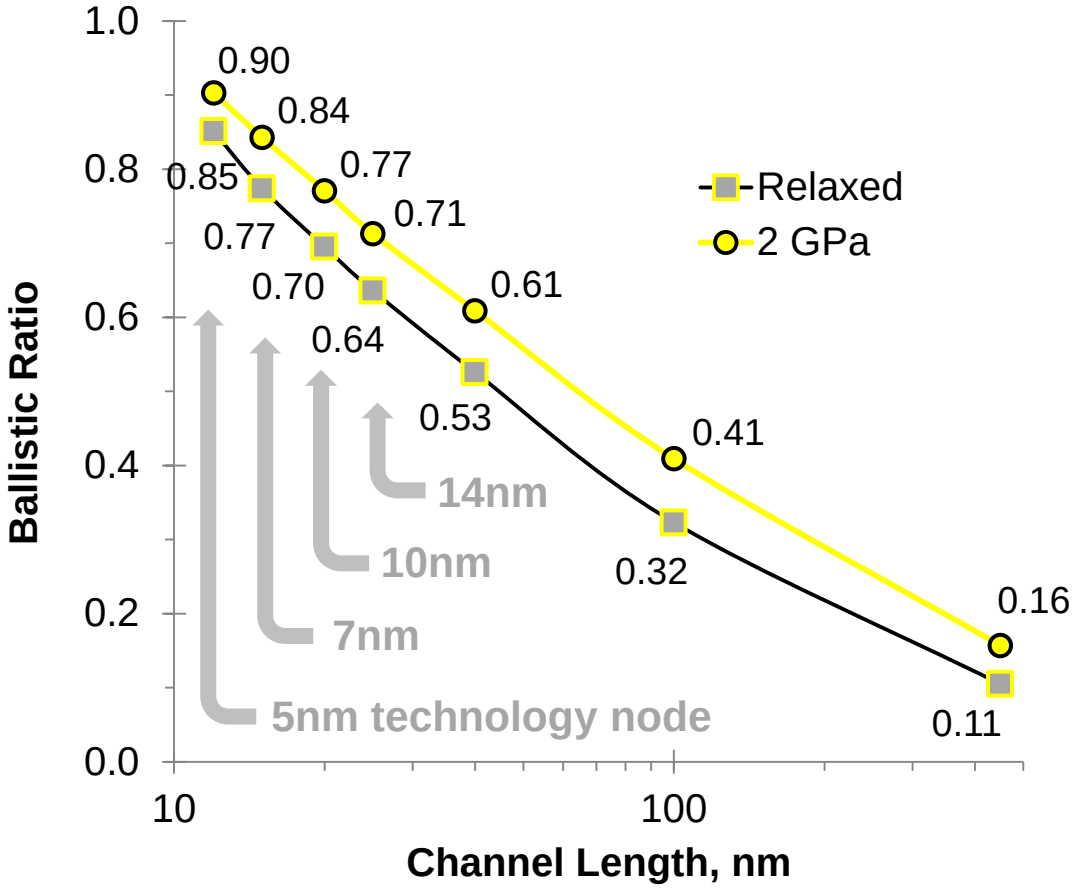


- Considering cell heights (pitches) of 360 nm, it is impractical to have separate SRB's for NMOS and PMOS

7nm Stress Engineering: SRB + S/D Epi

	Si channel	SiGe channel	Ge channel
NMOS +1.5 GPa			
PMOS -1.5 GPa			

Ballistic Transport Evolution



Si NMOS FinFET with 6nm wide fin

- Ballistic transport is currently ~64%
- Is expected to rise to ~84% at 7nm node
- Even higher for Ge and InGaAs
- Therefore, ballistic transport approximation is reasonable for 7nm node

Calculated in Sentaurus Monte Carlo

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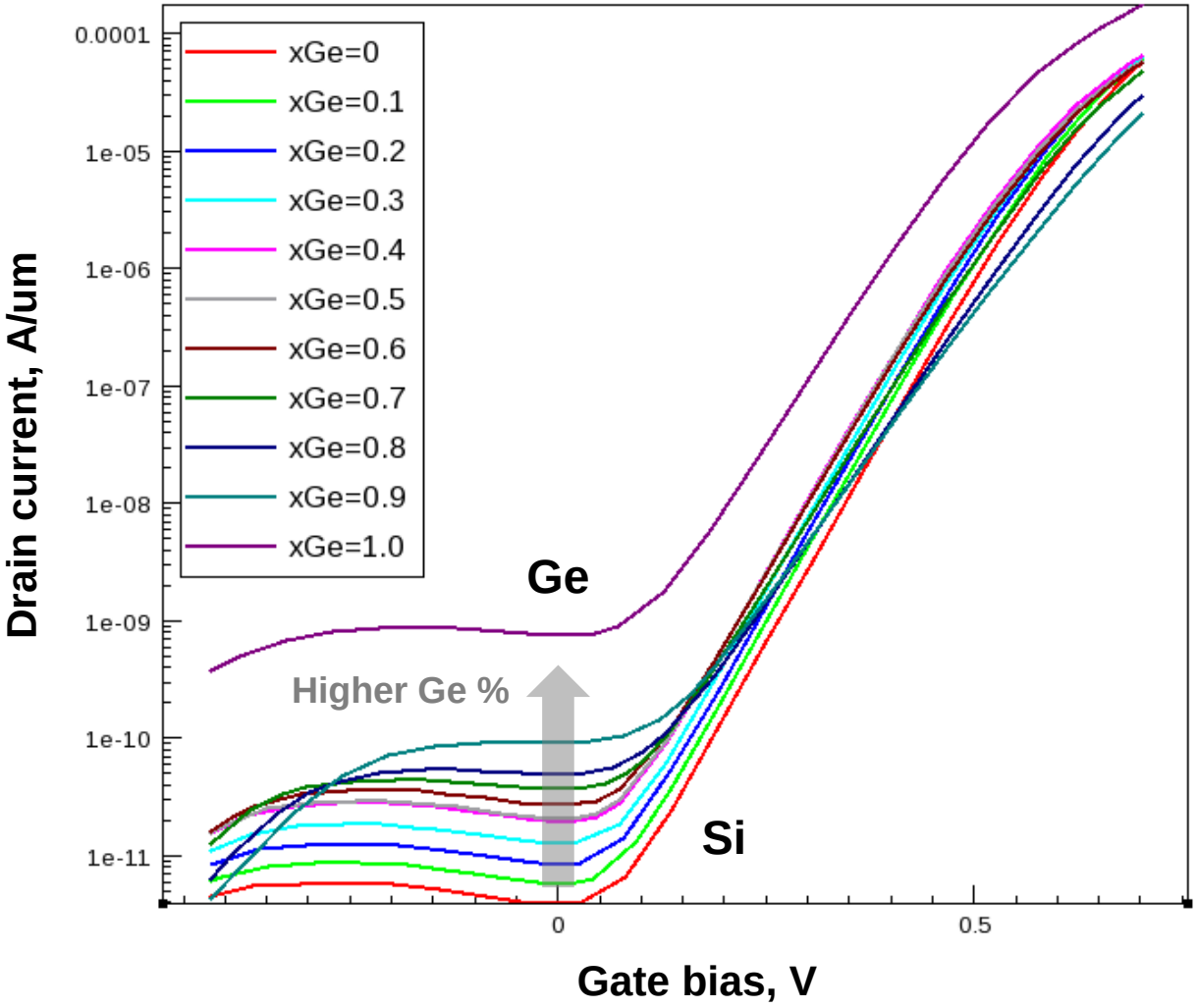
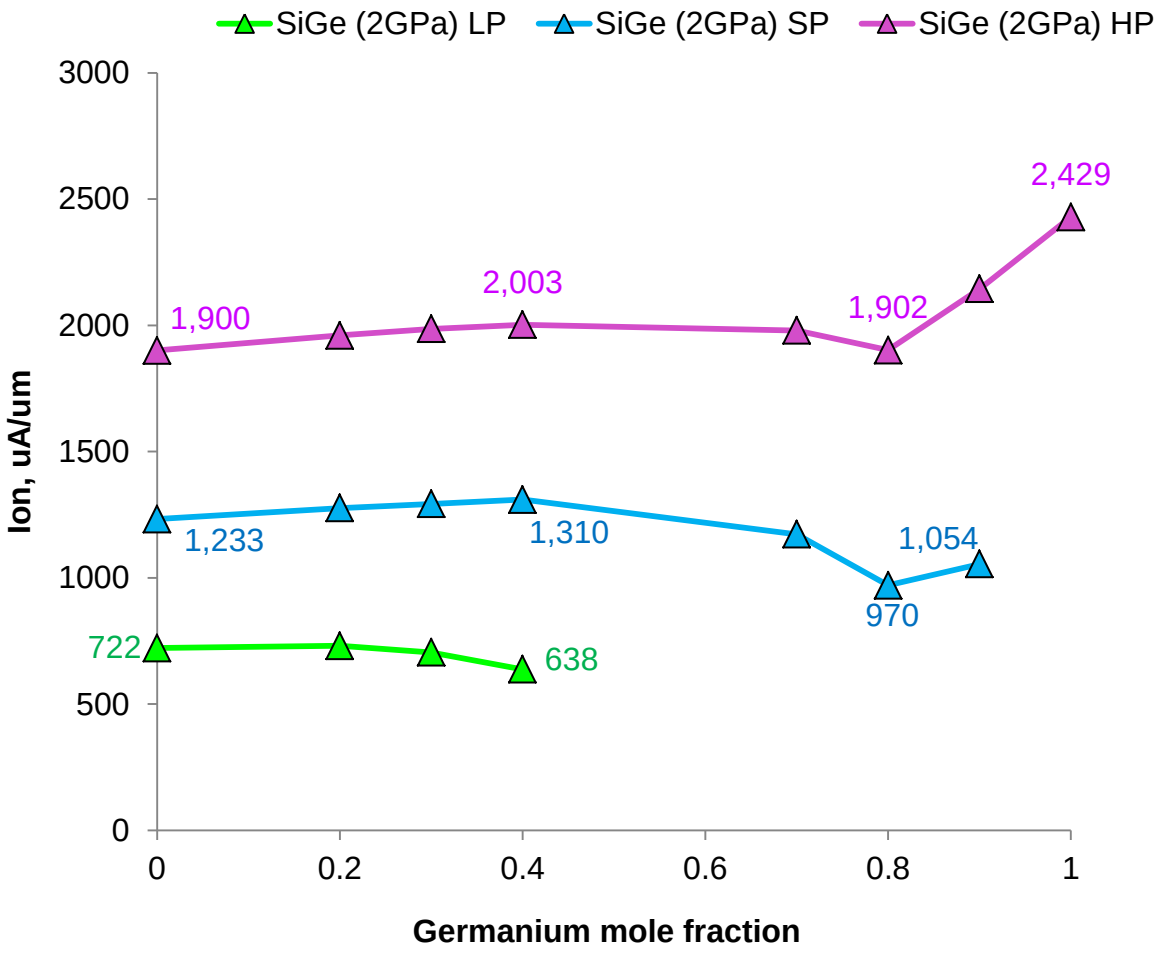
Stress Free SiGe: IdVg Curves



- Vdd = 0.7 V in this project
- BTBT model calibrated by IMEC

Strained SiGe: 2 GPa Tensile Stress

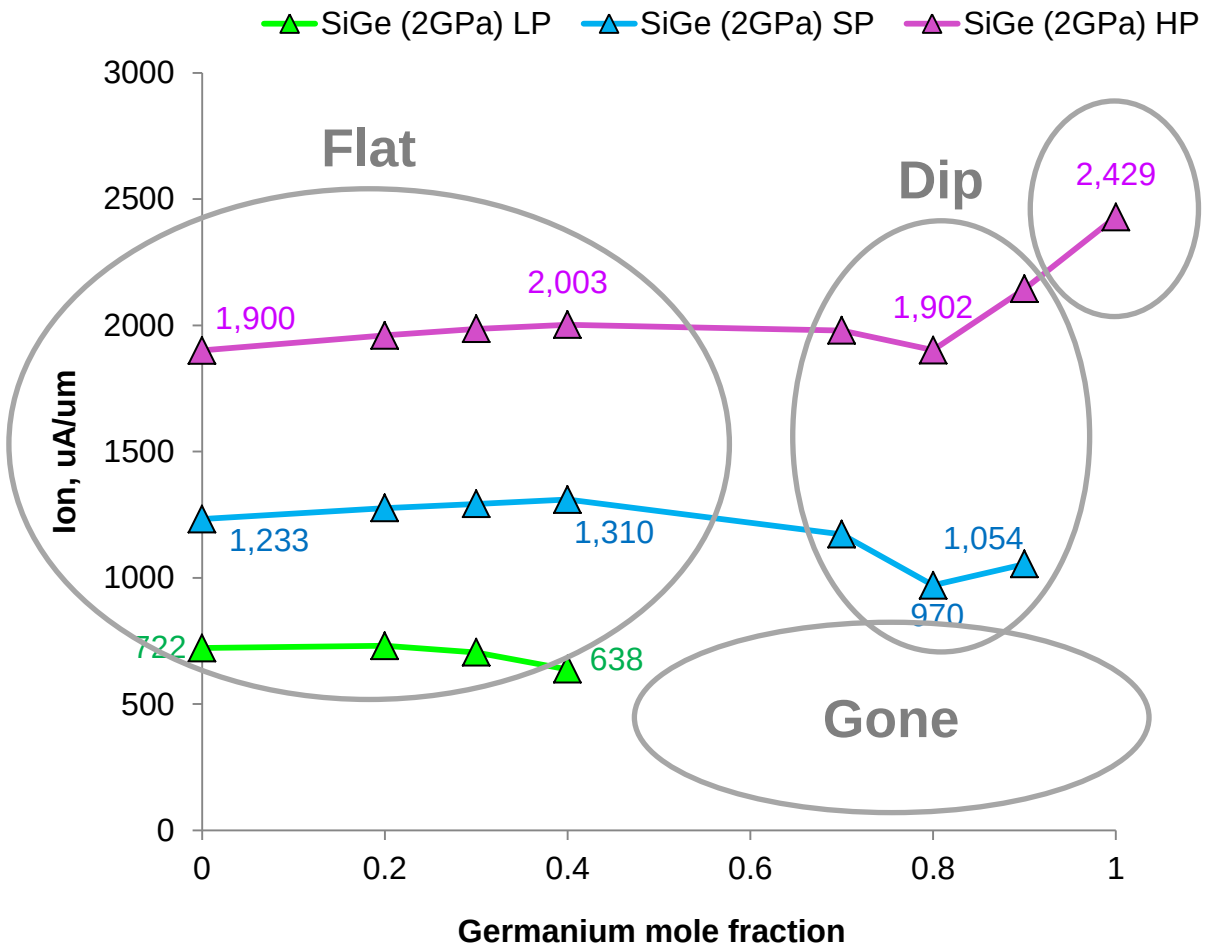


HP: 100 nA/um (Servers)

SP: 1 nA/um (Laptops)

LP: 50 pA/um (Mobile)

Strained SiGe: 2 GPa Tensile Stress

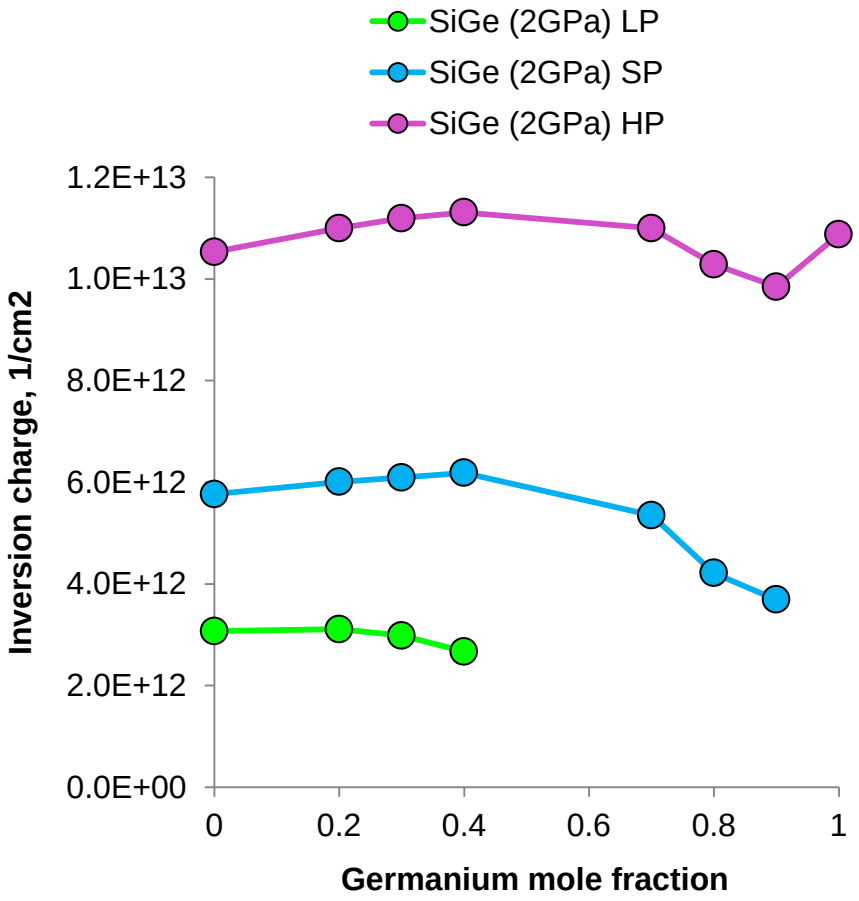


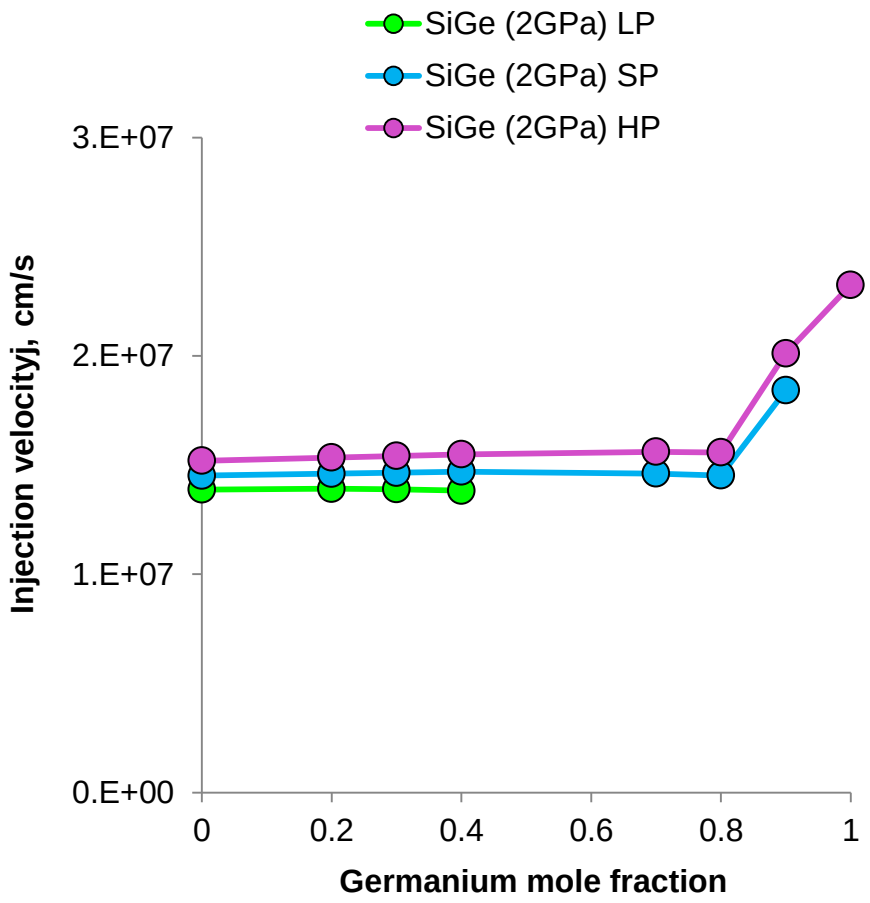
HP: 100 nA/um

SP: 1 nA/um

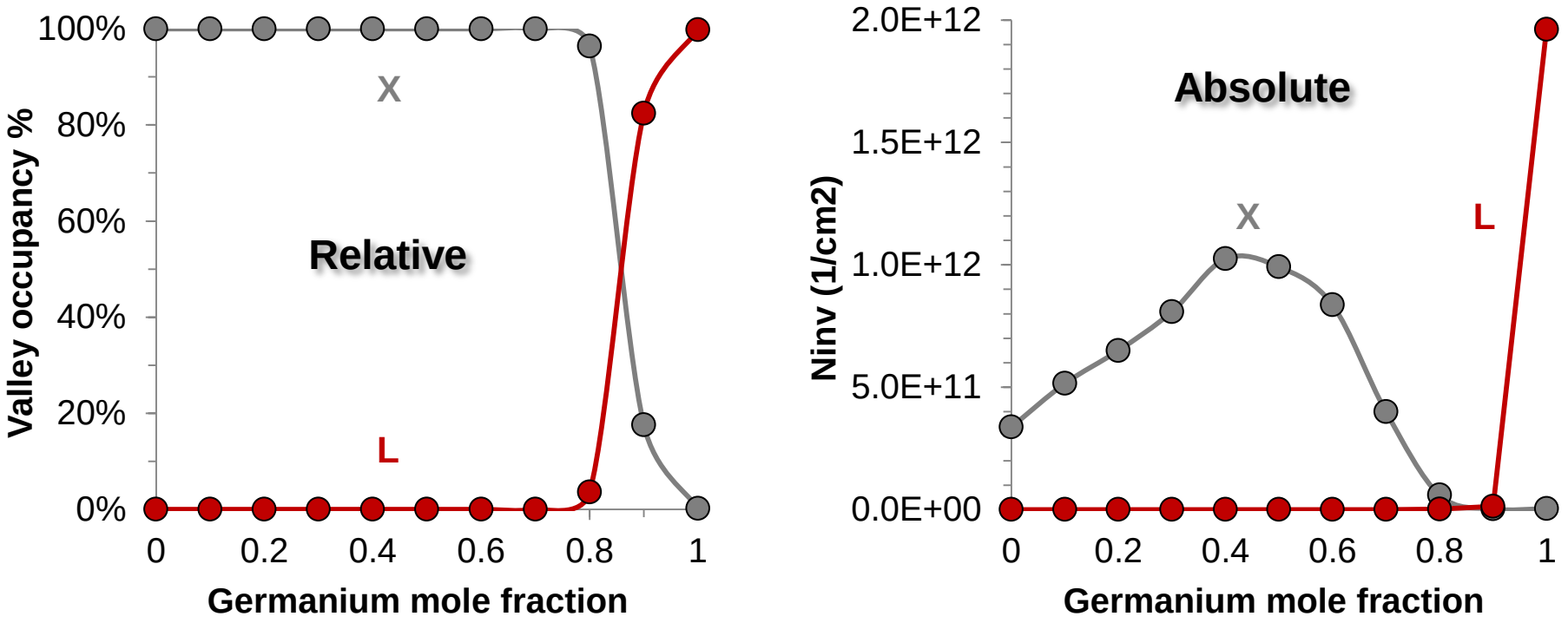
LP: 50 pA/um

Strained SiGe: N_{inv} and V_{inj}



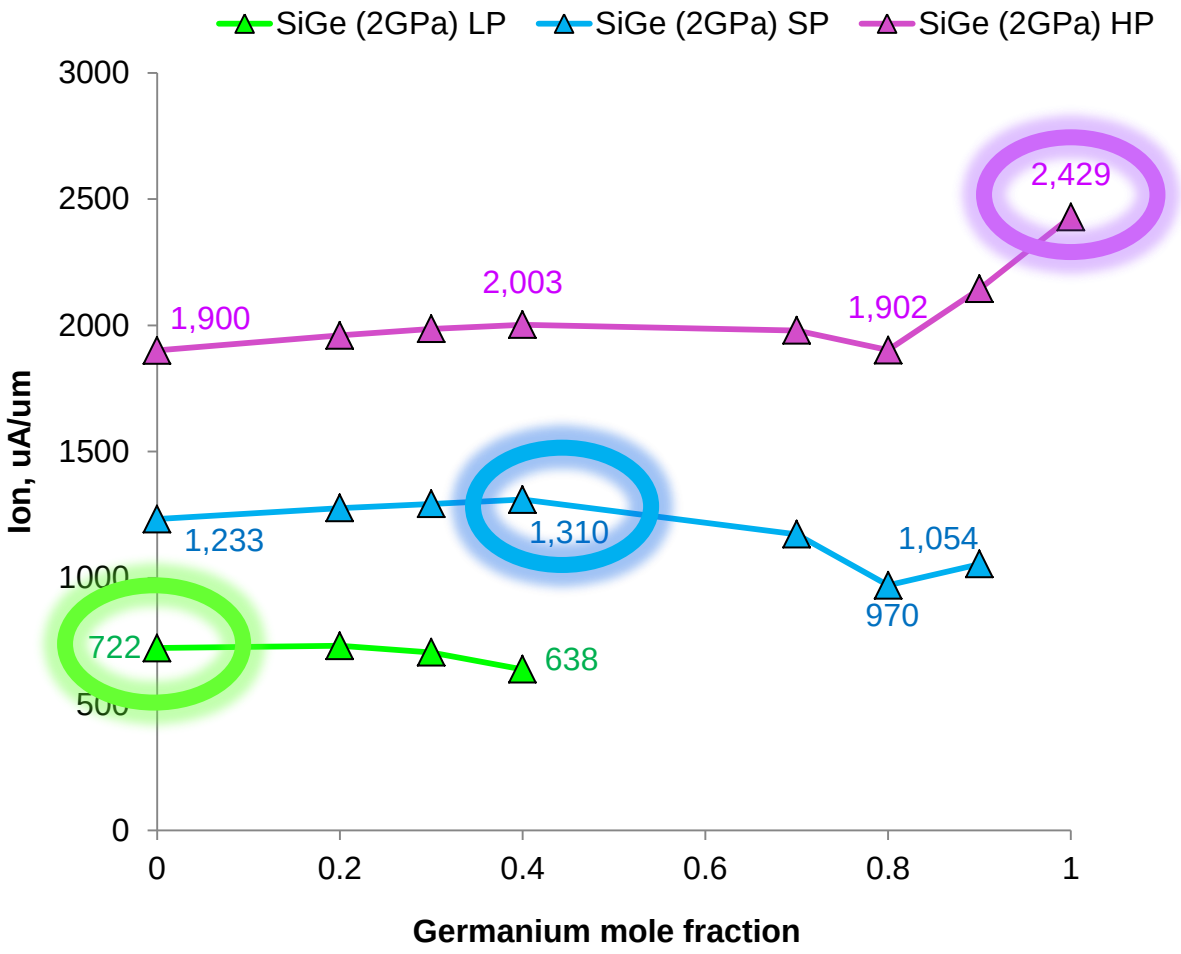


Delta & Lambda Valley Population



- Here, Vgs = 0.7 V and gate WF is adjusted to have min Ioff at Vgs = 0
- There are too few electrons at 80% to 90% Ge mole fractions

Strained SiGe: LP, SP & HP Champions

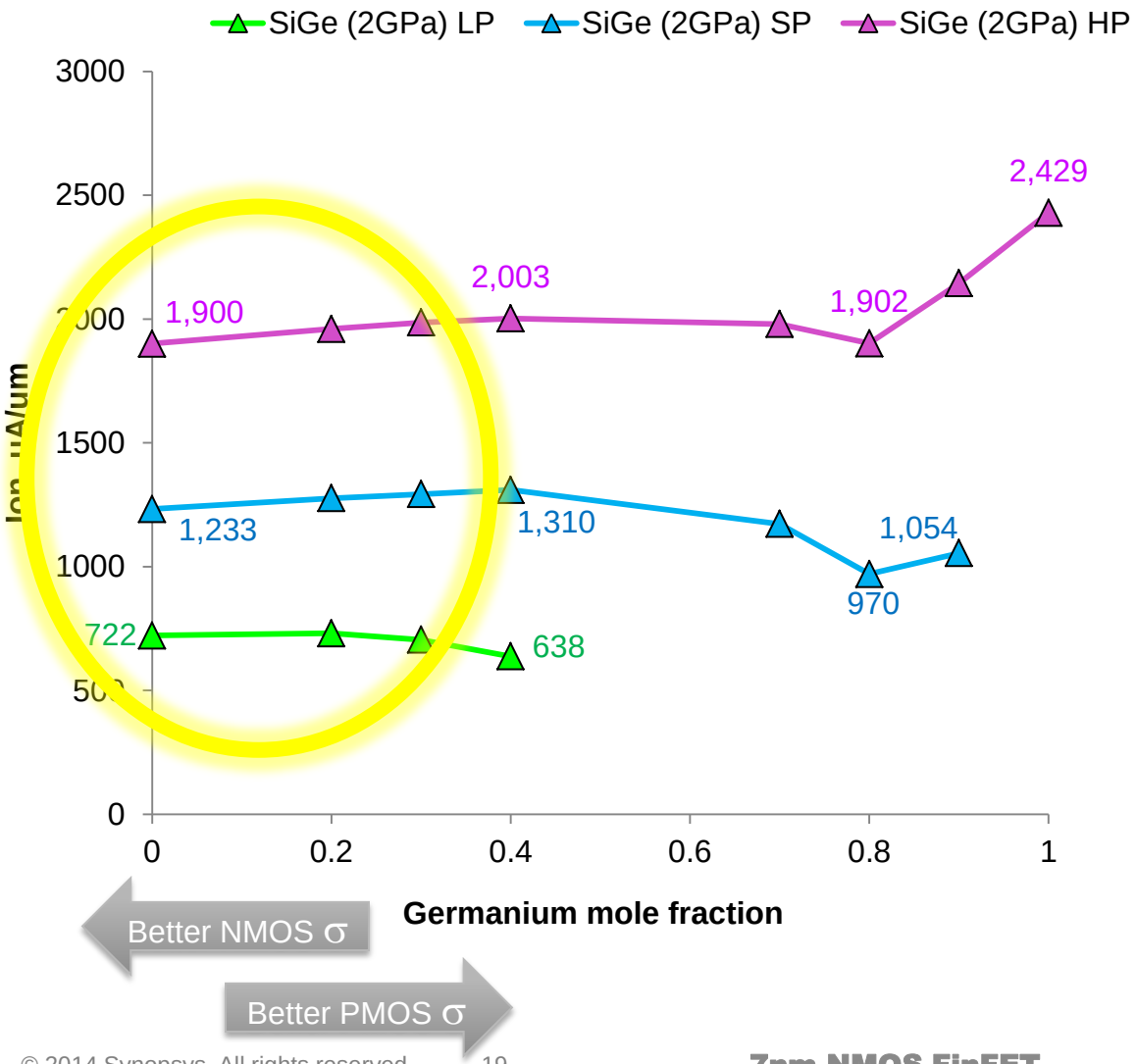


HP: Ge

SP: Mid-range SiGe

LP: Si

Strained SiGe: Combination Champion



- Only Si and SiGe with low Ge % can match LP spec
- HP performance penalty to pure Ge is ~20%
- The choice between pure Si vs SiGe with low Ge % can be made based on PMOS/NMOS stress trade-off

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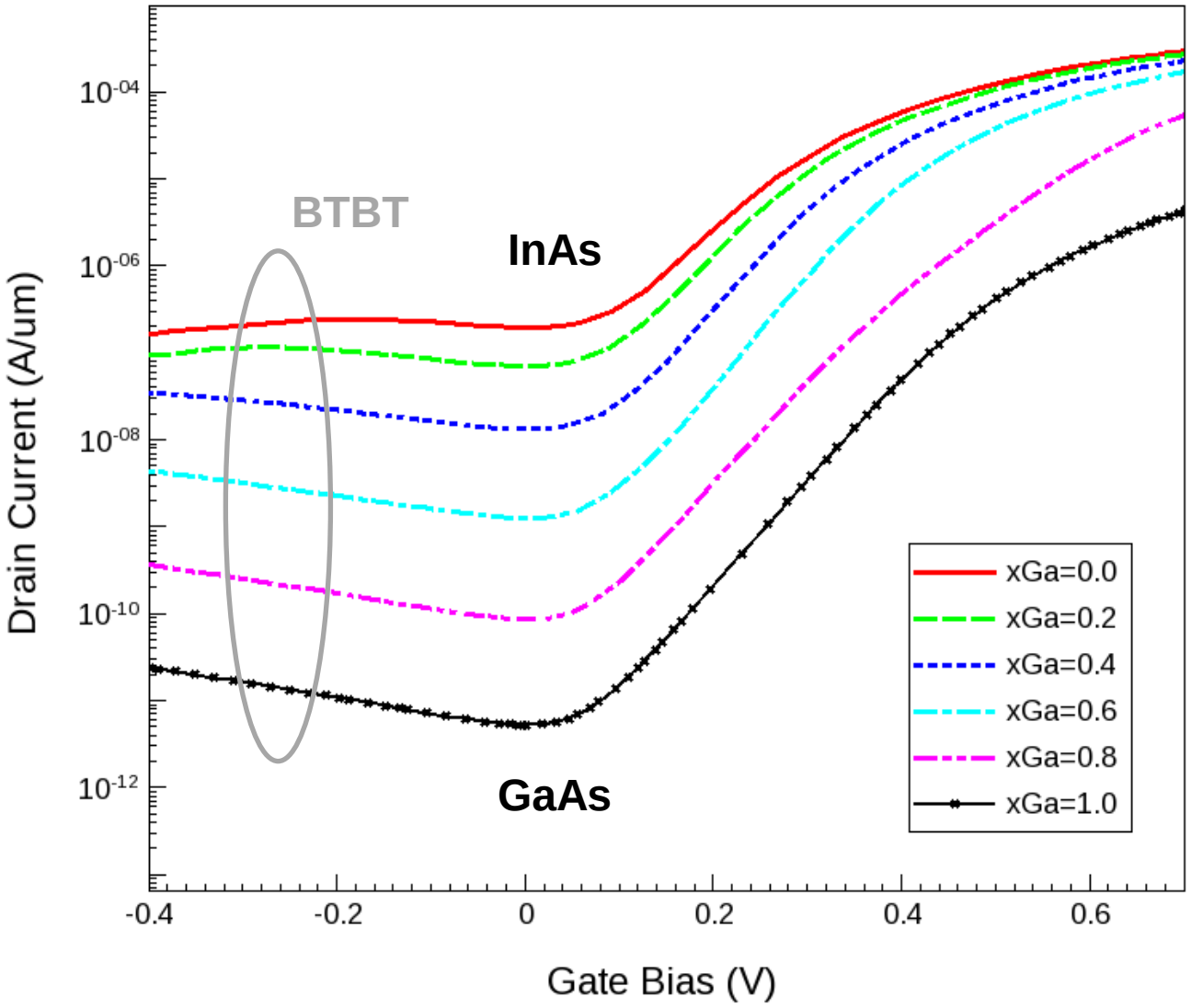
IdVg After Work-Function Adjustment

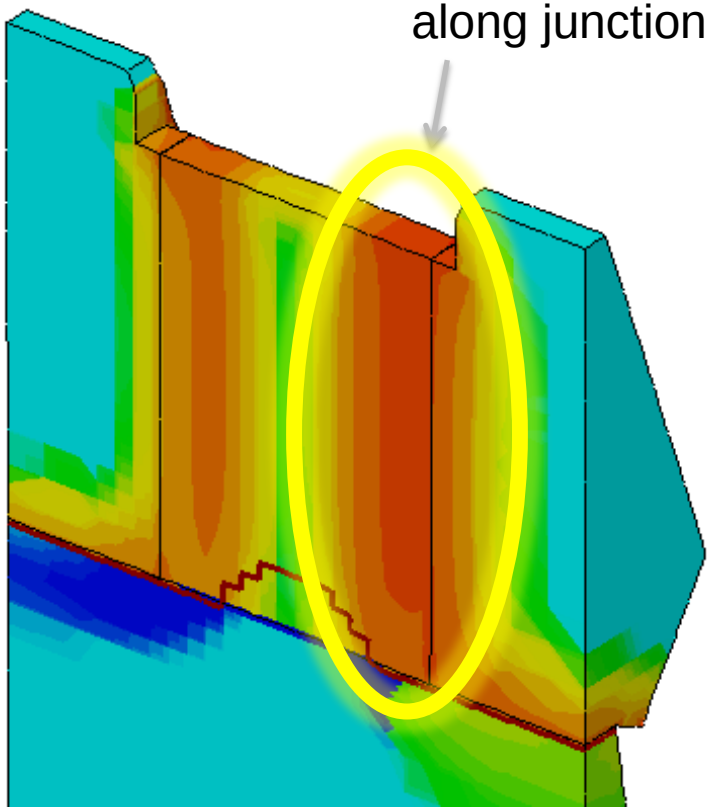


- BTBT model calibrated by IMEC
- Vdd = 0.7 V

Leakage Patterns

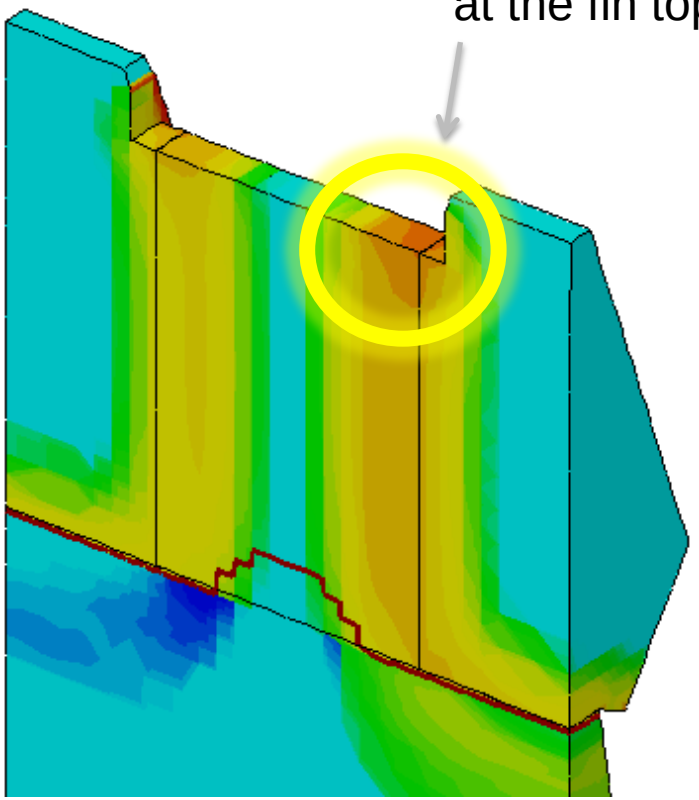
InAs

BTBT is spread along junction



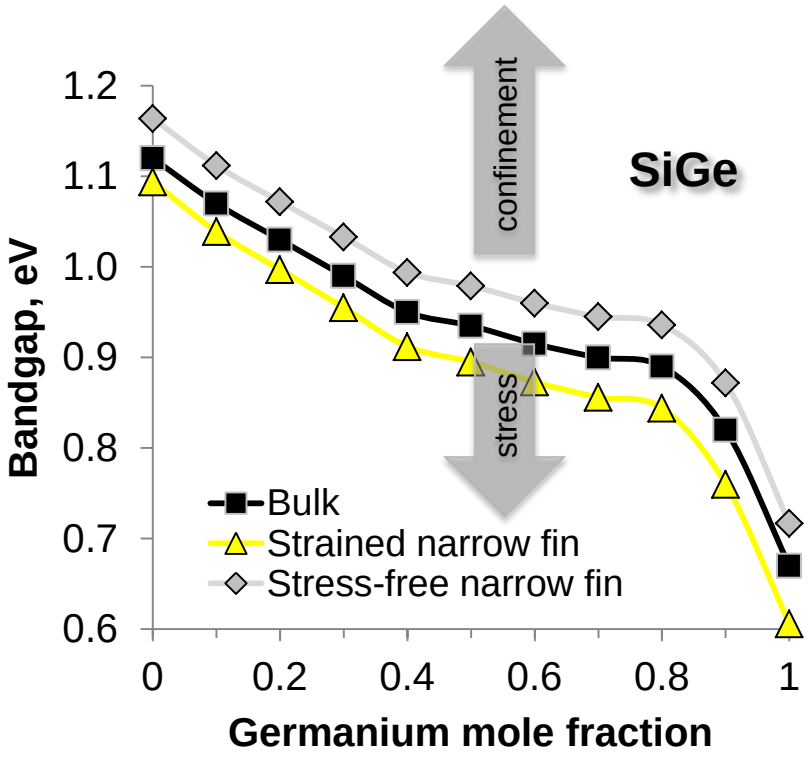
GaAs

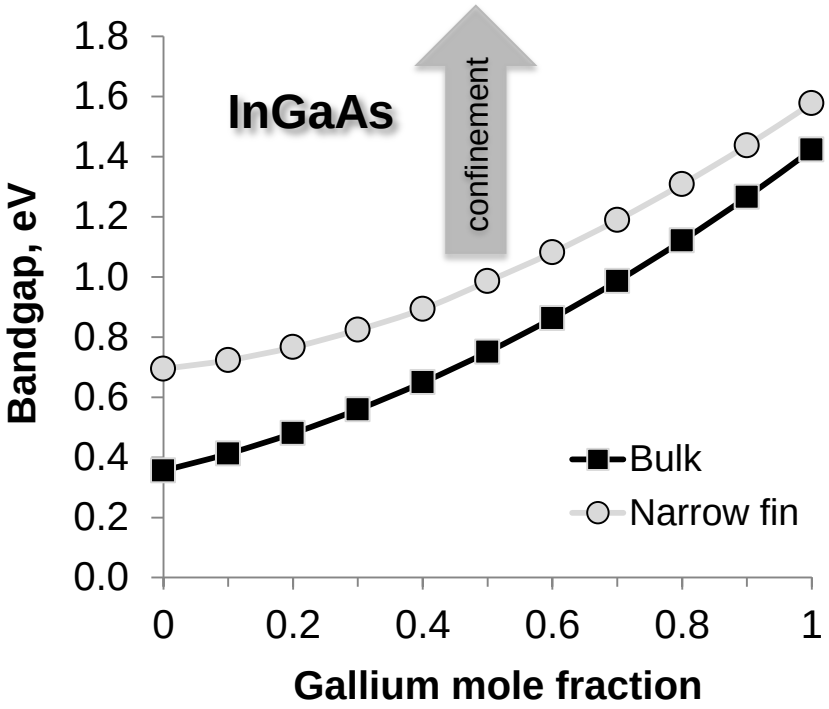
GIDL happens at the fin top



Vgs = -0.3 V

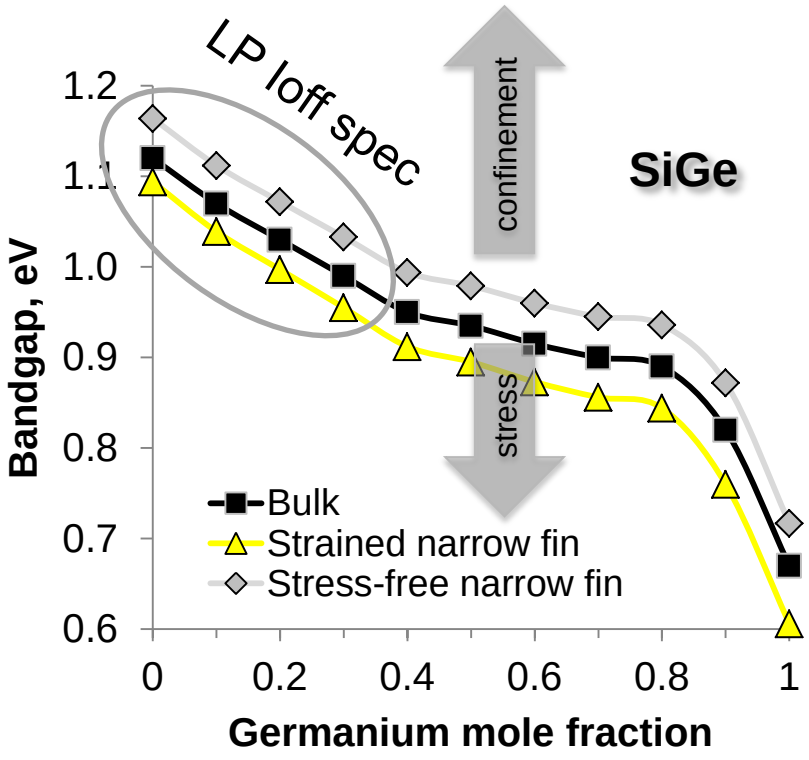
Band Gap Widening and Narrowing

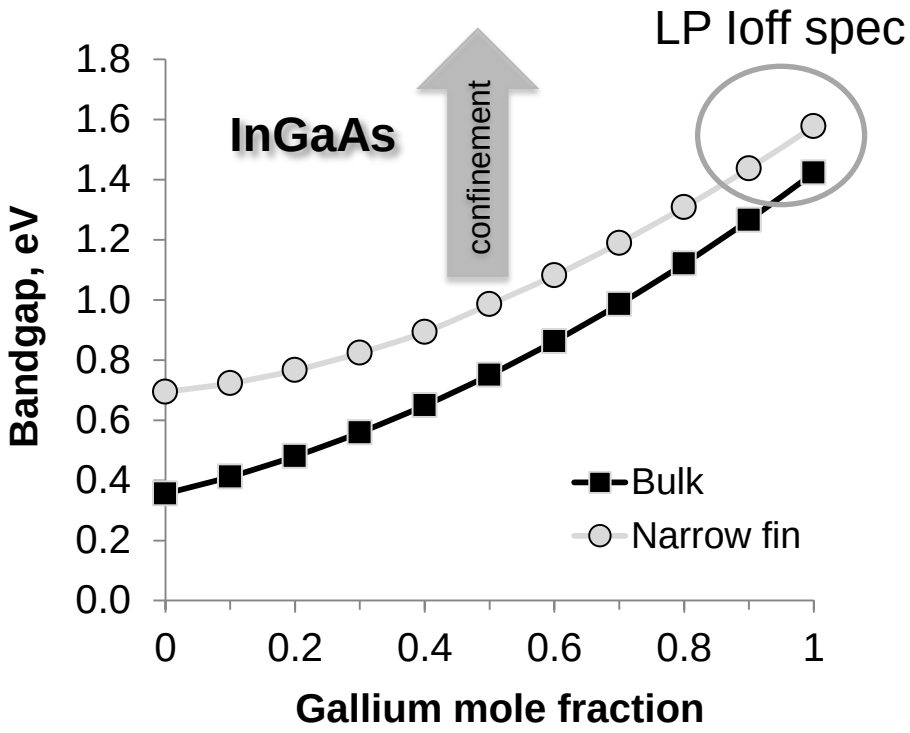




- For SiGe, 6nm wide fin widens bandgap by 40 mV to 50 mV
- Tensile uniaxial 2 GPa stress pushes it down by 70 mV to 100 mV
- For GaAs, the widening is 155 mV, and for InAs it grows to 340 mV

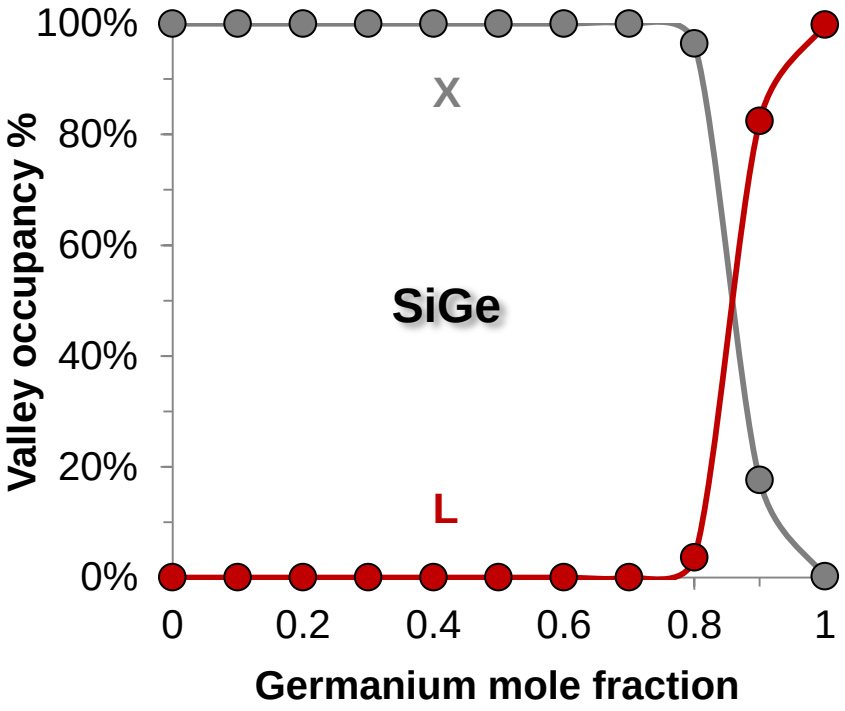
Band Gap Widening and Narrowing

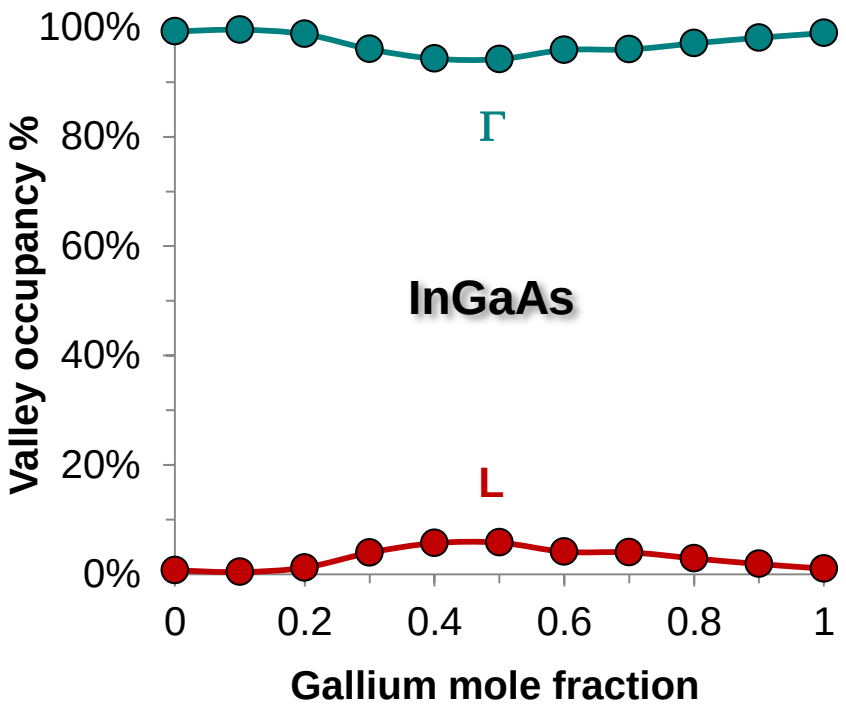




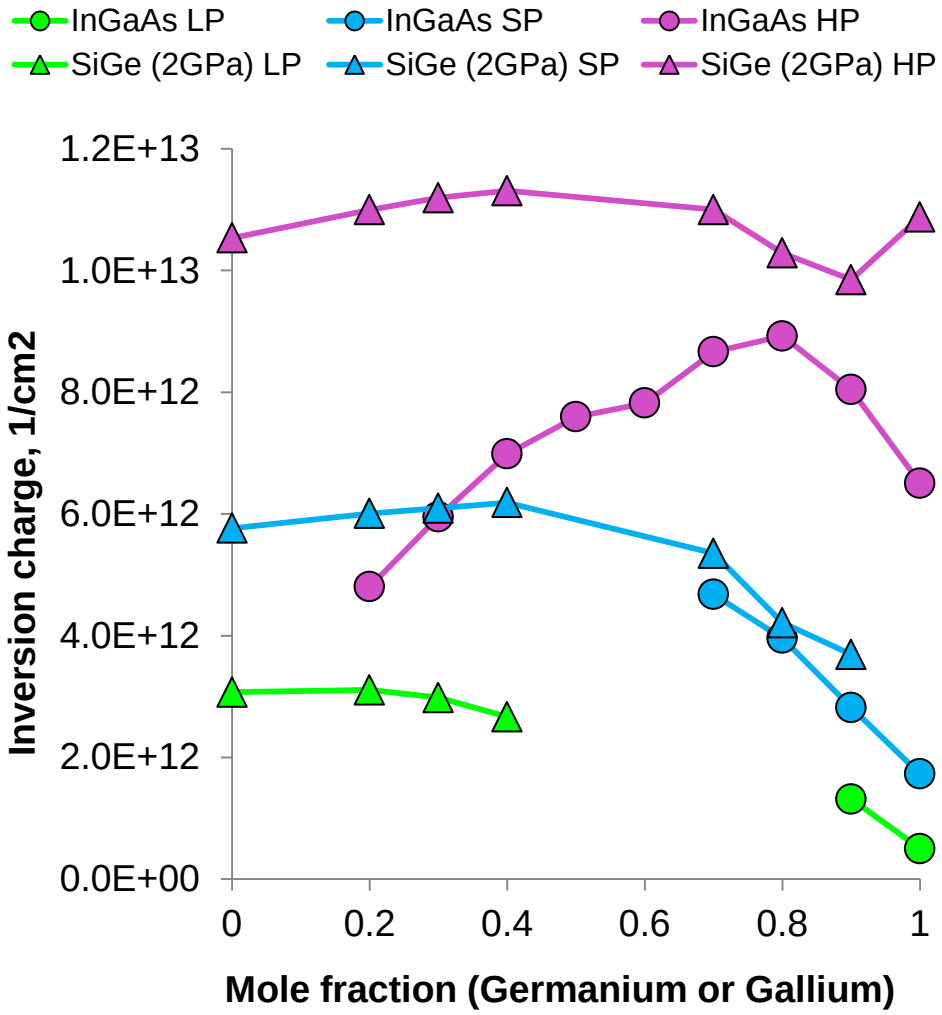
- High mobility materials need to have bandgap wider than silicon!

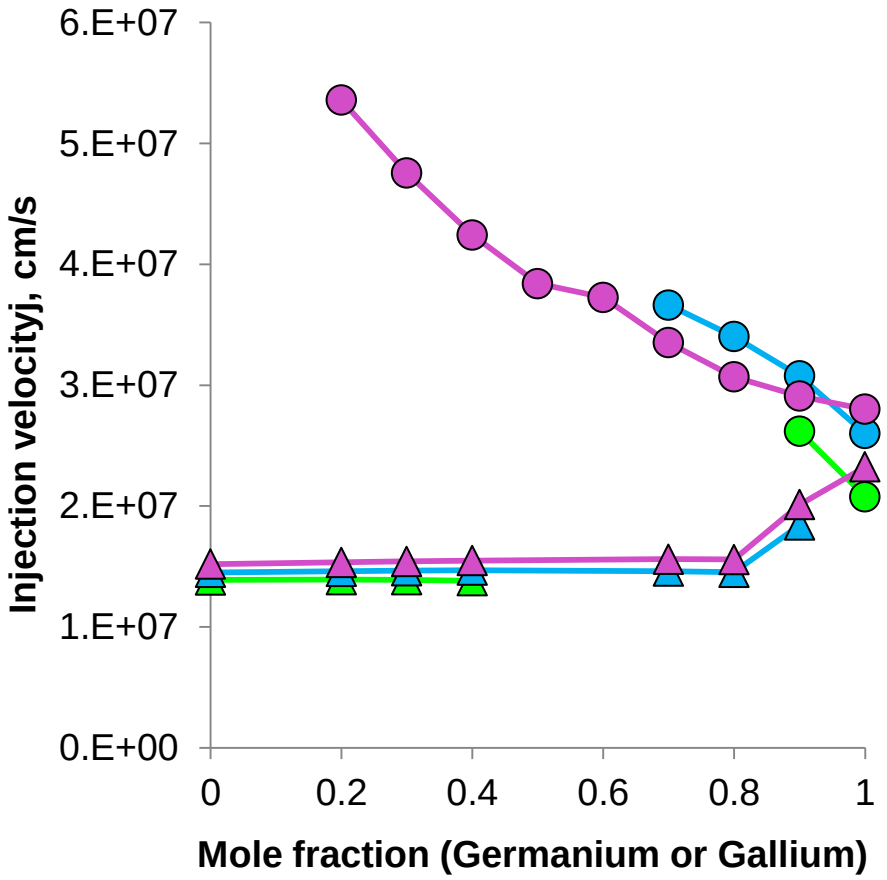
Gamma, Delta & Lambda Valleys



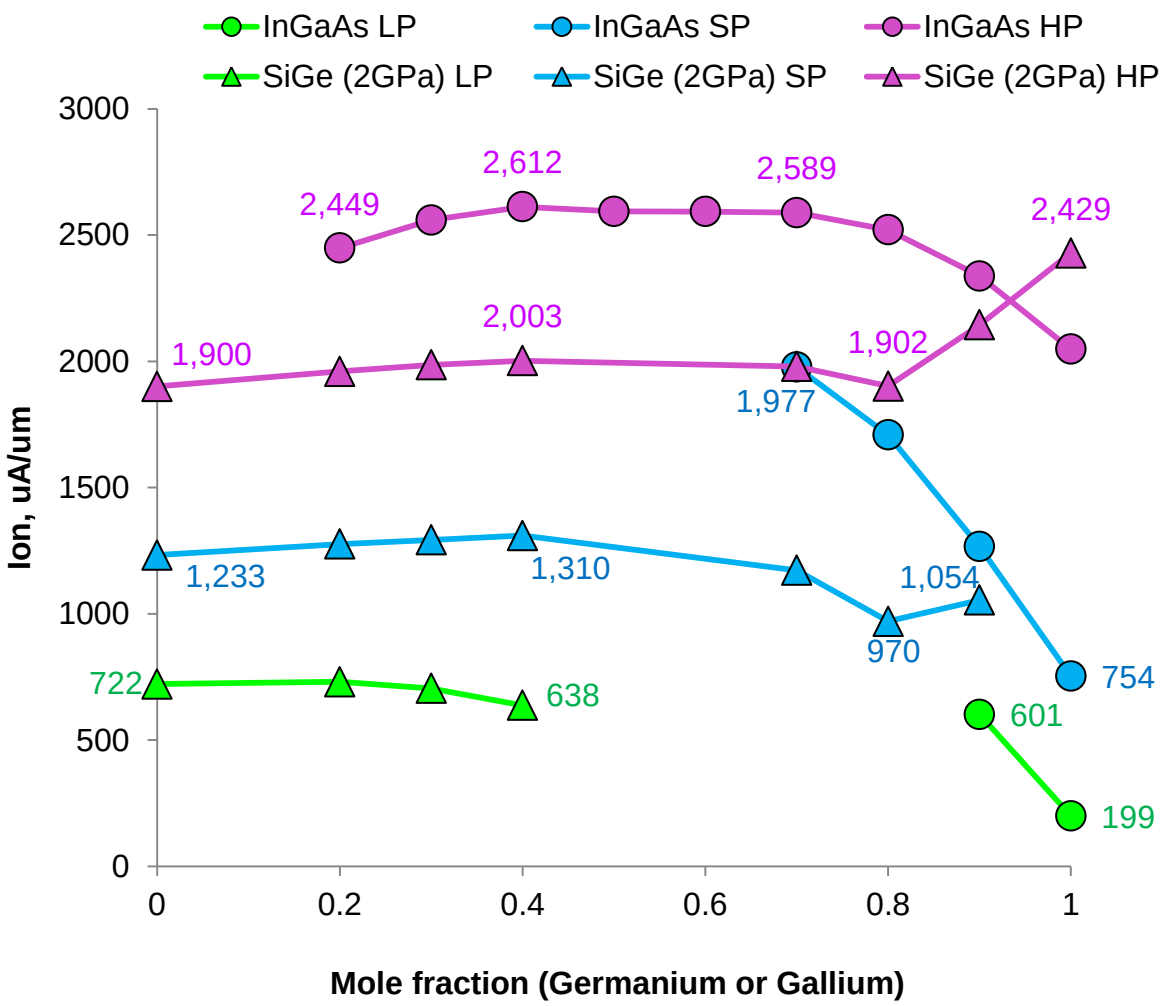


Group IV vs III-V: N_{inv} and V_{inj}

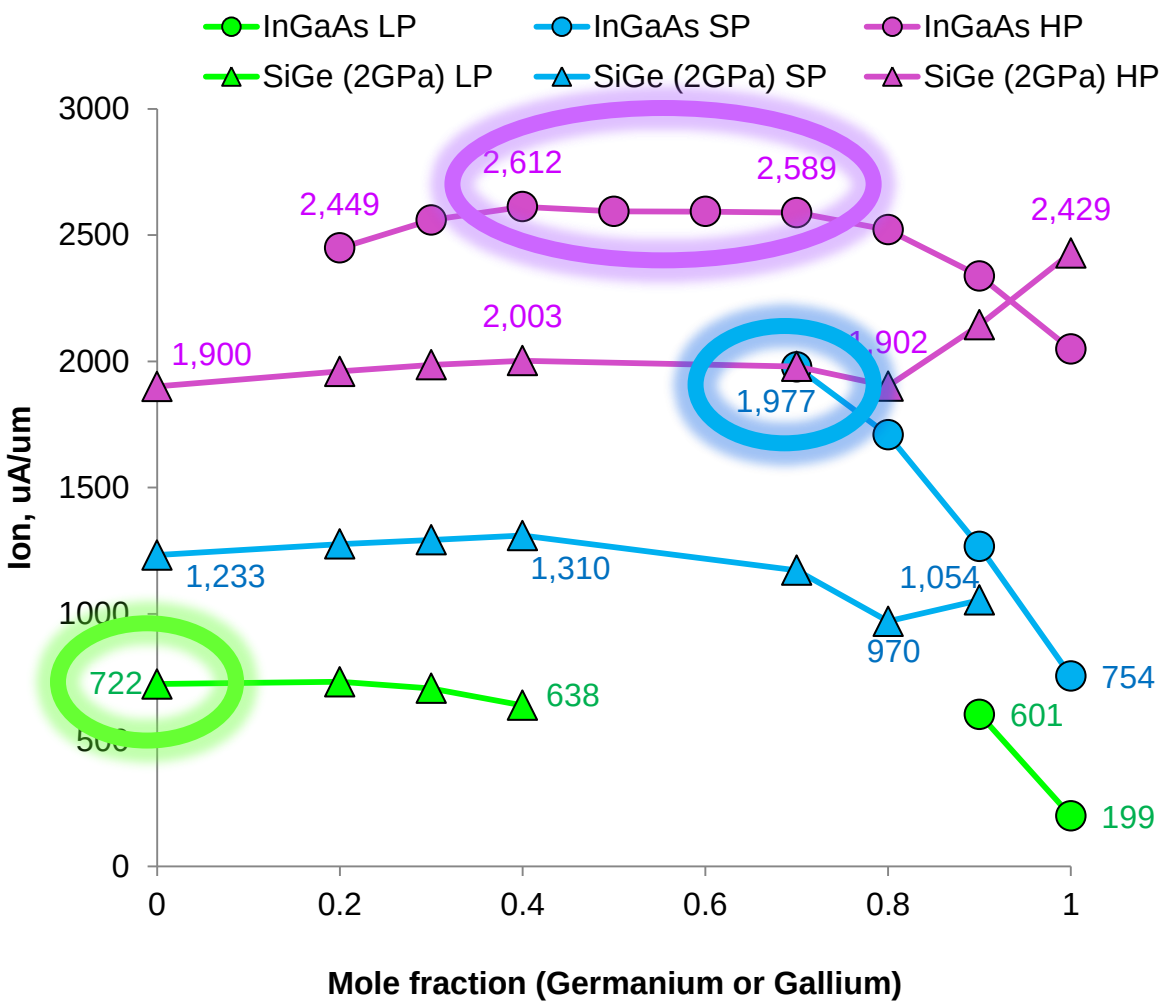




Group IV vs III-V



Group IV vs III-V: LP, SP & HP Champions

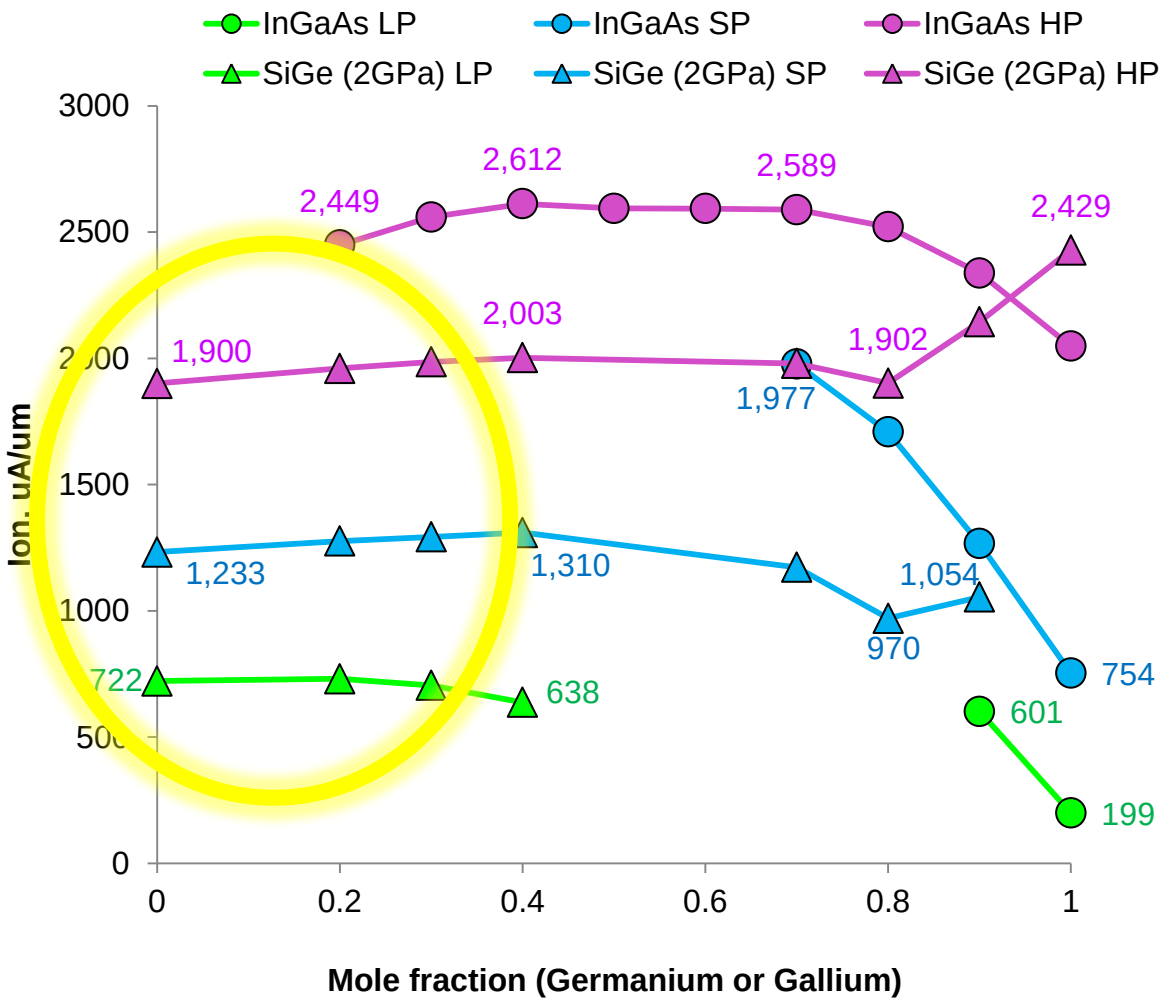


HP: Mid-range InGaAs

SP: 30% In InGaAs

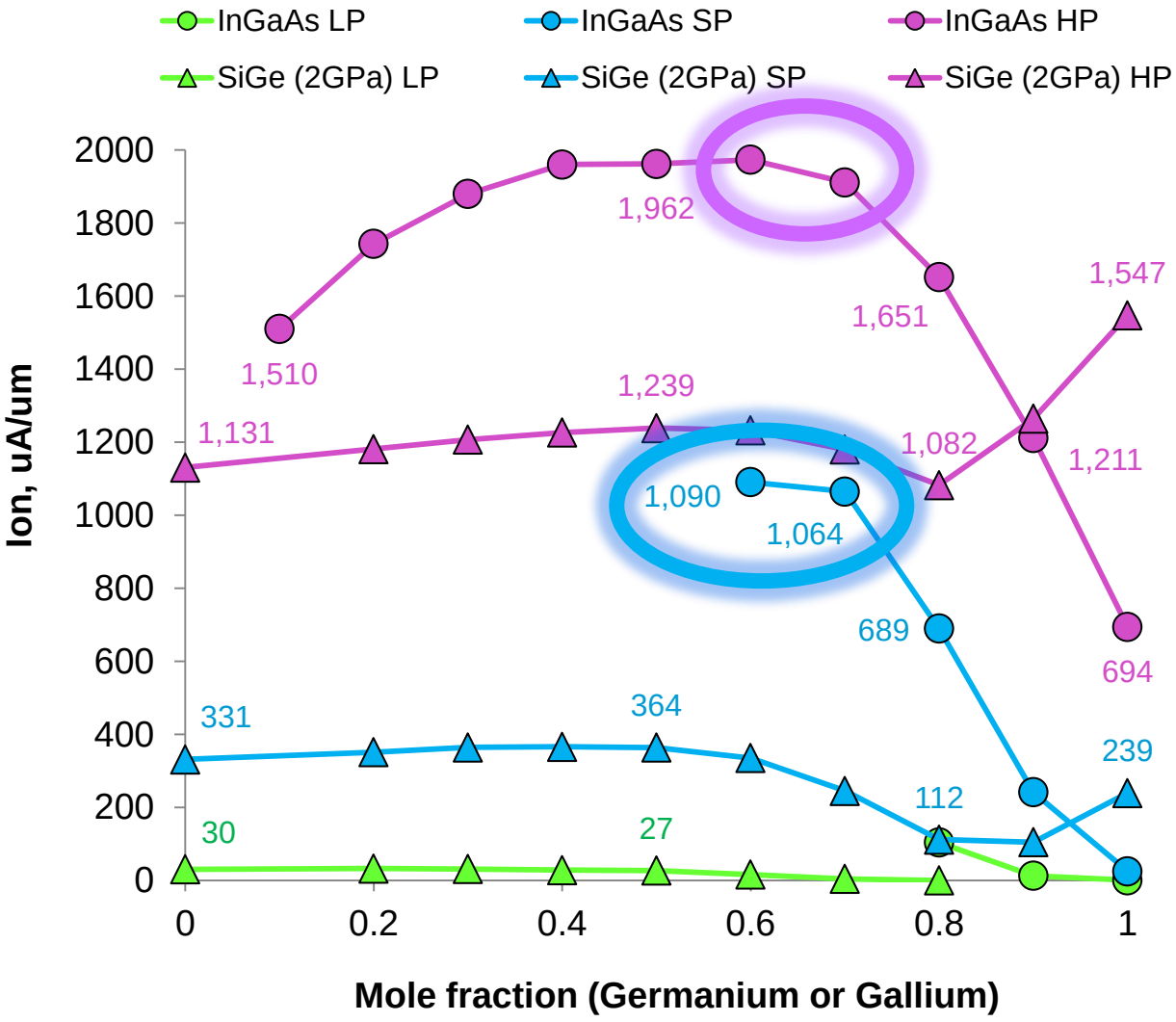
LP: Si

Group IV vs III-V: Combination Champion



- Only Si, low Ge SiGe, and GaAs can match LP spec
- InGaAs with 10% In has competitive performance, but is too sensitive to In content
- This would bring severe variability
- So, silicon looks the best…
- SiGe with low Ge % can be used for stress engineering

0.5 V Vdd Instead of 0.7 V Vdd



- InGaAs with 30% In really shines at SP and HP specs
- Nobody can pull off LP at 0.5 V Vdd. Would you like your iPhone to be ~30x slower?
- To have 0.5 V Vdd, variability has to go down ~2x. That is a stretch.
- The best InGaAs composition has Si-like bandgap

Summary

- It is a close race, no clear winner
- The best choice depends on particular chip spec