The long and winding road to FinFETs: a bit of past, present and future

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Introduction
FinFET technology challenges and trends
FinFET circuit layout challenges

Why do we need FinFETs today?







Multigate architectures



Brief history of FinFETs



Brief history of FinFET circuits



Technology design challenges

- Fin Patterning
- Fin Shape
- Fin Dimensional Variability
- Fin Doping
- Stress for Fins
- Fin Orientation
- Fin Isolation
- FinFET Parasitic Capacitance
- FinFET Reliability
- Alternative Fin Materials
- Passive Elements in FinFET Technology
- FinFET Performance

Fin patterning – needs and challeges

Design requirements:

- Dense, sub-optical fin pitch
- High aspect ratio (height to width >2)
- Litho challenges:
 - Fin pitch is below optical (193i) litho resolution
 - If litho-etch-litho-etch approach considered - inherent overlay error between two fin patterns impacts down-stream processing;
 - Fin width much smaller than narrowest litho line (Lgate)
 - Line edge roughness (LER) of the process leads to substantial local fin width variability (LWR).



Fin patterning – solutions: SADP

- Solution to overlay problem: spacer-defined self-aligned double patterning (SADP)
 - Fin pitch down to ~40nm with 193i scanner.
 - Narrower fin pitches would require SADP or litho method to be applied twice.
 - Lower LER → lower LWR, or fin width variation.
 - EUV lithography may not be able to improve on the LER over optical (193i)



Fin patterning – solutions: "Sea-of-fins"

- Lithographic restrictions require regular patterns at 20nm node and below
 - Unidirectional fins generally on one pitch
 - Typical approach "sea-of-fins"
 - Unwanted fins and pieces of fins are subsequently removed by "fin-cut" masking steps.
 - Removal of single fins challenging pairs of such sacrificial fins may need to be designated for removal.



Fin shape

- FinFETs with sloping sidewalls have benefits:
 - Are more sturdy mechanically thus less vulnerable to damage during processing;
 - Assure better fill of trenches between fins with fin isolation dielectric;
 - Assure easier gate etch and spacer removal off fin sidewalls
- FinFETs with sloping sidewalls have a significant drawback:
 - Poor short channel control at the fin bottom
 - Need to go to more rectangular shape



Fin dimension variability.

- Fin <u>height and pitch</u> variation major impact on drive current and AC performance at scaled dimensions
- Unlike in planar devices all finbased devices suffer from the same percentage of device width error.



C-Y. Kang et al., VLSI 2013

Device doping

- FinFET generally requires much smaller channel doping than planar devices.
- Source/drain doping challenging due to implant damage, dopant distribution
- Alternatives:
 - High temperature (300-400C) implants,
 - Plasma-based doping
 - Monolayer doping methods
 - In-situ doped epitaxy



Source-Drain engineering: silicide

- Selective epitaxy in source/drain area shapes contact area for subsequent silicidation.
 - Epitaxial growth just merging neighboring fin delivers more area for placement of silicide contact than fully merged fins with flat top surface.



Source-Drain engineering: stress

- Selective epi of SiGe replacing Si fin in s/d area adds stress to PMOS FinFET channel.
- Stress benefit saturates for fin recess ~20nm below STI surface
 - 3D modeling



Stress by SRB

FIN

m

S N N

Si substrate

Fins can be stressed in a similar fashion to that of planar devices

 Stress by buried relaxed epi buffer layer (SRB) has been found by modeling more effective than source/drain stressors in scaled FinFETs



Fin orientation

- Hole mobility is sizably higher on (110) surface than on (100) but the difference decreases with increasing strain
- Electrons flow somewhat slower along (110) plane than on (100) in planar devices.
- In FinFETs, quantum confinement results in quite different behavior electron mobility becomes comparable or better for (110) sidewall conduction than for (100)



Fin isolation – source-to-drain

Source-to-drain leakage.

 Junction-based isolation will likely be very challenging for FinFET devices with gate length Lgate~<15nm.

Alternative solutions:

- Dielectric layer below channel
- Semiconductor buffer layer below channel with appropriate band structure

Simulation results



loff=0.3nA/um

Fin isolation – device-to-device

Device-to-device leakage.

- S/D junction-to-substrate area is much smaller in FinFETs → leakage to substrate is lower
- Required STI trench depth shallower by ~3x

PLANAR STI – INTEL 32nm



FINFET STI – INTEL 22nm



FinFET parasitic capacitance vs planar.

- FinFET has inherently higher parasitic capacitance than planar device.
 - Primarily of gate-to-fin capacitance between part of the gate above the fin and the top of the fin
- Can be optimized down to about 5% above planar device's.
- This capacitance decreases with decreasing fin pitch and increasing fin height, per effective device width



Source: M. Guillorn et al., VLSI 2008

Reliability

- NMOS TDDB and PBTI observed better in transition from planar 32nm to FinFET-based 22nm technology node (Intel).
- PMOS TDDB and NBTI appears unchanged for FinFETs
- Lower transverse field in FinFET is credited for improved reliability.



Source: S. Ramey, et al., IRPS (2013)

Alternative fin materials

- Increasing power density in scaled technologies will require novel channel solutions for higher mobility.
 - Today: Strained Si channel
 - Tomorrow: Alternative channel material with higher mobility
- Leading contenders:
 - NMOS: III-V material is favored for NMOS, particularly InGaAs (SiGe or Ge possible)
 - PMOS: Ge or SiGe with high Ge content
- Key challenge Integration of CMOS on Si substrate.



Alternative fin materials – All III-V?

Can we use one high-mobility material for both NMOS and PMOS?

- Antimonides, specifically InGaSb, show very good electron mobility and decent hole mobility.
- Adequate band edge off-sets for electrons and holes to latticematched buffer material: AlGaSb, for quantum well formation. There would be:
 - >One lattice-matching structure
 - One quantum confinement structure
 - Same gate dielectric and perhaps the same s/d contact material



Alternative fin materials – Integration schemes



DC Performance - NFET Benchmark

- Best III-V channel planar NMOSFETs exceed Si FinFET in performance (Gmsat vs. Ssat at 0.5eV)
- III-V FinFETs catching up



DC performance - PFET Benchmark

Best Ge channel FinFET NMOSFETs exceed Si FinFET in performance (Gmsat vs. Ssat at 0.5eV)



AC performance – planar vs. fin

- Comparison of AC performance using compact modeling
 - Figure-of-merit involving various logic gate configurations
 - As much as 40% gain can be realized in transition from planar to FinFET technology even with Vdd lowered from 0.9 to 0.8V
 - Same baseline design rules (pitches)



Passive elements in FinFET technology

Challenges with incorporating diodes and passive elements in FinFET technology are rather minor.

- Reference diodes and ESD can be realized either in:
 - Long, gated fin diodes and long channel FinFETs
 - Or in the Si bulk substrate.
- Resistors can be done in:
 - Thin films (gate, MOL or BEOL metals),
 - Or in fins.
- Decoupling capacitors can be realized in:
 - Fins
 - Or MIM capacitors.

Nanowires

- At very short gates FinFET body may have to be converted to that of nanowire (aka Gate-All-Around) to control short channel leakage, and DIBL.
- Wires cannot be large in diameter due to device pitch limits.
 - To compete with FinFETs on per-foot-print current drivability, several (2-3) wires need to stacked.
- Vertical wires may offer yet another density scaling option



Vertical Nanowires



Etched Si Nanowires



Source: Steegen, IMEC ITF 2014

Layout Design Methodology

- One size of fins on chip (width, height)
- Wide devices are realized with large number of fins simple.
- Narrow devices and particularly SRAM transistors:
 - STI width between SRAM n and p devices may require customized fin pitches, different than those used in the logic cells in order to further minimize SRAM cell size.
- <u>Taller fins</u> can deliver more effective device width per foot print (with height limits defined by process manufacturability) – potential area saving or performance boost.
- Fin pitch selection related to:
 - Process challenges
 - Optimization of "gear-ratio" between fin pitch and metal 2 pitch in standard logic cell design.

SRAM

- SRAM design tradeoff between stabile operation and cell size.
- Densest SRAM cell design would use 1-1-1 approach:
 - One-fin pull-up transistor (PU), one-fin pass-gate transistor (PG) and one-fin pulldown (PD).
 - This configuration would provide the smallest SRAM cell size with lowest stand-by leakage.
 - However, cell would likely require write assist and read assist circuitry.
- Larger cells, such as 1-2-2 or 1-2-3 (PU-PG-PD)
 - Would require less operation assistance, perhaps only for reading the cell.



FinFET design ecosystem

- Most of electronic design automation (EDA) tools need to be adapted for FinFET designs.
- This process has been largely completed and tools are available from key vendors (Synopsis, Mentor Graphic and Cadence).
- Leading semiconductor foundries are capable of providing full EDA support for their customers.

Tool/Function	Tool status
Spice Simulation	
RC Extraction	
DRC	
LVS/LPE	
RTL Synthesis	
Floorplan/Placement	
Routing	
Static Timing Analysis	
DFT, IR drop, Signal Integrity	

Summary

High performance logic has adapted FinFET technoloy and will continue to use it for several generations into the future.

- SoC products will follow shortly after.
- New materials for fins will likely be introduced into products in this decade.

 Substantial changes are brought up into circuit-design world by FinFET.

Design ecosystem for FinFETs is available.

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