Doping FinFETs: Trade-offs for Beamline Implantation, Plasma Doping, and Diffusion from Doped Epi/CVD Films

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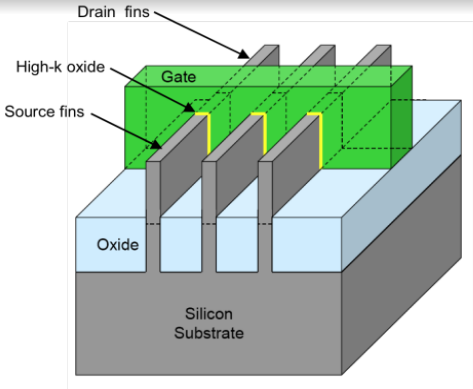
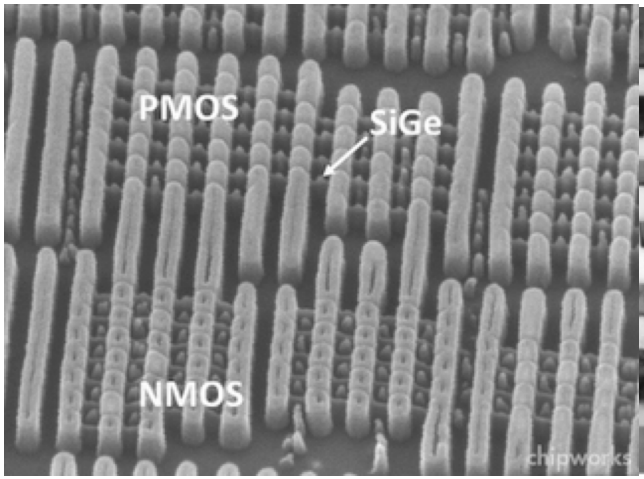
Outline

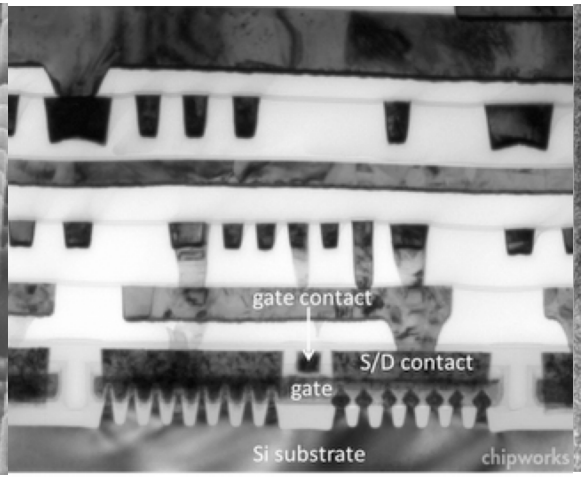
- Introduction to FinFET doping
- Advantages and concerns with implant-based FinFET doping
- Advantages and concerns with deposition-based FinFET doping
- Summary

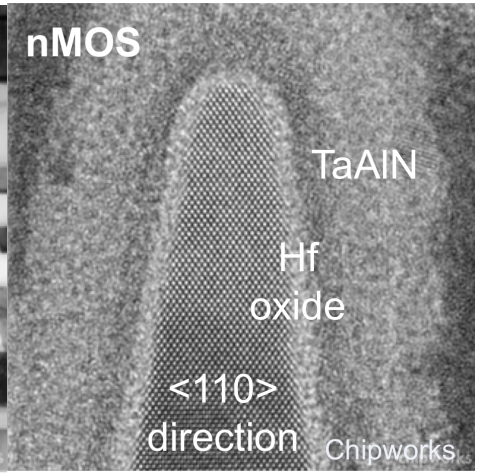
Three-Dimensional (3D) Transistors

- FinFETs or tri-gate transistors
  - In production for Intel's 22 and 14 nm technologies
  - Scheduled for foundry production at Global Foundries, TSMC, Samsung, etc.



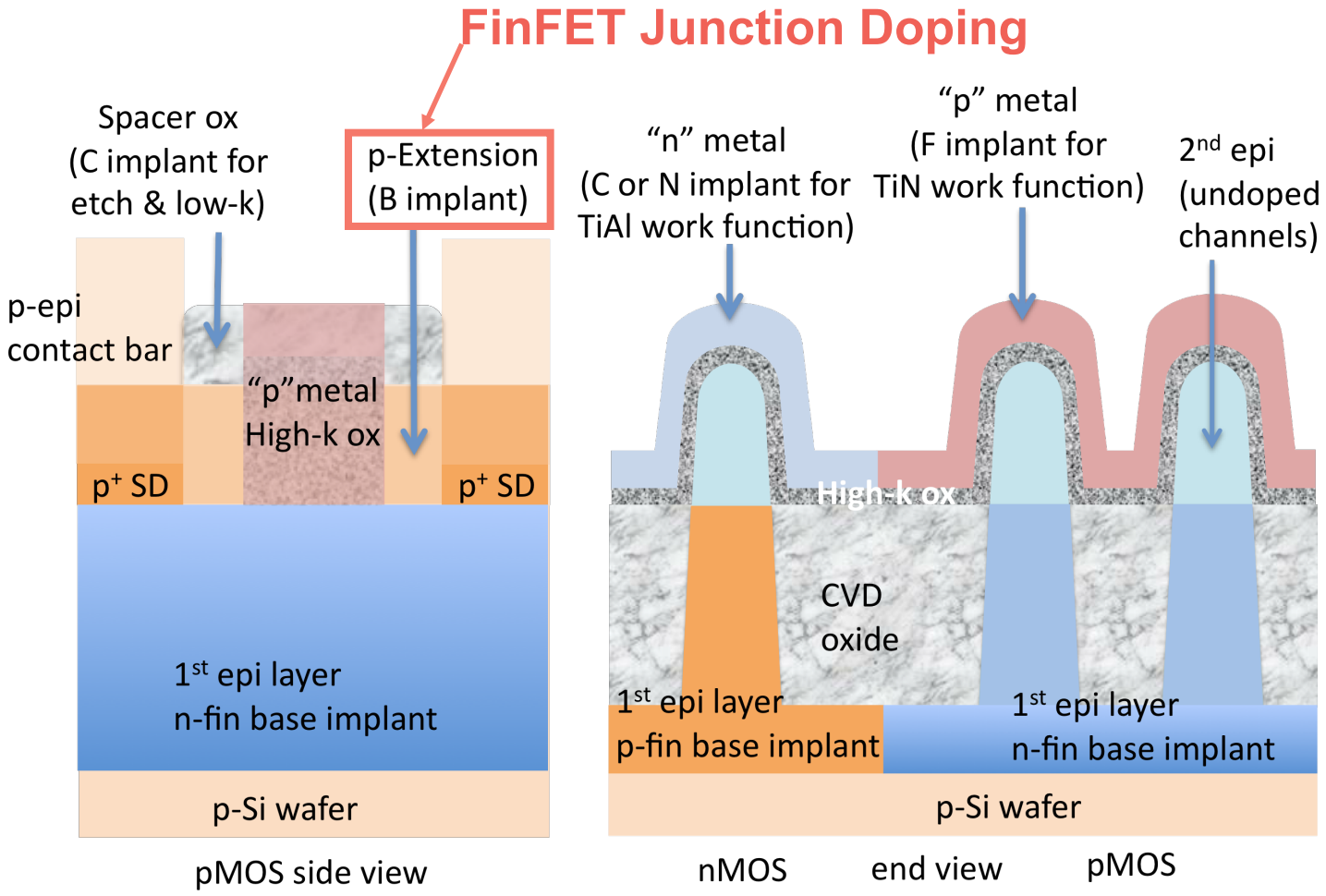






Intel 22 nm FinFET: Images by Chipworks

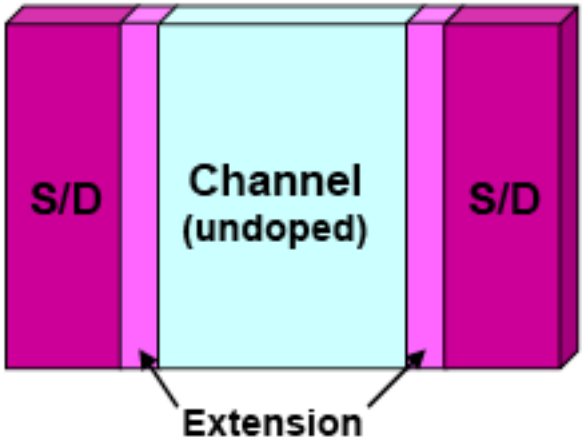
Potential Implants for Bulk FinFET Doping and Materials Modification

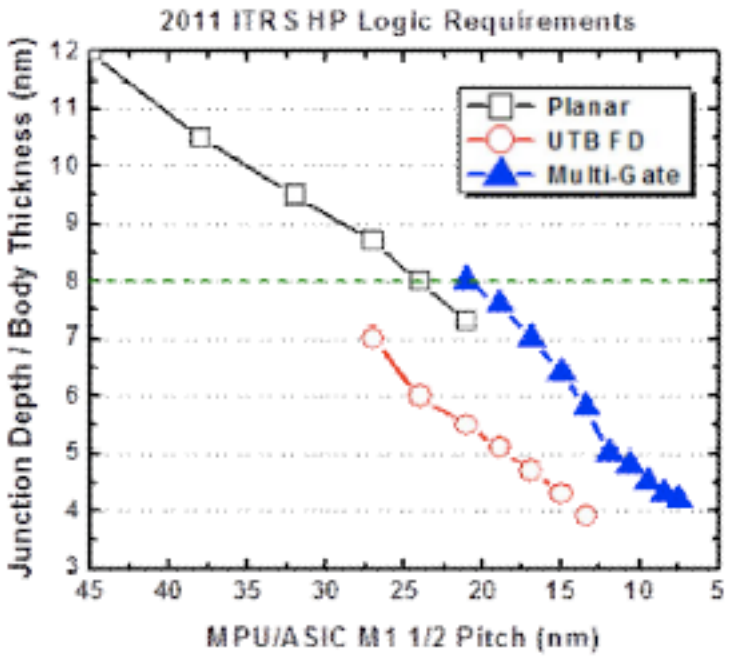


Courtesy of Michael Current, 2013

ITRS 2011 Roadmap for Junction Depths

FinFET Device w/Extension





- Uniform current at top, middle, and bottom of fin
  - Uniform source/drain extension doping
- Lateral junction depth (gate/SDE overlap) is key for FinFETs
  - Short channel effect control
  - Approximately equal to ITRS X_j values
- 10 nm node requires Multi-Gate with <5 nm X_j

Sematech and DNS, IWJT 2012, Paper I1-03

Doping Requirements for N10 FinFETs

- Ultra-shallow, abrupt, and damage-free junctions with high active dopant concentrations
  - $X_j < 5$ nm
  - Minimal amorphization thickness
- High retained dose over entire Fin surface (after cleans, caps, and anneals)
  - Minimal oxidation on FinFET sidewalls from PR ash
- Good process uniformity and repeatability (wafer-to-wafer, day-to-day)
- No fin erosion (corners or fin height)
- Compatibility with standard photoresist patterning processes

General FinFET Doping Issues

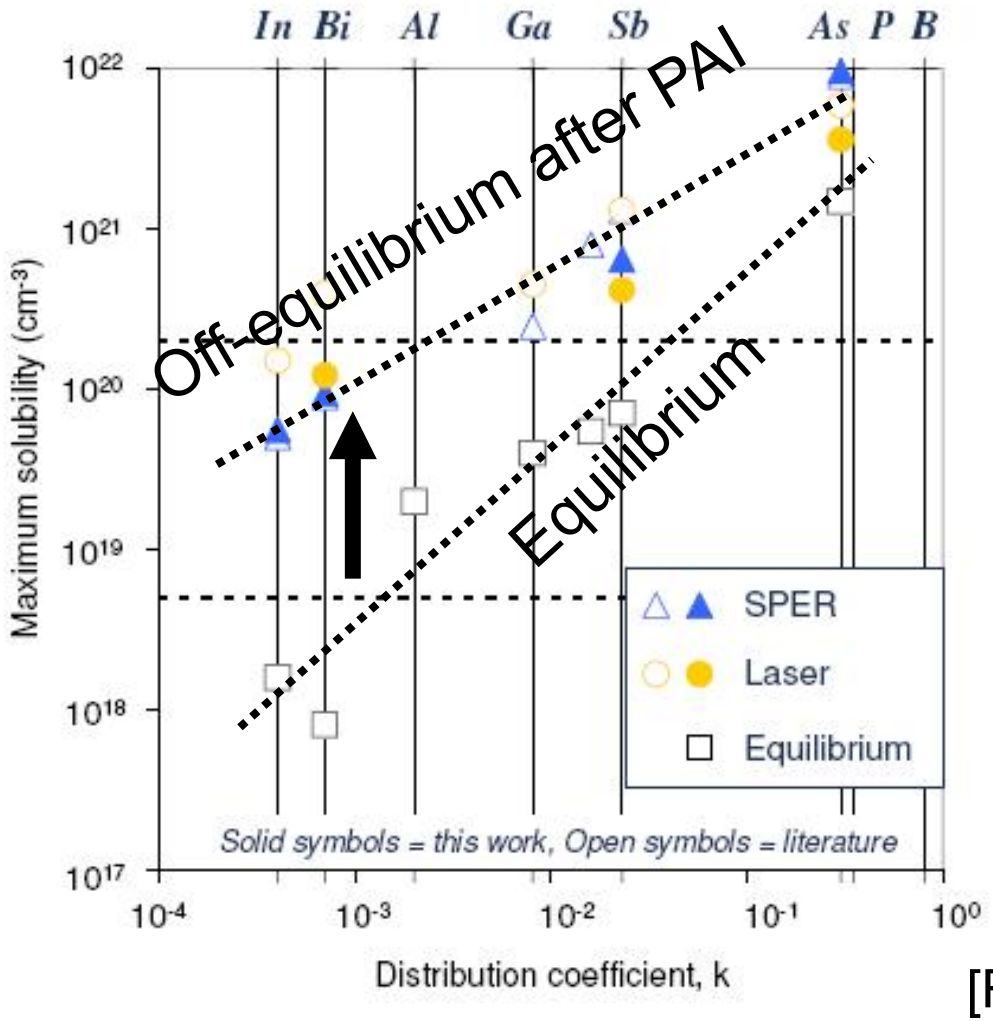
- Hard mask needed for all techniques other than implant and Plasma Doping
- Fin cannot be completely amorphized
- Difficult to strip photoresist with Plasma Doping (high dopant surface concentration)
- Surface oxidation after doping results in dopant loss during cleans
- Surface diffusion-based techniques are sensitive to surface condition and cleanliness
- Dopant profile in Si determined by anneal
  - Need some diffusion to get dopant from surface into Si and under gate, so need more than millisecond anneal ("diffusion-less")
  - Anneal temperature limitations may limit electrical activation

FinFET Doping Candidates

- Implant-based
  - Tilted beamline implant
  - Plasma Doping
- Deposition-based
  - In-situ doped epi + diffusion
  - Monolayer Deposition (MLD) + diffusion
  - Deposited thin film (PECVD/ALD) + diffusion
  - PECVD + beamline implant knock-on + anneal (SEN MTI technique)

Advantages and Concerns with Implant-Based FinFET Doping

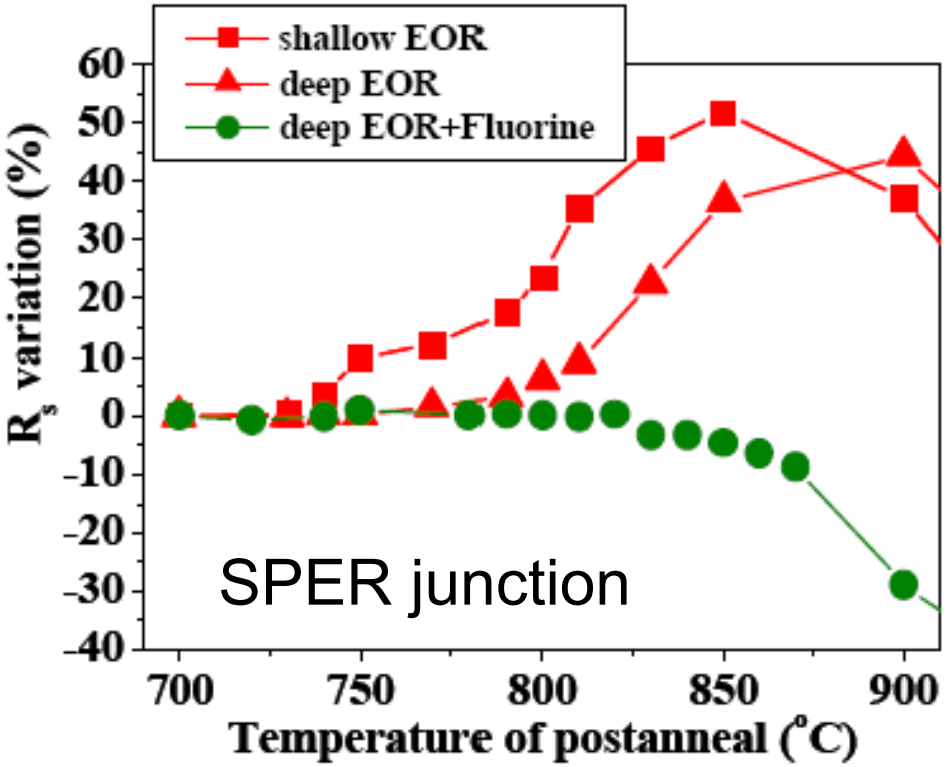
Off-Equilibrium Annealing after PAI Can Improve Solid Solubility and Sheet Resistance



- Melt laser
- Sub-melt laser

[R. Duffy, Spring MRS 2006]

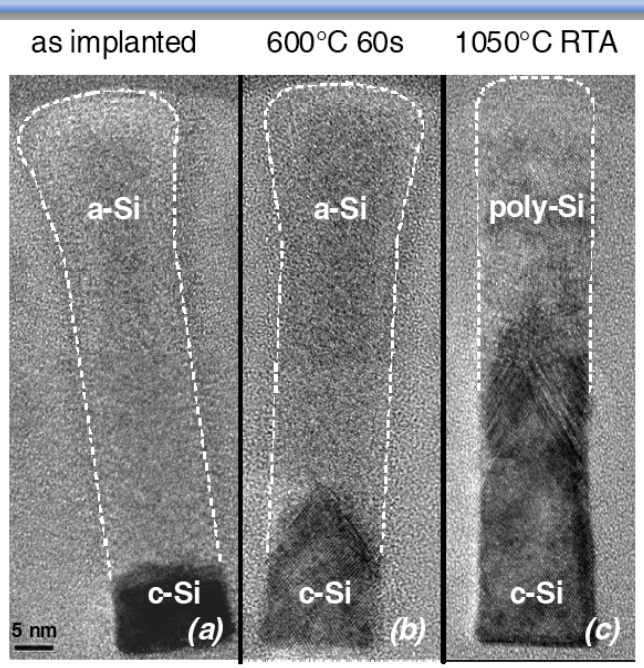
Dopant De-Activation During Subsequent Thermal Process Steps

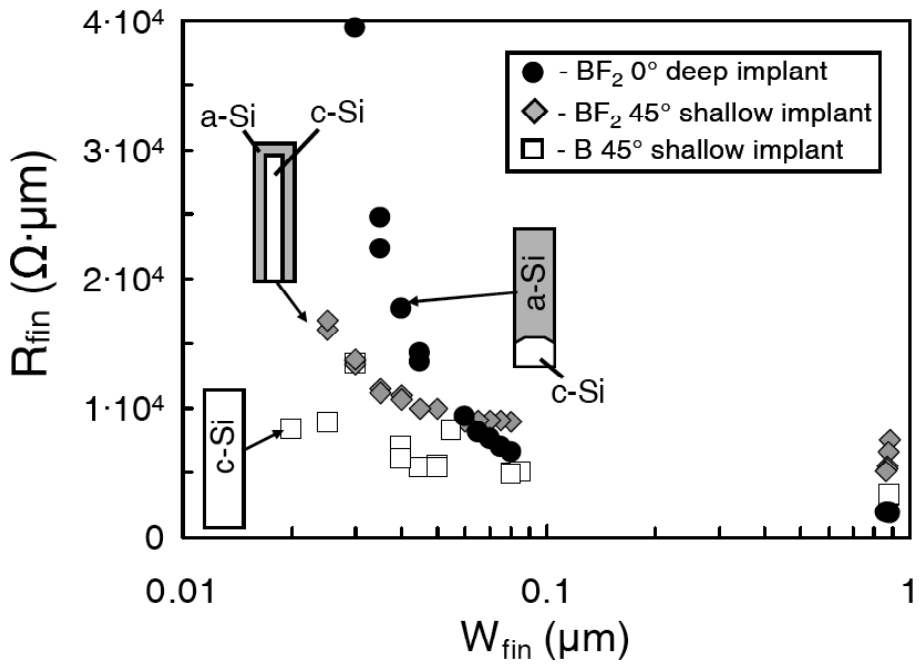


- SPER junctions are de-activated by interstitials emitted from EOR-defects during post-anneal
- C/F trap the interstitials and prevent de-activation
- This does not happen only for SPER junctions, but any junctions with EOR defects (Laser and Flash Anneal)
- Concern with any >700C thermal processes after junction formation

[B.J. Pawlak *et al*., Appl. Phys. Lett. **84**, 2004]
[N.E.B. Cowern *et al.* Appl. Phys. Lett. **86**, 2005]

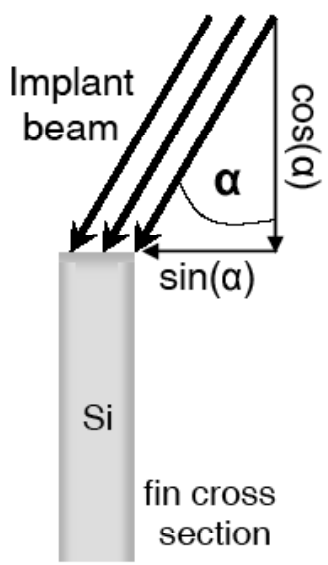
Challenges due to Fin Amorphization



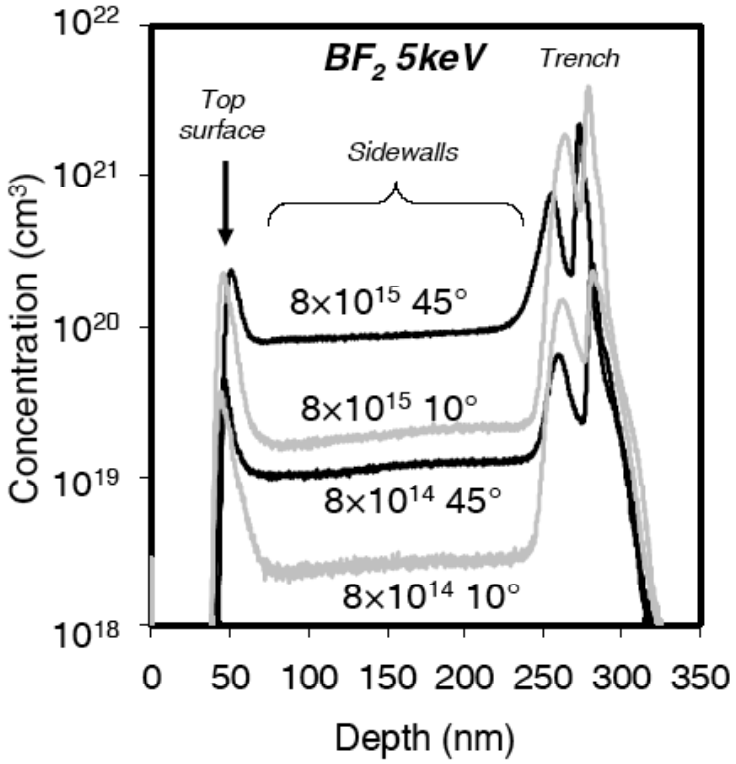


- Complete fin amorphization leaves only small area of crystalline seeds at channel and fin bottom to enable re-crystallization
  - Leads to growth of twin boundaries and large areas in poly-crystalline form
  - Reduced dopant activation and poor carrier mobilities due to residual defects and poly-crystalline Si
- Must minimize fin amorphization

Shadowing and Dose Retention Issues with Beamline Implant



a)

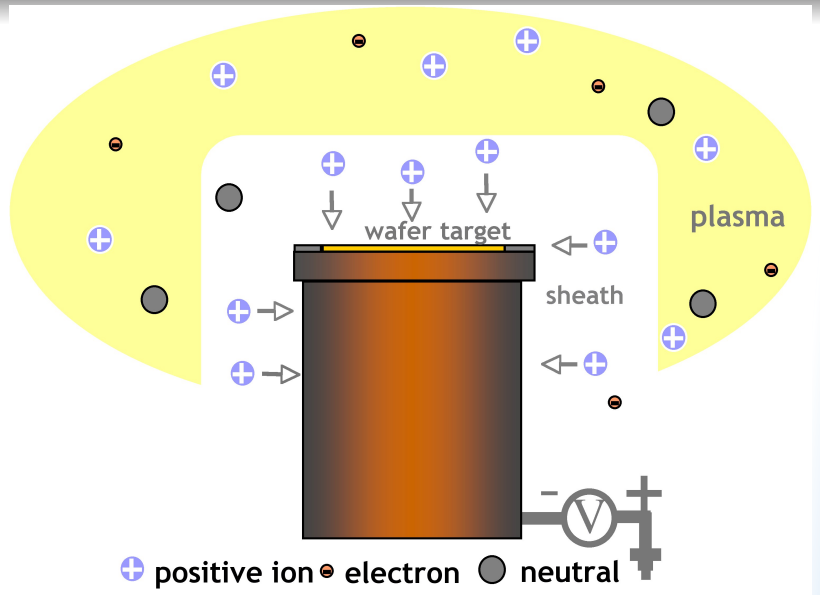


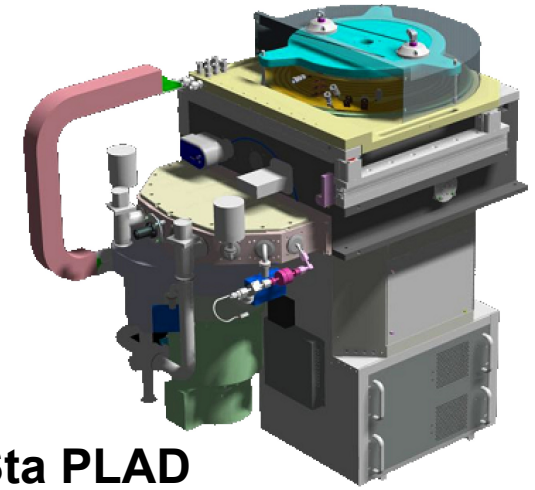
b)

- Tilt angle is limited due to shadowing from tight fin spacing, high aspect ratios, and presence of PR and other films for litho
- Sidewall doping with 10° beam is ~10 times less than that with 45° beam
  - Due to ion reflection, limited ion penetration into sidewall, and sputtering

Plasma Doping:
High-Dose Doping & Materials Modification

- Negative voltage repels electrons and creates plasma sheath of positive ions
- Electric field accelerates positive ions and implants them into wafer
- Voltage determines implant depth
  - "Accelerator size" is sheath thickness
  - 100 V – 10 kV
- Simultaneous implantation of whole wafer
- Many doping and materials modification applications
  - Very high doses (> 10^{16} cm^{-2})
  - 2 applications used in production of almost all DRAM devices today

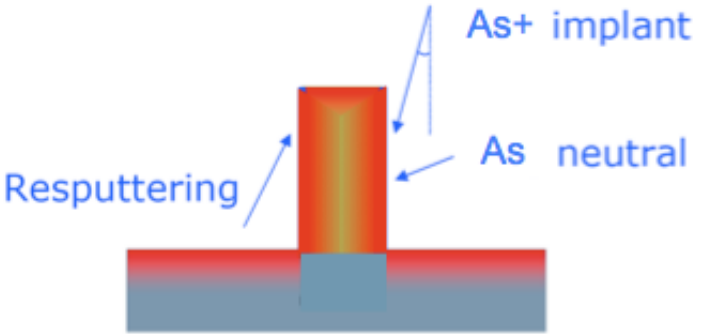




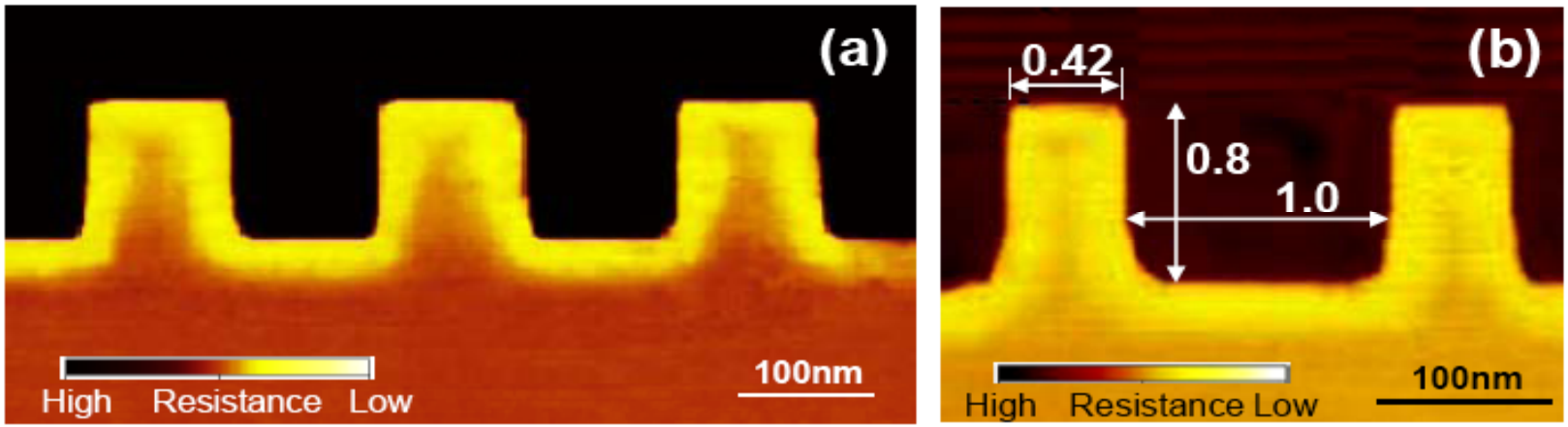
Varian VIISta PLAD

FinFET Plasma Doping

- 3D Plasma Doping is a combination of:
  - Direct implant
  - Re-sputtering from bottom between fins
  - Deposition
- Multiple process knobs for optimization of doping conformality
  - Implant influenced by electric field and gas molecule collisions
- High throughput at low ion energies
  - Minimize fin erosion and amorphization
  - Ultra-shallow junction depths

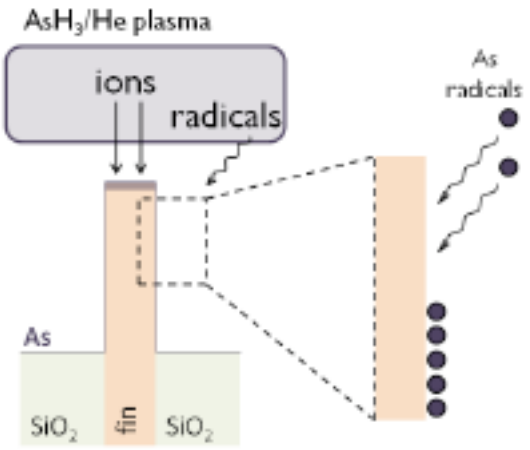


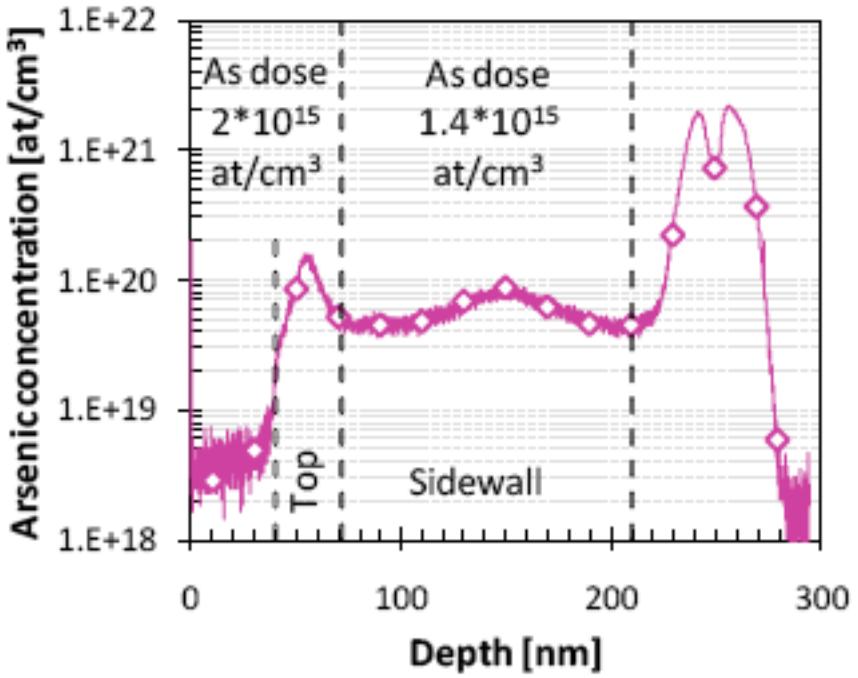
UJT Plasma Doping Process & Results



- He PAI + USJ dopant (B_2H_6 or AsH_3) implant = SRPD (Self-Regulatory Plasma Doping)
  - 1) He PAI
  - 2) B_2H_6 is "absorbed by the sponge" formed in Step 1
- Excellent conformality demonstrated (SSRM)
  - Similar doping depth on top and sides of fin
  - No fin erosion (corners or fin height)
- 10% I_{on} improvement at IMEC

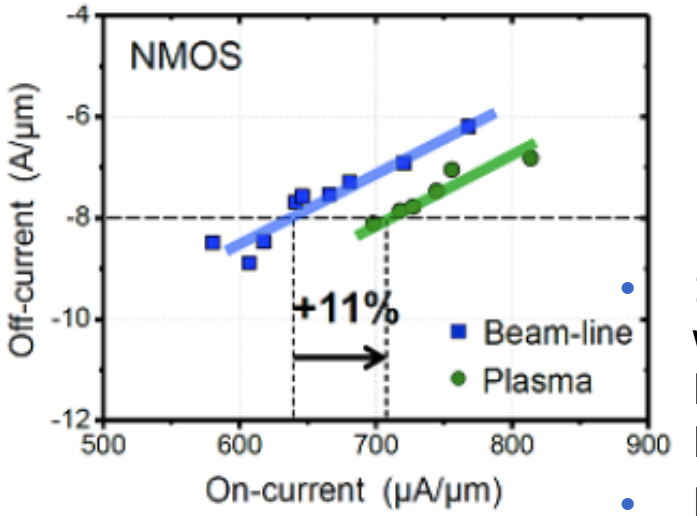
UJT AsH_3/He Plasma Doping

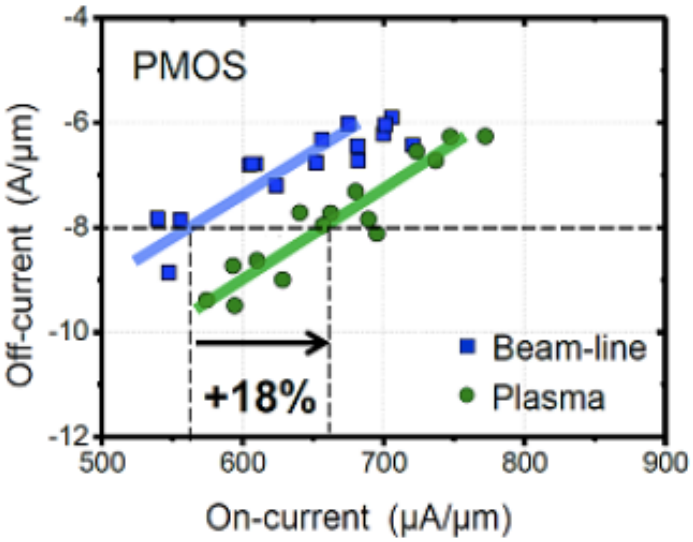




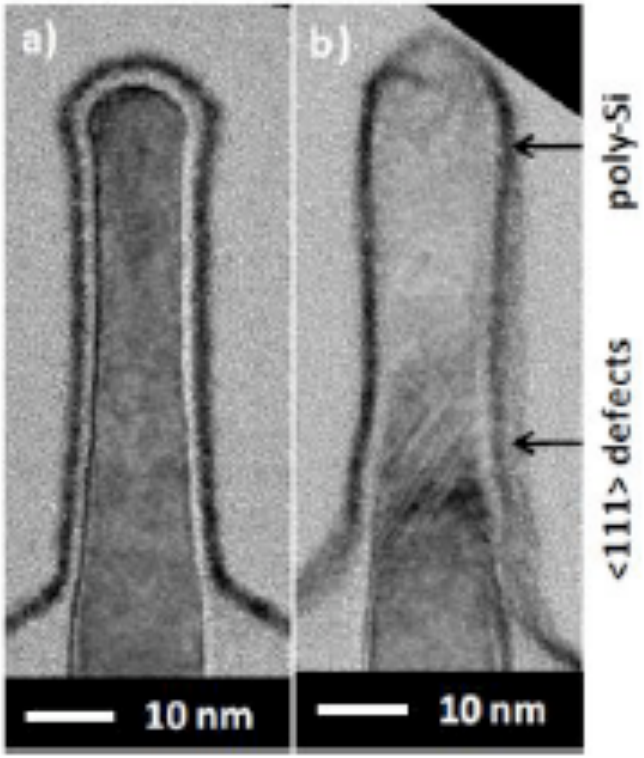
- Sidewall doping by adsorption of As radicals and subsequent thermal drive-in
- SIMS through Fin data after anneal show sidewall/top As dose ratio ~ 0.7
- IMEC, IWJT 2012, Paper I3-02

Plasma Doping vs. Beamline Implant for FinFET Devices





- >10% gain in I_{on} with Plasma Doping for both PMOS and NMOS
- IBS & CEA-LETI, IIT 2012, p. 71



- TEM comparison of fin crystalline quality with UJT SRPD and beamline implant
- IMEC, IWJT 2012, Paper I3-02

Process Integration Issues with Plasma Doping

- Difficult to strip photoresist with Plasma Doping (high dopant surface concentration)
- Surface dopant loss due to oxidation during PR strip and subsequent HF cleans
- Additional enhanced oxidation after Plasma Doping implants
  - Enhanced by presence of high dopant concentration and/or high density of broken Si bonds
- Perfectly conformal implant?
  - Difficult to find process space
  - Plasma is too directional; need more scattering
- Poor quality of regrown fin Si after Plasma Doping
  - Especially after AsH_3 Plasma Doping
  - Must minimize fin amorphization

Plasma Doping vs. Beamline Implant

- Advantages of beamline implant
  - Dose control, uniformity, and repeatability
  - Particles
  - Tool maturity
- Advantages of Plasma Doping
  - More process knobs to optimize conformality by balancing direct implant, deposition, and re-sputtering
  - Higher throughput for lower energies required to minimize amorphization
- Same process integration issues (e.g. surface dopant loss)
- Both are compatible with photoresist
  - Hard mask required for patterning with other deposition-based techniques
    - Additional processing steps
    - More expensive

Advantages and Concerns with Deposition-Based FinFET Doping

Effect of Thermal Budget Limits on Dopant Diffusion and Activation

- Need some diffusion to get dopant from surface into Si and under gate, so need more than millisecond anneal ("diffusion-less")
  - For 2 nm diffusion, need 10 msec at 1200C
- Anneal temperature limitations may limit electrical activation

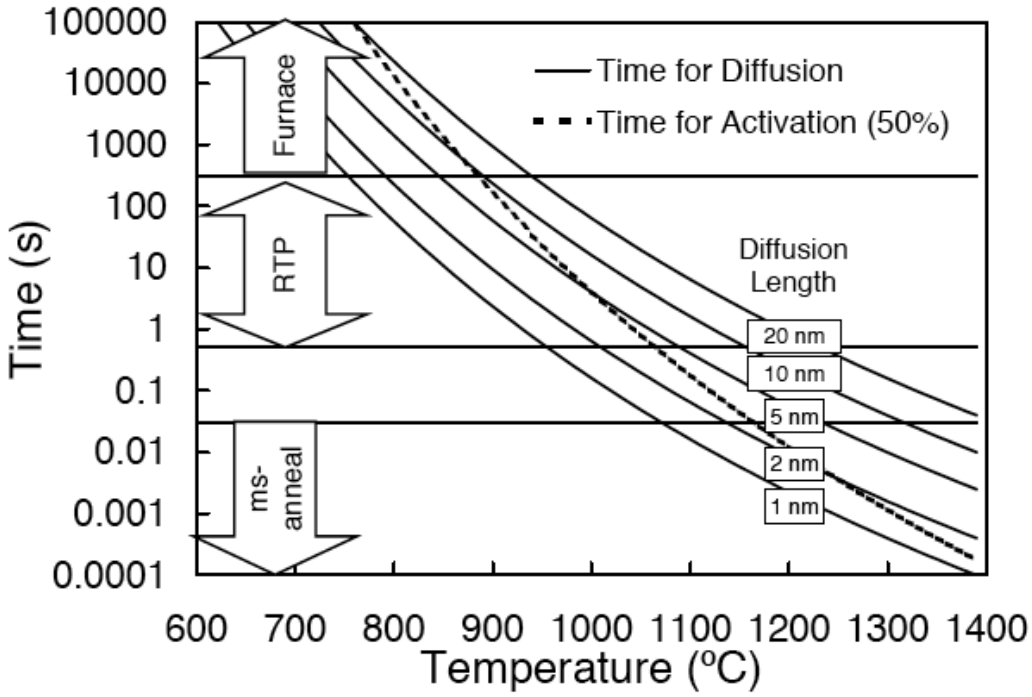
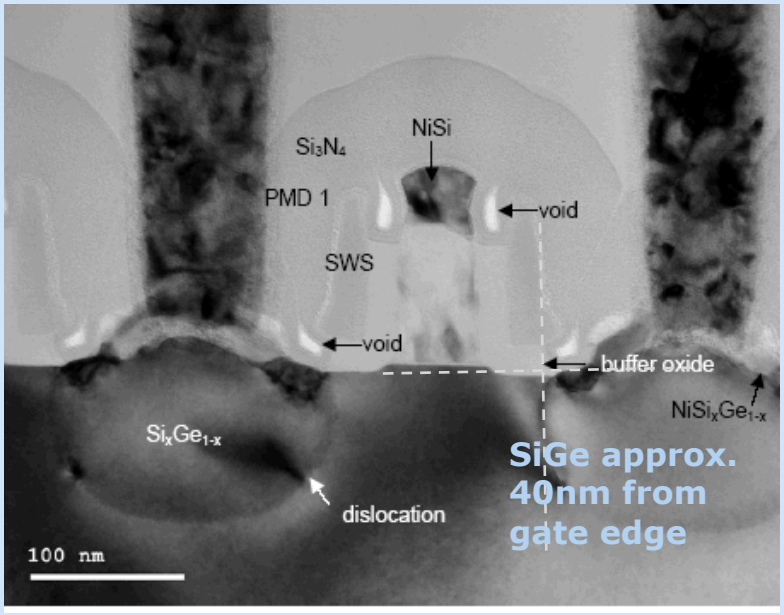


Figure 4.1 Thermal budget limitations for advanced processing. Intrinsic diffusion lengths for Boron are shown as a function of thermal cycle [Holton00] as compared to the criterion for 50% electrical activation of a 10^{15} B/cm^2 implant at 250 eV [Mokhberi02]].

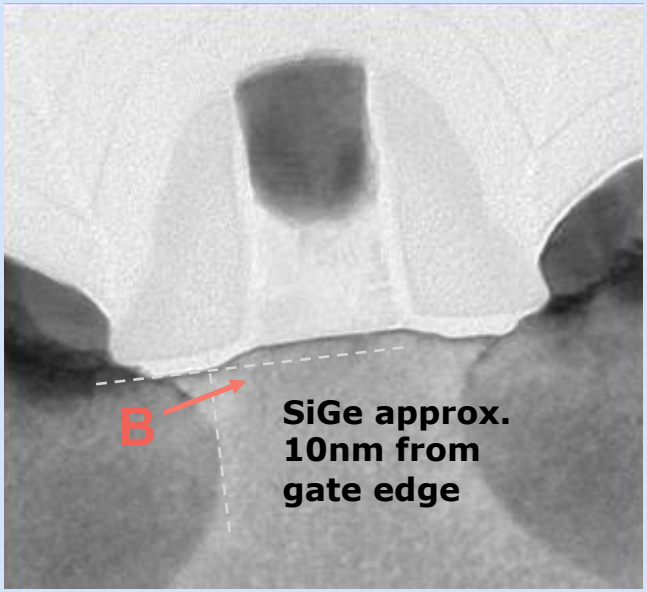
Courtesy of M. Current

In-situ Doped Epi + Diffusion

90nm Device with Recessed SiGe

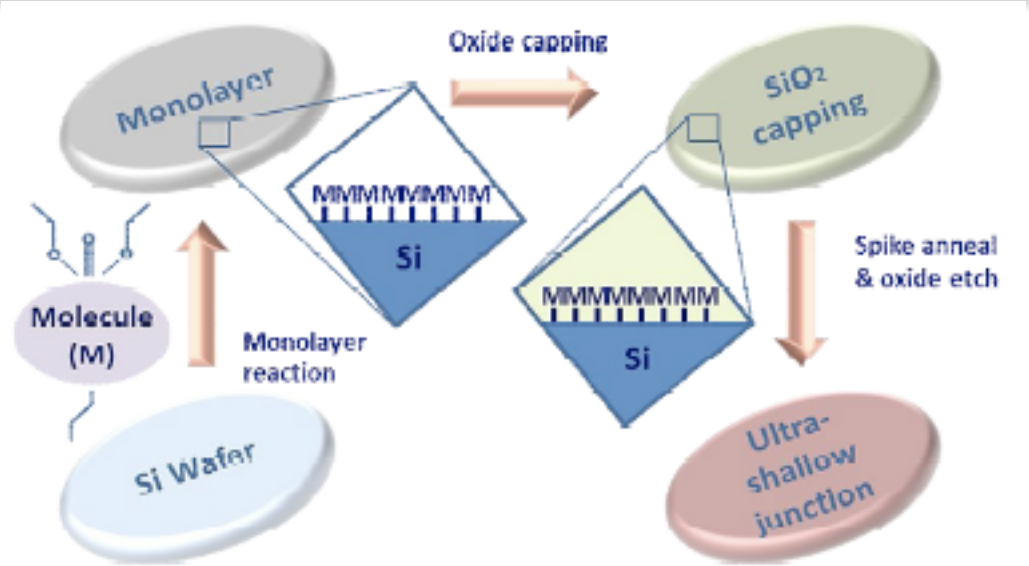


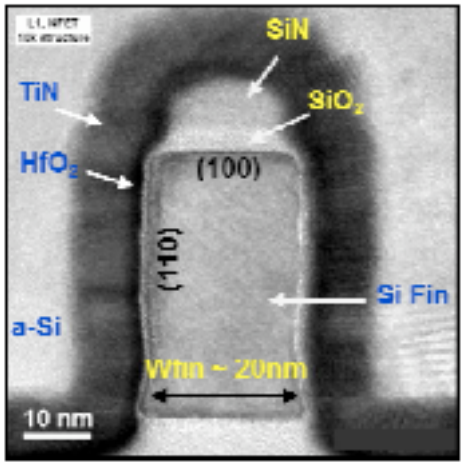
65nm Device with Recessed SiGe



- Diffuse dopant from epi source/drain into source/drain extension region
  - PMOS: B from SiGe
  - NMOS: P from Si:C

Monolayer Doping (MLD) + Diffusion





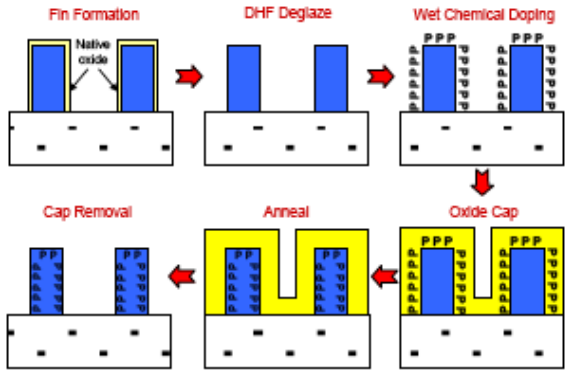
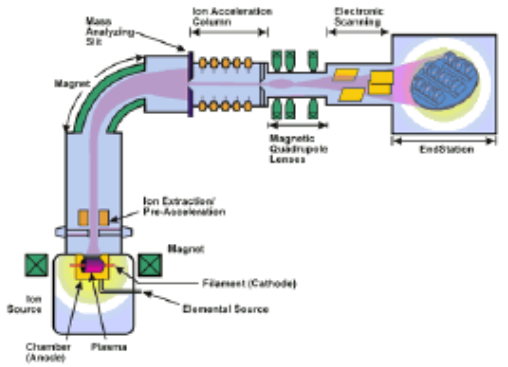
Sematech and DNS, IWJT 2012, Paper I1-03

- Monolayer of dopants is assembled on Si surface
  - Uniform sticking of covalently bonded, dopant containing molecules
  - Molecular footprint of precursor tunes areal dopant dose
- Subsequent thermal treatment breaks dopant molecules and results in thermal diffusion of dopant atoms into Si substrate
  - Thermal treatment temperature and time govern junction depth

Comparison of MLD and Beamline Implant

Non-Planar Doping Module

SEMATECH

Approach	MLD (Partner: DNS)	Beam Line
Process Steps		
Doping Uniformity	Uniform & Conformal around Fin (by means of wet chemical doping)	Poor Uniformity, Non-Conformal
FIN Damage	No Damage (Wet Chemical Doping)	Severe Ion Implant Damage
Junction Doping	Fin-Width, Thermal Budget Dependent	Good
Remarks	❑ Defect-Free ❑ USJ (<10nm) & highly conformal ❑ Cap layer selection is critical	▪ Industry standard process ▪ Severe Fin damage ▪ Junction depth >20nm

Deposited Thin Film (PECVD/ALD) + Diffusion

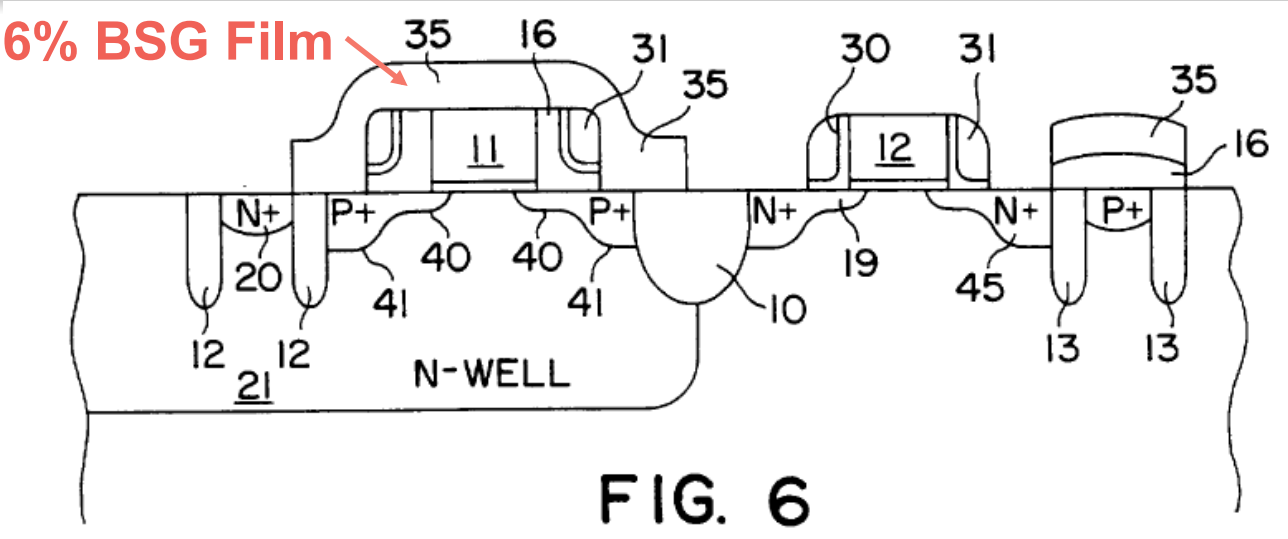
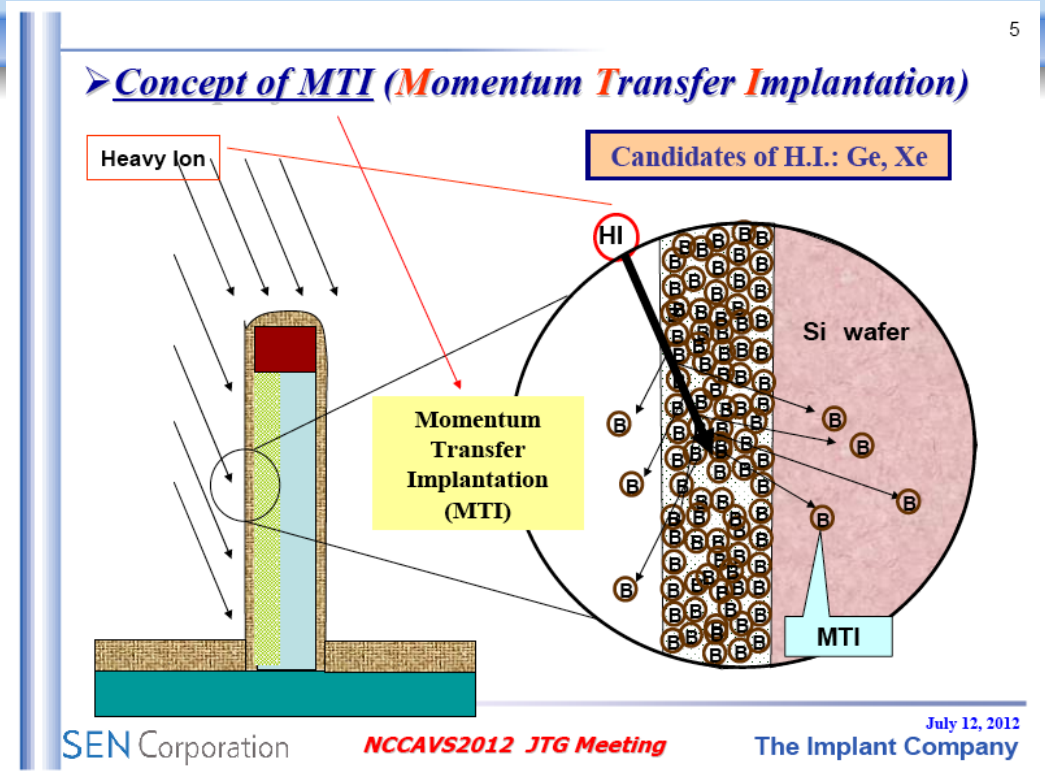


FIG. 6

"Formation of Source/Drain from Doped Glass," Intel Patent Application **WO1997013273**

- Deposit thin film containing desired dopant
  - PECVD, ALD, CVD
- Subsequent thermal treatment results in thermal diffusion of dopant atoms into Si substrate
  - Thermal treatment temperature and time govern junction depth

PECVD + Beamline Implant Knock-on + Anneal: Momentum Transfer Implant (MTI)



- 1. 3 nm B or P deposition (PECVD in LEDA with 0V)
- 2. Beamline implant at 10° tilt
  - Ge^+ for B (~1E15)
  - Xe^+ for P (mid E14)
  - Knock B or P dopant into Si fin sidewalls
- 3. Anneal to diffuse and activate dopant
- No amorphous layer produced

Advantages and Concerns of Deposition-Based FinFET Doping

- Advantages
  - Very good conformality
  - No amorphization, so residual damage is minimal

- Concerns
  - Hard mask needed for patterning, as opposed to photoresist
    - MTI may be able to use photoresist
  - Sensitive to surface condition and cleanliness
    - MTI is less sensitive to surface condition
  - Dopant profile in Si determined by anneal
    - Need some diffusion to get dopant into Si, so need more than millisecond anneal ("diffusion-less")
    - Anneal temperature limitations may limit electrical activation
    - No amorphous layer to give higher, non-equilibrium dopant activation

Summary: FinFET Doping Trade-offs

- Several candidates for FinFET doping
- All have advantages and concerns
- No clear winner
  - Different technologies may be used by different companies
  - Different technologies may be used for PMOS and NMOS