Damage Accumulation & Annealing
in planar and vertical CMOS Channels

Michael Current

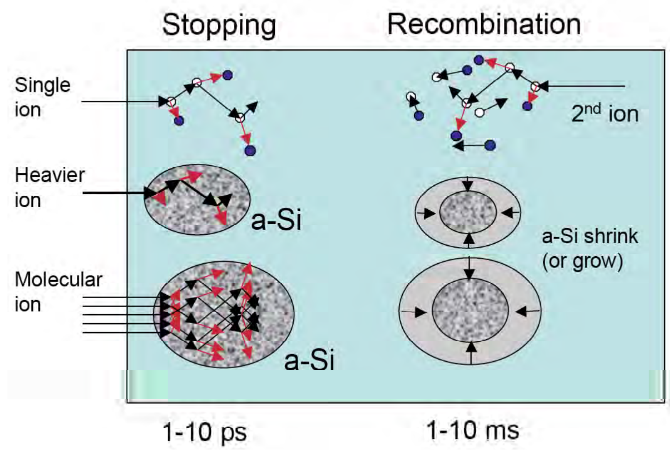
1. Basics of Primary of State of Damage (M_{ion}, E_{ion}, target atom binding)
2. Damage Accumulation Effects (Dose, J_{beam}, T_{wafer}, molecules)
3. Edge Effects (planar mask edges, vertical fin surfaces)
4. Chasing "damage-less" Implants ("Hot fins")
5. Probing "Top Hat" Defects (Cathodoluminesence)
6. Summary

Basics of Primary of State of Damage (M_{ion}, E_{ion})

"Electronic" Stopping: ion collisions with single electrons

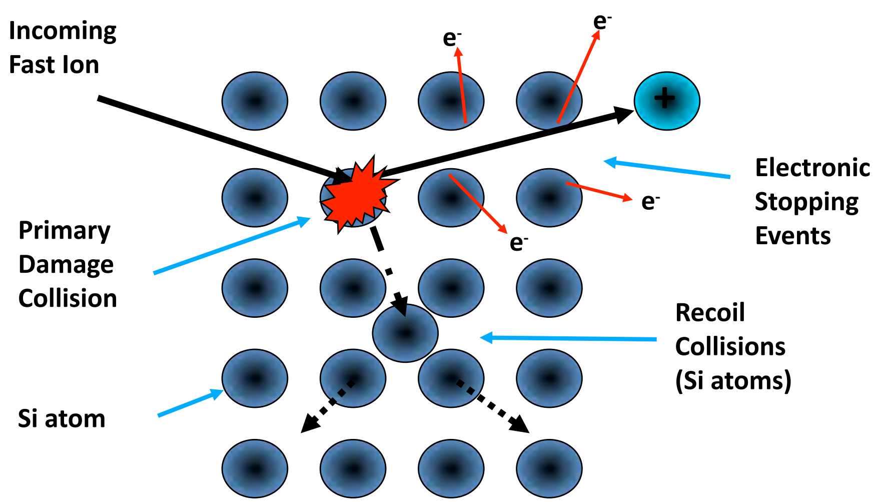
"Nuclear" Stopping: ion collisions with Si core electrons (and nuclei)

Each ion stopping tracks results in many "primary recoils" generating vacancies & interstitials, Frenkel pairs.



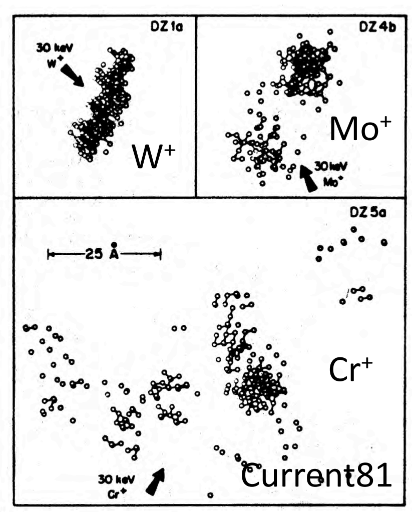
$$n_{FP} = [E_{ion} - Q_{elelctronic}]/2E_D$$

$$E_D(Si) \approx 15\text{-}45 \text{ eV}$$



Vacancies in W

DZs in



Damage Accumulation Effects

(Dose, J_{beam}, T_{wafer}, molecules)

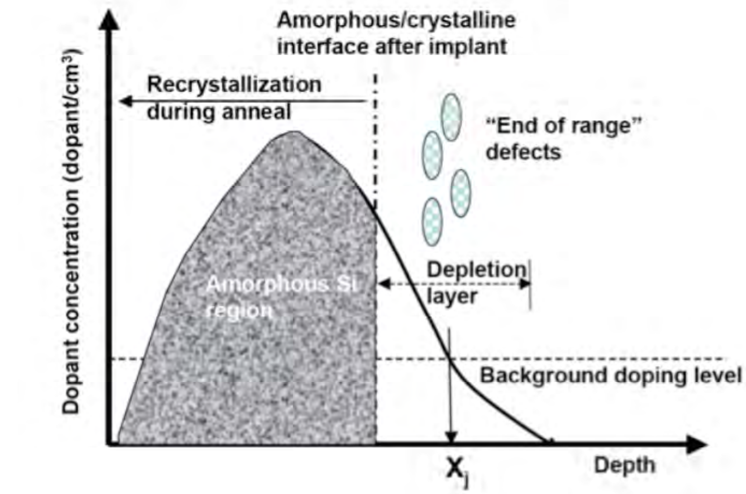
Total number of **accumulated defects** during an implant depends on:

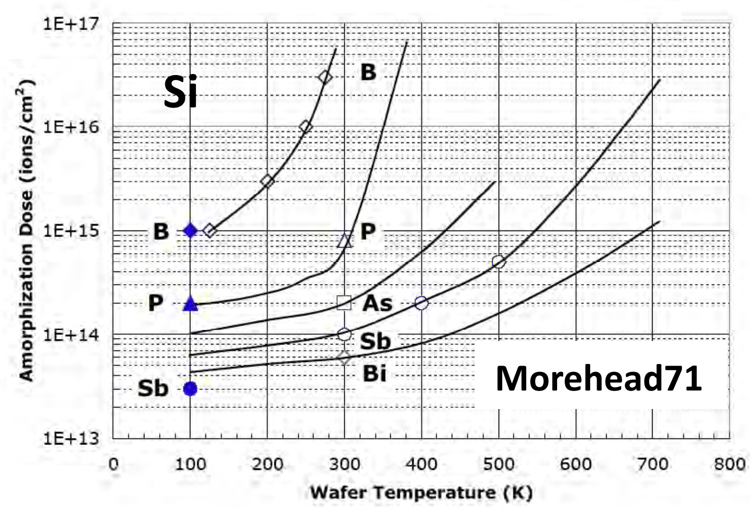
1. **Ion energy**, atomic number, mass, **dose**.

2. **Target** atomic number, mass, binding energy, **temperature** (defect diffusion rate).

3**. Ion flux rate** (beam current density, scan rate).

At low (≈100 uA) beam currents, the **a/c transition** conditions depend on **ion mass** & **wafer temperature**.

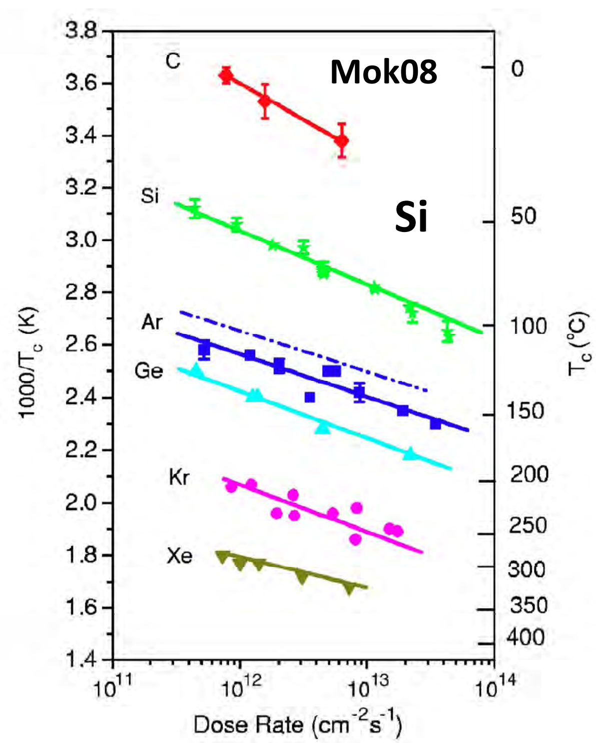




Damage Accumulation Effects

(Dose, J_{beam}, T_{wafer}, molecules)

At higher (> 1 mA) beam currents, the **a/c transition *also*** depends on **ion flux rate**.



20 keV B in Si, $5x10^{15}$ B/cm^2

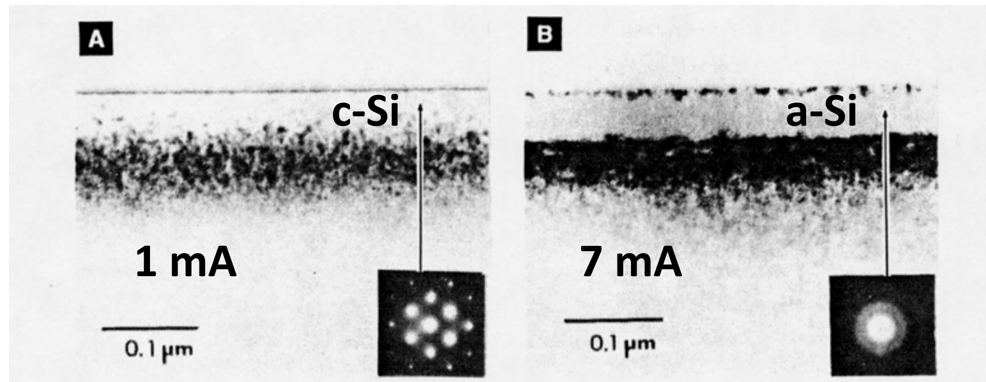


Figure 5. Cross-sectional TEM images, before annealing, of samples implanted with $^{11}B^{+}$, 20 keV, $5x10^{15}$ atoms/cm^2 using a) 1 mA and b) 7 mA. The electron diffraction pattern from the surface region is provided as an inset for both samples.

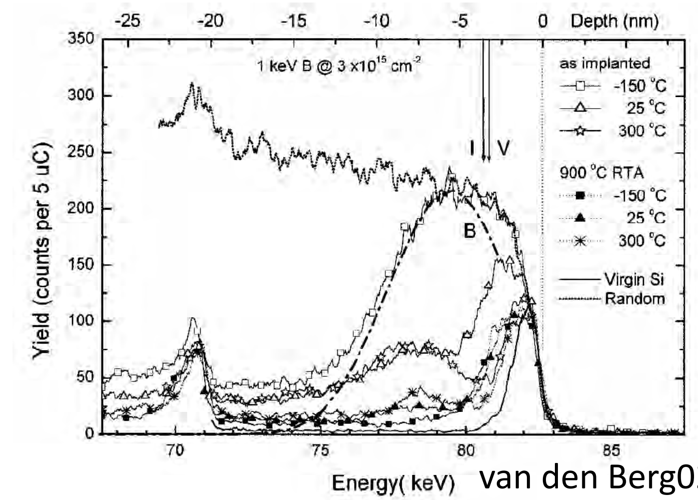
R. Simonton et al. 1992

Higher damage accumulation:
- * **Higher mass** ions (also ***molecular*** ions)
- * **Lower** Si **temperature**
- * **Higher** beam **current density**
- * **Slower scan** speeds

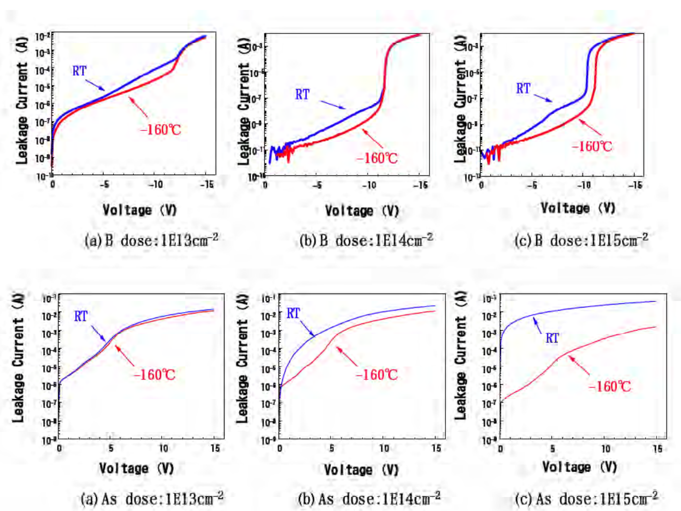
Cryo-implants: *Minimize* EOR damage by *maximizing* a-Si thickness

Cryo (<0 C) implants generally result in thicker a-Si layers, with the idea that fewer EOR defects are left to form damage, enhance B & P diffusion, etc.

Lower junction leakage currents have been reported.



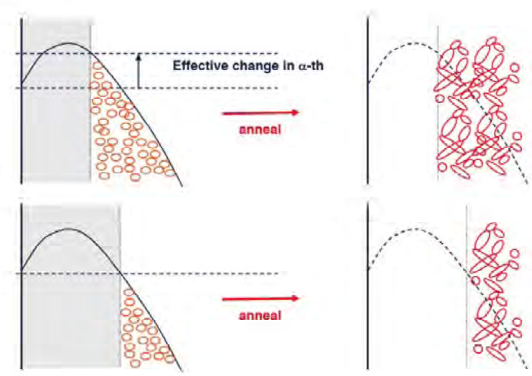
van den Berg02



Suguro01

Low damage accumulation
Low ion mass, low current
High temperature
Shallow a/c, rough a/c interface
Dense EOR damage, high leakage

High damage accumulation
High ion mass, high current
Low temperature
Deep a/c, smooth a/sc interface
Sparse EOR damage, low leakage



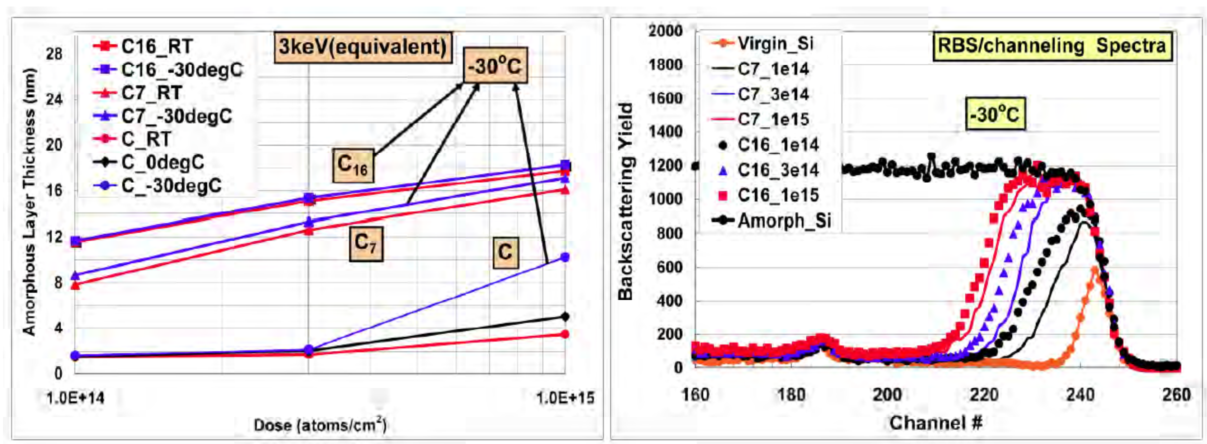
M. Ameen

Molecular Ions:

Another (better) way to *increase* damage accumulation

When ***many atoms*** hit Si in **the same ≈ps timeframe**, *strong collective collisions* greatly ***increase*** net damage.

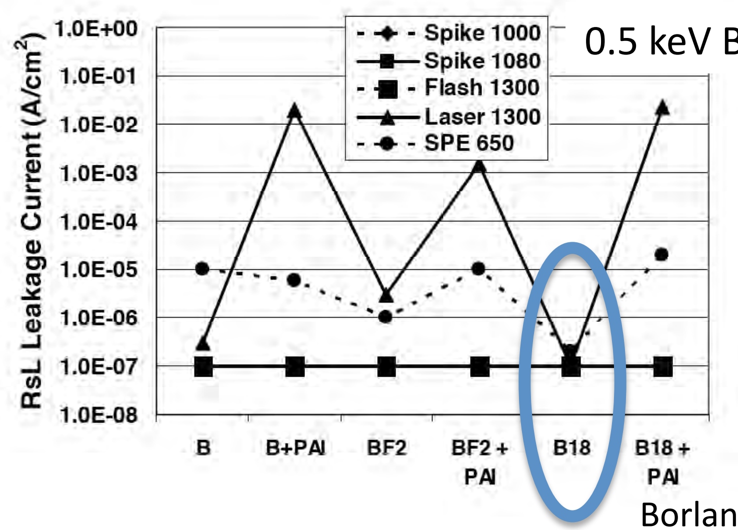
Thicker a-Si layers, especially at Room Temp (≈25 C).



Sekar11

Molecular ions (C_7H_7, $C_{16}H_{16}$, $B_{10}H_{14}$, $B_{18}H_{22}$, etc. implants make deeper a-Si layers than single ions with the same equivalent energy.

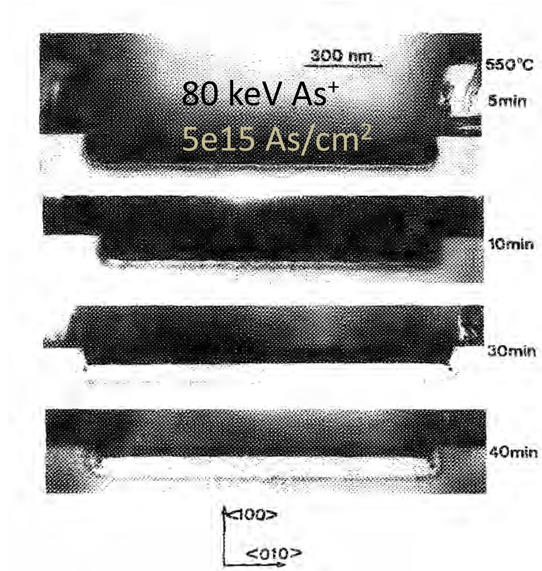
Junction leakage for molecular ion doped junctions is *systematically* low.

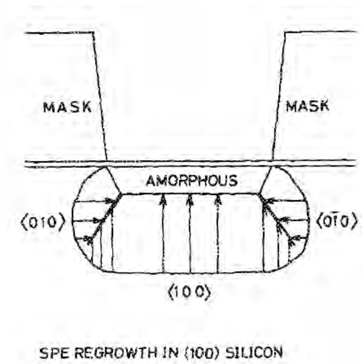


Borland06

Edge Effects:1   Planar mask edges

Different re-growth rates for various crystal directions lead to “pile up” defects & strain at edges of masks during annealing of high-dose implants.





M. Horiguchi /Hitachi JAP89

Net residual damage is the sum of “End-of-Range” damage beyond the original a/c interface & mask edge “facets”.

104908-4   Saenger *et al.*   J. Appl. Phys. **101**, 104908 (2007)

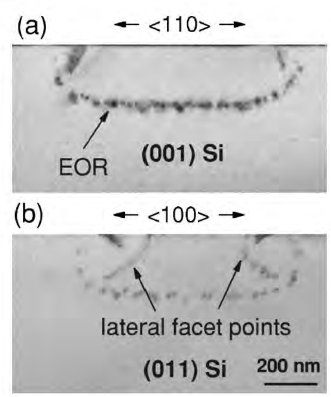
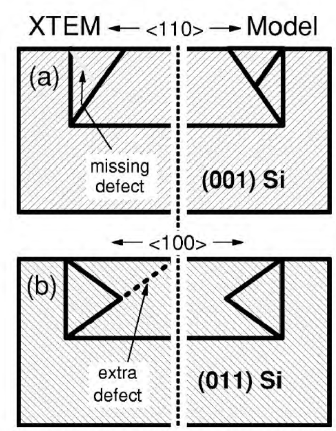


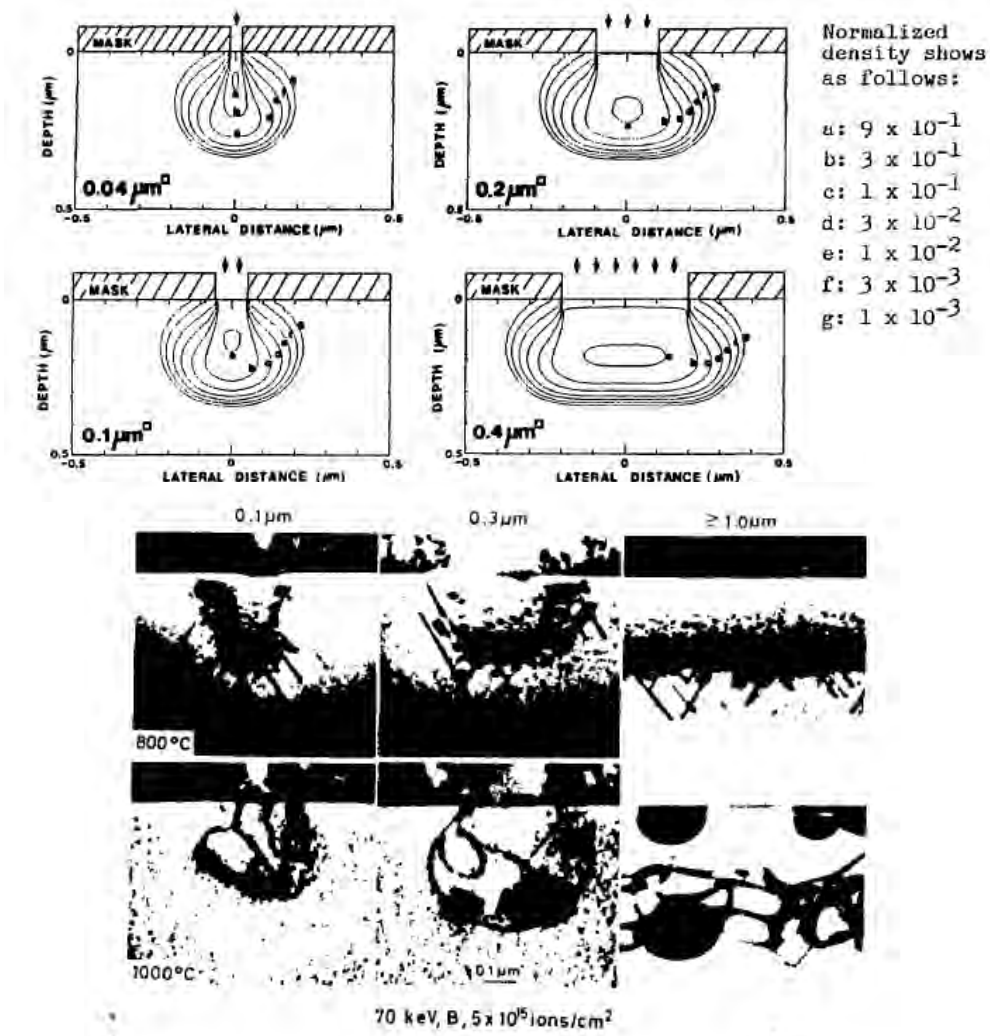
FIG. 7. Cross-sectional TEM images of ⟨110⟩-aligned *a*-Si lines in (a) (001) Si and (b) (011) Si after annealing at 900 °C for 6 min.



Karen Saenger /IBM JAP07

Edge Effects:1.2   Small mask opening effects

70 keV B^+



M. Tamura/Hitachi MRS89

For “small” (<ΔX> >> W_{mask}) mask openings,

1. Delivered dose below the mask decreases.

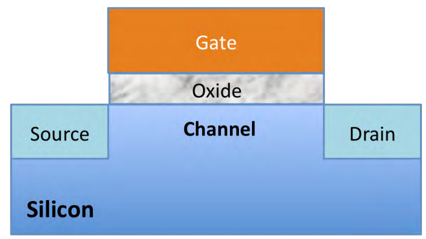
2. Peak of implant profile into the mask is shallower.

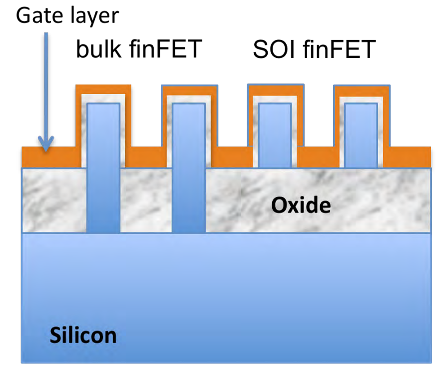
3. Dislocation networks are trapped below the mask (and do not anneal out).

After the Roadmap: Go vertical!

The transition from *planar* to *vertical* devices has been underway for over a decade.

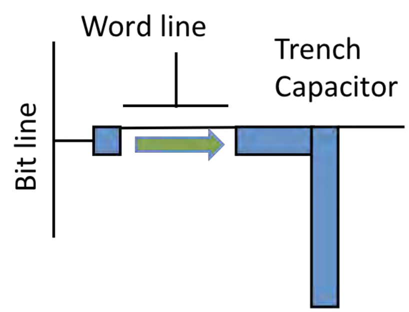
In **logic** devices, the implementation is in the form of *finFET* transistors in bulk-Si and SOI.



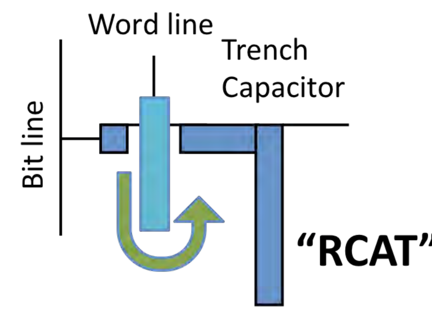


In **DRAM** devices, the implementation is in the form of *recessed channel gates* in array transistors.

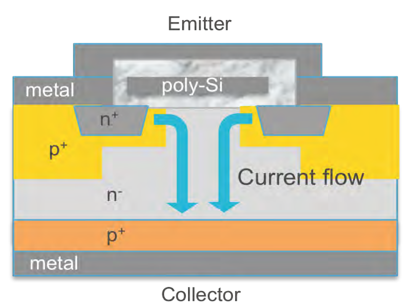
Planar Access Transistor

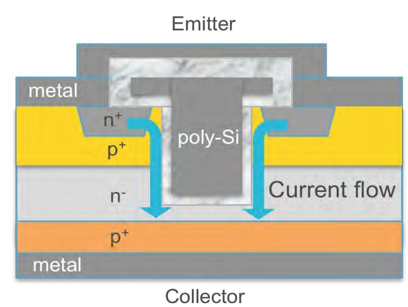


"Recessed Channel" Transistor



In **power switches**, the implementation is in the form of trench-based IGBT devices; "*trenchMOS*", etc.





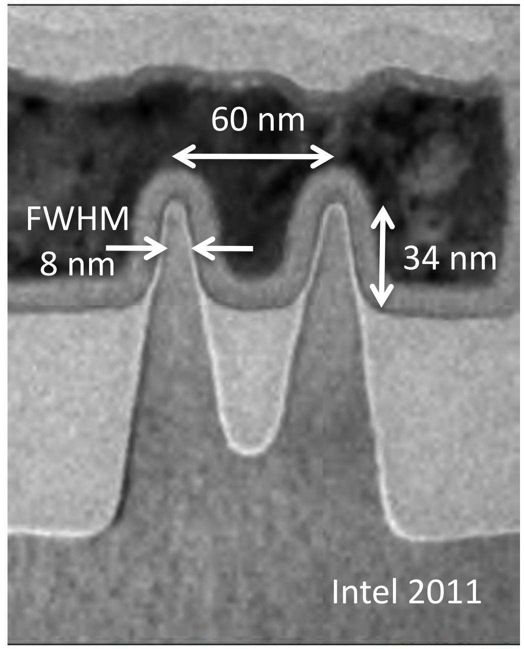
Intel finFETs

Note:
For a fin width of ≈6 nm, the 14 nm Intel fin channel meets the formal definition of a ***2D quantum confined structure*** in Si.

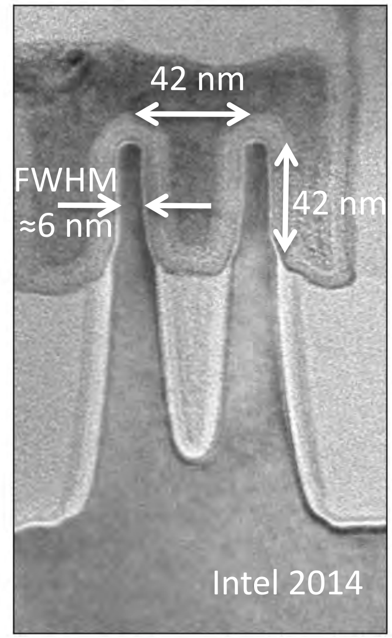
Dimension ≈ exciton radius

$$w_{fin} \approx a_{Bohr} = 5 \text{ nm}$$

Expect quantum driven changes in band gap, density of carrier states, etc.



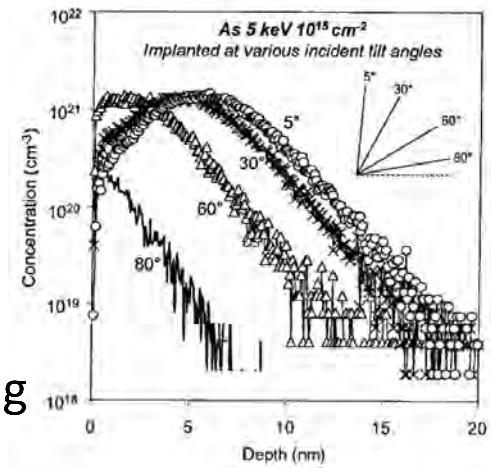
22 nm 1st Generation Tri-gate Transistor

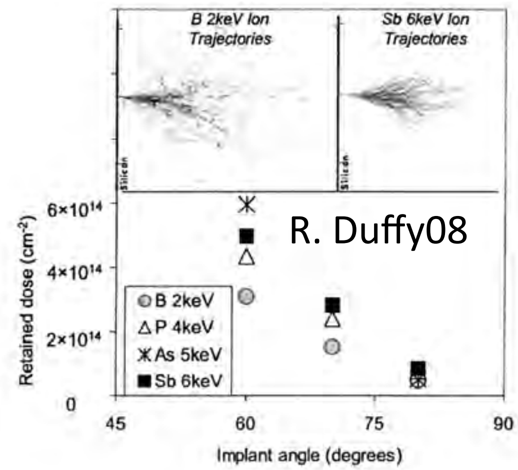


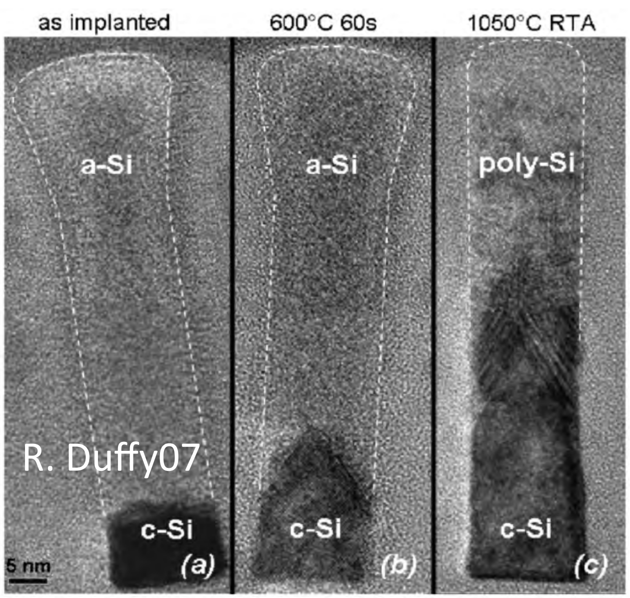
14 nm 2nd Generation Tri-gate Transistor

Edge Effects:2 Vertical Fin Surfaces

Dose incorporation:
Glancing angle implants are limited by ion reflection and sputtering.
Damage:
If entire body of the fin is amorphized, regrowth of c-Si during annealing is slow and imperfect.







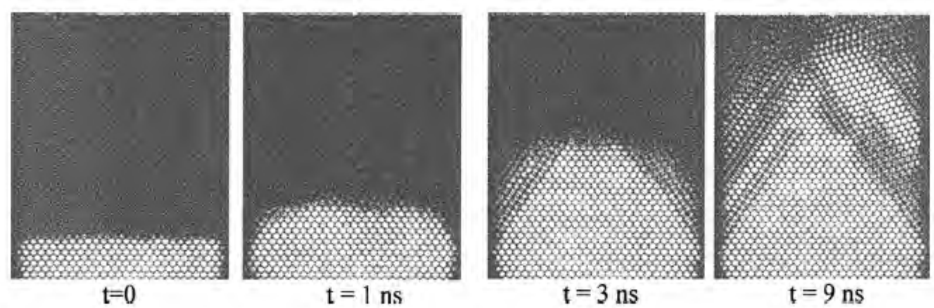


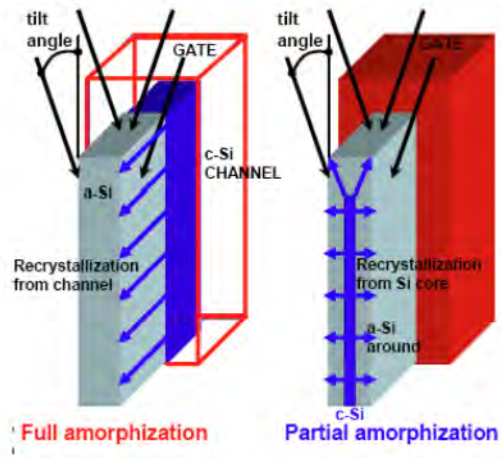
FIG. 6. Molecular dynamics simulations of the evolution of a 14 nm fin structure. A covering amorphous layer surrounds the Si fin. A crystalline seed is left at the bottom to promote solid-phase epitaxial regrowth. Poor regrowth causes {111} twin boundaries and polycrystalline Si.

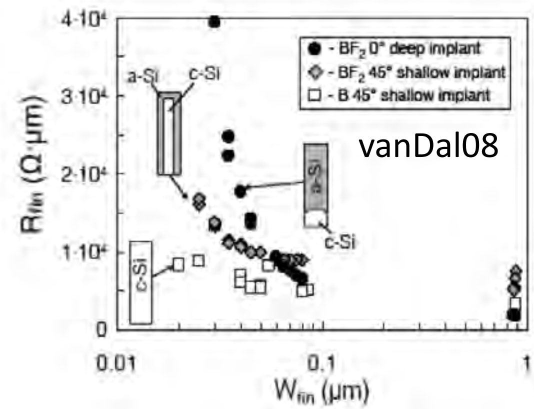
L. Pelaz09

How to avoid a-Si in a 6nm fin core?

$E_{ion} \approx 100$ eV ??

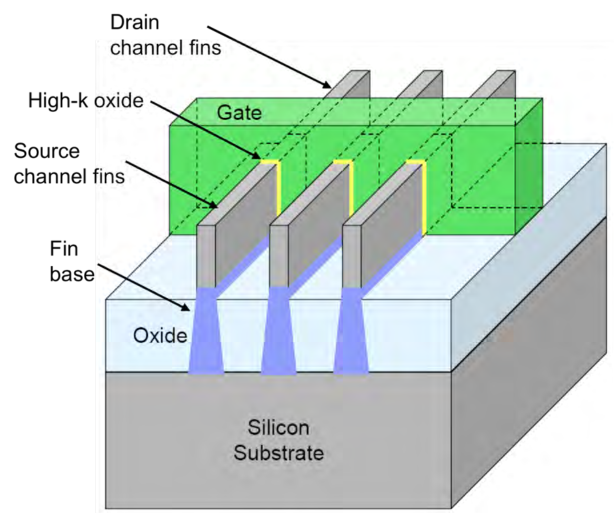
Low-energy & glancing angle implants can leave a central c-Si “seed” and lead to good dopant resistivity.

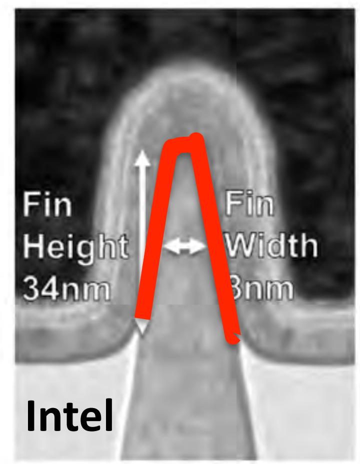




But:

To limit a-Si layer thickness to ≈2nm, B^+ ion energies need to be ≈100 eV or so.





How to Avoid Amorphous Fins?

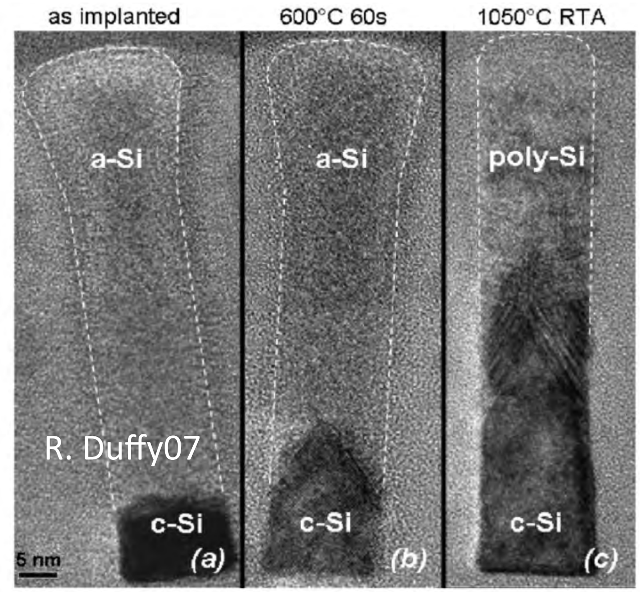
Try ***elevated implant temperatures***.

“Hot” implants has a long history:

1. 1970’s “dynamic annealing” implants
   (try to avoid separate anneals).

2. SIMOX (mid-80’s-early 2000s)
   Oxygen implants at ≈600 C
   (avoid to Si amorphization for SOI).

3. “Hot fins”.



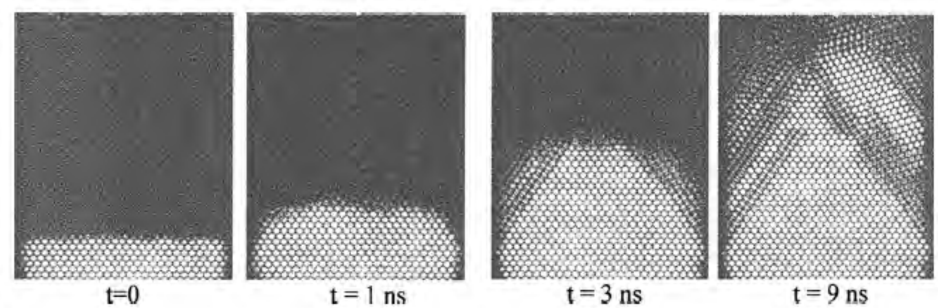


FIG. 6. Molecular dynamics simulations of the evolution of a 14 nm fin structure. A covering amorphous layer surrounds the Si fin. A crystalline seed is left at the bottom to promote solid-phase epitaxial regrowth. Poor regrowth causes {111} twin boundaries and polycrystalline Si.

L. Pelaz09

"Hot" Implants: *Decrease* damage accumulation

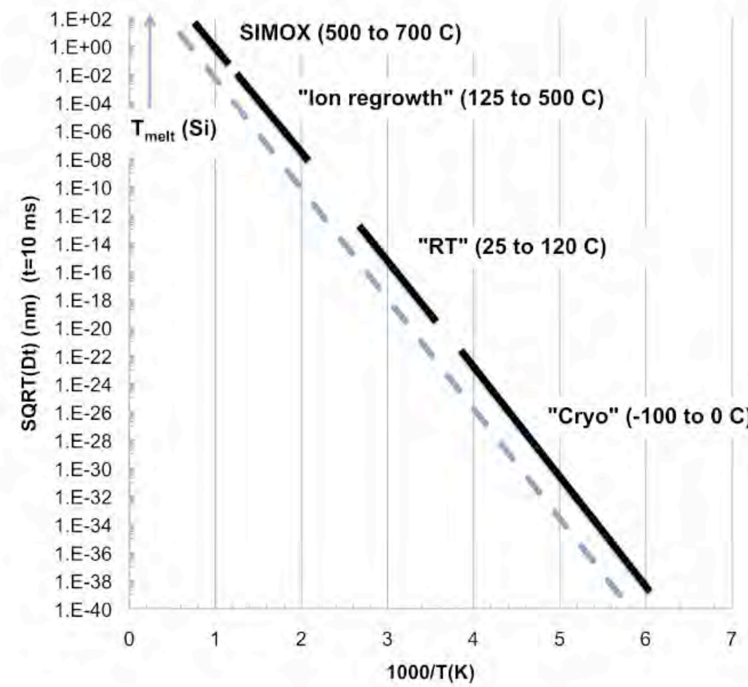
For "hot" implants, defect annealing occurs during the implant process. ***"Dynamic annealing"***

1. SIMOX: high-dose (≈10^{18} O/cm^2, ≈650 C)

2. "Hot fins" (≈10^{15} B or P/cm^2, ≈300 C)

3. Damage layer re-growth (≈10^{16} Ne/cm^2, ≈350 C)

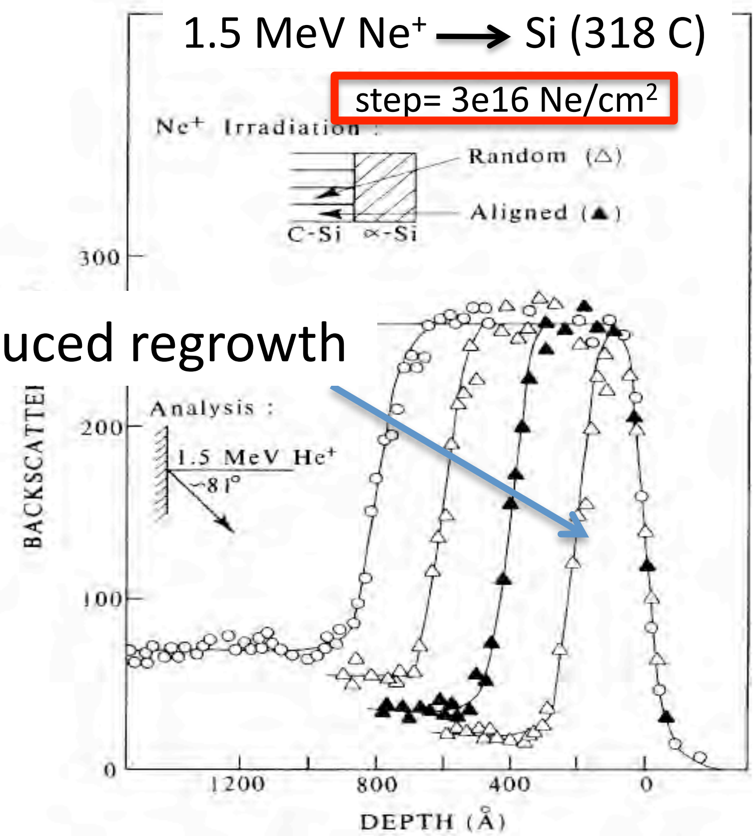
4. Device effects occur at 30 to 50 C.

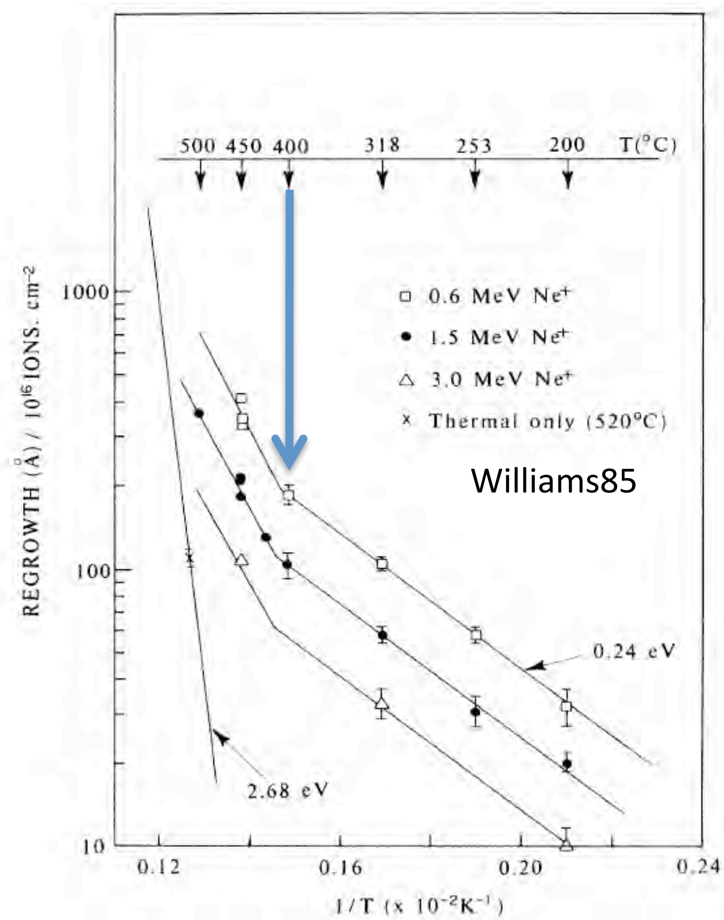


Ion-induced a-Si *Re-growth* at ≈320 C and higher

For Si at 200 to 500 C, high-dose, deep ions can *re-grow* a-Si layers.

Kinetics increases sharply >400 C.





"Hot" implants into thin-SOI layers

If high-dose implants result in completely amorphized thin Si on oxide (SOI), then no c-Si seed exists to provide good re-qrowth.

Similar to the finFET damage problem.

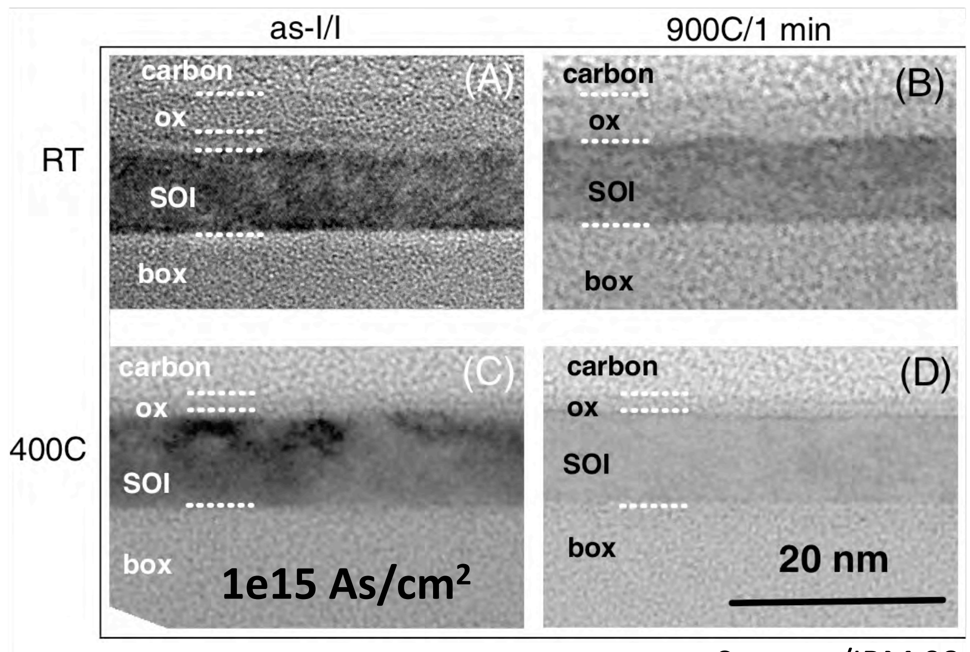
Implants at 400 C can result in "clean" TEM images after anneals...but....

1. Dopant activation not ideal
2. Recoil mixing at Si/SiO_2 interface pumps O into Si layer.

Hot implant defects need sophisticated analysis for activation, mobility and recombination effects.

Table II. Rs (Ω/sq) for 8 nm SOI samples implanted with various doses of 0.75 keV As^+.

Treatment	as-implanted		900 °C/1 min	
Dose/Implant Temperature	RT	400 °C	RT	400 °C
0.5×10^{15} /cm^2	36-45 k	6.2 k	2.3 k	2.1 k
1×10^{15} /cm^2	32 k	4.8 k	1.3 k	1.8 k
2×10^{15} /cm^2	52 k	4.0 k	800	1.7 k



Saenger/IBM 08

Residual Damage after "hot" implants

TEM images can see a-Si regions & strain-inducing defects (dislocation loops, 311s, etc.).

But not "point" (or small) defects.

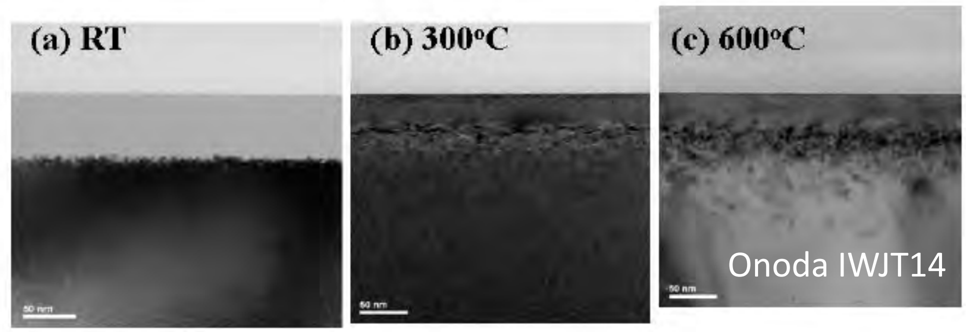


Fig. 3 Cross sectional TEM results of As^+ implanted at (a)RT, (b)300°C and (c)600°C.

Heated implants on "fat" (30 nm) fins show modest improvements in drive currents.

Is this worth giving up the COO economies of PR masking?

5 keV As, 1e15/45°
$T_{implant}$ = 500 C

n-finFET, Wfin = 30 nm

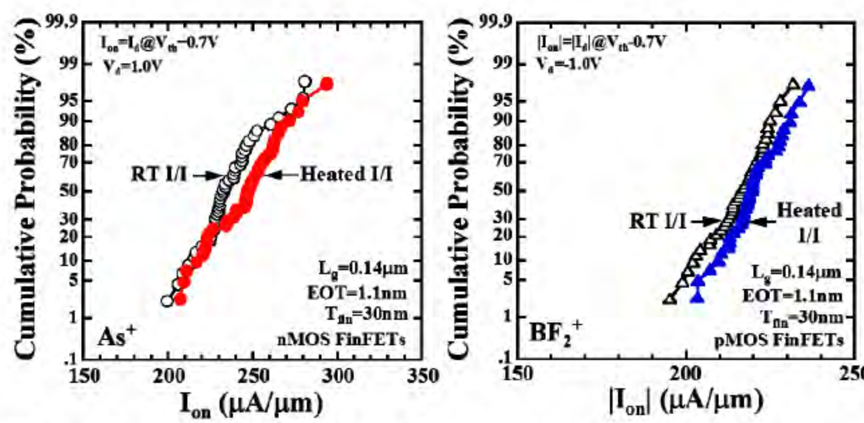


Fig. 13 Ion distribution in nMOS and pMOS FinFETs processed by room temperature or heated ion implantation. Onoda IWJT14

KMC Defect Models

Kinetic MonteCarlo models of implant damage and annealing suggest that there is ***a lot more going on*** with hot implants than reducing a-Si formation.

Hot implant effects:

1. Dopant out-diffusion.
2. {311} Si-rod defects at >400 C.
3. Twin defects formed at top of fin regions.

After anneal:

1. {311} defect growth.
2. Vacancy cluster growth for 400 C implant.

as-implanted

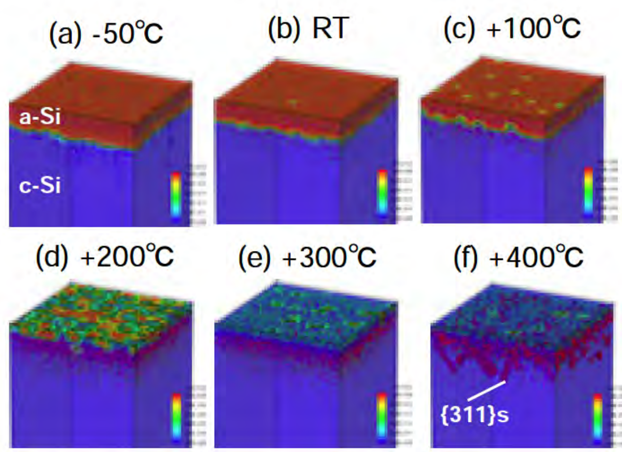


Fig. 3. KMC simulations for As 5keV implant with 6 different implant temperatures, (a) -50 ˚C, (b) Room Temperature (RT), (c) 100 ˚C, (d) 200 ˚C, (e) 300 ˚C, and (f) 400 ˚C, respectively. As implant temperature is increased, the depth of the amorphous-Si layer is reduced. {311} defects are formed during implant at higher implant temperature.

after anneal

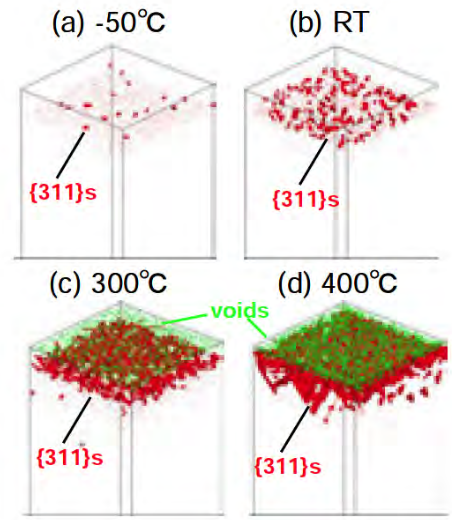
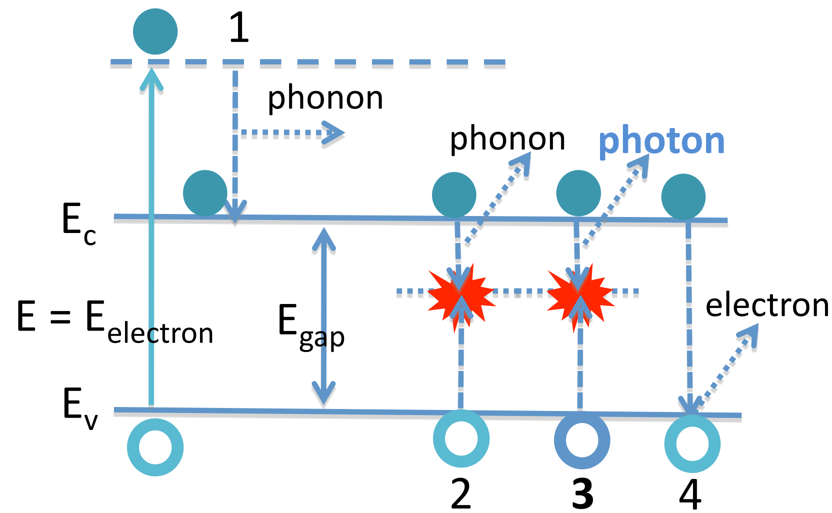


Fig. 4. KMC simulations of defects for As 5keV implant and low temperature SPER with different implant temperatures , (a) -50 ˚C, (b) Room Temperature (RT), (c) 300 ˚C, and (d) 400 ˚C, respectively. As implant temperature is increased, residual {311} defects are increased and elongated. Void (vacancy clusters) is also increased at high implant temperature.

Noda IEDM13

Cathodoluminesce

Probe: ***Electrons***
Interaction: Carrier recombination
Signal: Photons



Excitation, diffusion and recombination of carriers is similar to photo-reflectance (“Therma-Wave”, etc.)

Signal now is direct emission of PL photons during defect-assisted recombination.

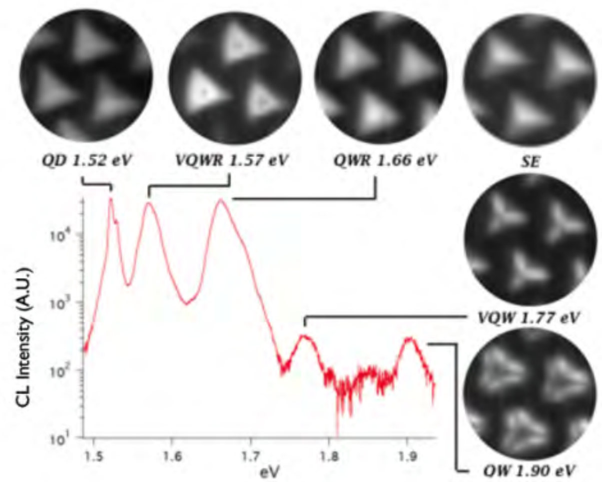
Competing mechanisms are:
1.Non-radiating recombination
(SRH: Shockley-Read-Hall)
3. Auger excitation of Si atoms
(with internal emission of an electron).

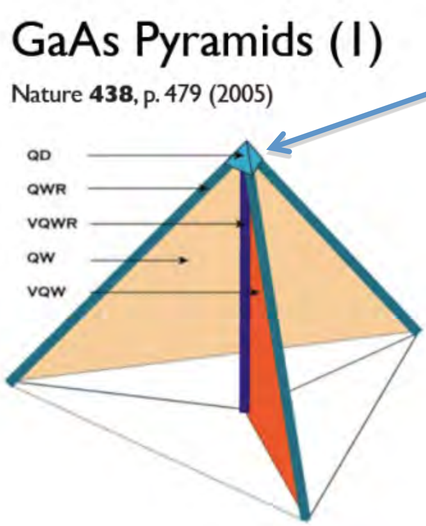
Transitions: Excitation ($E>E_{gap}$)
1. Fast relaxation (phonon)
2. SRH recombination (phonon)
3. **Cathodoluminesence (photon)**
4. Auger (electron)

Cathodoluminesce: GaAs nano-dots &wells

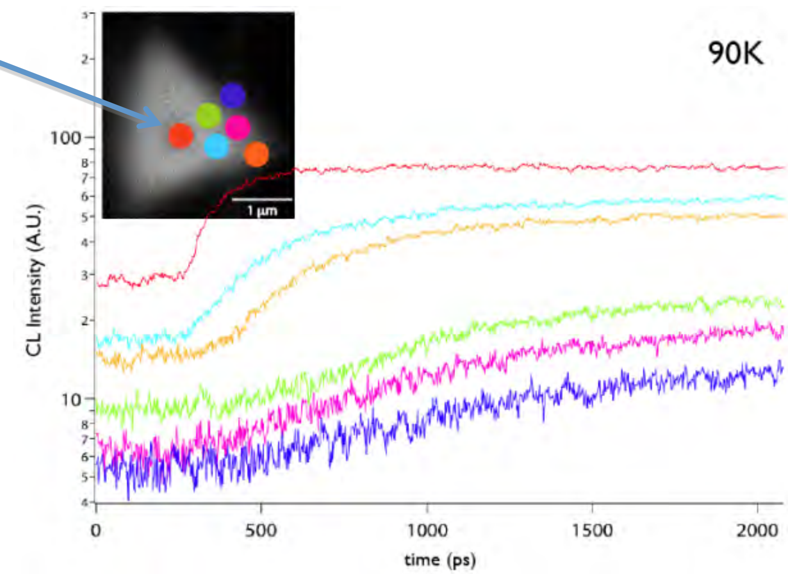
Carrier confinement ("quantum wells") can be localized to various structures in nano-scale semiconductors.

GaAs example has QW regions along ridges, vertical planes and at the "dot" at the top of the pyramid. Band structure variations and carrier diffusion leads to different light emission and response times.





"dot"



Summary

Damage accumulation and ***edge effects*** *combine* to leave *net residual damage* in both planar & vertical structures.

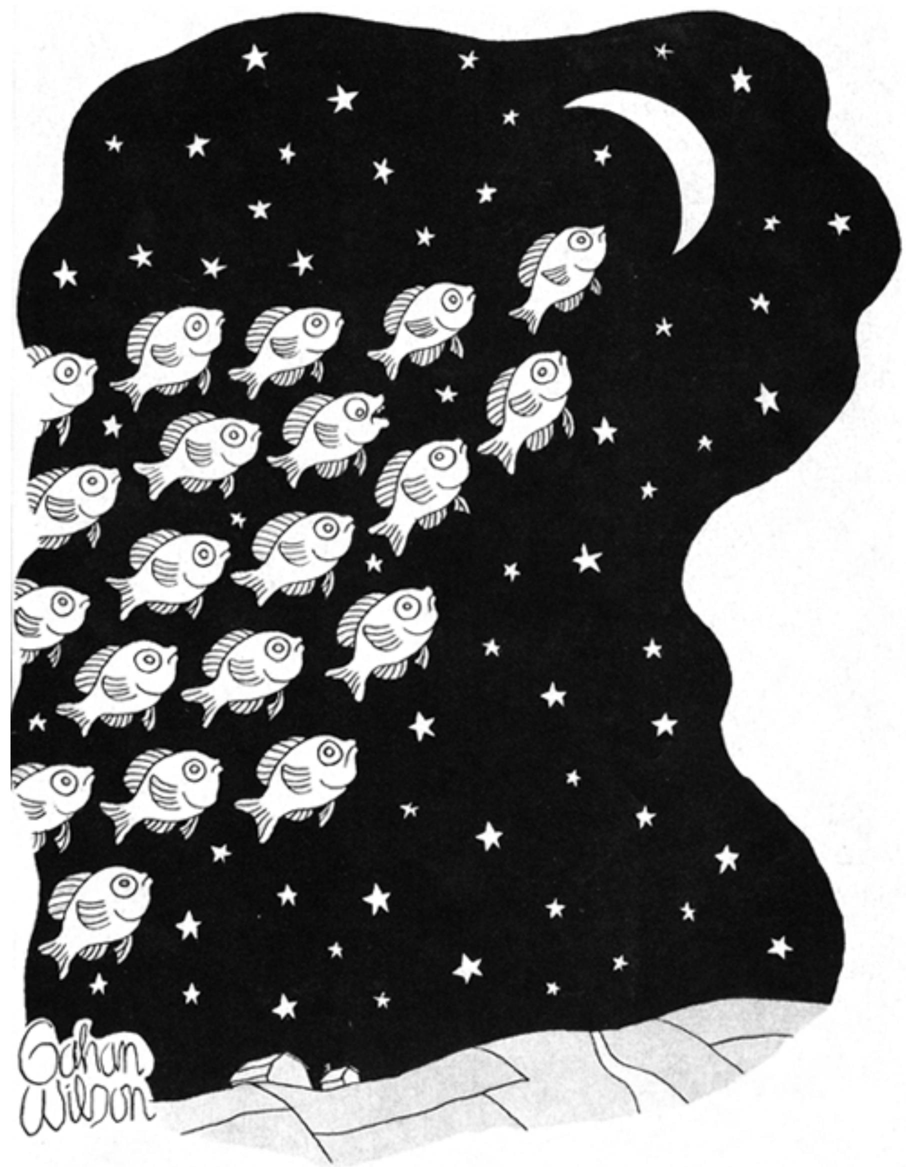
Edge effects in planar & fin structures are very different.

Device goals (as always):

Lower leakage current
Higher drive currents

In **planar** junctions:
Lower leakage/ higher I_{on} by ***maximizing*** implant damage accumulation (cryo, molecules, etc.).

In **fin** structures:
Lower leakage/higher I_{on} by ***minimizing*** damage accumulation in fin core (hot, recoil doping, diffusion doping, or ??).

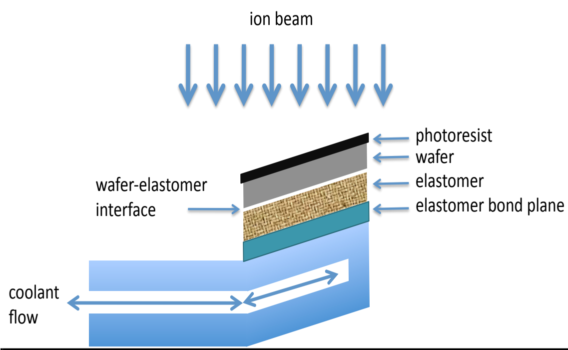


"I knew he was lost the moment we left the water."

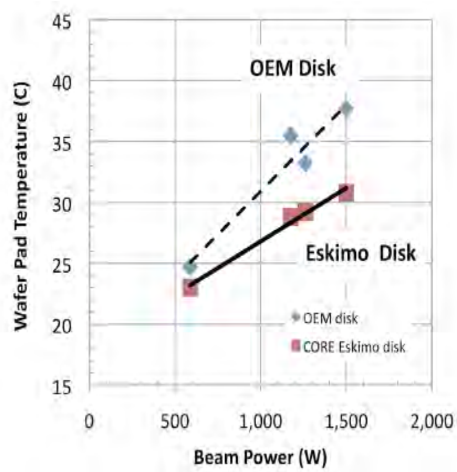
Device effects near room temperature !!!

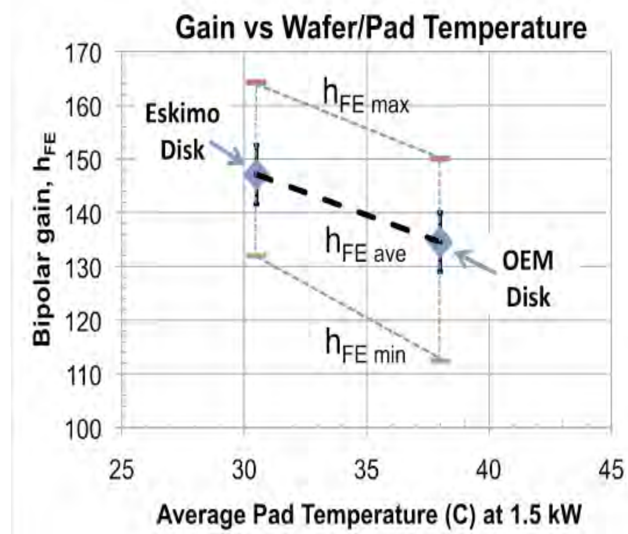
Systematic controls on wafer coolant temperature and improved heat transfer materials can control kW implant wafer temperatures to ≈30 C.

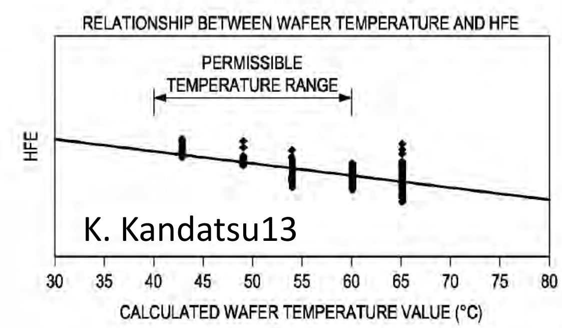
Cooler implants result in *improved* bipolar transistor *gain*.



Structure	Thickness (um)	κ (W/m-K)
Resist layer	1	0.2-0.3
Si wafer	725-775	149
Elastomer	75-300	0.4







Springer/ IIT14

Elastomers for Control of Wafer Temperature in the <50°C Range During High Dose Ion Implantation

Jeff Springer and **Walt Wriggins**, CORE Systems, Fremont, CA USA
Juergen Kusterer and **Karl Zotter**, Texas Instruments, Freising, Germany
Michael I. Current, Current Scientific, San Jose, CA USA

Recoil Implants for finFET Doping

Recoil mixing of surface dopant films gives:

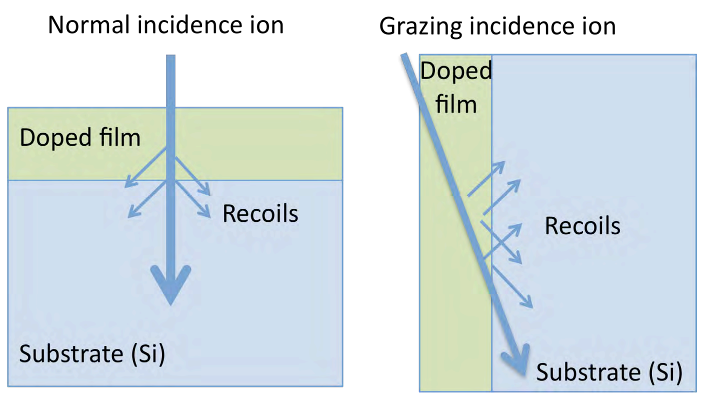
* High efficiency doping (recoils per ion)
* Shallow damage and doping profiles

Recoil mixing often used with PIII process.

The key to good delivered dopant dose control is to have a thin, conformal, uniform thickness dopant film with stable dopant concentration.

ALD is good for precision dep of thin films.

Grazing ion incidence results in a ***lot*** of recoils along the ion path.



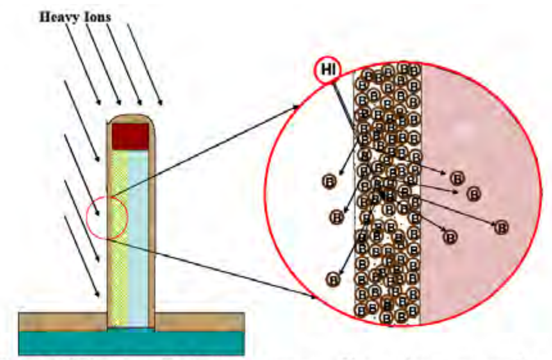
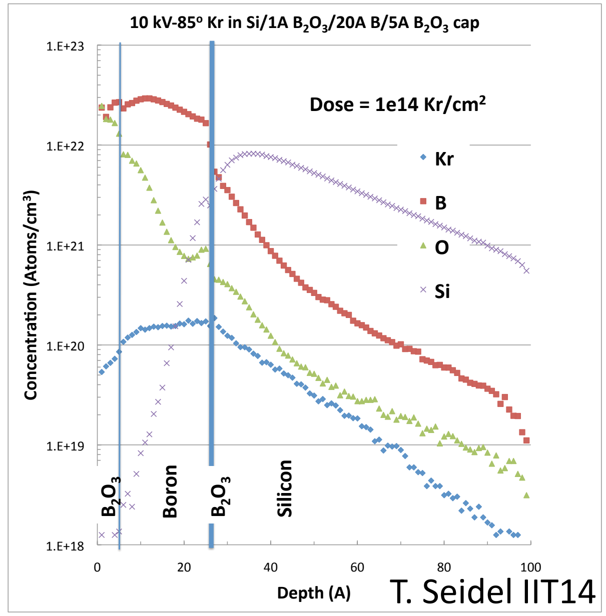
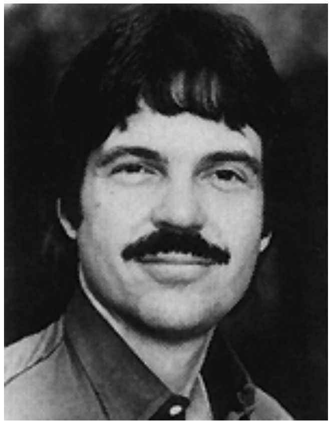


Fig. 1 MTI sidewall doping concept. Heavy ions are used to drive deposited boron atoms into the silicon crystal. The incident heavy ion stops inside the boron film or just inside the surface of the silicon.

G. Fuse SSDM10



T. Seidel IIT14



Food for thought….

- GUI (Graphic User Interface)
- Smalltalk
- Laptop computers
- Object oriented programming

"The best way to predict the future is to invent it."

Alan Kay, Xerox/PARC ~1971-81.

"Don't worry about what anybody else is going to do…
The best way to predict the future is to invent it.
Really smart people with reasonable funding can do just about anything that doesn't violate *too many* of Newton's Laws!"

But, getting ideas is the easy part.....

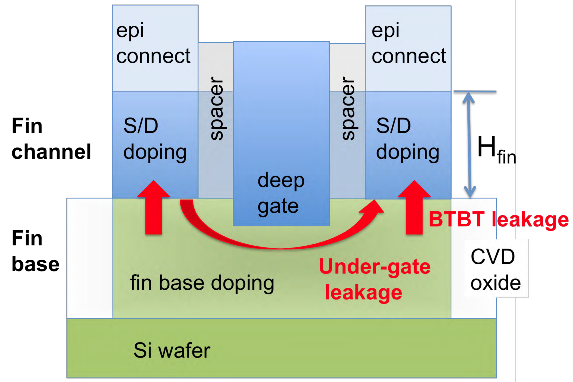
"Getting the ideas is easy . . . the hard part is hitting one key at a time."

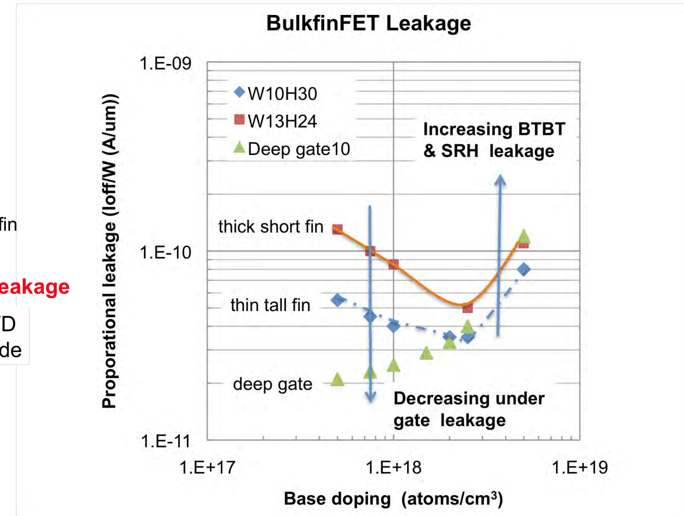
currentsci@aol.com

Bulk finFET Base Doping

Bulk finFET base doping is critical for leakage current.

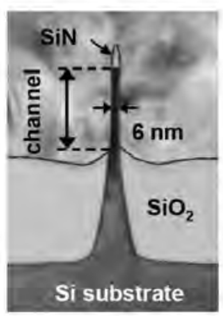
* **Too low** base dope: *Under-gate current flow*
* **To high** base dope: *Junction tunneling*

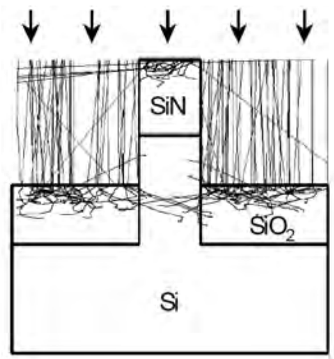




Numerous fin base doping methods have been reported.

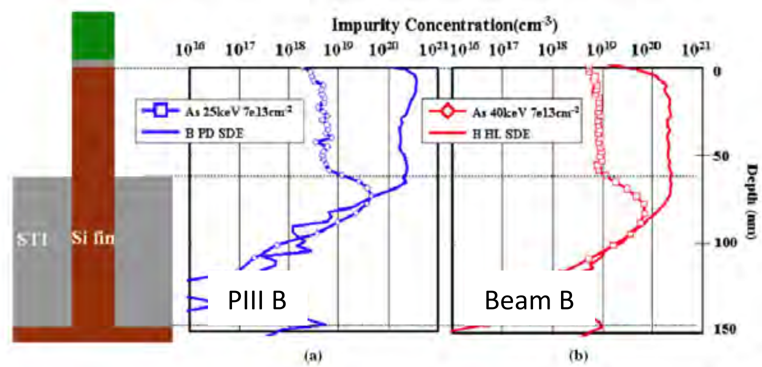
Lateral straggling doping





H. Kawasaki07

High-energy (<X>≈fin channel) doping



T. Izumida11

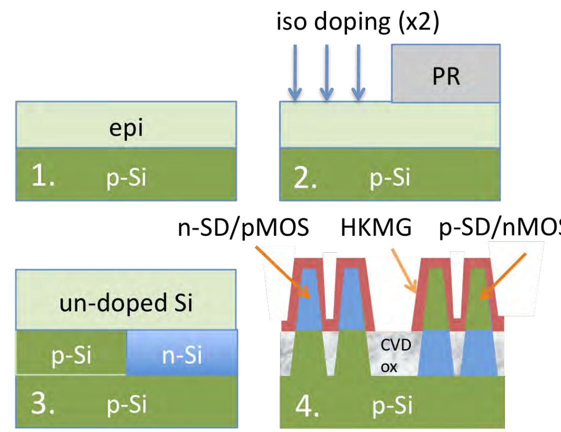
Bulk finFET Doping

* Bulk fin base doping can be done with good dose controls when combined with 2 (undoped) epi steps.

•SD doping, contacts and extensions, are done later with conformal methods.

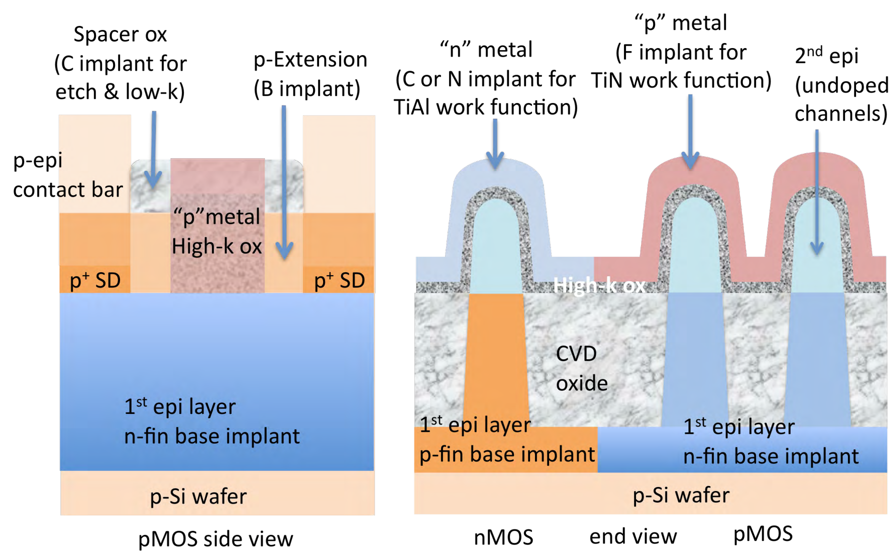
Note: finFET channels (under HKMG) are best left *un-doped* for high mobility & good Vth controls.

1. Epi dep for fin base
2. **Planar implant** for base doping then
3. Epi dep for fin channel
4. Fin etch
5. CVD ox dep for base iso
6. Gate HK ox and metal dep
7. Gate etch & spacer formation
8. **Conformal implant** for SD extension & contacts
9. Epi dep for SD contact & fin connects



Other finFET implants include:

1. *C implants into spacer* to change local plasma etch rate and dielectric constant.
2. Implants to *adjust* the *work functions* of metal (TaAl, TiN, etc.) gates with N^+, Al^+, La^+, etc.



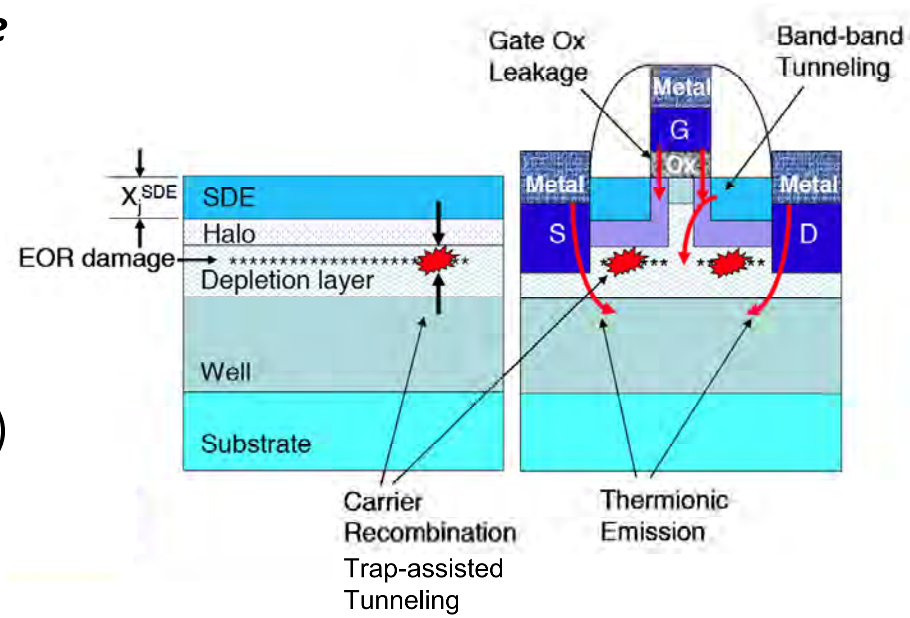
Junction Leakage Current Controls

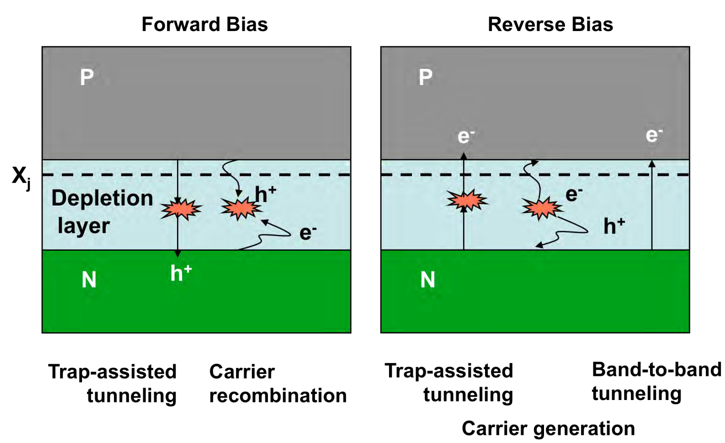
With the use of HKMG stacks, ***junction leakage*** dominates transistor off-power loads.

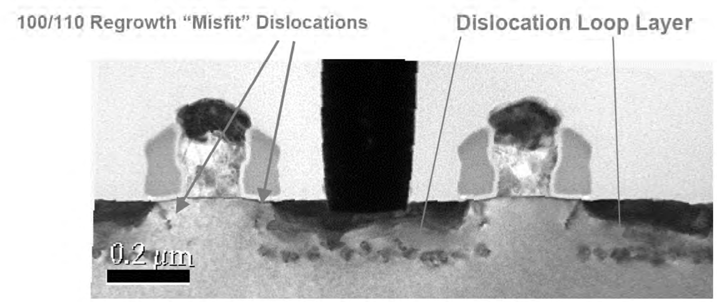
Junction leakage mechanisms:

1. Carrier recombination/generation (SRH)
2. Trap-assisted tunneling (TAT)
3. Band-to-band tunneling (BTBT)
4. Thermionic emission (from metal contacts)

Defect-driven leakage (SRH, TAT) can be controlled by implant/anneal process.







XTEM Pentium Transistors (Courtesy of Intel)