# FinFET Doping Options at 22nm, 14/16nm and 10nm Nodes

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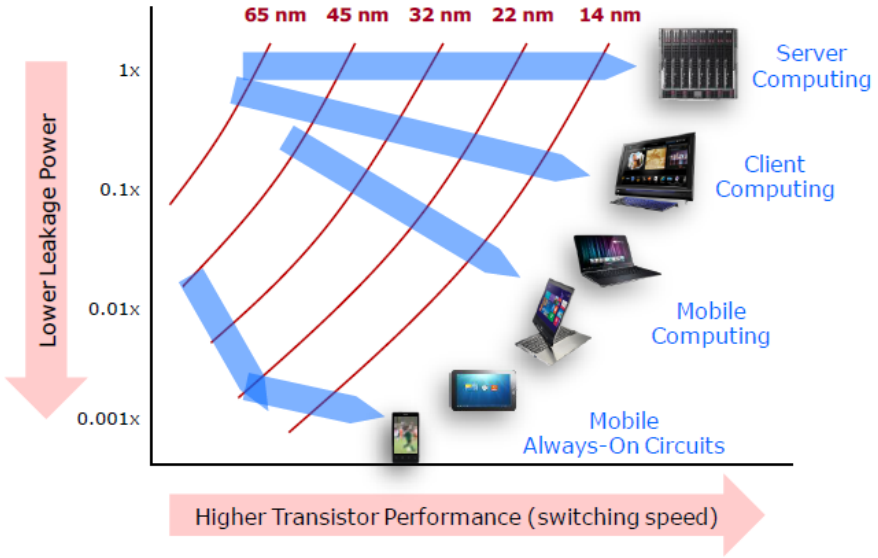
J.O.B. Technologies
AVS-WCJUG Meeting
Oct. 14, 2014

# Outline

- Introduction
  - Internet of Things driving Mobile Device Market (low leakage and long battery life for always “ON” devices)
  - Device Roadmap Planar-bulk→bulk-FinFET→Nanowire
- 22nm Node: Bulk-FinFET
- 14/16nm Node
- 10nm Node: High mobility SiGe or Ge Fin/channel Formation
- Summary

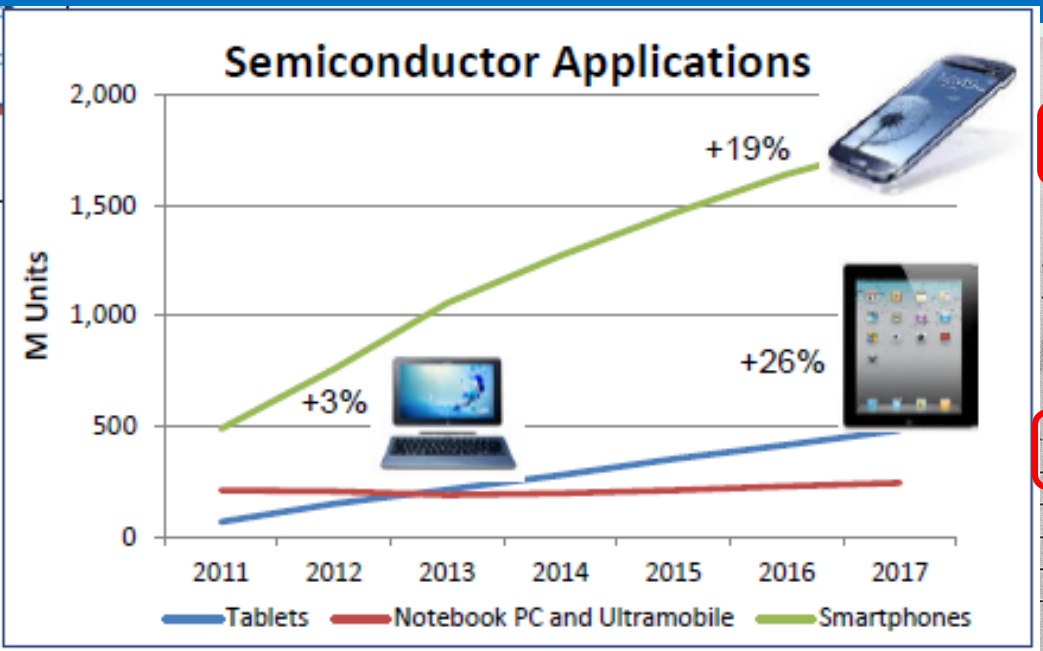
# Transistor Performance vs. Leakage




Q2/14 smartphone=301.3M units!

| Operating System | 2Q14 Shipment Volume | 2Q14 Market Share | 2Q13 Shipment Volume | 2Q13 Market Share | 2Q14/2Q13 Growth |
|---|---|---|---|---|---|
| Android | 255.3 | 84.7% | 191.5 | 79.6% | 33.3% |
| iOS | 35.2 | 11.7% | 31.2 | 13.0% | 12.7% |
| Windows Phone | 7.4 | 2.5% | 8.2 | 3.4% | -9.4% |
| BlackBerry | 1.5 | 0.5% | 6.7 | 2.8% | -78.0% |
| Others | 1.9 | 0.6% | 2.9 | 1.2% | -32.2% |
| **Total** | **301.3** | **100%** | **240.5** | **100%** | **25.3%** |

## *... To Support a Wide Range of Products*




Ref: Gartner Q3'13 – CAGR: 5 years 2012-2017

**TABLET AND MINI-TABLET SHIPMENTS**

| Worldwide | 2012 | 2013 | United States | 2012 | 2013 |
|---|---|---|---|---|---|
| Apple | 45.6% | 34.0% | Apple | 46.3% | 42.3% |
| SAMSUNG | 11.4% | 18.2% | SAMSUNG | 6.8% | 17.3% |
| Asus | 4.7% | 5.6% | Amazon.com | 18.1% | 11.9% |
| Amazon.com | 7.2% | 4.5% | Asus | 6.6% | 6.5% |
| Lenovo | 1.5% | 3.6% | E-Fun | 0.7% | 2.4% |
| Others | 29.5% | 34.2% | Others | 21.6% | 19.6% |
| **Total units** | 144.2M | 218.6M | **Total units** | **50.1M** | 54.9M |

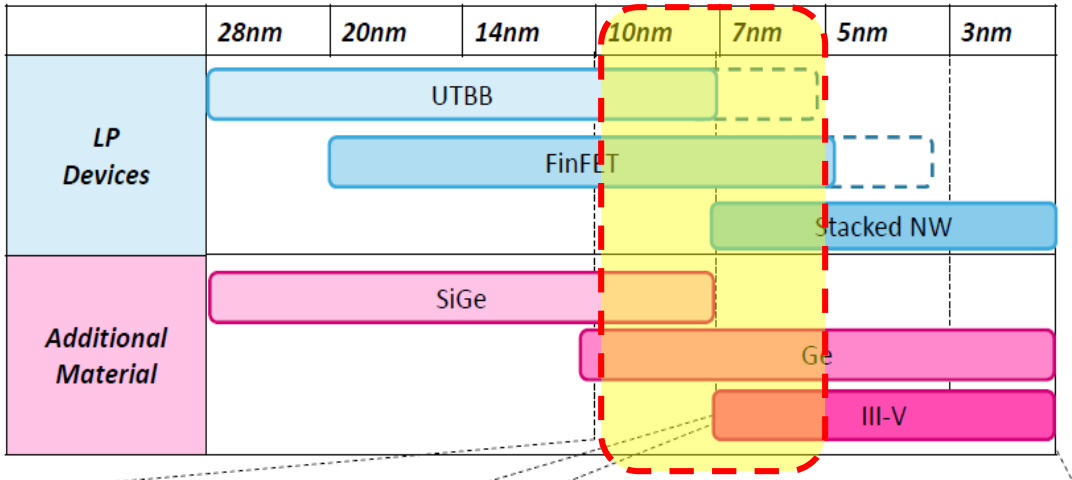
**SMARTPHONE SHIPMENTS**

| Worldwide | 2012 | 2013 | United States | 2012 | 2013 |
|---|---|---|---|---|---|
| SAMSUNG | 30.3% | 31.3% | Apple | 39.9% | 39.1% |
| Apple | 18.7% | 15.2% | SAMSUNG | 26.7% | 29.6% |
| Huawei | 4.0% | 4.8% | LG | 7.2% | 9.4% |
| LG | 3.6% | 4.7% | ZTE | 4.9% | 5.0% |
| Lenovo | 3.3% | 4.5% | Kyocera | 1.8% | 3.4% |
| Others | 40.1% | 39.4% | Others | 19.5% | 13.5% |
| **Total units** | 725.3M | 1.0B | **Total units** | 120.1M | 136.6M |

SOURCE IDC

## Conclusion






**Challenges at 10nm**

- « Conventional » boosters efficiency
- Variability sources (metal gate) for Vmin
- Low Parasitics

**Challenges at 7nm (and below)**

- Integration of new Device structure (SNW)
- Electrostatic control with new channel materials (s-Ge, III-V)
- Variability sources for Vmin < 0.5V

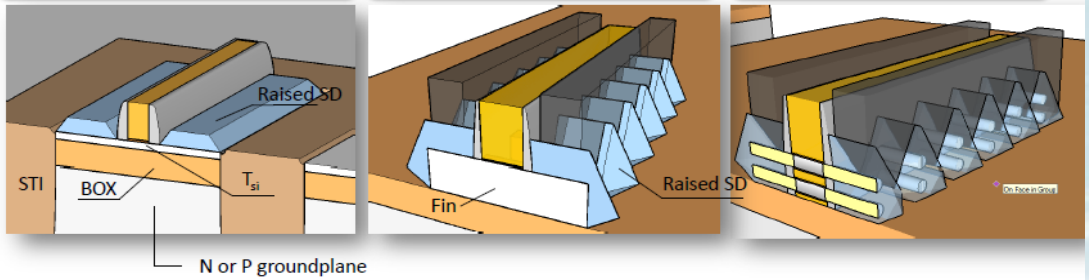
***2014: SiGe-FinFET at 14nm**
***2016: Ge-FinFET at 10nm**
***2018: Nano-wire at 5nm (Si, SiGe and Ge)**

IEDM-2013 short course

## Transistor Structure for 10nm and 7nm nodes



| UTBB<br>Ultra Thin Body & BOX | FinFET/Trigate | Nanowire |
|---|---|---|




- Undoped channel
- Back-gate control using thin BOX capacitive coupling
- Raised S/D

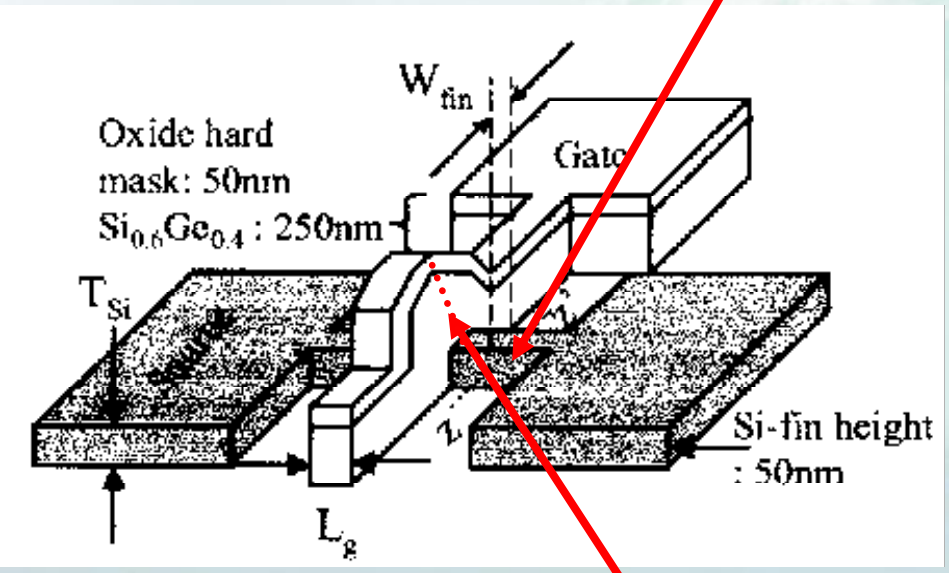
- « Vertical » double gate
- Undoped or doped channel
- Multi-Fin
- Raised S/D

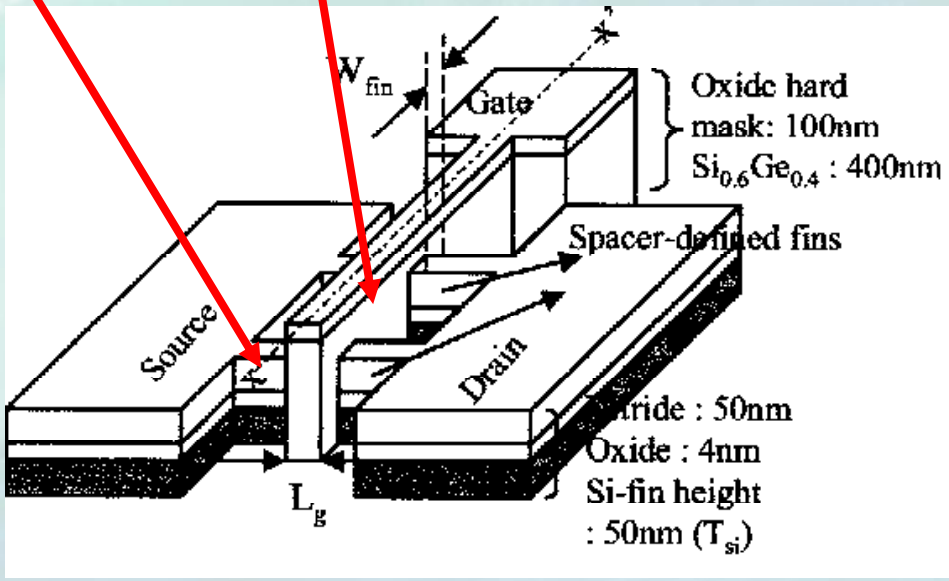
- Gate-All-Around
- Undoped channel
- Multi-wires
- Raised S/D

# Single & Multi-FINFET Double-Gate Devices

**Plasma Doping for Multi-FIN Gate/Poly**

**High Tilt Implant For LG-SS/D**




Y.K. Choi et al, IEDM-2001

**Asymmetric n+/p+ Poly/Gate**

Borland, Moroz, Iwai, Maszara & Wang, Varian/Synopsys/TIT/AMD/TSMC, **Solid State Technology, June 2003**

# FinFET Doping Options

3-D FinFET require some form of S/D extension doping under the side wall spacer for gate overlap control. Two basic method of doping are either:

- **Direct junction doping by implantation** with or without diffusion using:
  1)Beam-line tilted implantation for electrical conformal doping (JOB reported and Intel doing for 22nm FinFET)
  2)Plasma implantation for chemical conformal doping (IMEC reported not conformal)
  3)Plasma deposition followed by tilted beam-line knock-on doping (SEN reported)
- **Deposited doped layer** requiring lateral dopant diffusion using:
  1)Plasma deposition doping and diffusion (IMEC reported, limited by dopant solid solubility)
  2)Doped epi deposition and diffusion (IBM reported, limited by dopant solid solubility)
  3)Monolayer deposition and diffusion (Sematech/CNSE reported poor dopant solid solubility limited)

The problem with lateral dopant diffusion in crystalline-Si is the dopant activation level which will be limited by dopant solid solubility in silicon and therefore the peak annealing temperature. However, higher dopant activation can be realized at low temperatures if the junction is amorphous and recrystalized by using SPE (solid phase epitaxy) recrystalization of the junction as also shown in the data by Intel. Using **LPE** (liquid phase epitaxy) recrystalization or liquid phase dopant diffusion will result in the Highest Dopant Activation Efficiency as I reported EU-PVSEC-2012 by using laser-melt annealing. This is why monolayer doping and deposition doping will not be as good as implanted junctions provided the Right/Optimum implant condition is used. This means Hydrogen surface passivation for high enough retained dose and controlled amorphous junction depth <10nm.

# Outline

- Introduction
- 22nm Node: Bulk-FinFET
  - Intel's HP-logic FinFET, SRAM-FinFET and SOC-FinFET
- 14/16nm Node
- 10nm Node: High mobility SiGe or Ge Fin/channel Formation
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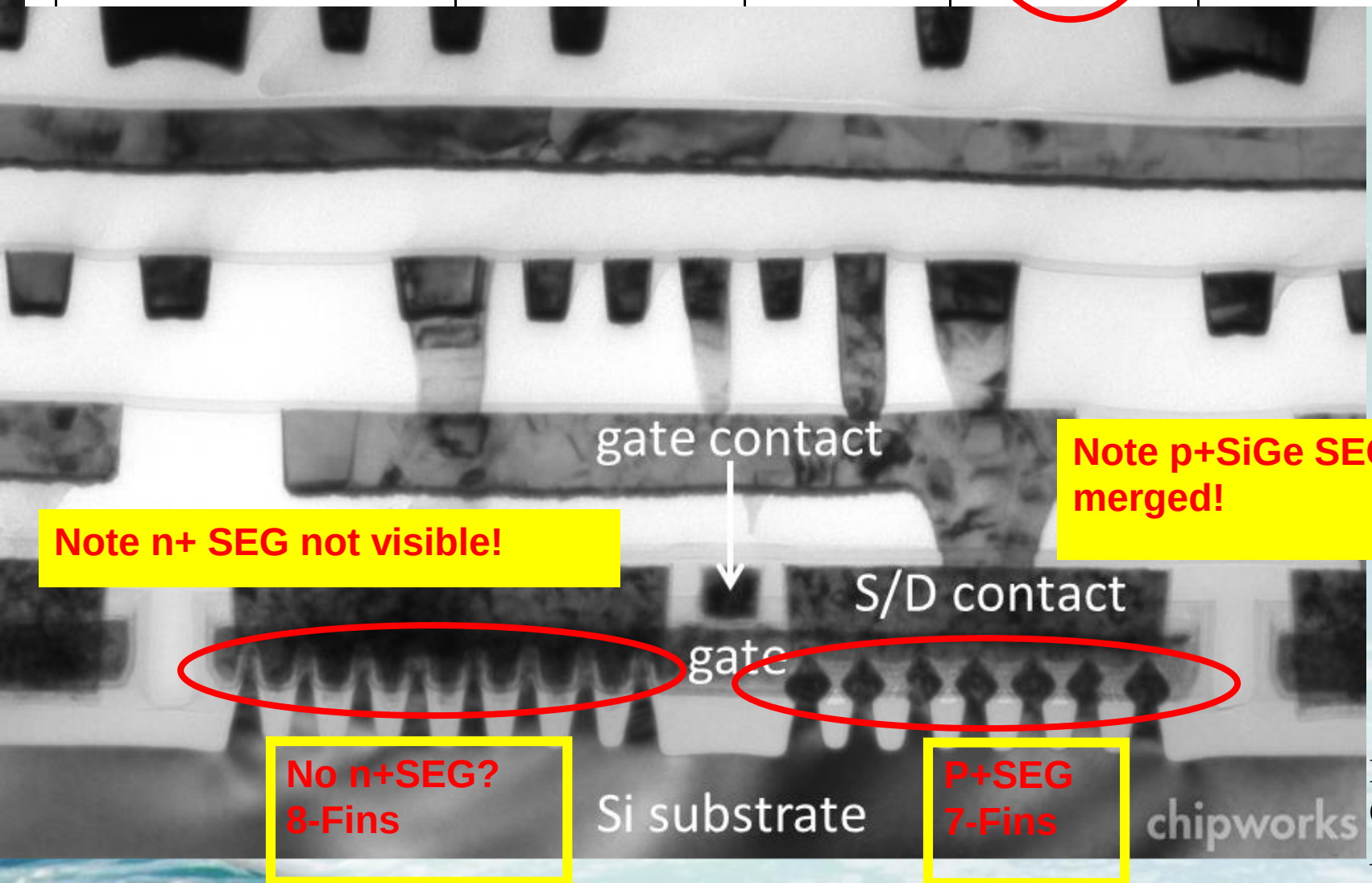
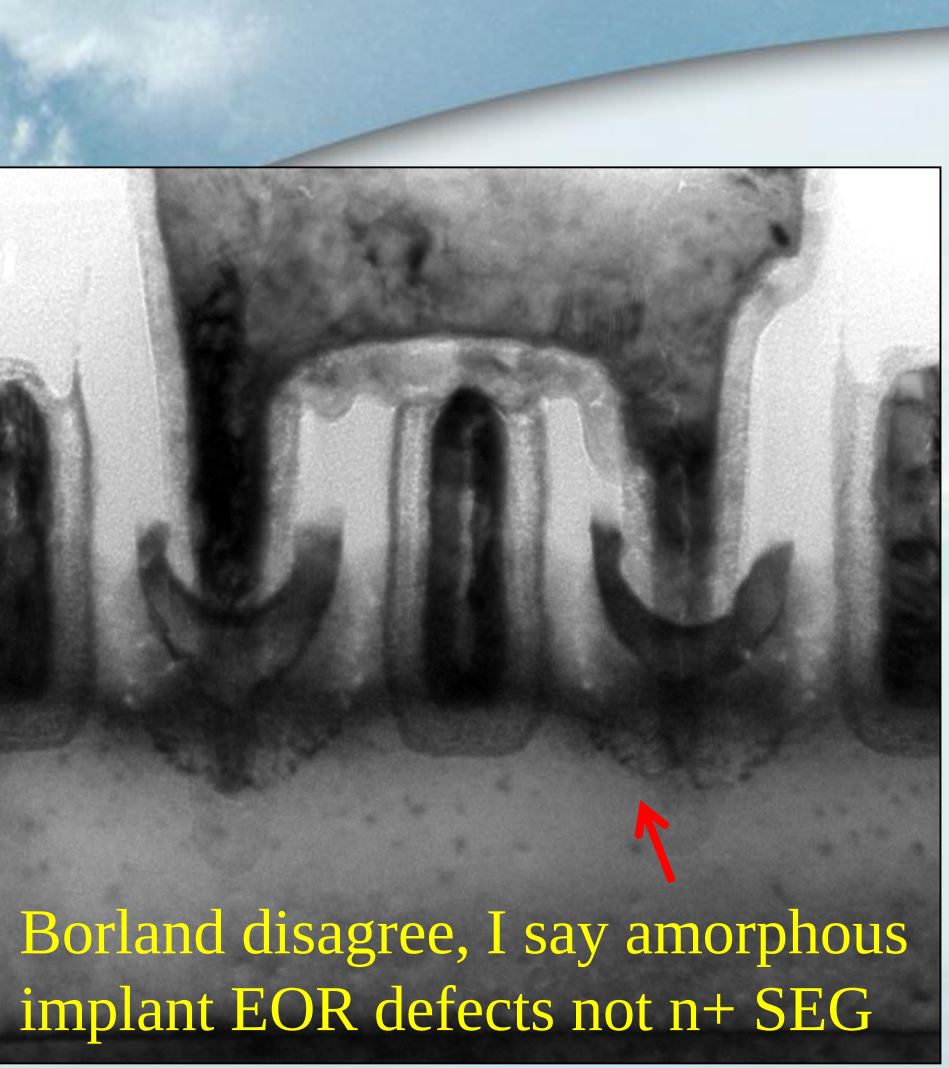
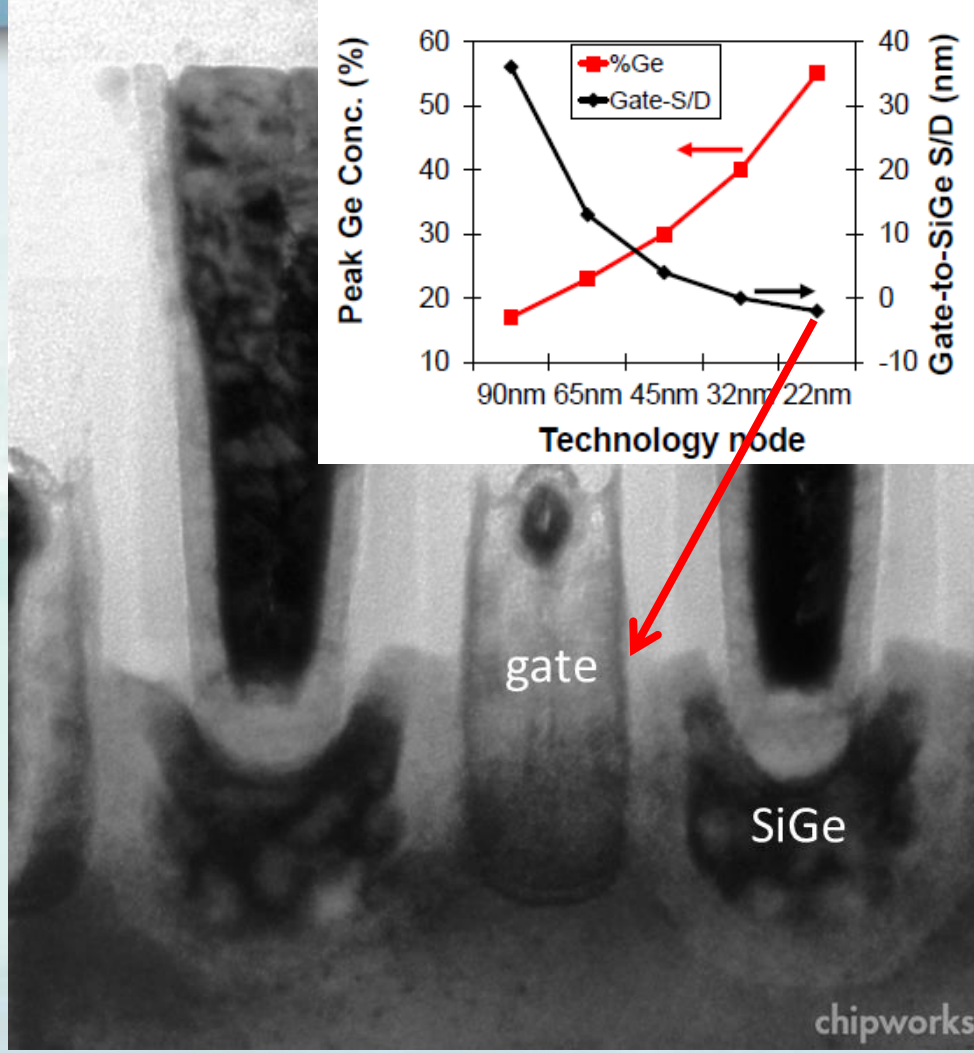
# 22nm Design Rules

| Layer | Dielectric | Pitch (nm) | Thick (nm) | Aspect Ratio |
|---|---|---|---|---|
| Isolation | -- | 60 | 100 | -- |




Dick James, Chipworks, April 2012




Dick James, X-TEM, Chipworks, April, 2012

**Intel 22-nm nMOS Epi or Not? To understand Intel's 22nm FinFET process details you must know what they did for 32nm planar!**

# Intel IEDM-2012 paper 3.1 on 22nm Tri-gate SoC Technology

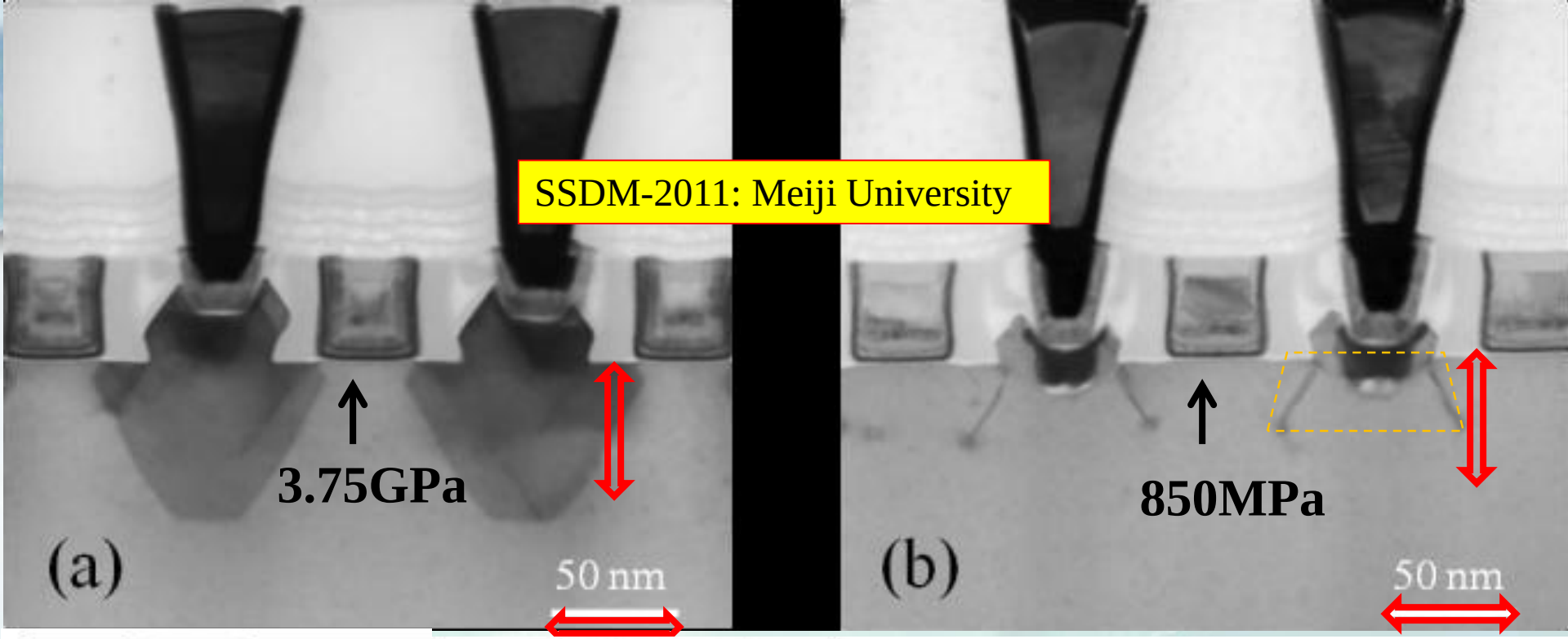
device and reliability targets, and is fabricated with an overall process sequence similar to the 32nm planar SoC technology, with the exception of the addition of fin-related diffusion fabrication [3].

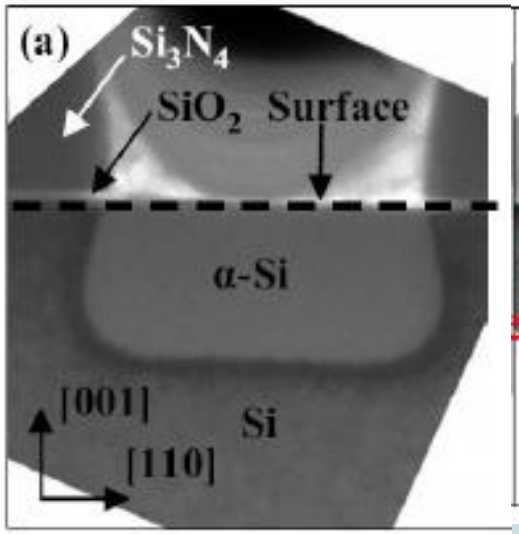
transistor pitch scaling. High Ge-embedded epitaxial SiGe technology is used for PMOS, raised S/D technology is used in NMOS, and fifth-generation strained silicon technology is used to provide compressive and tensile stress on P-ch and N-

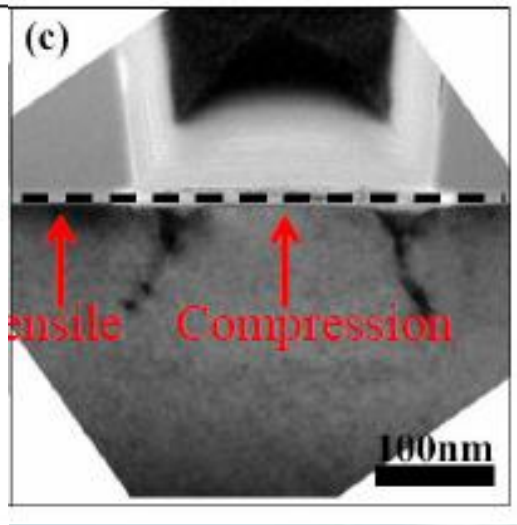
**Like for 32nm planar**

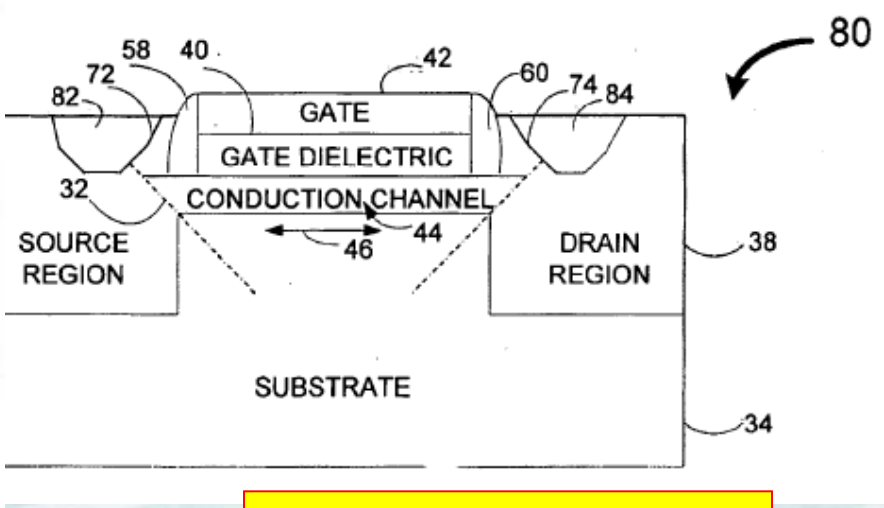
**-pMOS**: SDE-implant, S/D recess etch then eSiGe

**-nMOS**: SDE-implant, S/D -implant + amorphous Stacking Fault stressor and raised S/D epi



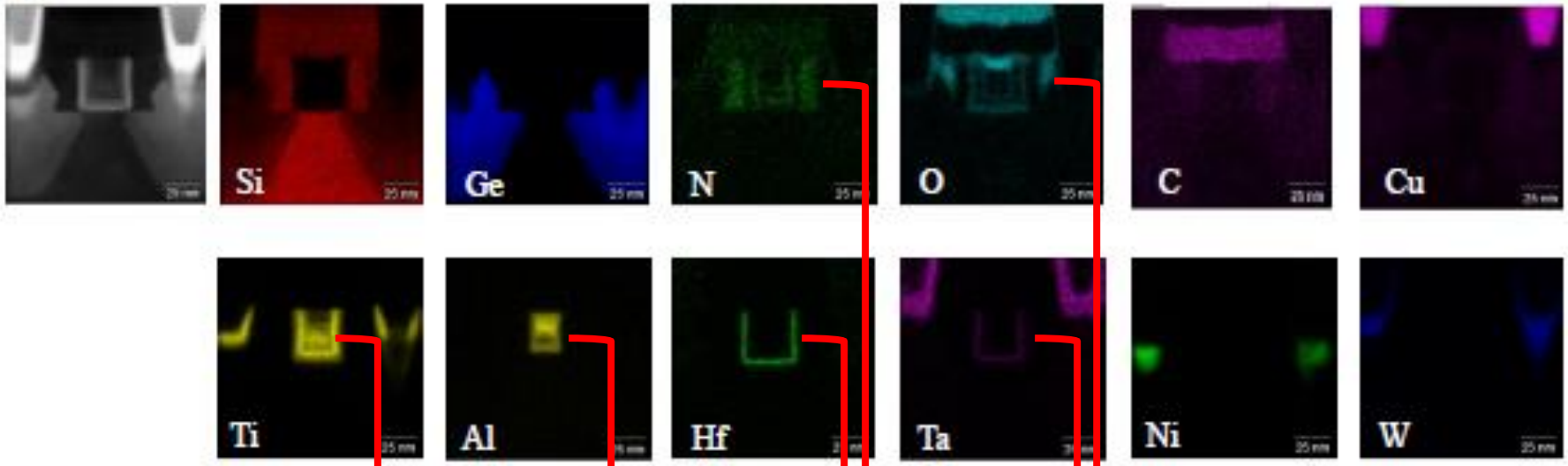




J.O.B. Technologies (Strategic Marketing, Sales & Technology)

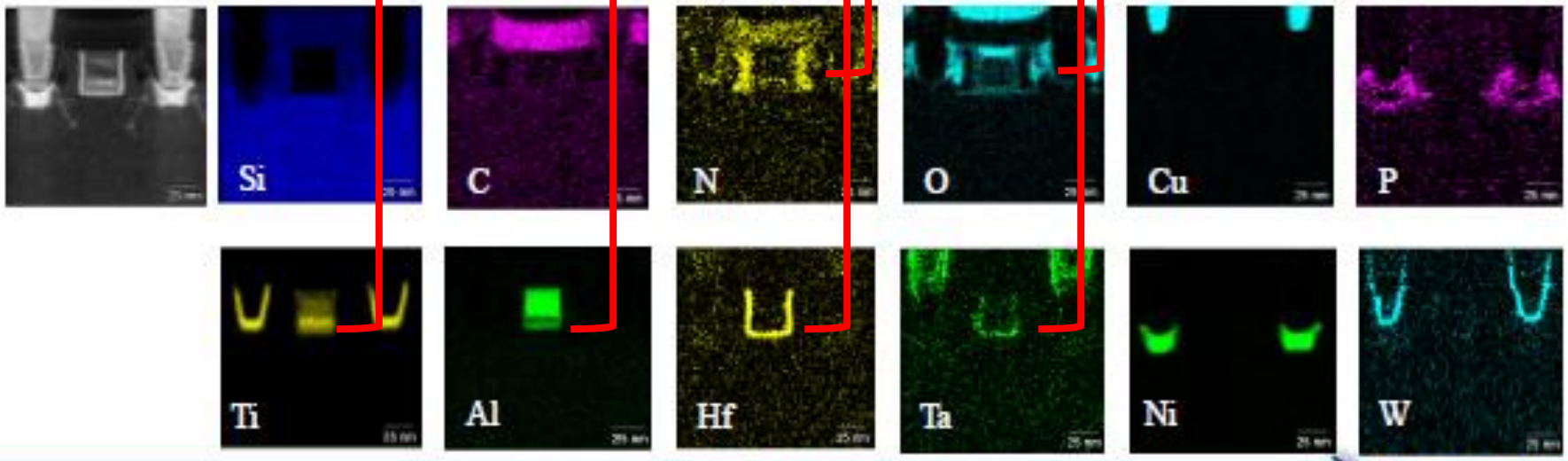
Uof FL 2008

Intel Patent Feb 8, 2010
Filed: April 14, 2008

(a) pMOSFET




(b) nMOSFET



# Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering

Jack Kavalieros, Brian Doyle, Suman Datta, Gilbert Dewey, Mark Doczy, Ben Jin, Dan Lionberger, Matthew Metz, Willy Rachmady, Marko Radosavljevic, Uday Shah, Nancy Zelick and Robert Chau

Components Research, Technology and Manufacturing Group, Intel Corporation,
Mail Stop RA3-252, 5200 NE Elam Young Parkway, Hillsboro, OR 97124, USA
Email : Robert.S.Chau@Intel.com

**VLSI Sym 2006**

TriGate FIN patterning is achieved using a reactive ion etching process, optimized to achieve highly vertical sidewall profiles for FIN. Following tip-extension implant and spacer formation we introduce selective silicon (NMOS) and embedded SiGe (PMOS) epitaxy for raised source/drains. Tensile strained nitride layers patterned over NMOS transistors are also investigated to enhance electron mobility [5].

The near mid-gap workfunction allows us to set the $V_T$ of the TriGate devices with a significantly lower dopant concentration ($10^{17}cm^{-3}$) in the channel as compared to the planar bulk Si technology. This in turn enables stronger gate coupling, improved channel mobility and volume

For PMOS Trigates we introduce in-situ boron doped SiGe raised source/drains as illustrated in x and y direction cross-sections of Figs.

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Marketi
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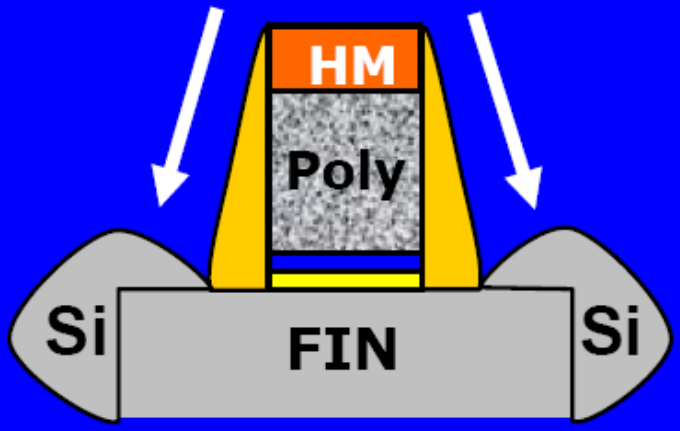
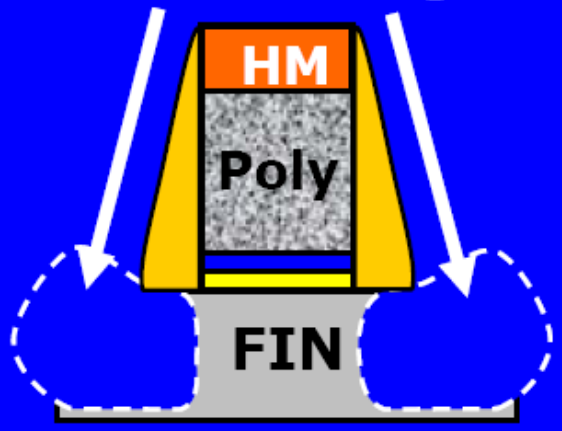
# Dual Epitaxial Raised S/D

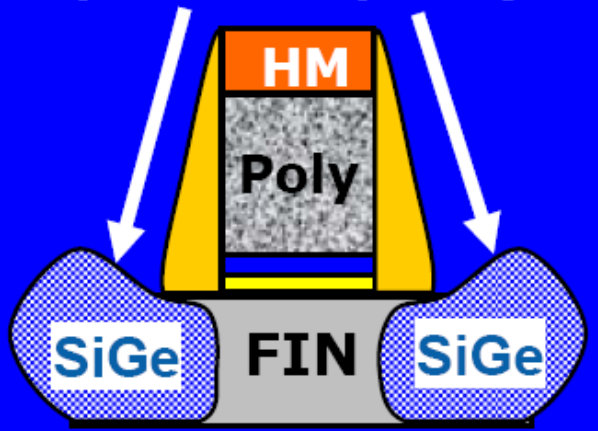
**Blanket Epitaxial Si Raised S/D Growth**

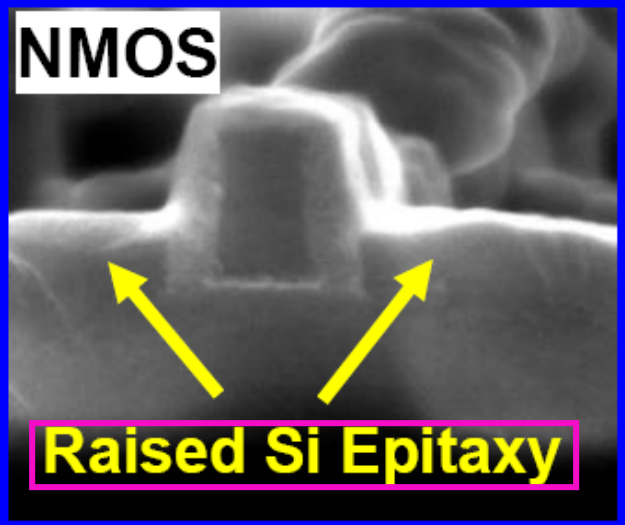


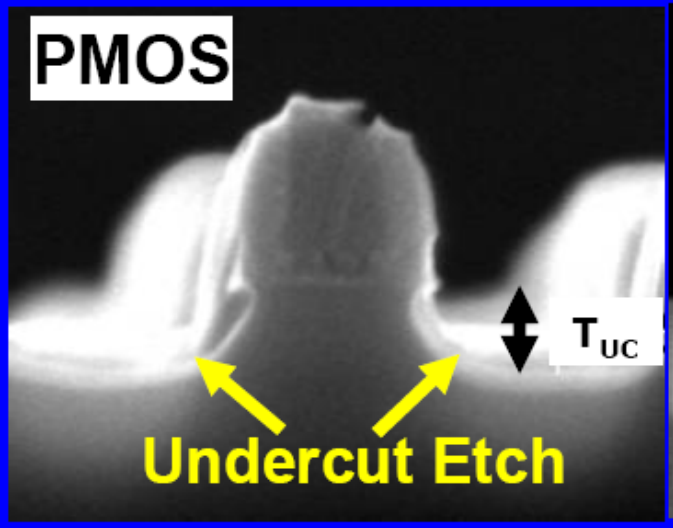

**Selective Undercut Etch PMOS regions**

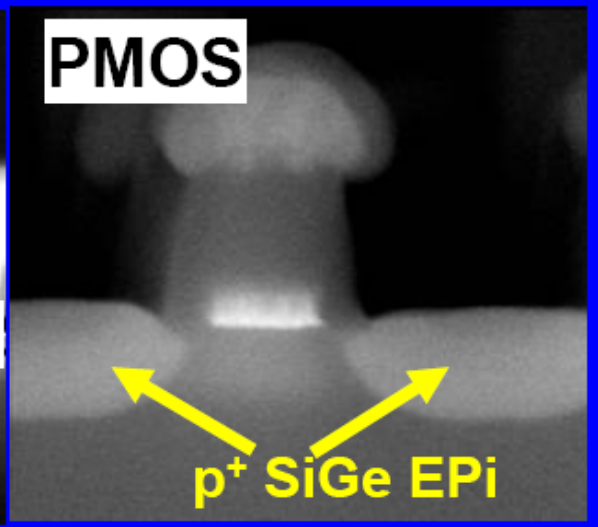



**In-Situ doped $p^+$ SiGe Epitaxy**

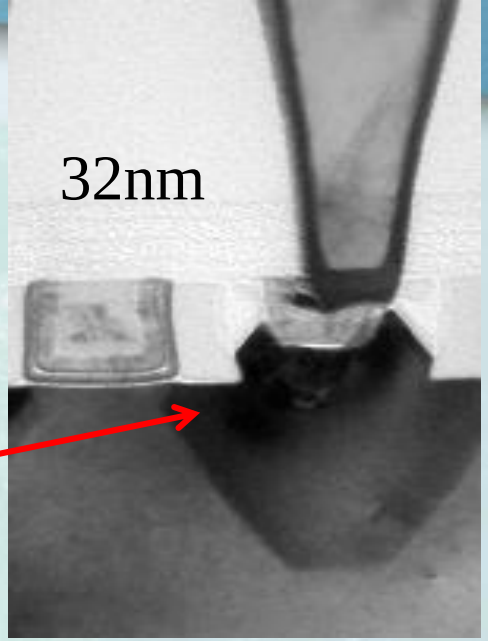


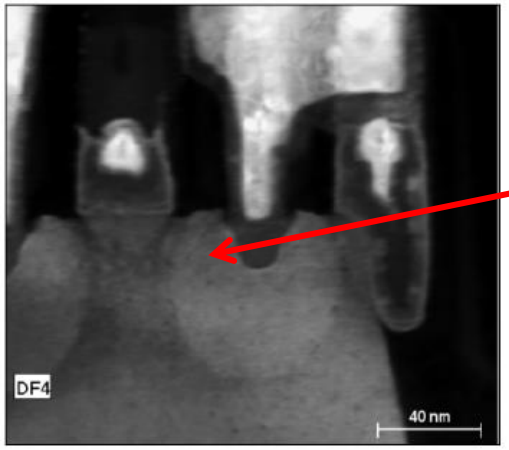



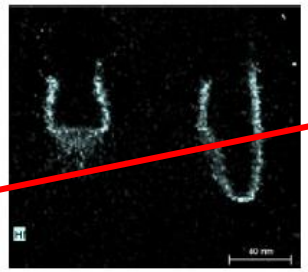



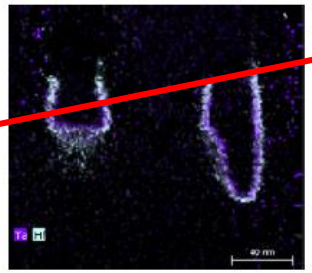



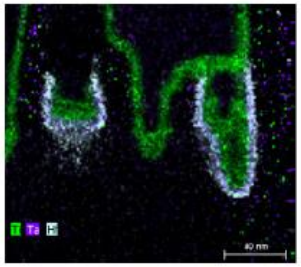
# Chipworks Teardown of Intel 22nm pMOS FinFET

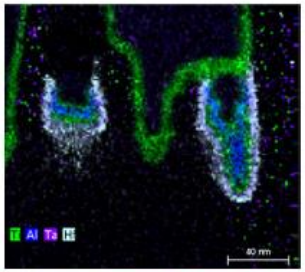


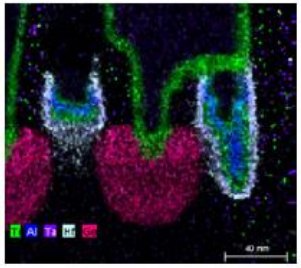



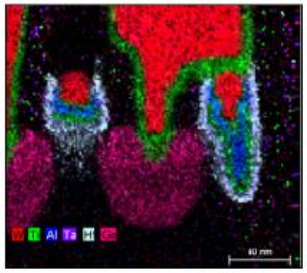



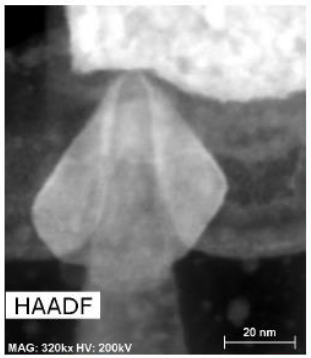



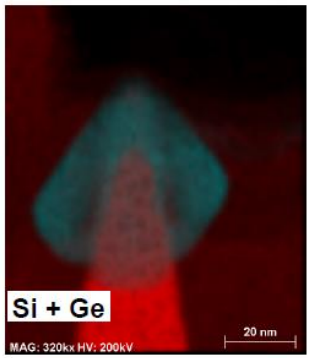



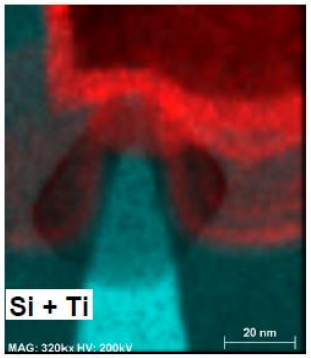



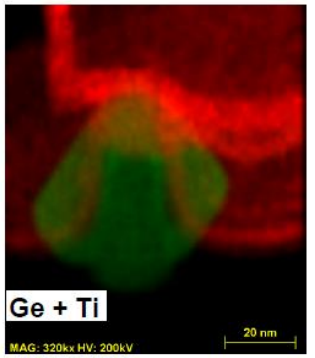

- 10-nm thin sample
- Shows the complex sequence of depositions in the gate stack

chipworks
inside technology



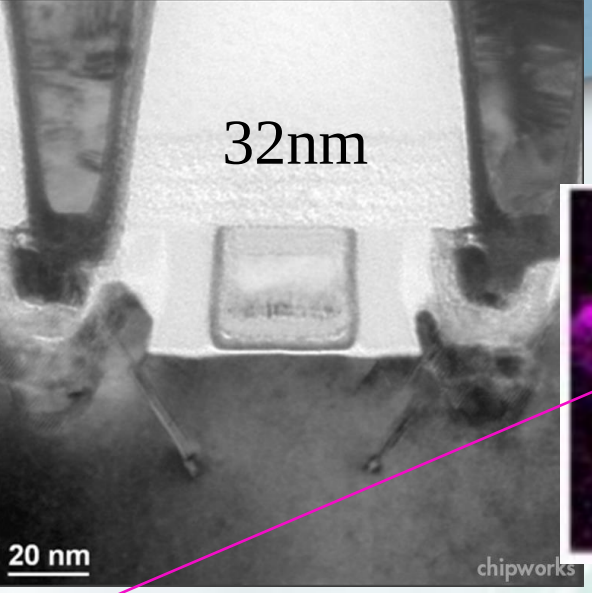



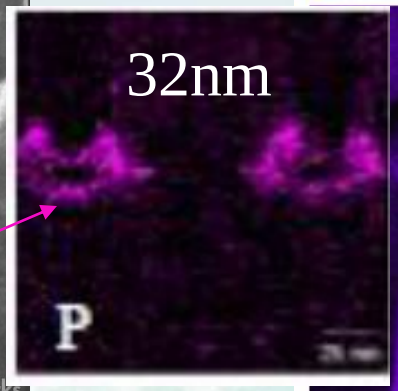



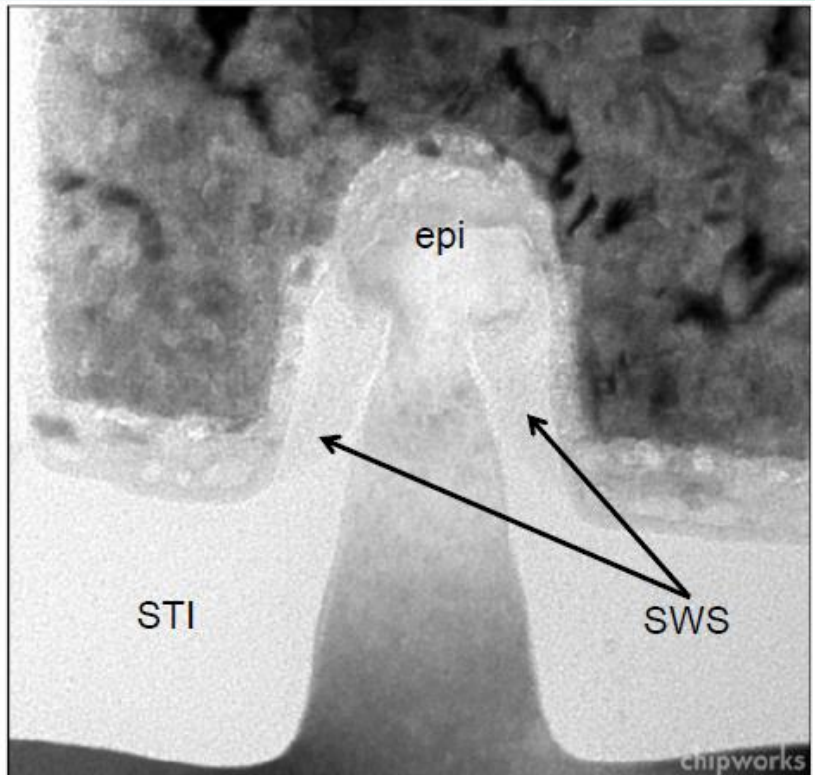

chipworks
inside technology

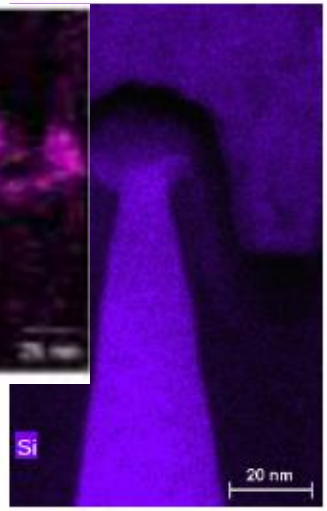
# Chipworks Teardown of Intel 22nm nMOS FinFET

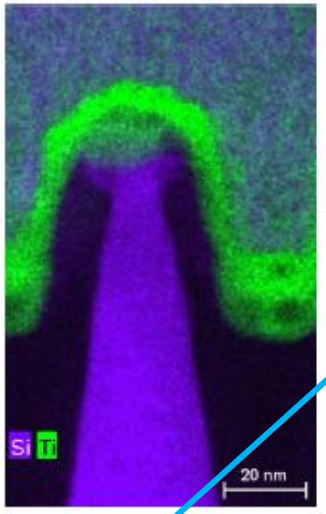


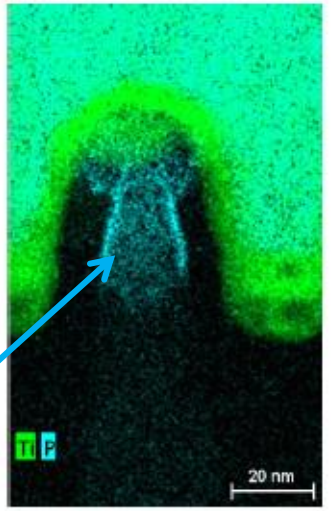




Phos doped Epi S/D has no recess etch!

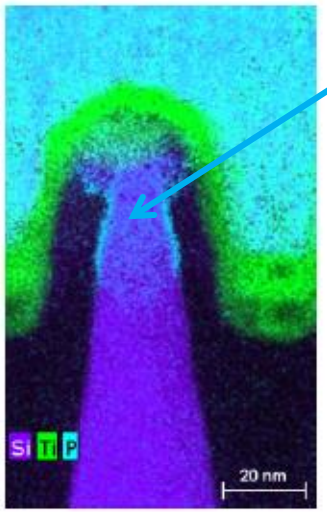


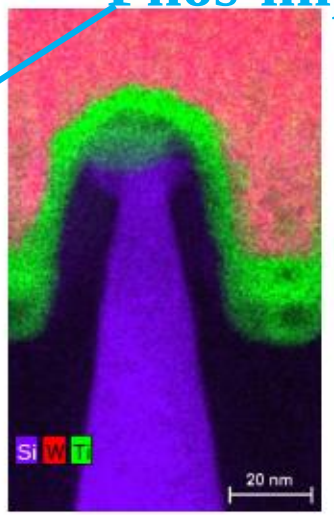



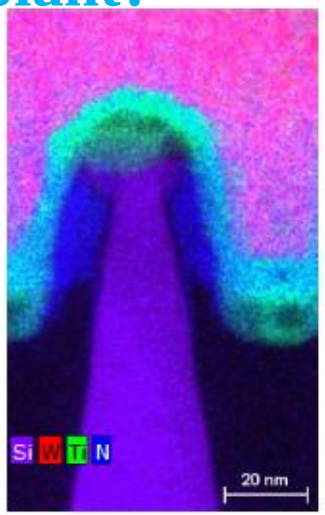




Phos-implant?




**Need to look for As also!**

chipworks
inside technology

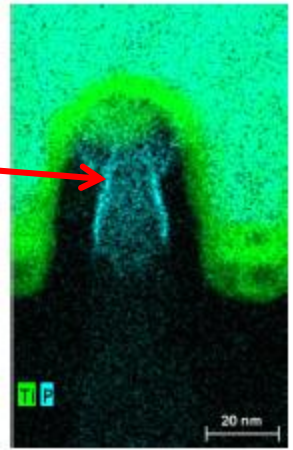
Dick James, Chipworks, Semicon/West 2013 WCJUG meeting

# Comparison of Junctionless and Conventional Trigate Transistors With $L_g$ Down to 26 nm

R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn

Two JAM channel dopings were fabricated, low doped (LD JAM) and high doped (HD JAM), with P doses of $1.5 \times 10^{13}$ and $6 \times 10^{13}$ $cm^{-2}$, respectively. IM received a B dose of $2.5 \times 10^{13}$ $cm^{-2}$. Dopants were activated using 950 °C/spike anneal before gate formation. The S/D areas were formed by Si etch and EPI Si deposition, reaching a P concentration of $3 \times 10^{21}$ $cm^{-3}$. S/D extensions were done with 45° As implants at 3.5 keV and $1.6 \times 10^{15}$ $cm^{-2}$ for all cases. For JAM, the

**But Pss~1.8E21/cm3 so this must be chemical and not electrical!**



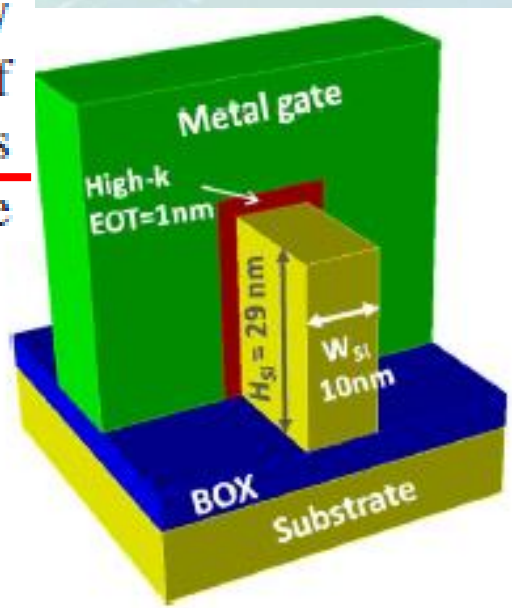




Fig. 1. Schematic of the fabricated trigate on SOI.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

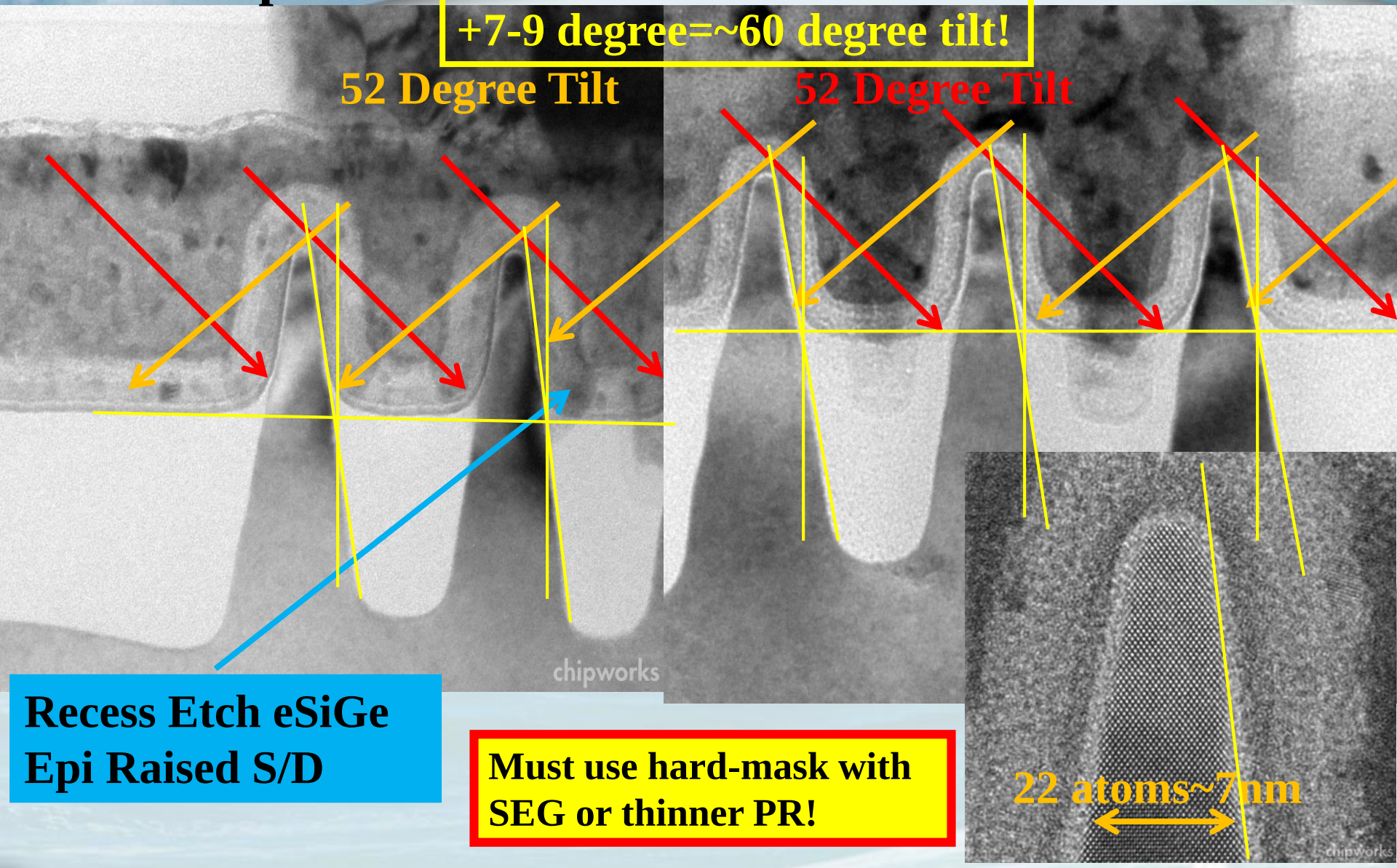
pMOS

nMOS

+7-9 degree=~60 degree tilt!

52 Degree Tilt

52 Degree Tilt

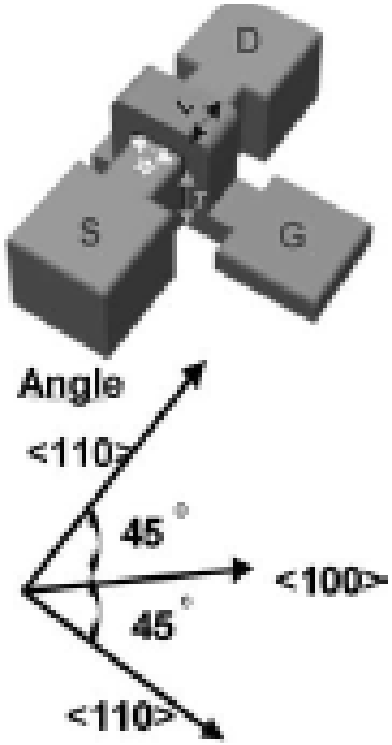



**Recess Etch eSiGe Epi Raised S/D**

**Must use hard-mask with SEG or thinner PR!**

# Revolutional Progress of Silicon Technologies Exhibiting Very High Speed Performance Over a 50-GHz Clock Rate

Tadahiro Ohmi, *Fellow, IEEE*, Akinobu Teramoto, *Member, IEEE*, Rihito Kuroda, *Student Member, IEEE*, and Naoto Miyamoto, *Member, IEEE*




pMOSFET transistors that are fabricated on silicon (551) surface along the ⟨110⟩ direction exhibit excellent current drivability that is completely similar to that of nMOSFET transistors on silicon (100) surface, leading to the realization of a balanced CMOS where the nMOSFET and pMOSFET transistors exhibit the same current drivability with the same effective device dimension [11]. Here, the silicon (551) surface is 8° off from the silicon (110) surface; it is very hard to be roughened even by alkali solutions [12], while the silicon (110) surface is very easily roughened.

**Ohmi, Tokoku Univ, SSDM-2013**

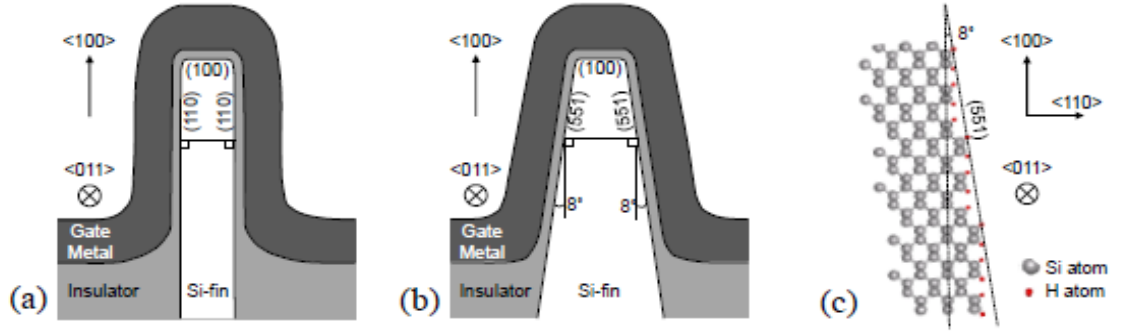



Fig.2 Cross sections of MuGFETs across transistor width direction for Si(100) substrate, <011> channel direction, (a) with (110) oriented facet surface and (b) with (551) oriented facet surface. (c) Schematic illustration of the (551) orientated facet Si surface.

**My Sony contact in July 2012 said 8 degree Fin slope for (551) plane reported by Tokoku Univ in 6/2007!**

# Intel 22 nm SoC Source/Drains

- Modified epi compared with Xeon device – shorter cycles?

Arsenic implant SDE causes amorphization of Fin so SPE forms Stacking Fault Stressor?



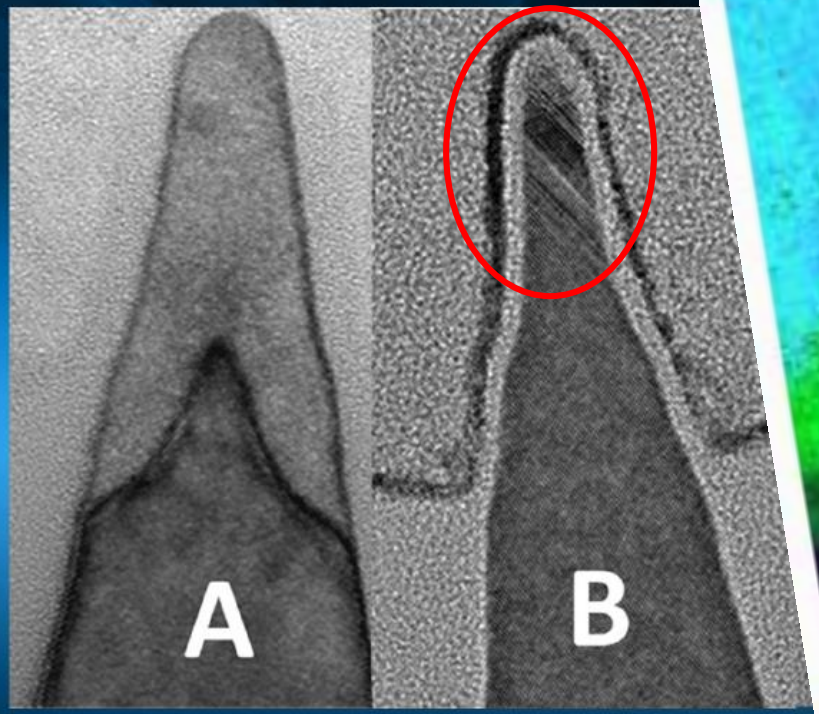
chipworks
patent knowledge • technology expertise • market understanding



Dick James, Chipworks, Semicon/West 2014 discussions

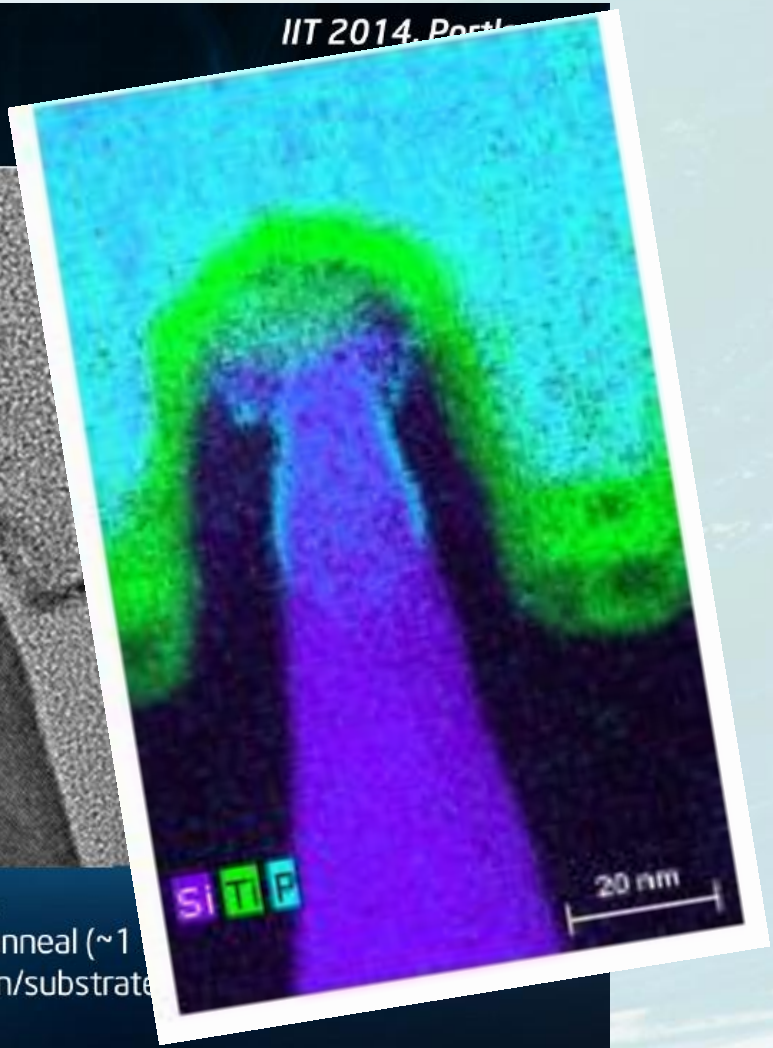
# June 30th IIT-2014 was Intel Paper

## Proof of Concept: TEM




(A) immediately after room temperature implant,
(B) after room temperature implant and a spike anneal (~1
(C) after heated implant alone (no anneal). Platen/substrate

Implant: As, 3 keV, ~2E15/cm2




My claims validated, **Intel** 22nm FinFET uses 45 degree high tilt amorphizing As-implant for SDE as I have said for past 2 years with excellent conformal electrical doping as I first reported at Insights 2009 5 years ago! During Q&A I suggested they try shallow amorphous implant with 1keV As to avoid HOT implant.

# High Tilt p+ & n+ Molecular Implantation For 3-D Structures: Retained Chemical Dose Versus Electrical Activation Limited Conformal Doping

John Ogawa Borland

J.O.B. Technologies, Aiea, Hawaii

&

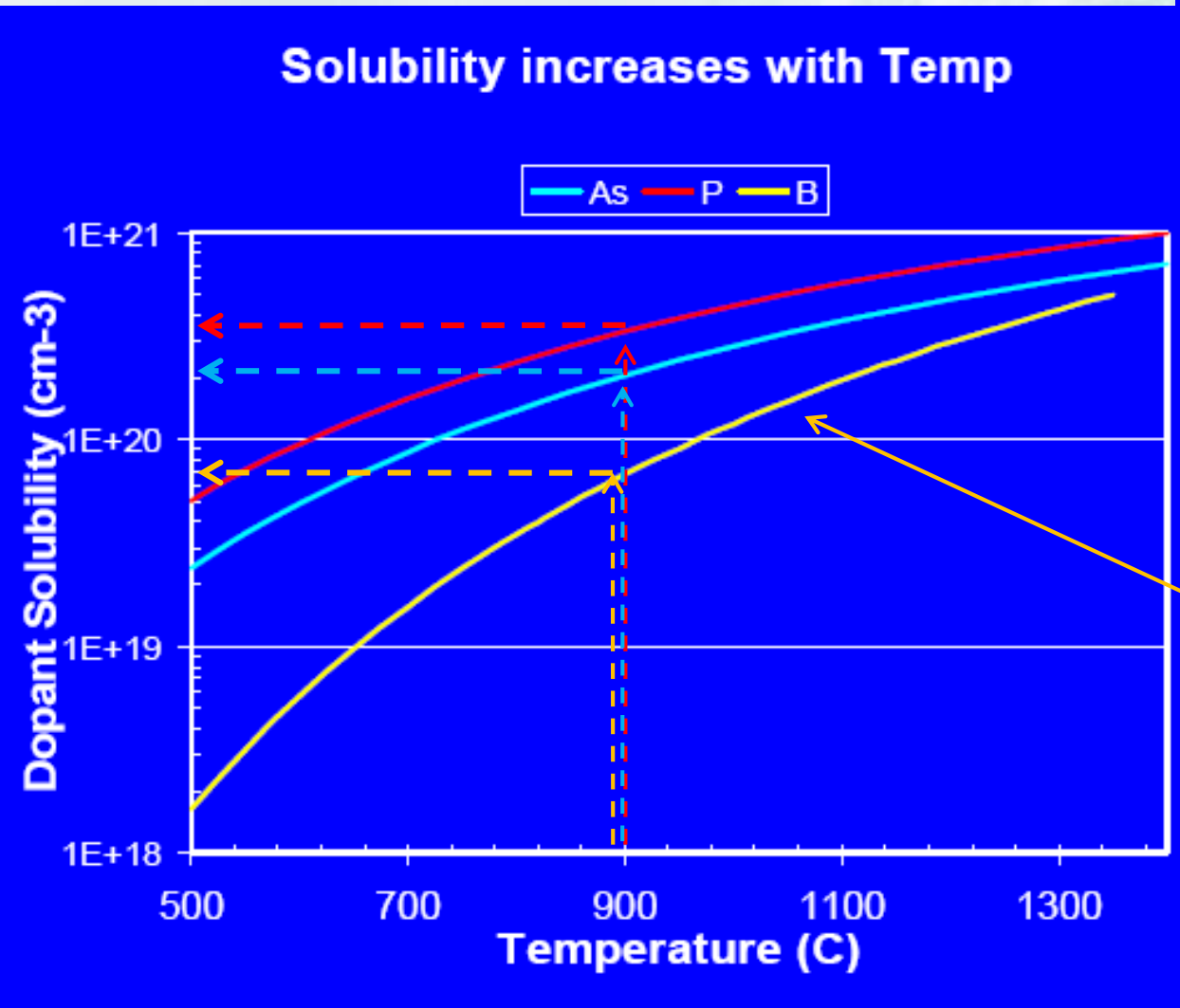
Masayasu Tanjyo, Tsutomu Nagayama and Nariaki Hamamoto

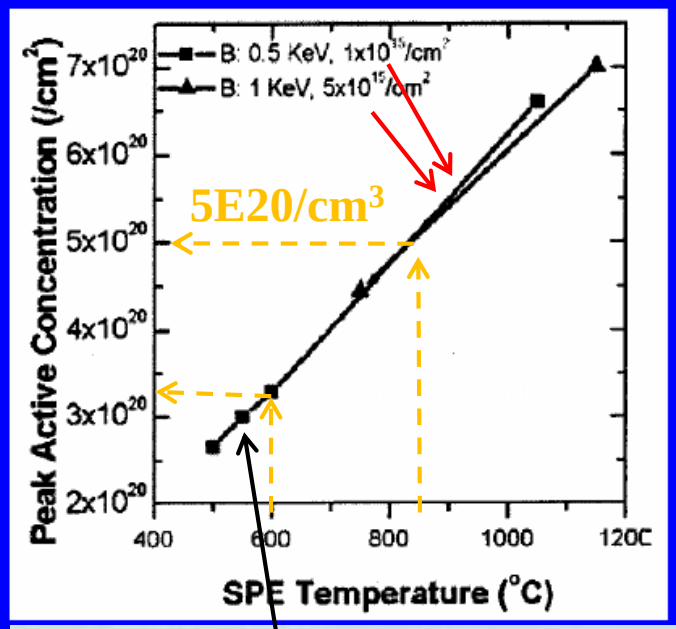
Nissin Ion Equipment, Kyoto, Japan

INSIGHTS 2009

April 28, 2009

**Any deposition doping requires lateral diffusion which will be limited by dopant solid solubility activation unless amorphous SPE or LPE as shown by Intel.**




Kennel, Intel, IEEE/RTP 2006

**With SPE Non-Equilibrium Activation of Boron >>Bss But Requires Amorphization!**

**Boron activation limited by low Bss (Boron solid solubility) and not by implanted dose**

**IWJT-2011 paper S8-2 by Vandervorst of IMEC** was very interesting because independently his presentation validated mine with the same message! Electrical dopant conformality and not chemical conformality is most important for 3-D Fin structure doping. IMEC used SIMS for chemical dopant and SSRM for electrical dopant analysis and concluded that at 45 degree tilt chemical conformality was only 36% but electrical conformality was 78% due to dopant solid solubility as determined by the 2-D SSRM image of the Fin in Fig.9 and Table1! This was exactly my Insights-2009 message. He showed that **65 degree tilt** was needed for 100% electrical conformal doping.

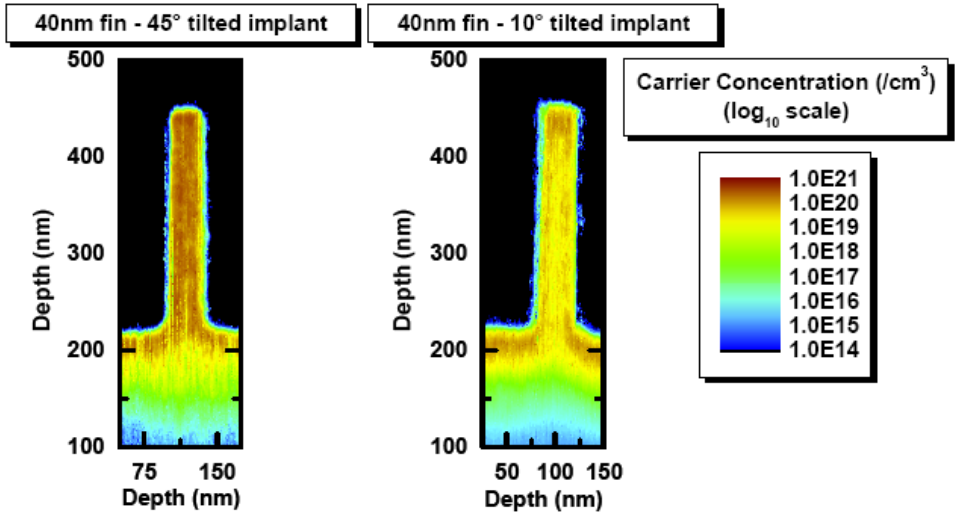



**Figure 9: 2D-SSRM map of active carrier concentration of $BF_2$ implanted at 45° and 10°**

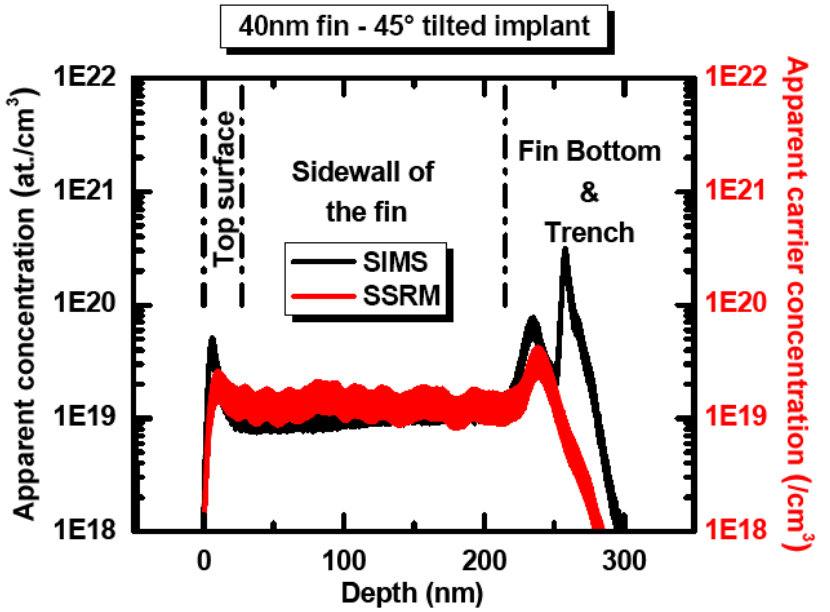
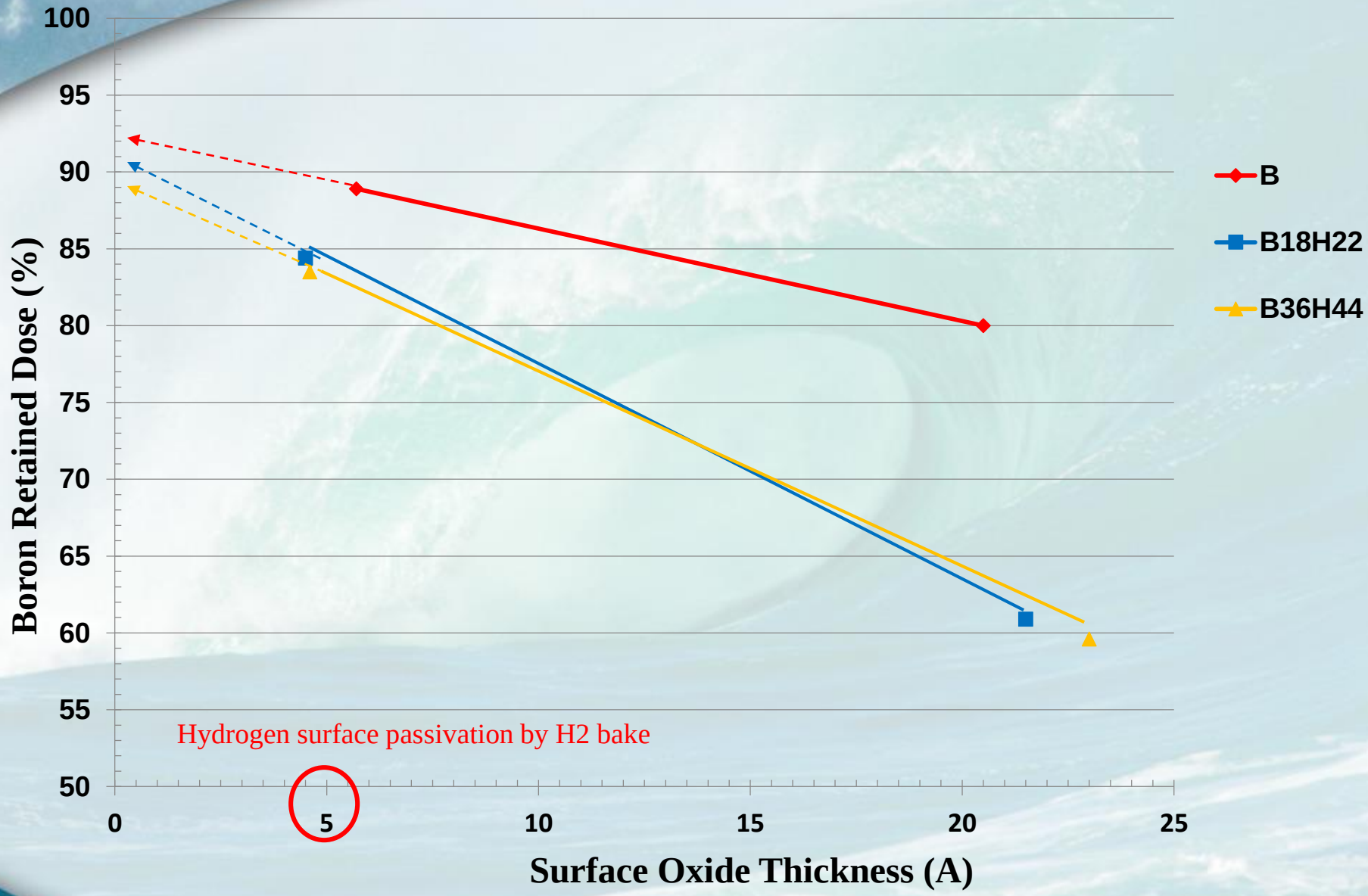


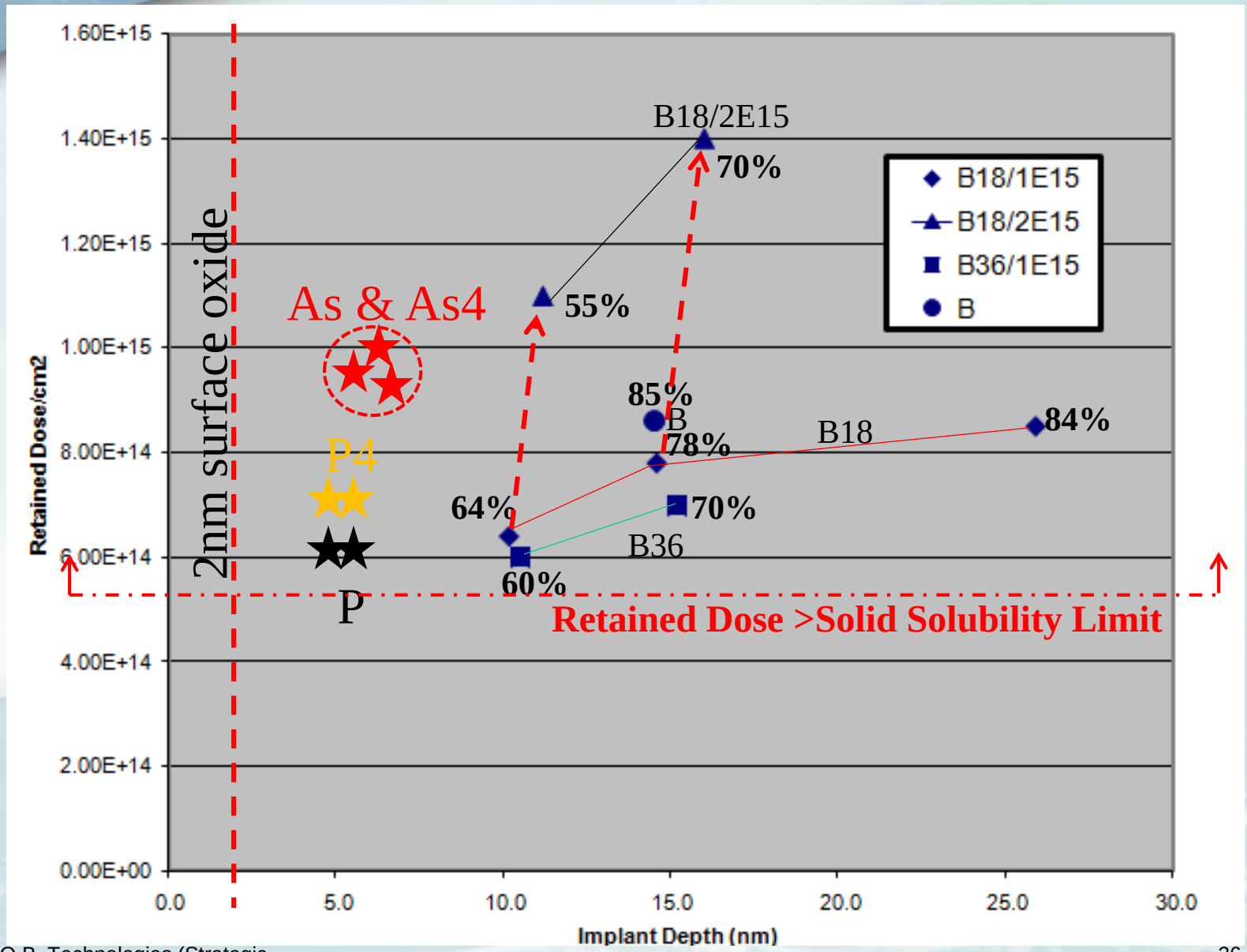

**Figure 10: SSRM vs. SIMS (45° implant). SSRM profile is calculated from figure 10. ([8] for the procedure)**






Borland et al., IWJT-2011

# B, B18, B36, As, As4, P & P4 Retained Dose






Borland et al., IWJT-2011

# Outline

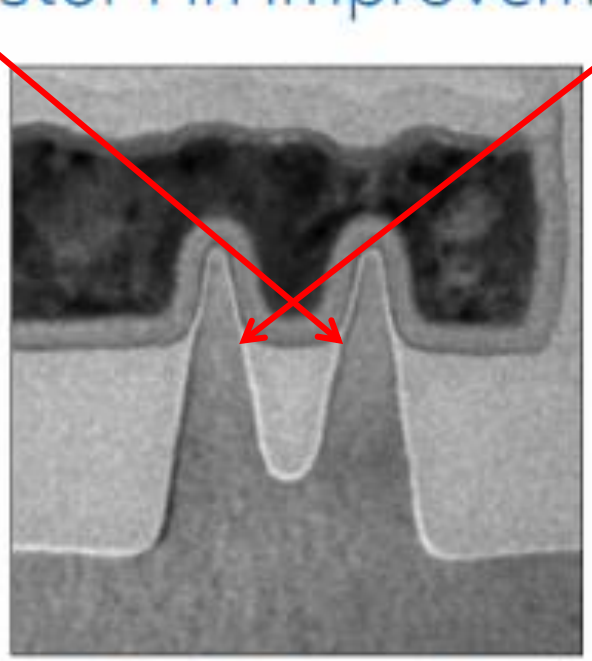
- Introduction
- 22nm Node: Bulk-FinFET
- 14/16nm Node
  - Intel's SOC bulk-FinFET
  - IBM/GF/Samsung/ST Alliance bulk & SOI FinFET comparison
  - TSMC bulk-FinFET
  - Doping & Annealing Issues to Reduce USJ Variability
- 10nm Node: High mobility SiGe or Ge Fin/channel Formation
- Summary

# Intel can still use Bi-mode up to 41 degree tilt implant!

Embargo until 8-11-14, 9 am PDT

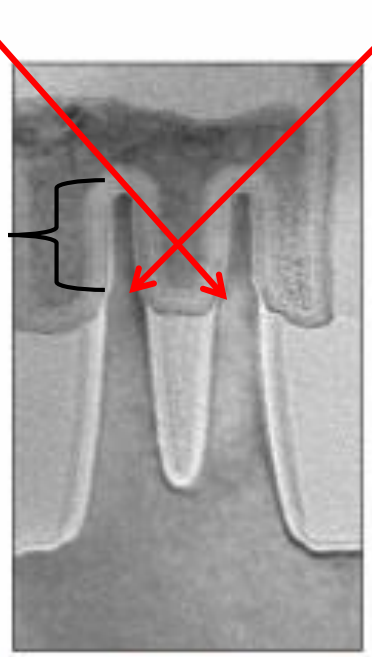
## Transistor Fin Improvement

**For 22nm I said 2 years ago Intel could use up to 52 degree tilt but they acutally use Bi-mode 45 degree tilt implant.**



22 nm 1st Generation
Tri-gate Transistor

Dark Image
SiGe-Fin?



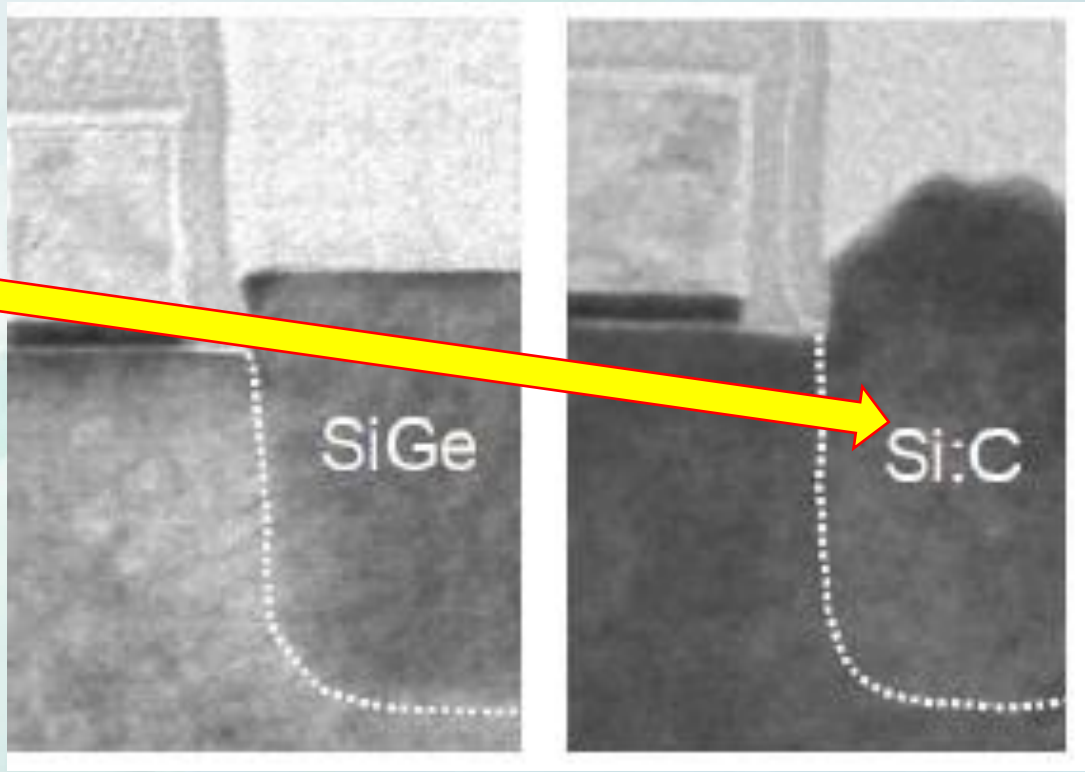
14 nm 2nd Generation
Tri-gate Transistor

**For 14nm I estimate Intel can use up to 41 degree tilt if twist is 0 degree for bi-mode but if twist is 45 degree then Quad-mode >45 degree is OK!**

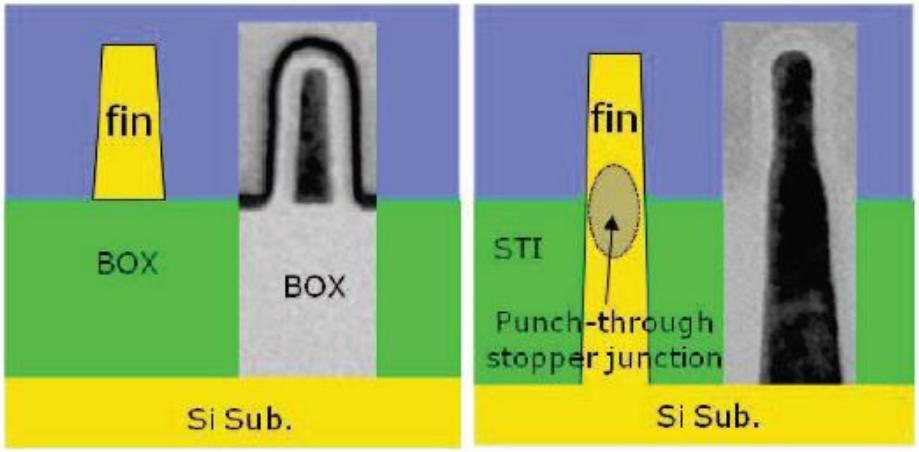
intel 25

# Key Points on IBM 22nm Node Technology at IEDM-2012, Will 14nm FinFET Be Similar?

- IBM IEDM-2012
  - 22nm PD-SOI 1st successful use of eSiC+P recess etch raised S/D epi in production at Csub~1.5% for 340MPa tensile channel strain (while Intel's **SF-stressor is up to 1GPa!)**
  - IBM simulations show eSiGe bulk-Fin only 1-2% better than SOI-Fin but IMEC, Synopsys and Samsung papers strongly disagree!



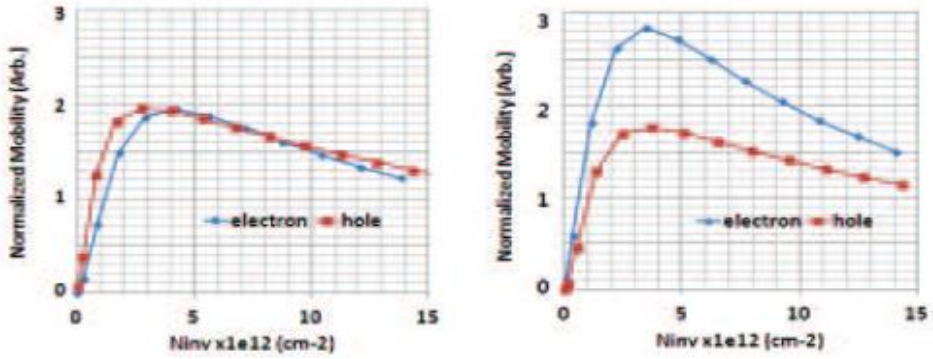
**VLSI Sym 2014 Paper 2.2**: Seo of **IBM/Samsung/ST/GF** on "A 10nm Platform Technology for Low Power and High Performance Application Featuring FINFET Devices with Multi Work function Gate Stack on Bulk and SOI". Finally reported good bulk-FinFET comparison to SOI-FinFET in fact the bulk FinFET pFET was better than the SOI-FinFET.




**(a) SOI-fin** **(b) Bulk-fin**

Fig. 4 Schematics and TEM of (a) SOI-fin and (b) Bulk-fin with punch-through stopper junction.

They used embedded p+SiGe S/D for pMOS and embedded n+Si-epi S/D for nMOS. For SOI-FinFET electron mobility is higher than hole mobility by 0.58x but for bulk-FinFET in Fig.8a electron and hole mobilities are nearly the same and the hole mobility in bulk is 11% higher than in SOI even though the bulk-FinFET must use channel doping which degrades mobility, bulk eSiGe stress is 10% higher than SOI-FinFET **(Fig.9).** SOI electron mobility is 43% higher. If they use SF-stressor for n+S/D bulk nFinFET will have higher electron mobility than SOI too.




**(a) Bulk FINFET** **(b) SOI FINFET**

Fig. 8 Long channel electron and hole mobility of (a) Bulk and (b) SOI FINFET.

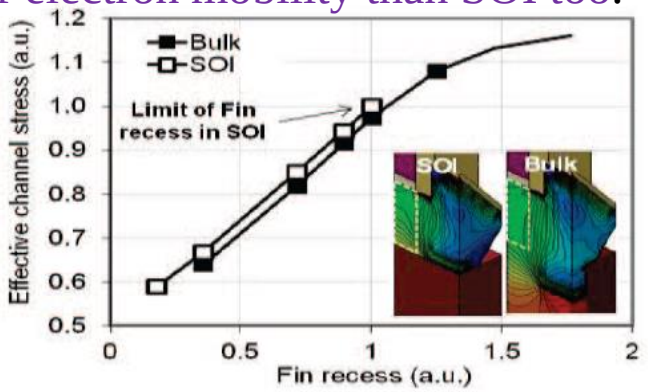
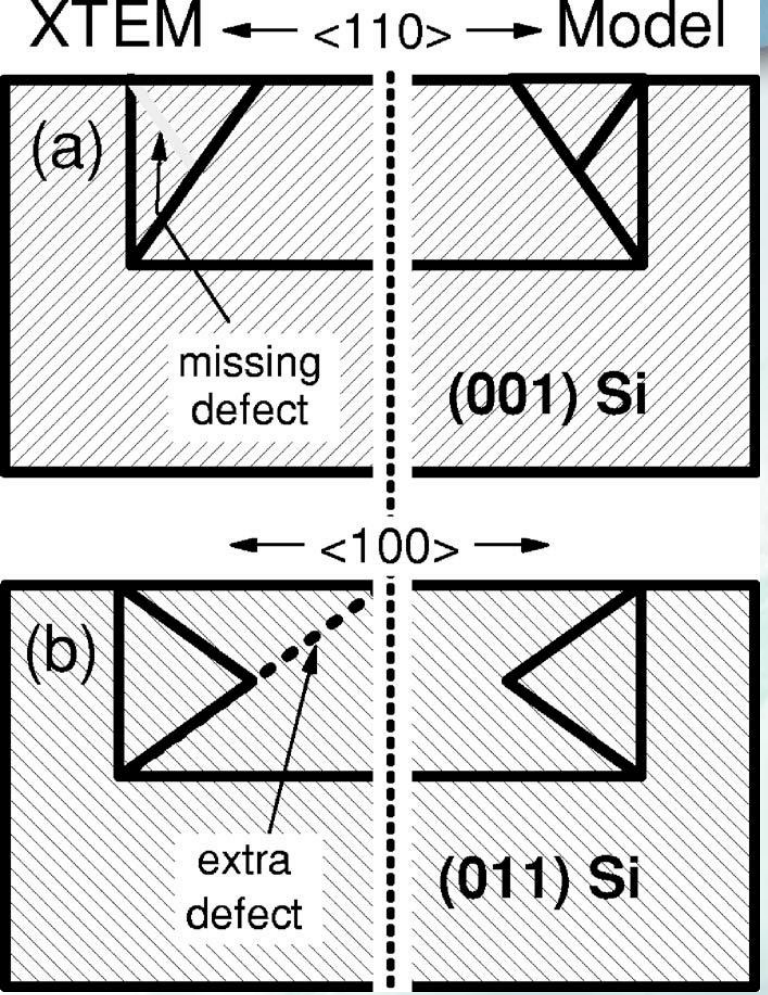
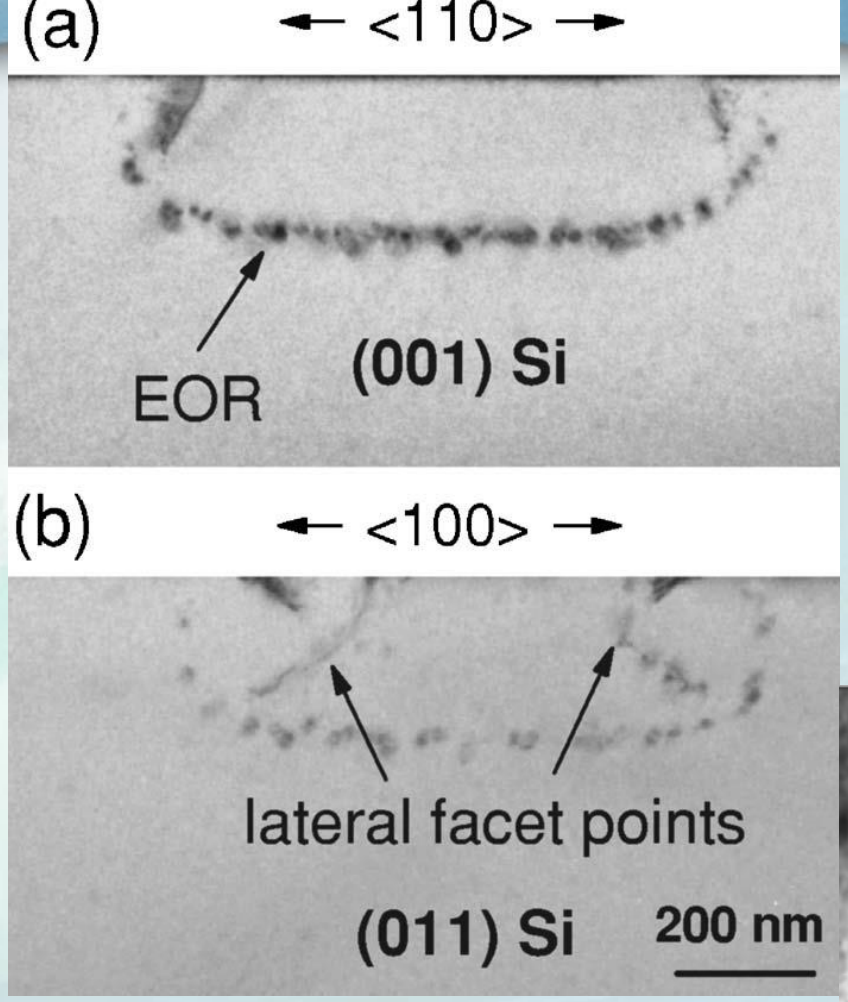
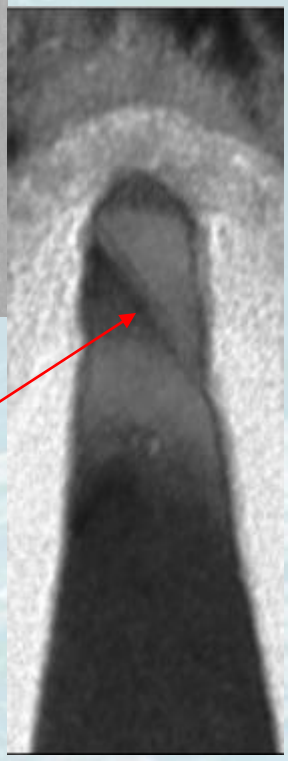



Fig. 9 Effective channel stress at short channel PFET as a function of fin recess. Deeper fin recess in bulk allows larger stress at channel.



K. L. Saenger,a K. E. Fogel, J. A. Ott, and D. K. Sadana, Research Division, IBM Semiconductor Research and Development Center, T. J. Watson Research Center
JOURNAL OF APPLIED PHYSICS 101, 104908 2007

Oct 2011 I discussed SF stressor for FinFETs and Saenger told me amorphous SF stressor should work with FinFET!

# 22nm Node n+ SiC Stressor Using Deep PAI+$C_7H_7$+$P_4$ With Laser Annealing

## IEEE/RTP-2009

John Borland[1], Masayasu Tanjyo[2], Nariaki Hamamoto[2], Tsutomu Nagayama[2], Shankar Muthukrishnan[3], Jeremy Zelenko[3], Iad Mirshad[4], Walt Johnson[4], Temel Buyuklimanli[5], David Susnitsky[5], Hiroshi Itokawa[6], Ichiro Mizushima[6] and Kyoichi Suguro[6]

1) J.O.B. Technologies, Aiea, HI

2) Nissin Ion Equipment, Kyoto, Japan

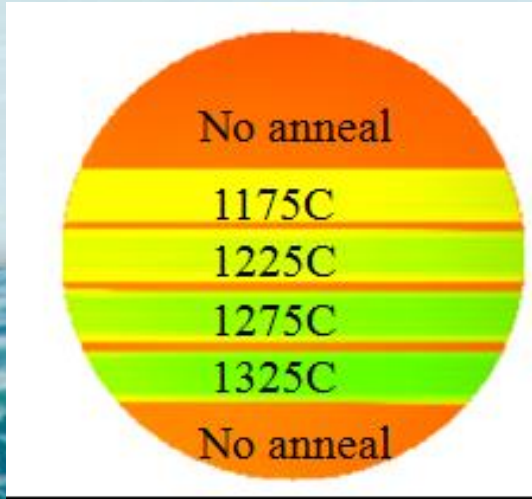
3) Applied Materials, Sunnyvale, CA

4) KLA-Tencor, San Jose, CA

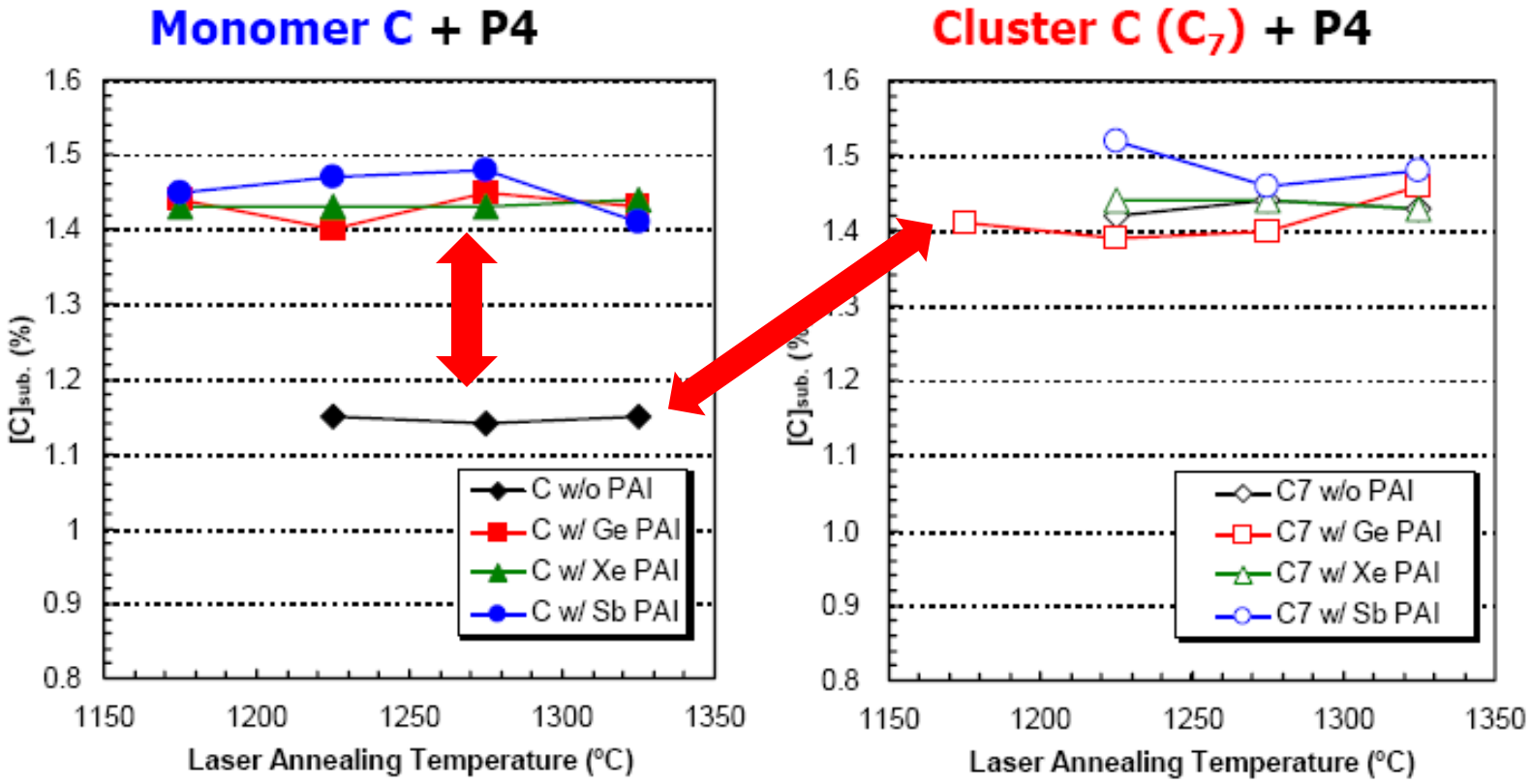
5) EAG, Sunnyvale, CA

6) Toshiba Corporation, Yokohama, Japan

**C/C7+P4,**
**Ge-PAI+C/C7+P4,**
**Xe-PAI+C/C7+P4,**
**Sb-PAI+C/C7+P4**



# Substitutionally Incorporated Carbon Concentration ($[C]_{sub}$)




- Monomer $C^+$: without PAI → low $[C]_{sub}$ → P4 effect on [C]sub is small
- Cluster $C_7^+$: High $[C]_{sub}$ independent on PAI condition
- There is no clear dependence on Laser anneal temperature

# 22/20nm FinFET CMOS

Will TSMC also use 20nm process doping and stressor method for 16nm FinFET too?

CC Wu, TSMC, IEDM-2010, paper 27.1

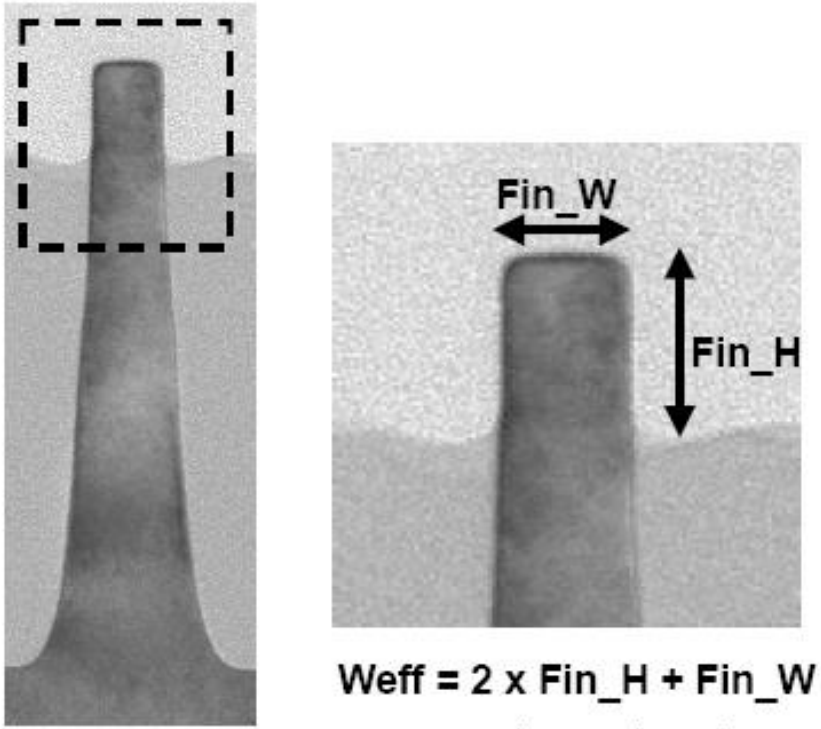



Figure 1. TEM Cross-section showing vertical fin sidewall in the area of interest.

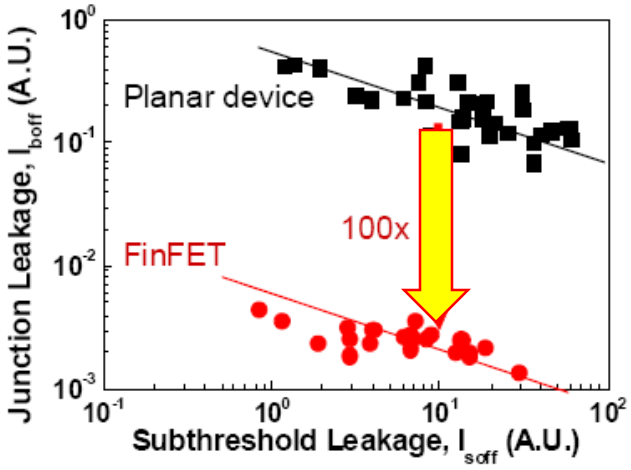



Figure 15. N-FinFETs junction leakage decreases by 100 times at the same $I_{soff}$ leakage compared to the planar NFETs using similar process conditions.

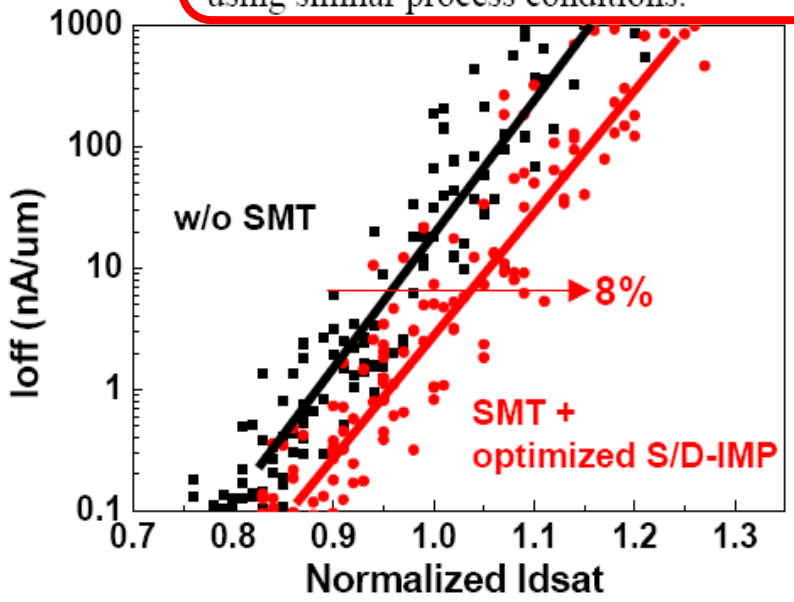
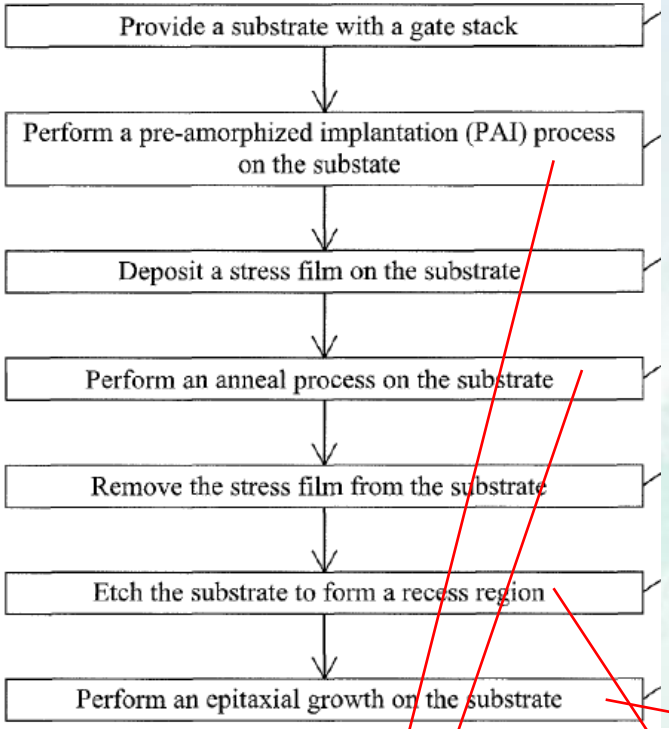



Figure 4. Stress-memorization-technique + optimized $N^+$ S/D ion-implantation provides 8% $I_{on}$-$I_{off}$ gain for the NFET.

# TSMC 20nm Node nMOS Stressor?




(12) **United States Patent**
**Tsai et al.**

(10) **Patent No.: US 8,674,453 B2**
(45) **Date of Patent: Mar. 18, 2014**

(54) **MECHANISMS FOR FORMING STRESSOR REGIONS IN A SEMICONDUCTOR DEVICE**

(75) Inventors: **Chun Hsiung Tsai**, Xinpu Township (TW); **Tsan-Chun Wang**, Hsinchu (TW); **Su-Hao Liu**, Jhongpu Township (TW); **Tsz-Mei Kwok**, Hsinchu (TW); **Chii-Meng Wu**, Taipei (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.** (TW)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 118 days.

(21) Appl. No.: **13/324,331**

(22) Filed: **Dec. 13, 2011**

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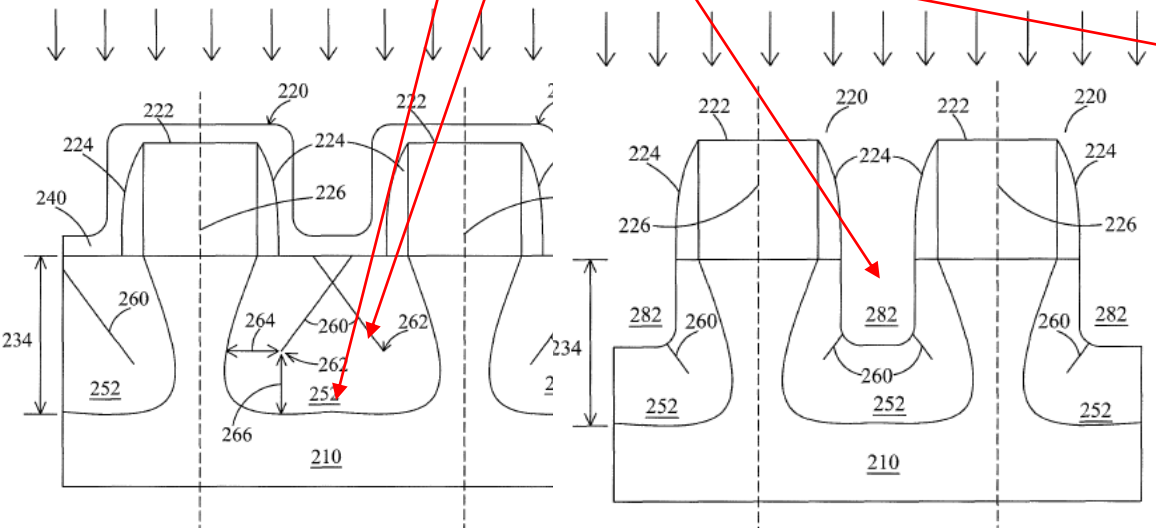
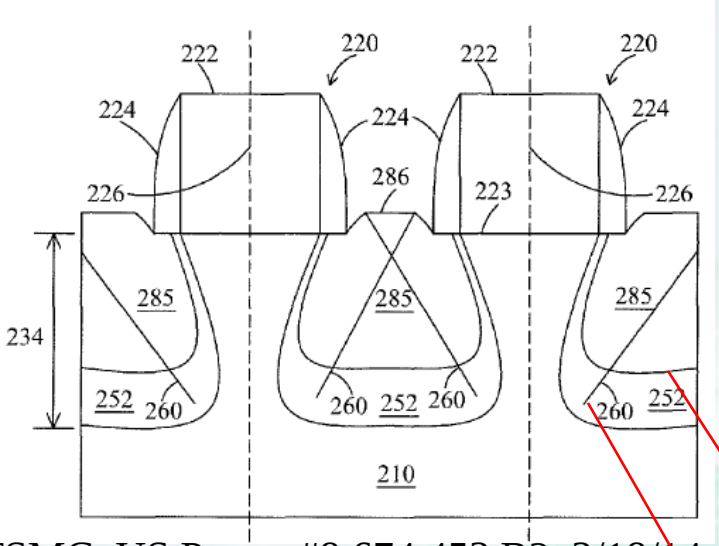
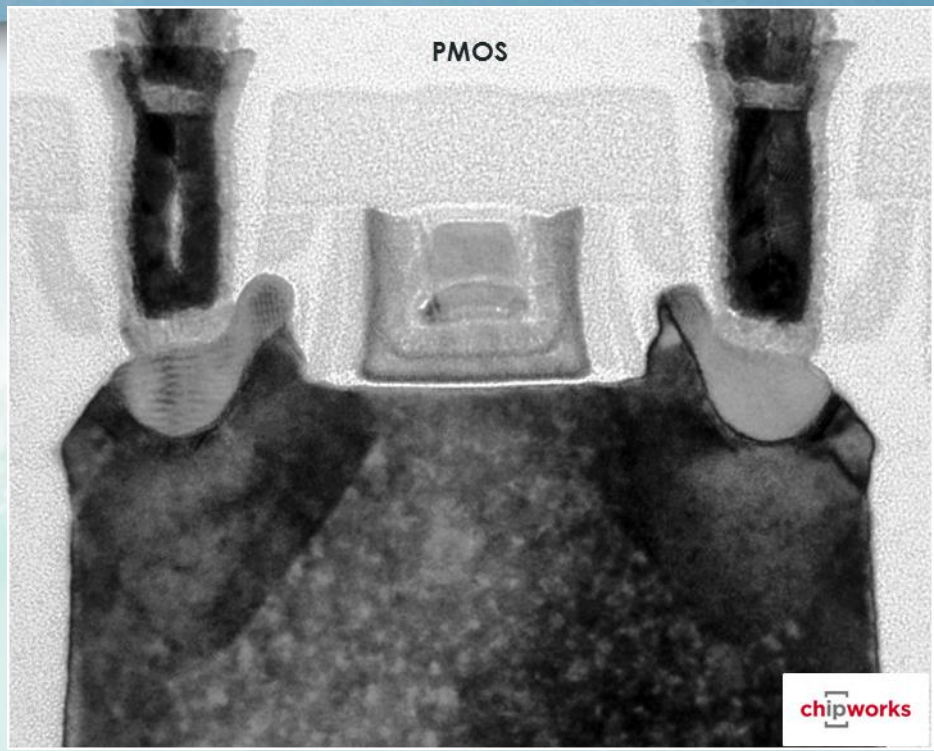
Fischer, P. R. et al., "Low Temperature Silcore Deposition of Undoped and Doped Silicon Films", ECS Transactions, 3(2) 203-215 (2006).



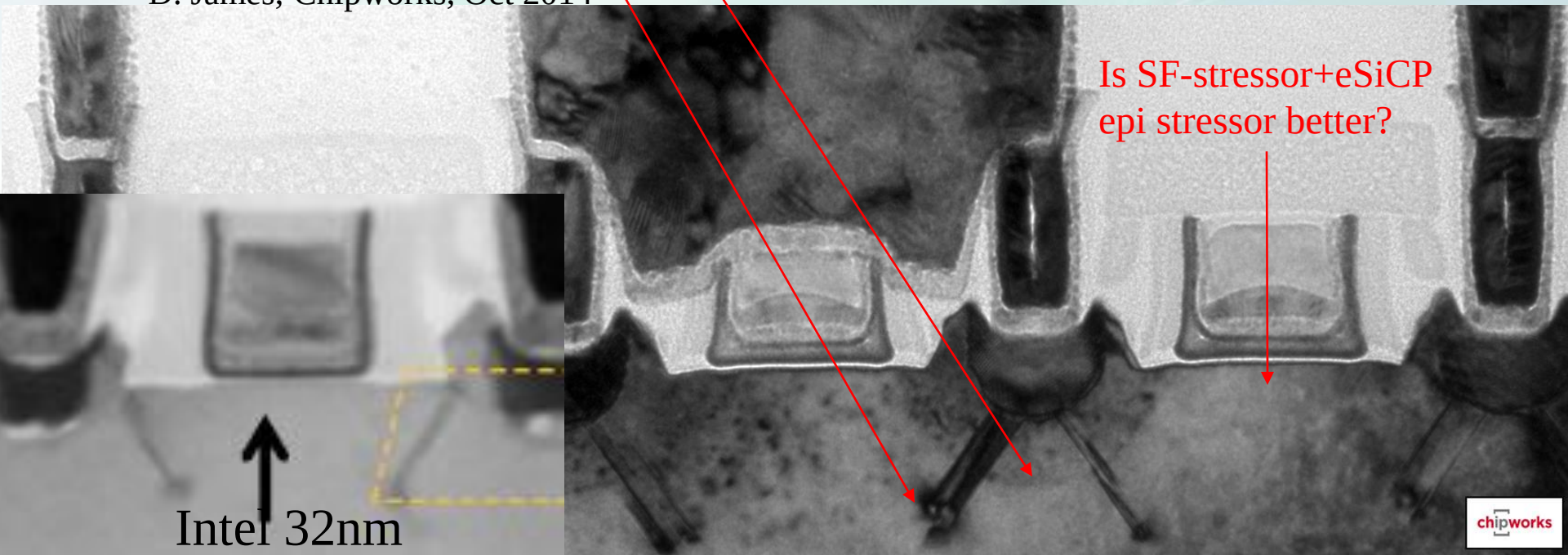
# TSMC 20nm Node:




TSMC, US Patent #8,674,453 B2, 3/18/14




D. James, Chipworks, Oct 2014






Intel 32nm

# Intel Reported Implant Variability Effects at IIT-2014 on nMOS-FinFET

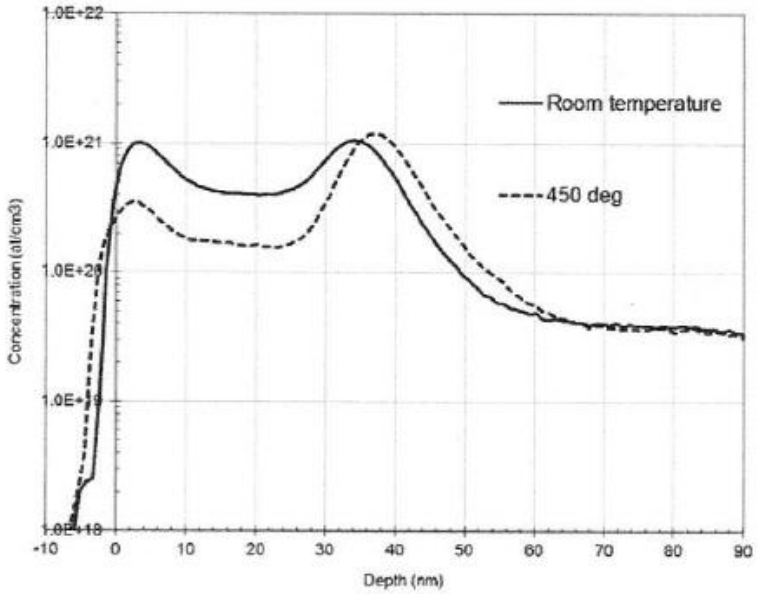



Fig. 3: SIMS profiles of 3.5 keV arsenic implanted at 30 degree incidence to wafer surface/fin top surface into fins nominally ~35 nm tall with ~42 nm pitch at room temperature and at 450 degrees.

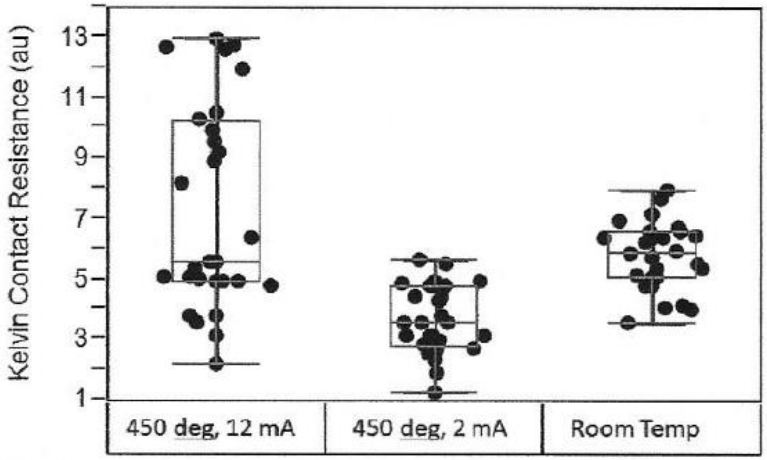



Fig. 6: Kelvin contact resistance for representative wafers at room temperature, 450 deg C at 12 mA beam current, and 450 deg C at 2 mA beam current

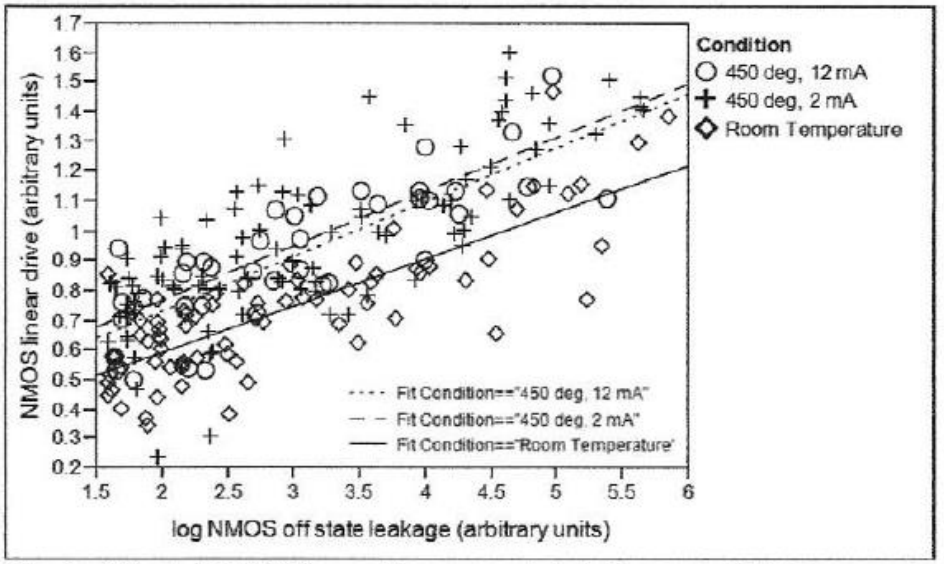



Fig. 5a: Trigate NMOS linear drive current plotted versus off state source-to-drain leakage for representative wafers at room temperature, 450 deg C at 12 mA beam current, and 450 deg C at 2 mA beam current

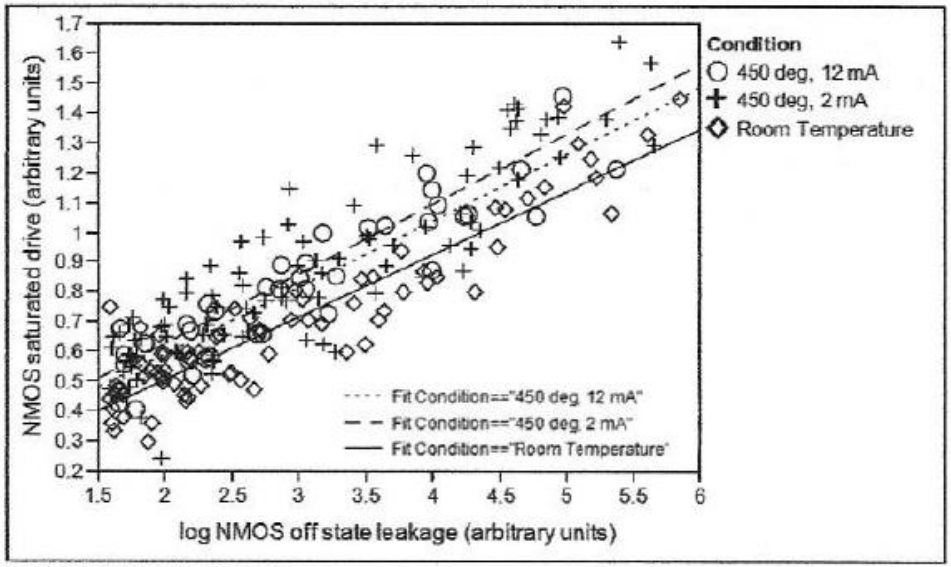



Fig. 5b: Trigate NMOS saturated drive current plotted versus off state source-to-drain leakage for representative wafers at room temperature, 450 deg C at 12 mA beam current, and 450 deg C at 2 mA beam current

# Simulation of 3D FinFET Doping Profiles by Ion Implantation

Liping Wang[1], Andrew R. Brown[2], Binjie Cheng[1] and Asen Asenov[1,2]

[1)] *School of Engineering, University of Glasgow, Rankine Building, Oakfield Avenue, Glasgow, UK G12 8LT*
[2)] *Gold Standard Simulations Ltd. Rankine Building, Oakfield Avenue, Glasgow, UK G12 8LT*

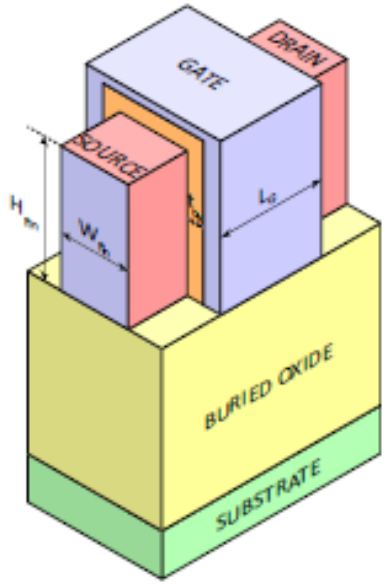



**FIGURE 1**. Schematic of an SOI FinFET

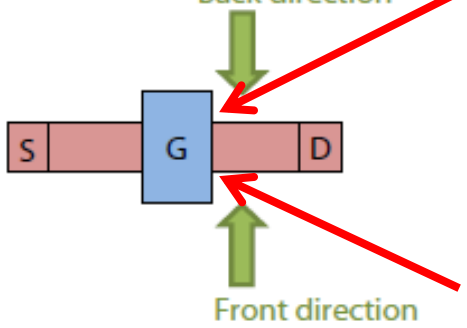



**FIGURE 2**. Tilted beam implantations for the fin from the front and back directions

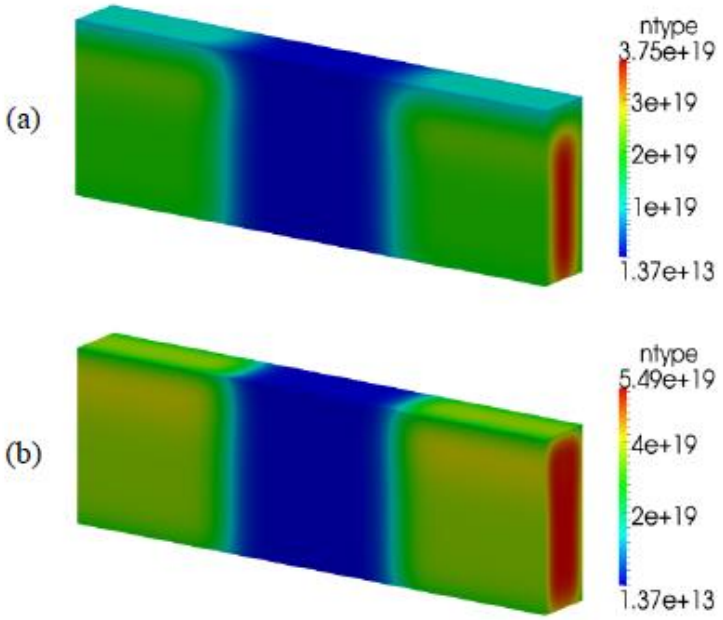



**FIGURE 8**. N type profile by tilted beam implantations (with color map using a linear scale) (a) without additional fin implantation (b) with additional fin implantation

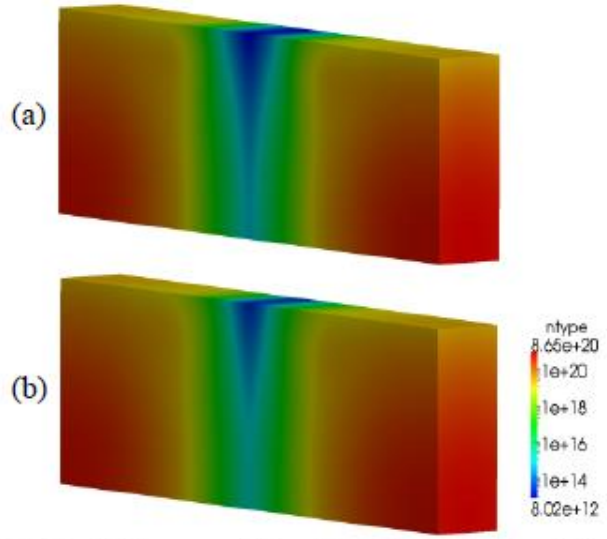



**FIGURE 6**. N type profile after all fin implantations and S/D implantation (with color map using a logarithmic scale) (a) before annealing (b) after annealing

# Reducing Variability Still Critical For FinFET So What Are The Sources For USJ Variability?

TOSHIBA

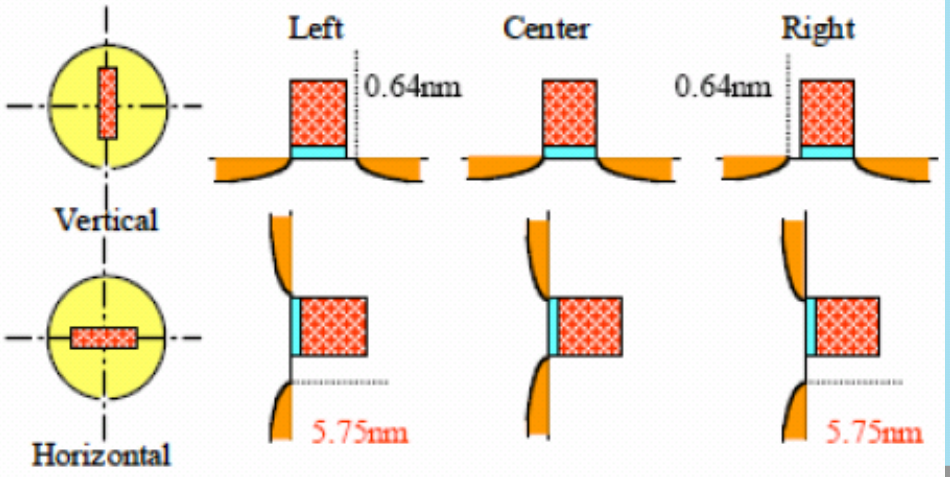


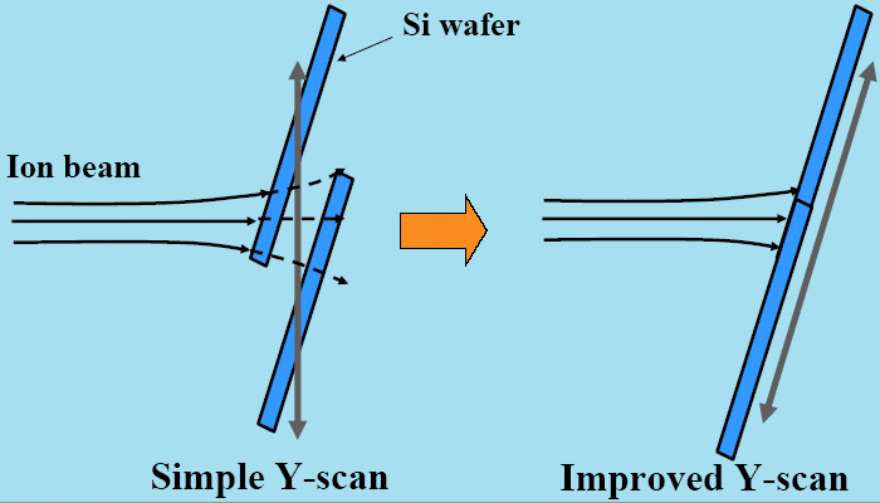

Fig.7 Calculated extension offset length for vertical and horizontal direction gate on various wafer position
(Gate electrode height=300nm, Tilt setting angle=0 deg.)

Kenji Yoneda et al.

IWJT 2002 Paper No. S2-3

TOSHIBA

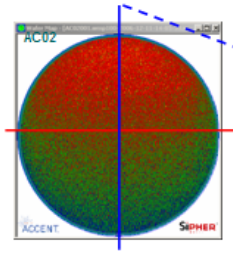
Improvement of incident angle variation



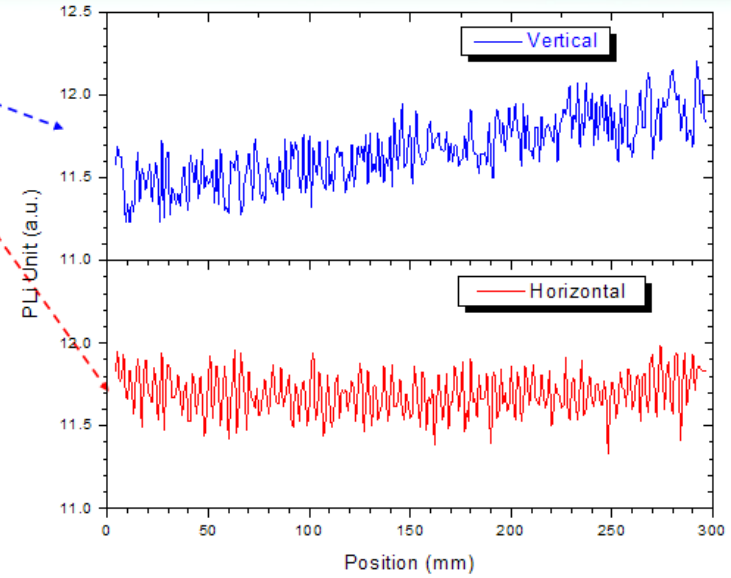

K. Suguro vTech 2005 @San Fransisco July 12, 2005

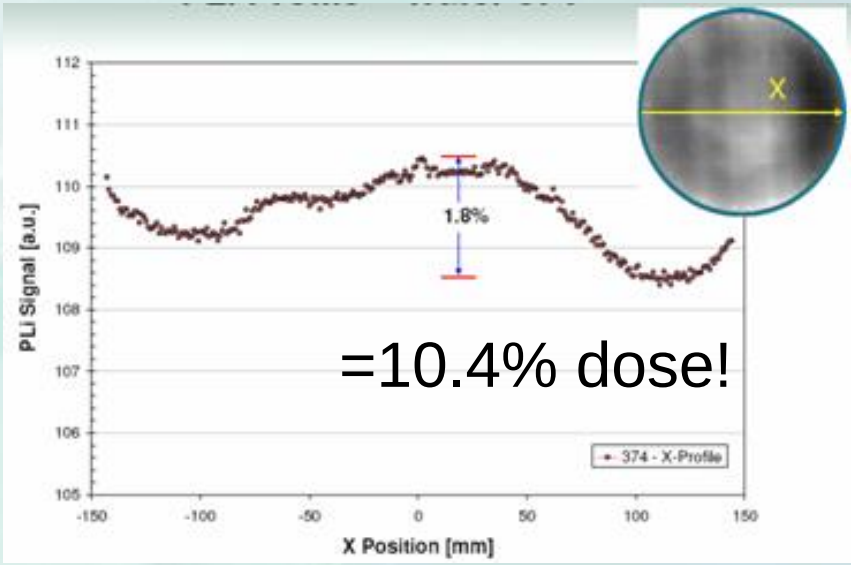
**Angle shadowing causes the vertical left to right asymmetry but the horizontal bottom asymmetry is caused by asymmetry in the spot beam size! So Suguro says ISO-SCAN needed (Aug 2004 he told me he sees asymmetrical dumbbell spot beam)**

# Implanter Unique Non-Uniformity Signatures Due To Localized Tilt Angle/Dose Variation!

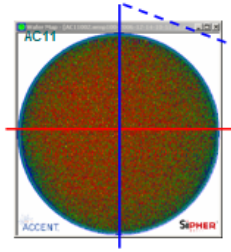


As 1.5keV 9E14
II Equip A

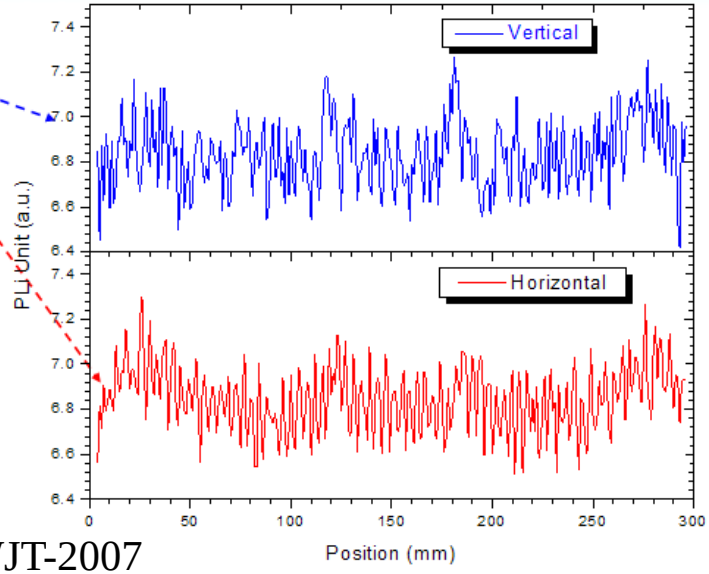


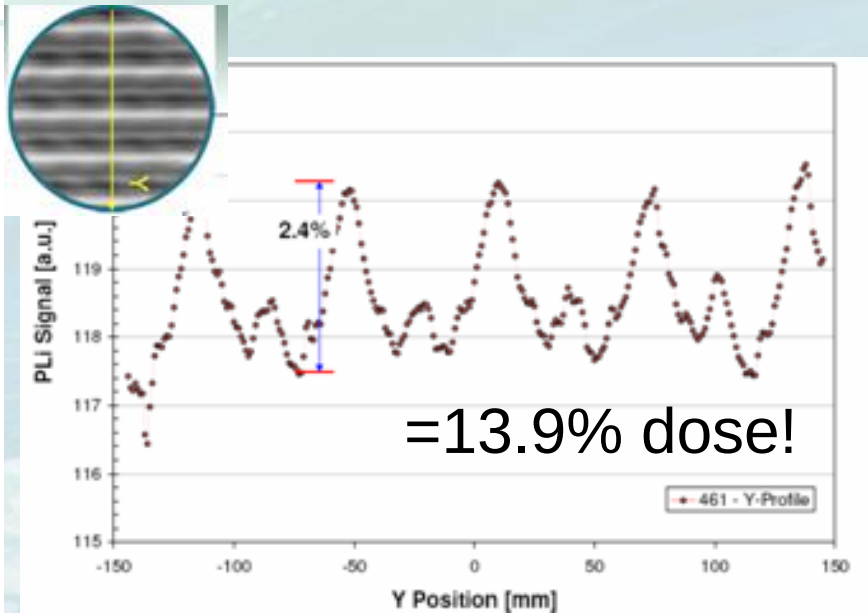




=10.4% dose!



As 1.5keV 9E14
II Equip B



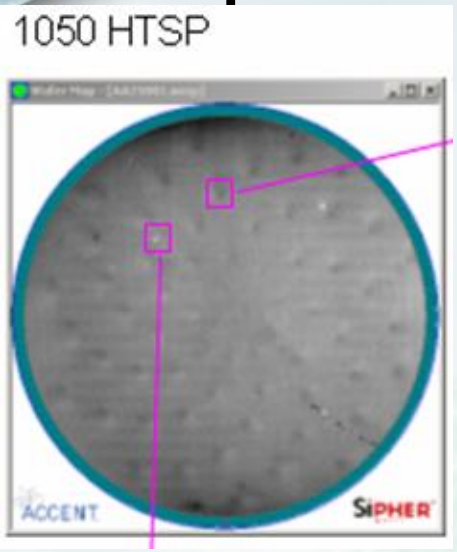

=13.9% dose!

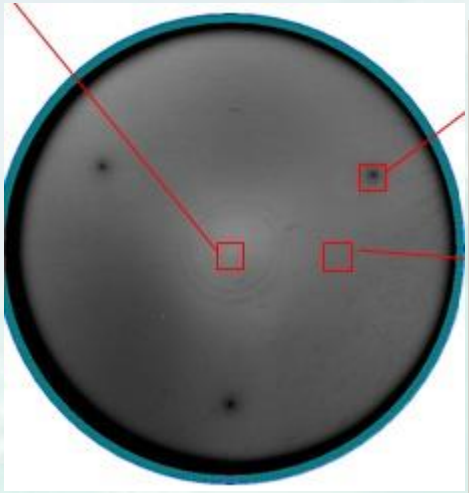
Borland et al., IWJT-2007

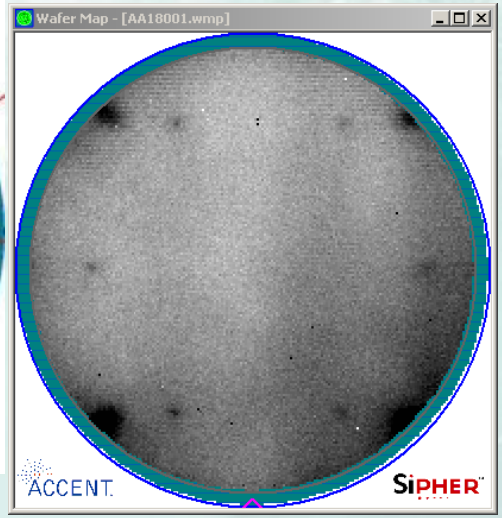
# Without Spike/RTA, msec Annealing Uniformity Signature Is Critical

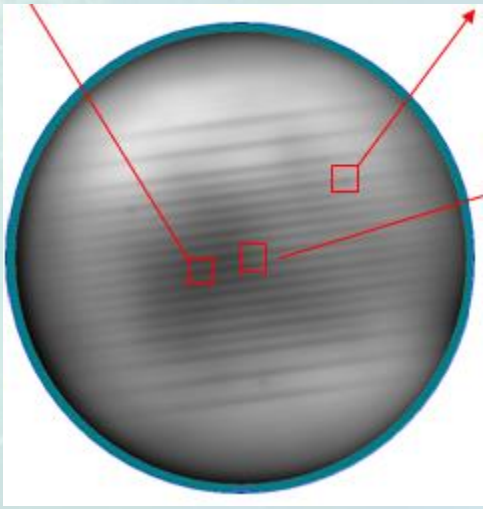
## Spike/RTA: no lamps

## Flash Anneal

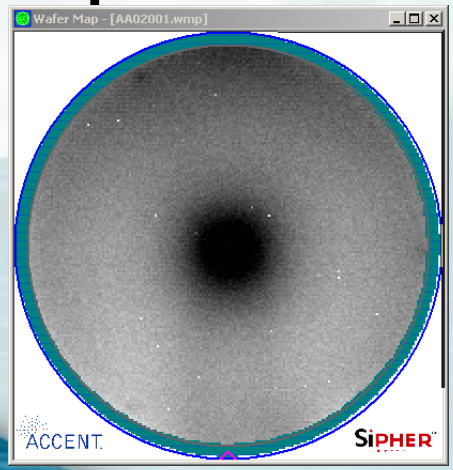


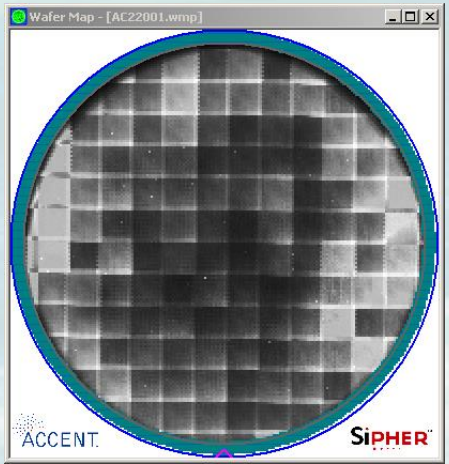


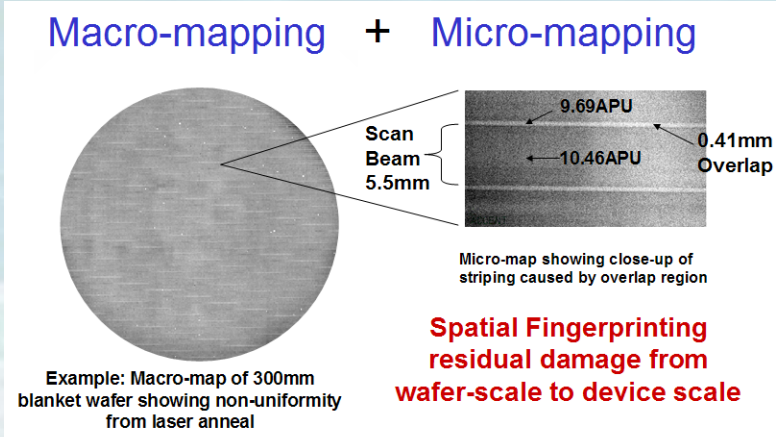



## Spike/RTA: lamps




## Laser Anneal



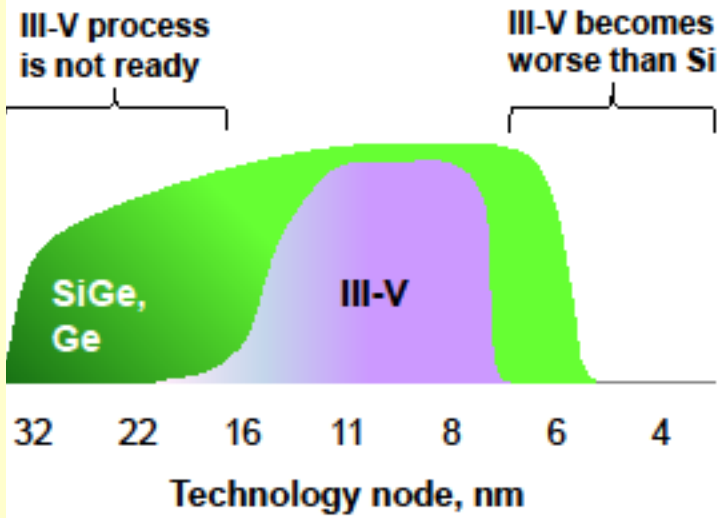

Borland et al., IWJT-2007

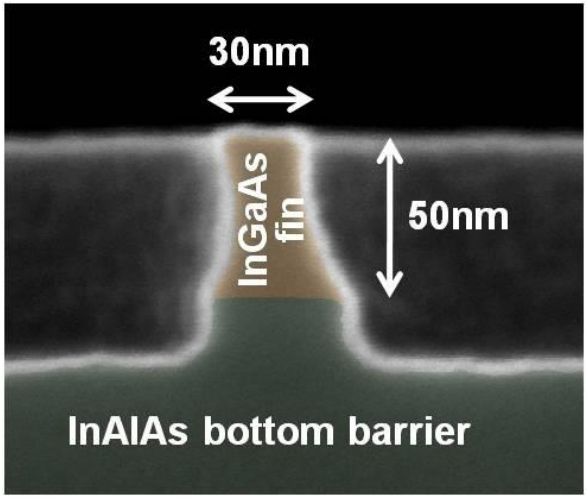
# Outline

- Introduction
- 22nm Node: Bulk-FinFET
- 14/16nm Node
- 10nm Node: High mobility SiGe or Ge Fin/channel Formation
  - Selective Ge-epi Fin, blanket Ge-epi, Ge-condensation, aGe-LPE (implant, plasma or GCIB)
  - Ge p+ and n+ USJ formation and junction leakage issues
- Summary

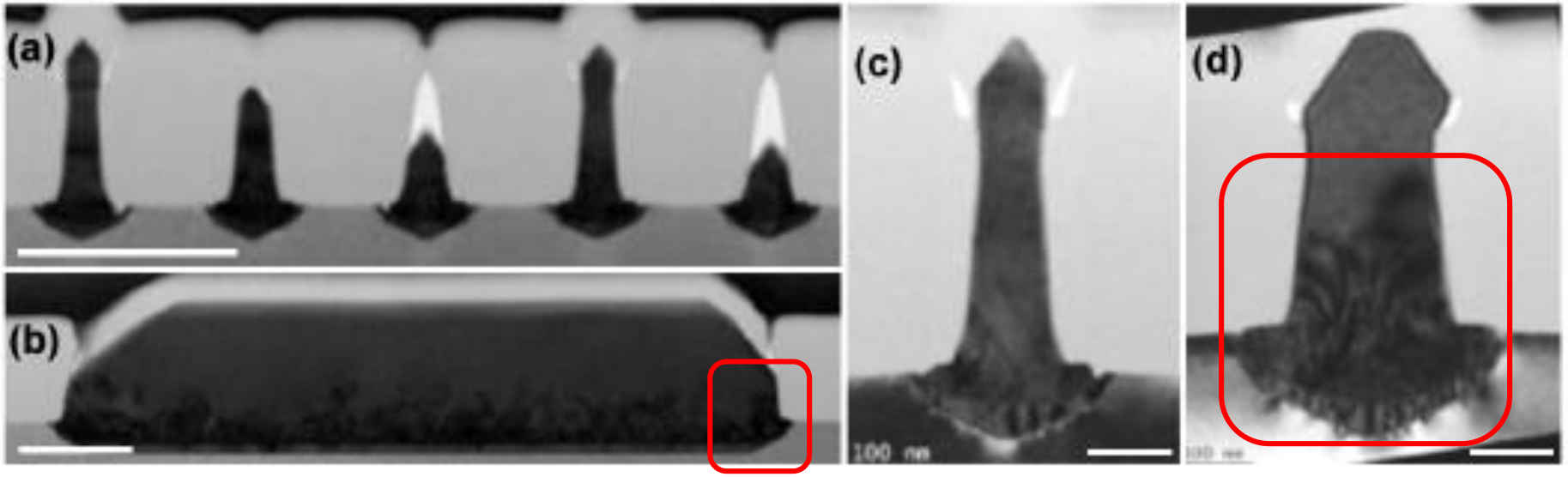
# Opportunity Window for Non-Si Channel

| Material | $\mu_e$ (cm²/Vs) | $\mu_h$ (cm²/Vs) |
|---|---|---|
| Diamond | 2200 | 1800 |
| Si | 1350 | 480 |
| Ge | 3900 | 1900 |
| InP | 5400 | 200 |
| GaAs | 8500 | 400 |
| InGaAs (53%) | 12000 | 300 |
| InAs | 40000 | 500 |
| GaSb | 3000 | 1000 |
| InSb | 77000 | 850 |




- Any new technology has to last at least 2 nodes
- SiGe channel is easier to manufacture
- High Ge content SiGe or even pure Ge to follow
- III-V materials have a narrow opportunity window




Ge/InP

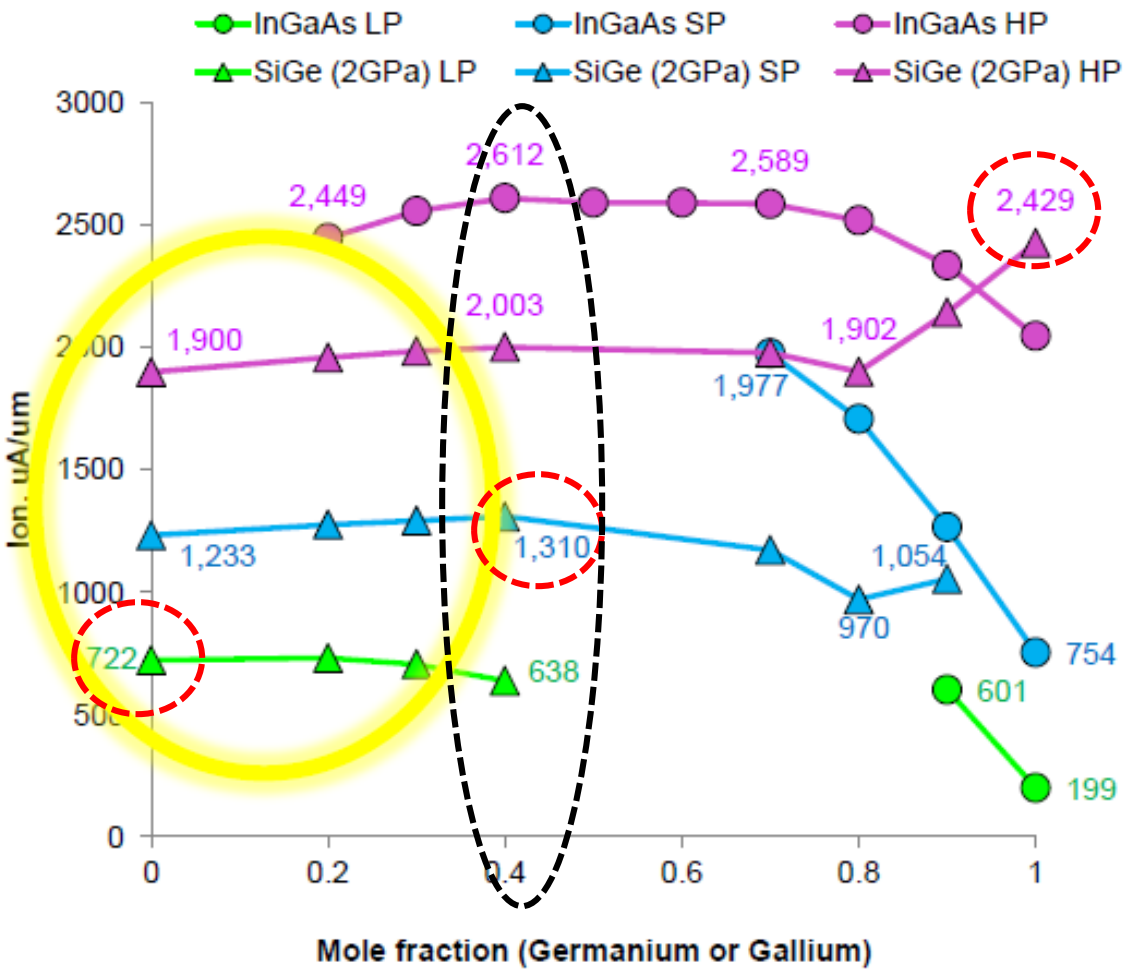
Figure 5. Cross-sectional TEM images, recorded along the (004) beam direction, of a sample where InP is grown in Shallow Trench Isolation (STI) structures by MOVPE. Trench widths are 80nm and 150nm for (a,c) and (b,d), respectively. Scale bars: (a,b) 500nm, (c,d) 100nm.

IMEC, ECS Oct 2012

Sadana of **IBM** gave the plenary talk "Doping Options for Dynamically Changing CMOS Landscape". His message for the 7nm node is that there are many issues with doping of III-V high mobility material making the reality of III-V for nMOS very difficult or unlikely.

IIT-2014

# Group IV vs III-V: Combination Champion




- Only Si, low Ge SiGe, and GaAs can match LP spec
- InGaAs with 10% In has competitive performance, but is too sensitive to In content
- This would bring severe variability
- So, silicon looks the best…
- SiGe with low Ge % can be used for stress engineering

Moroz, Synopsys, May 2014 ECS Conf.



7nm NMOS FinFET

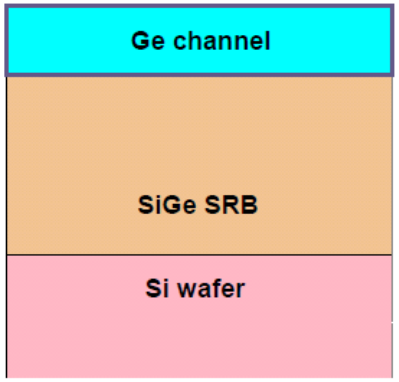


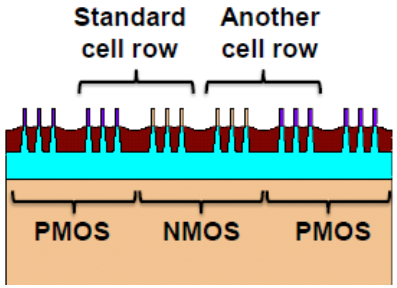
J.O.B. Technologies (Strategi
Marketing, Sales &
Technology)

Bohr, Intel said 9/18: Ge leading candidate for pMOS but for nMOS very low leakage problem due to BTBT for both Ge and III-V!

# Common SRB Epi for NMOS & PMOS

Wafer before fin patterning

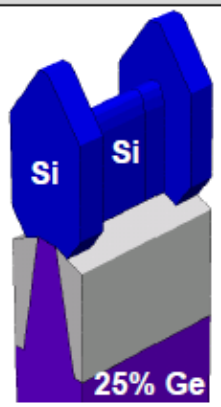
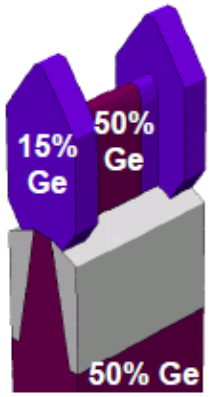
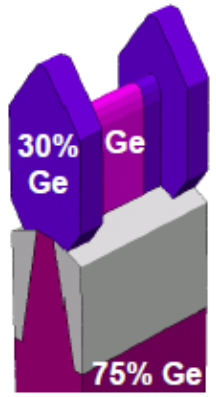
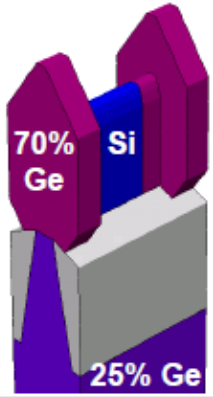
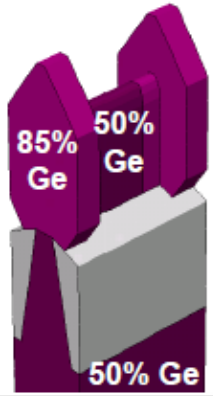
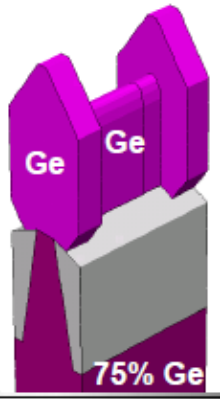



- Considering cell heights (pitches) of 360 nm, SRB's for NMOS and PMOS

 9

# 7nm Stress Engineering: SRB + S/D Epi

| | Si channel | SiGe channel | Ge channel |
|---|---|---|---|
| NMOS +1.5 GPa |   |   |   |
| PMOS -1.5 GPa |   |   |   |

Victor Moroz, Synopsys, July 10, 2014 WCJUG seminar.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

 10 Stress analysis in S-Process

Blanket Ge-layer first
then Ge-Fin etch

Selective Ge-epi Fin

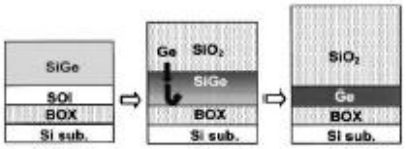
## Growing Ge Channels



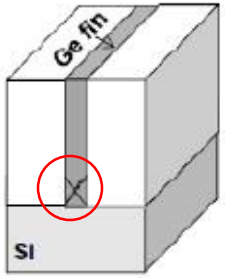
Ge on Si Bulk using SRB | GeOI using Wafer Bonding | GeOI using Enrichement | Aspect Ratio Trapping (ART)

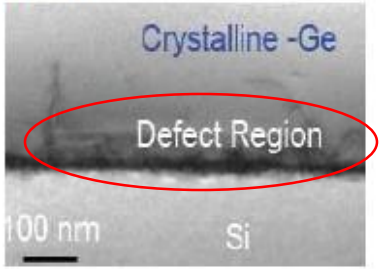
Currie et al., APL 1998 (MIT)

C. Deguet, ECS Proceeding 2005 (LETI)

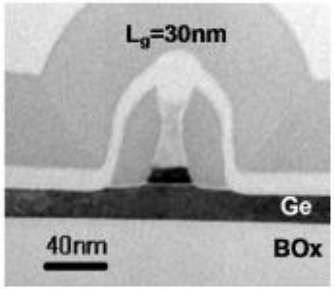



Nakaharai et al., APL 2003

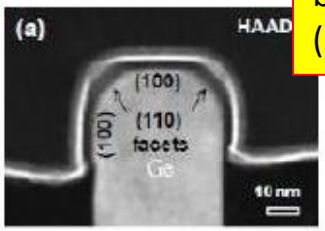



Nayfeh et al., APL 2004 (Stanford)




L. Hutin *et al.* IEEE EDL 2010,
VLSI-TSA 2010




M. Van Dal et al., TSMC, IEDM 12

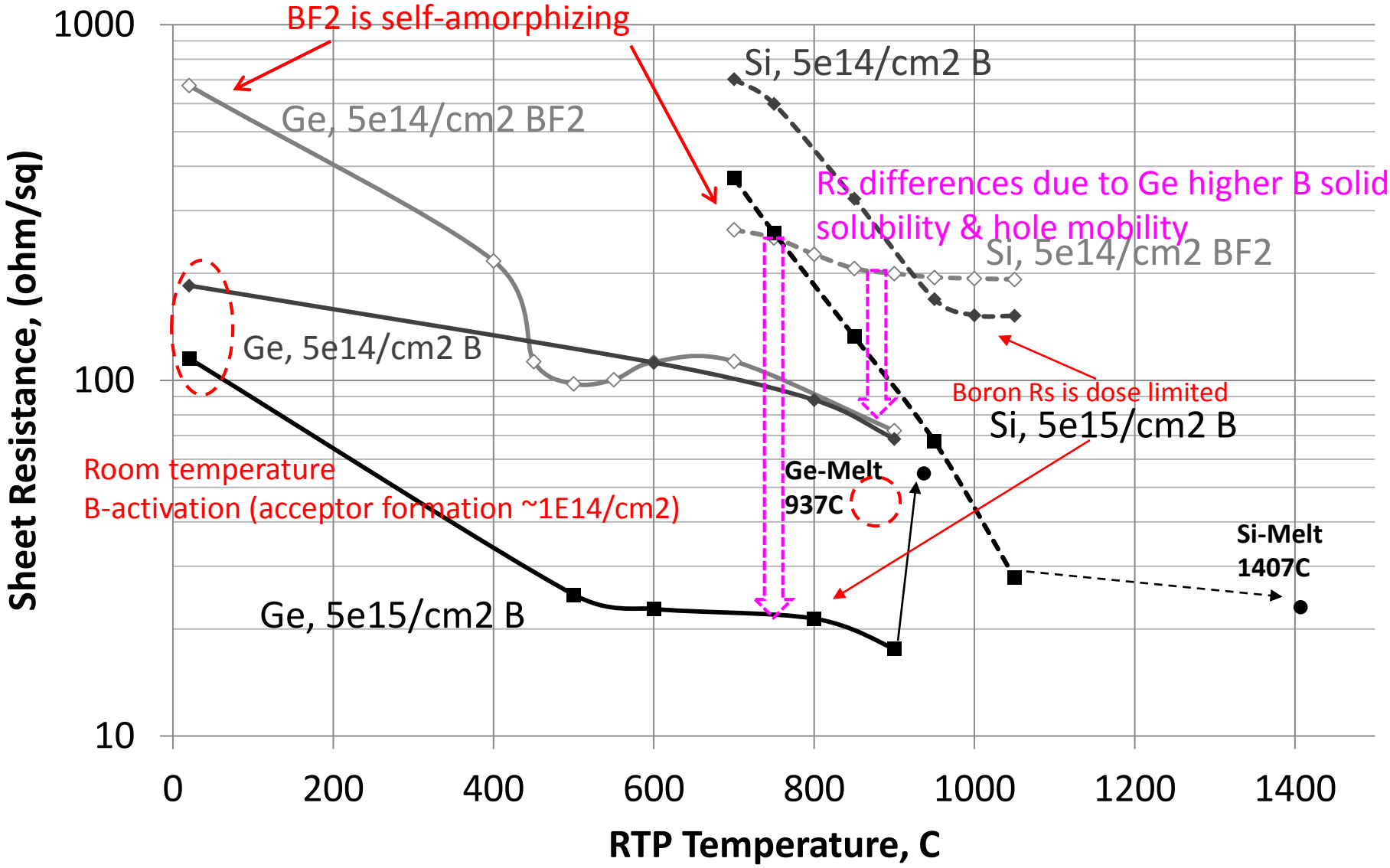
**Borland: Localized Ge-LPE by Laser Melt**

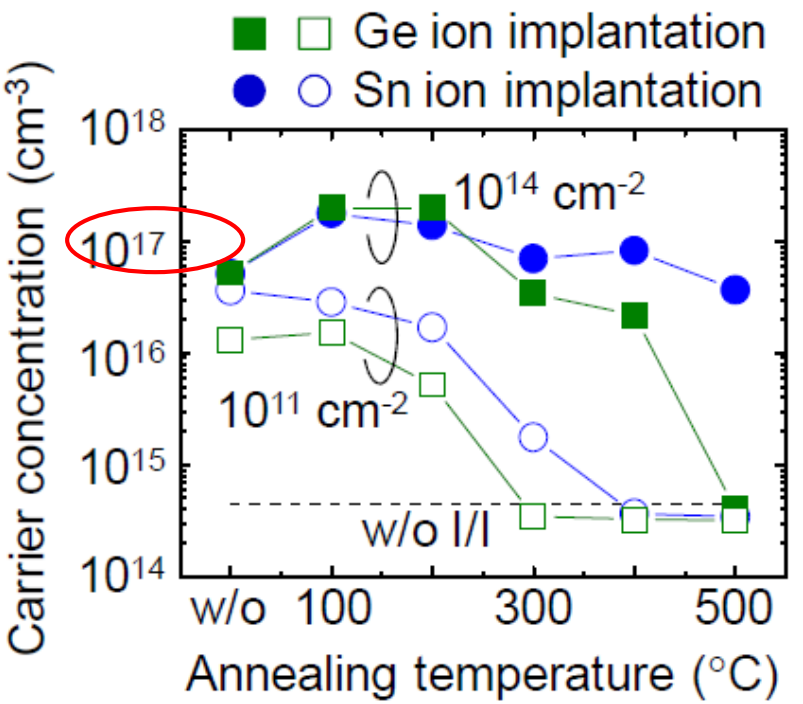
Oct 2004 ECS: Ge-GCIB/Infusion (E17/cm2)

June 2013 IWJT: Ge-plasma implant (1E17/cm2)

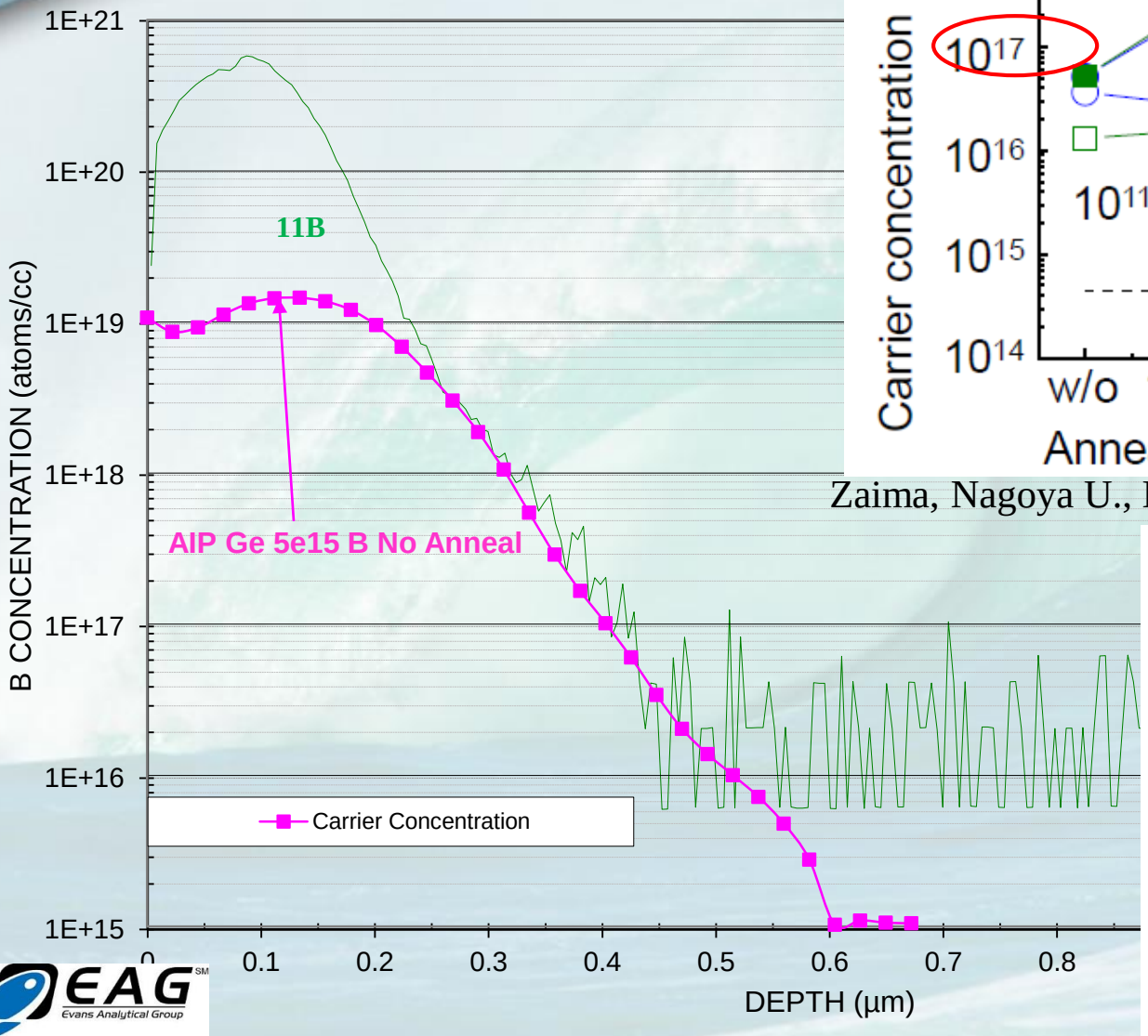
Oct 2014 ECS: Ge-beamline implant (5E16/cm2)

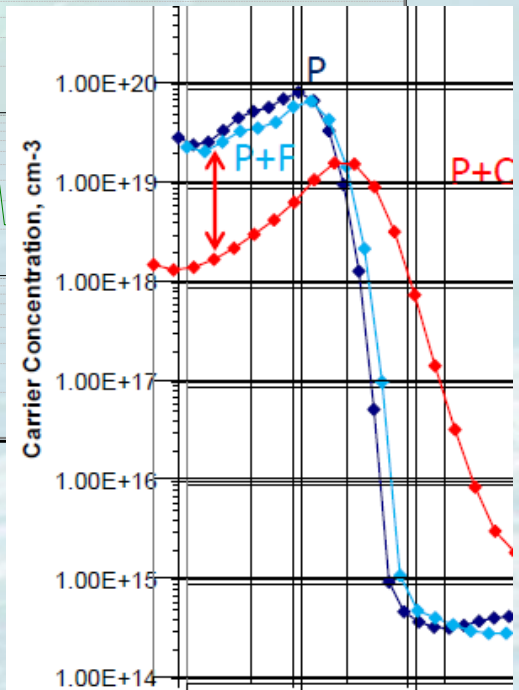
# Boron Activation in Si & Ge






Zaima, Nagoya U., ECS Oct 2014, paper P7-1772



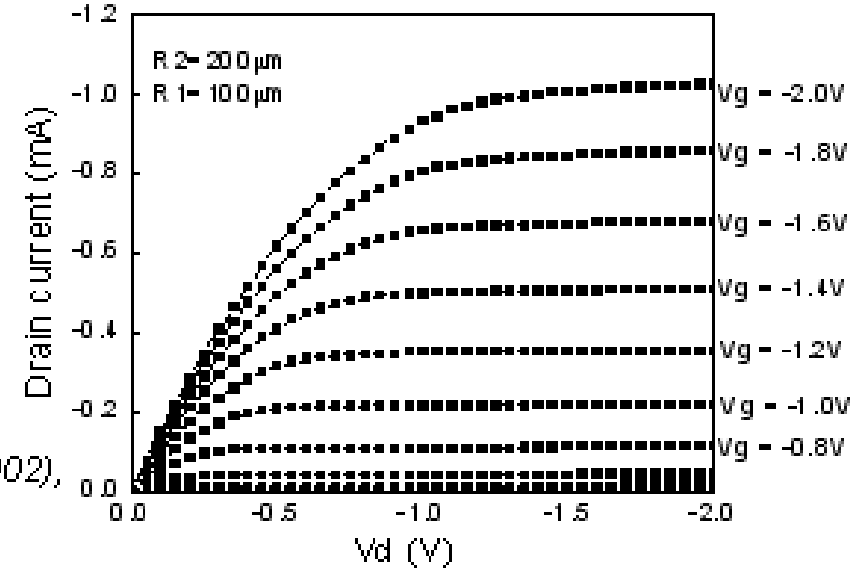




Borland & Konkola, IIT-2014

# Germanium MOSFETs

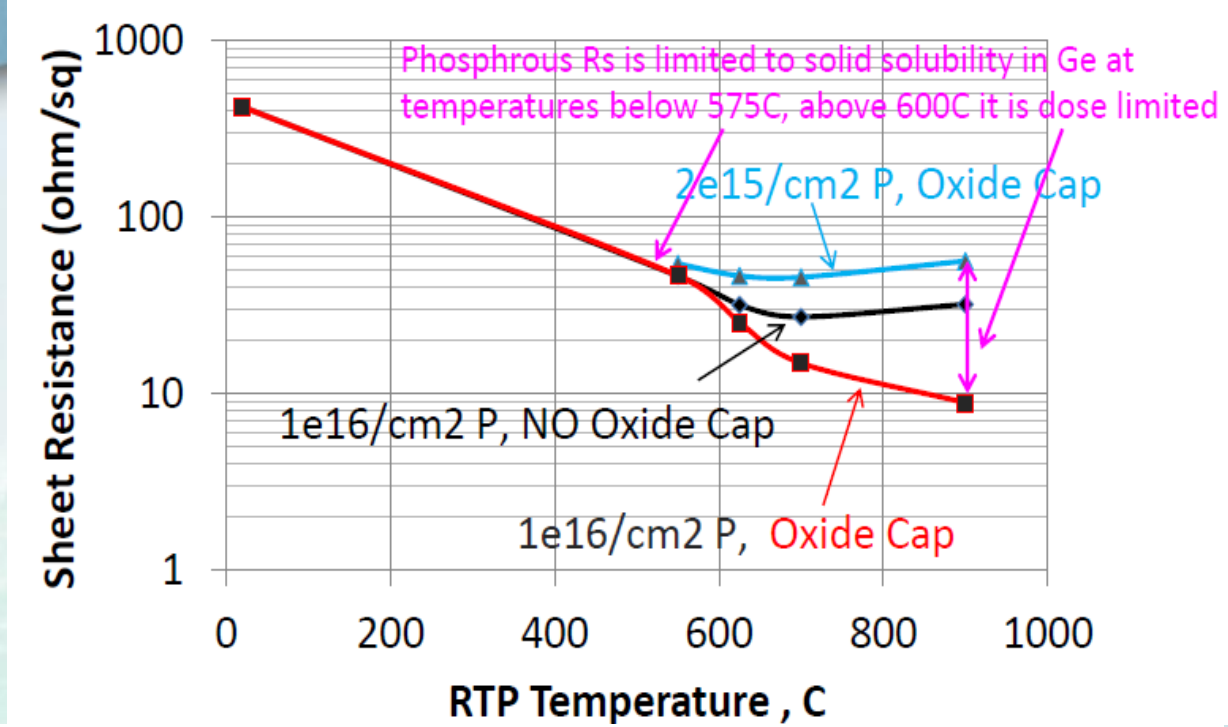
| | Ge | Si |
|---|---|---|
| $\mu_n$ ($cm^2/Vs$) | 3900 ← | 1500 |
| $\mu_p$ ($cm^2/Vs$) | 1900 ← | 450 |
| Eg (eV) | 0.66 | 1.12 |

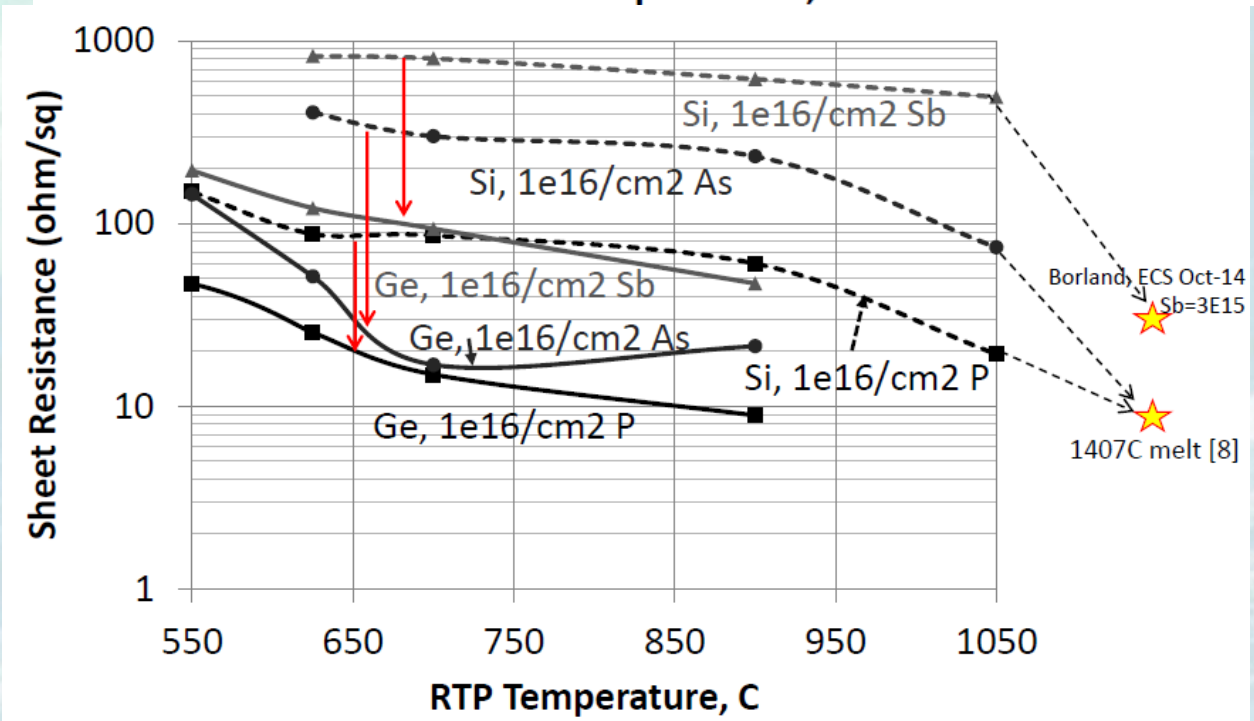
*Rosenberg et al. EDL 9, 639 (1988), Shang et al. IEDM(2002), Chui et al. IEDM (2002), Bai et al. VLSI (2003)*



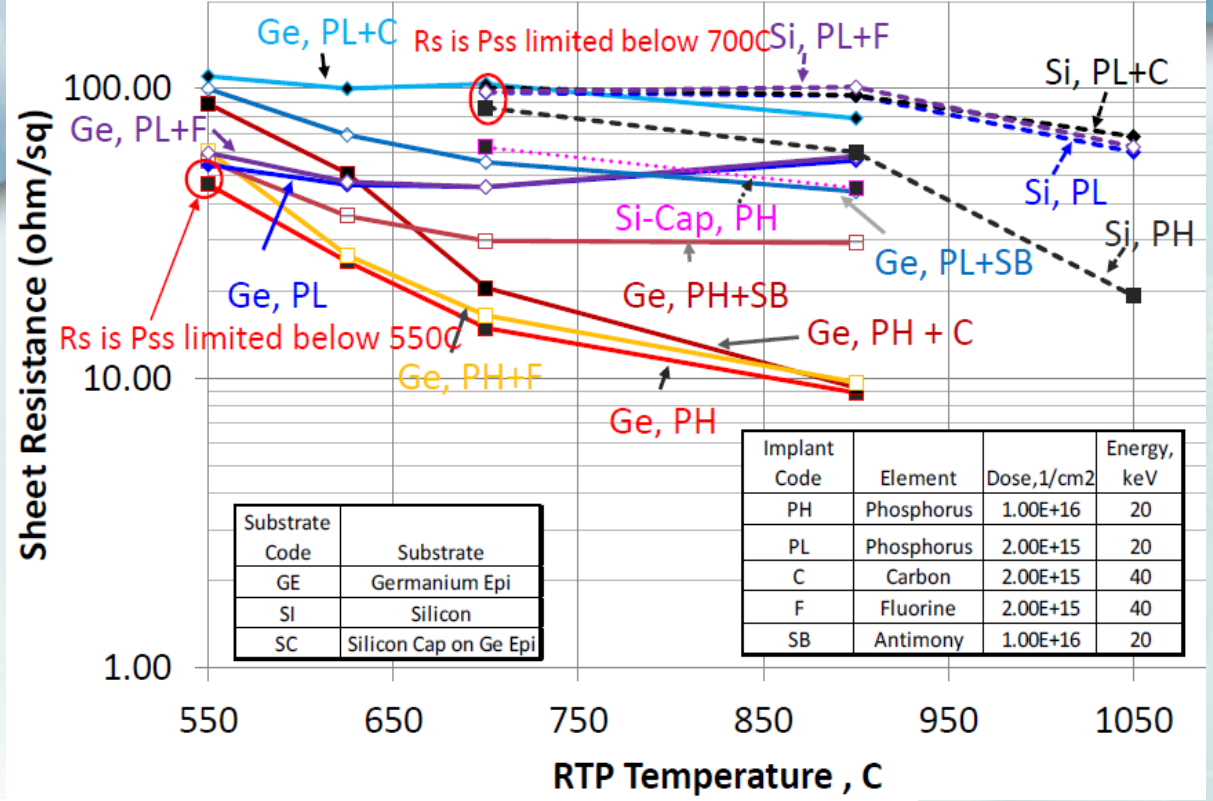

*Chen, Guha, Banerjee, et al. TED 2004*

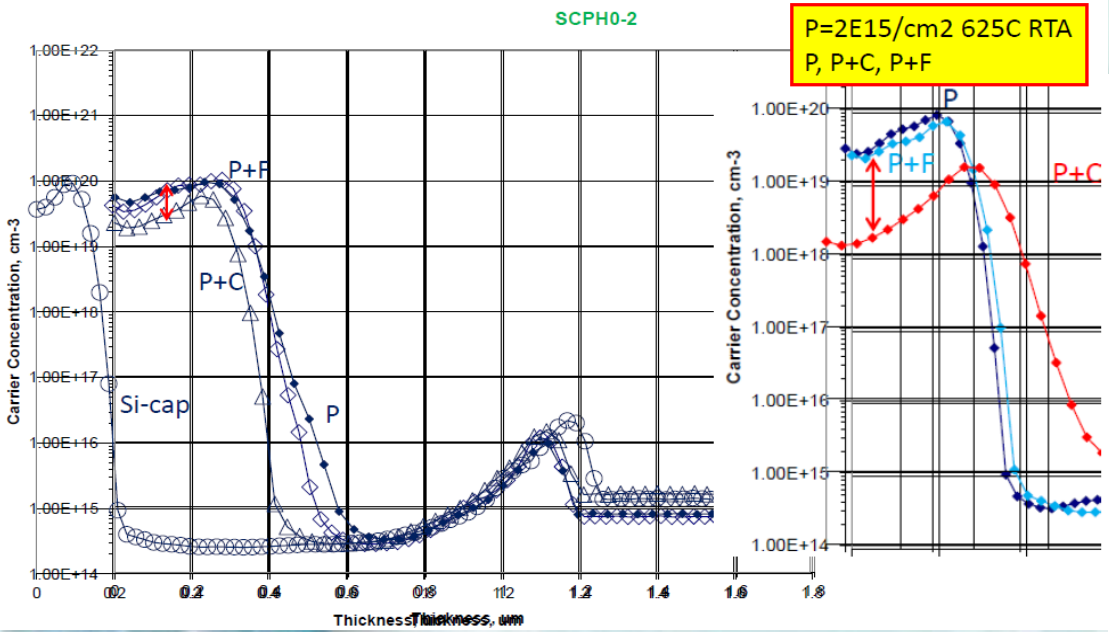
- Bulk Ge has higher electron (2.5x) and hole (4x) mobility than Si, and can potentially lead to faster MOSFETs and more balanced N vs. PMOSFETs.
- Native oxide on Ge surface is not stable; $GeO_2$ water soluble, GeO volatile at low T. Deposited high-k gate dielectrics promising
- Ge substrates brittle, lower thermal conductivity (0.6W/cm-K vs. 1.5 for Si)—Ge-on-Si
- Smaller Ge bandgap than Si broadens absorption spectrum; optoelectronic integration on CMOS?
- Performance *much worse than expected*, especially for NMOSFETs, probably because of poor interface between Ge and high-k gate dielectric, as well as poor dopant activation and interface between metal- source/drain
- Higher junction leakage in Ge, especially at high T
- Higher dielectric constant in Ge leads to worse electrostatics (DIBL, SS)



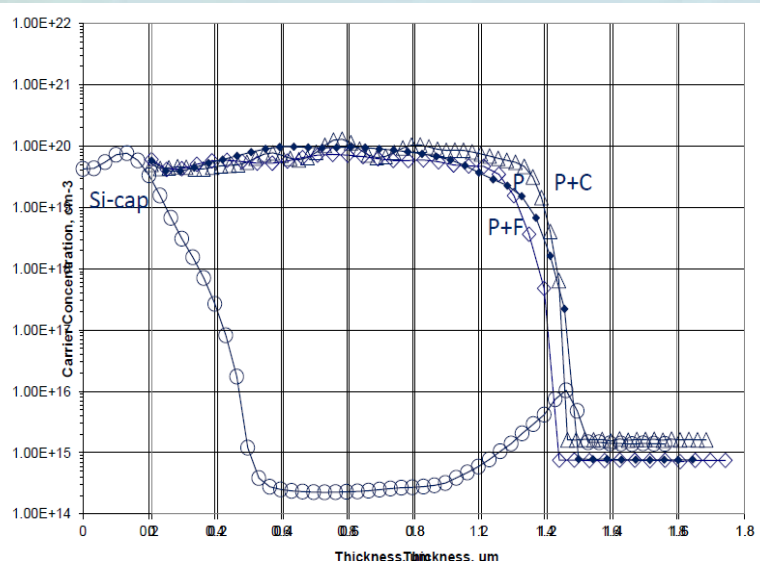




Borland & Konkola, IIT-2014



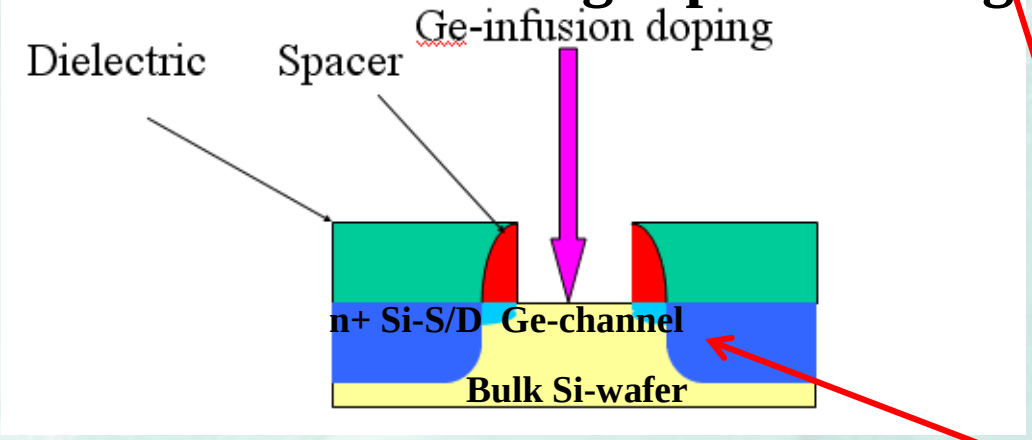




Borland & Konkola, IIT-2014



# Ge-channel Formation by Ge implant, plasma or GCIB doping (n+Si-cap S/D doping)

## nMOS Ge-channel formation using replacement gate process flow

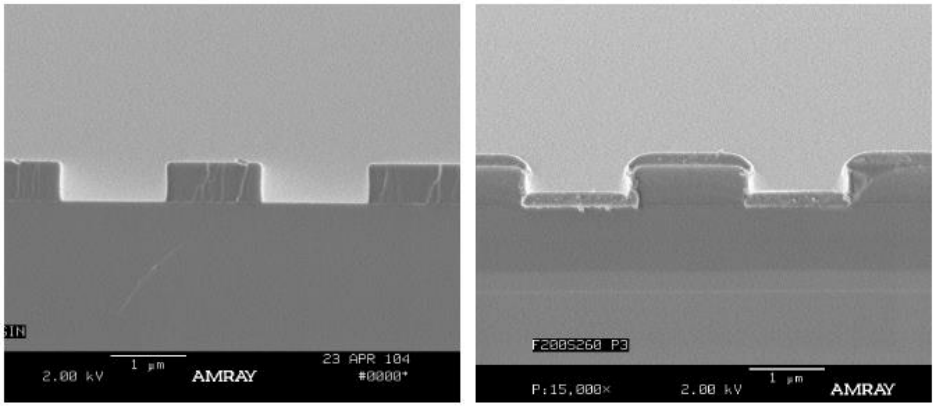



Borland et al., SST July 2005 & US Patent #7,259,036 Aug 22, 2007

**nMOS n+ Si-S/D**

***Room Temperature Processing : PR compatible***

200nm Ge Infusion Deposition On Photo Resist



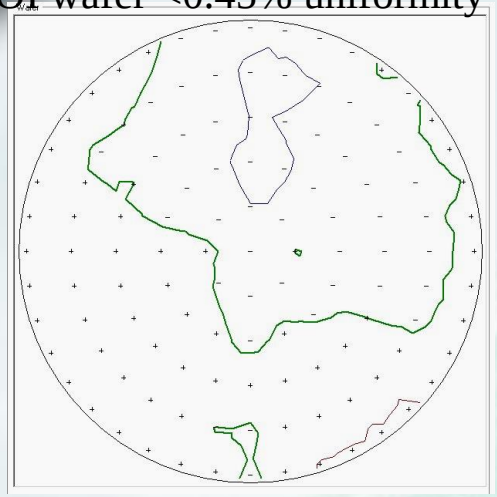

Borland et al., ECS Oct 2004

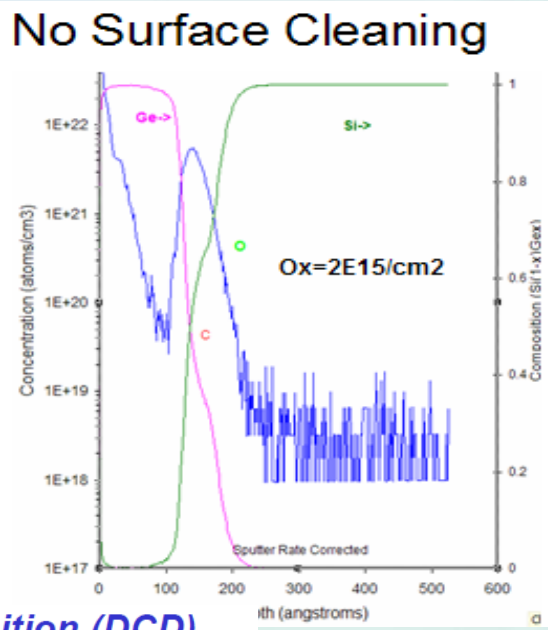
epion corporation

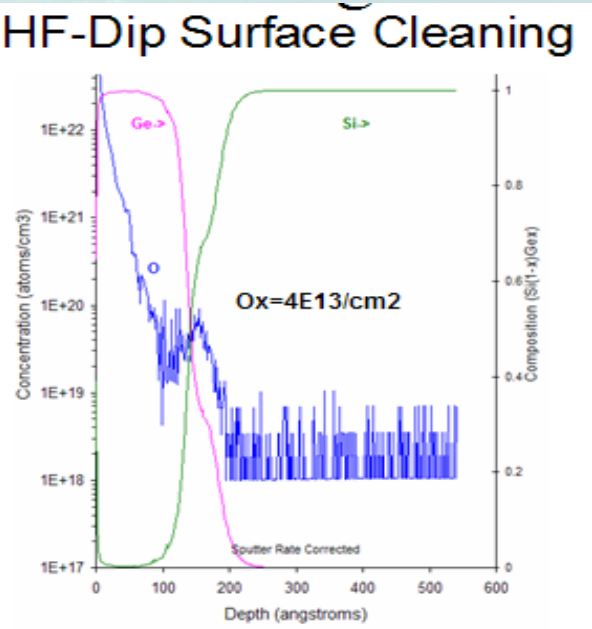
# GCIB Ge-Doping/Deposition (Solid Phase Epitaxy)

## Medium Dose Increase Bss, High Dose Dose Controlled Deposition (DCD)

70nm Ge-DCD on 300mm bulk
& SOI wafer <0.45% uniformity



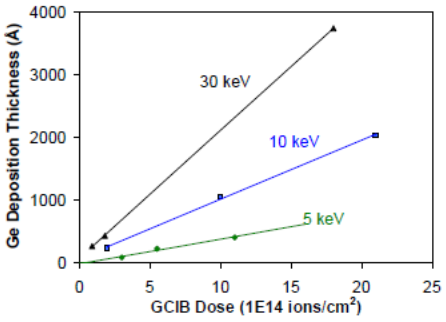


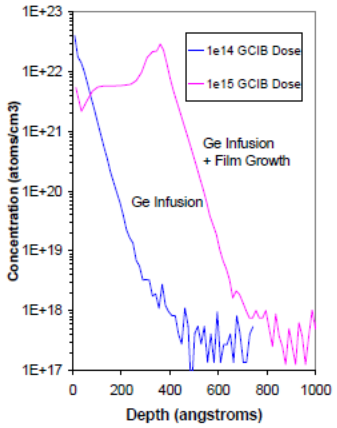



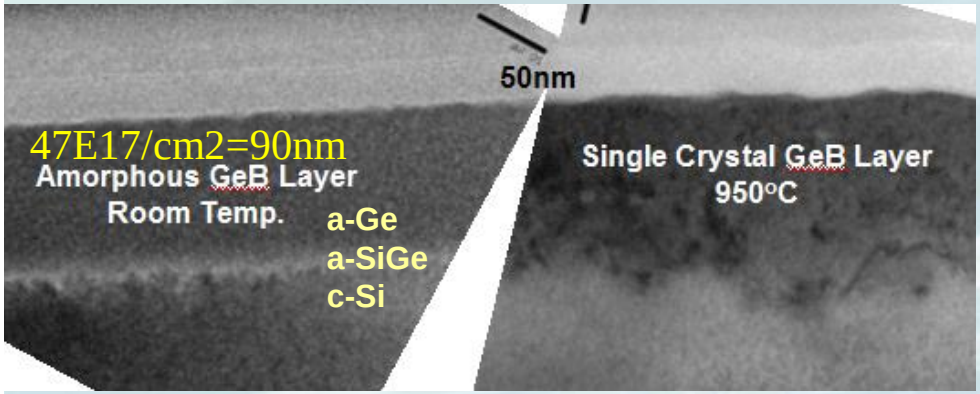

## *Ge-Infusion: Dose Controlled Deposition (DCD)*

Thickness has linear relationship to dose

Deposition rate is ~ to Energy




Borland et al., ECS Oct 2004



epion corporation

# Localized/Selective Ge & SiGe Formation By Liquid Phase Epitaxy (LPE) Using Ge+B Plasma Ion Implantation And Laser Melt Anealing

**IWJT June 6, 2013**

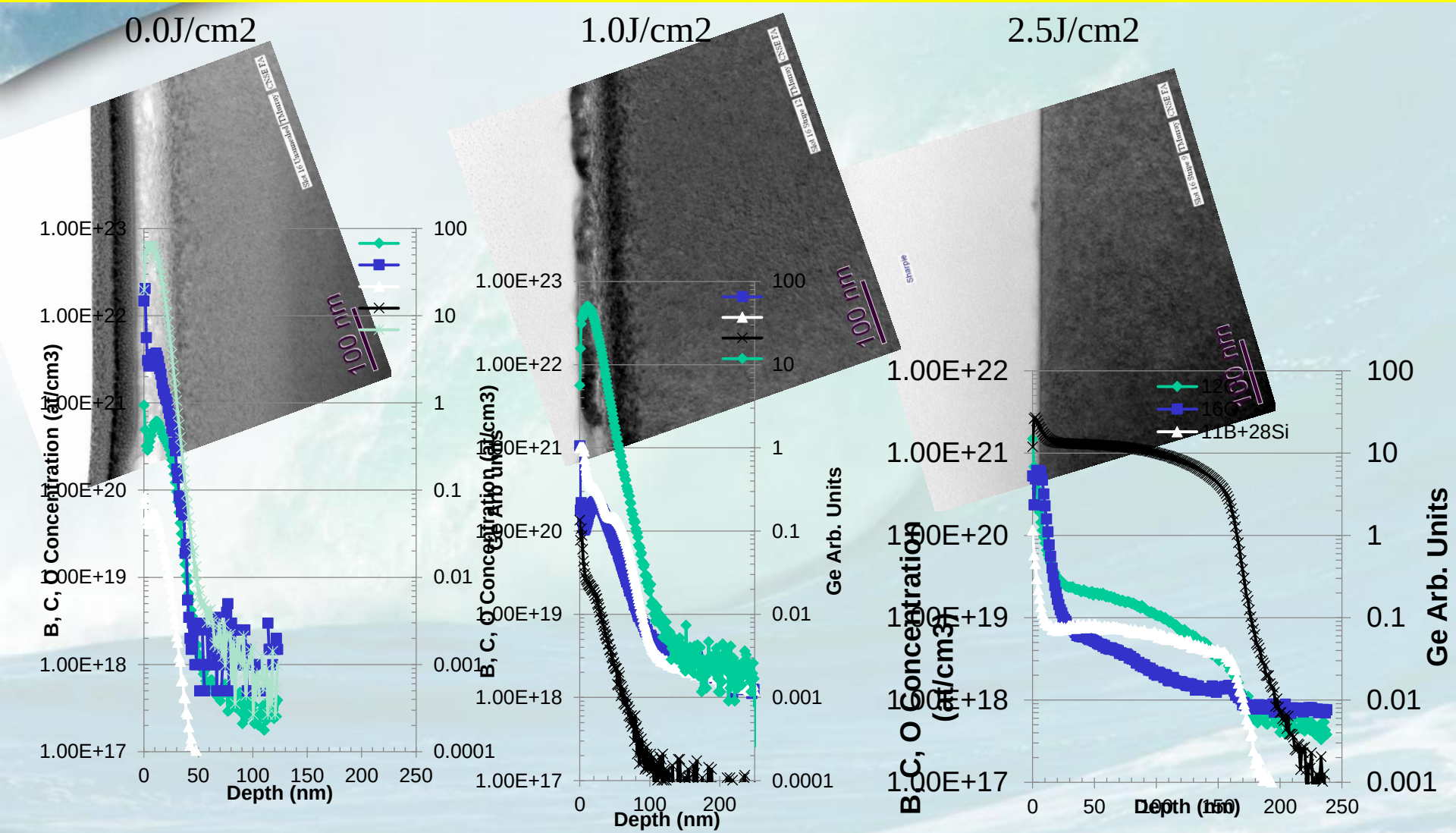
**JOB Technology, Micron, Innovavent, Excico, KLA-Tencor, CNSE, EAG & UCLA**

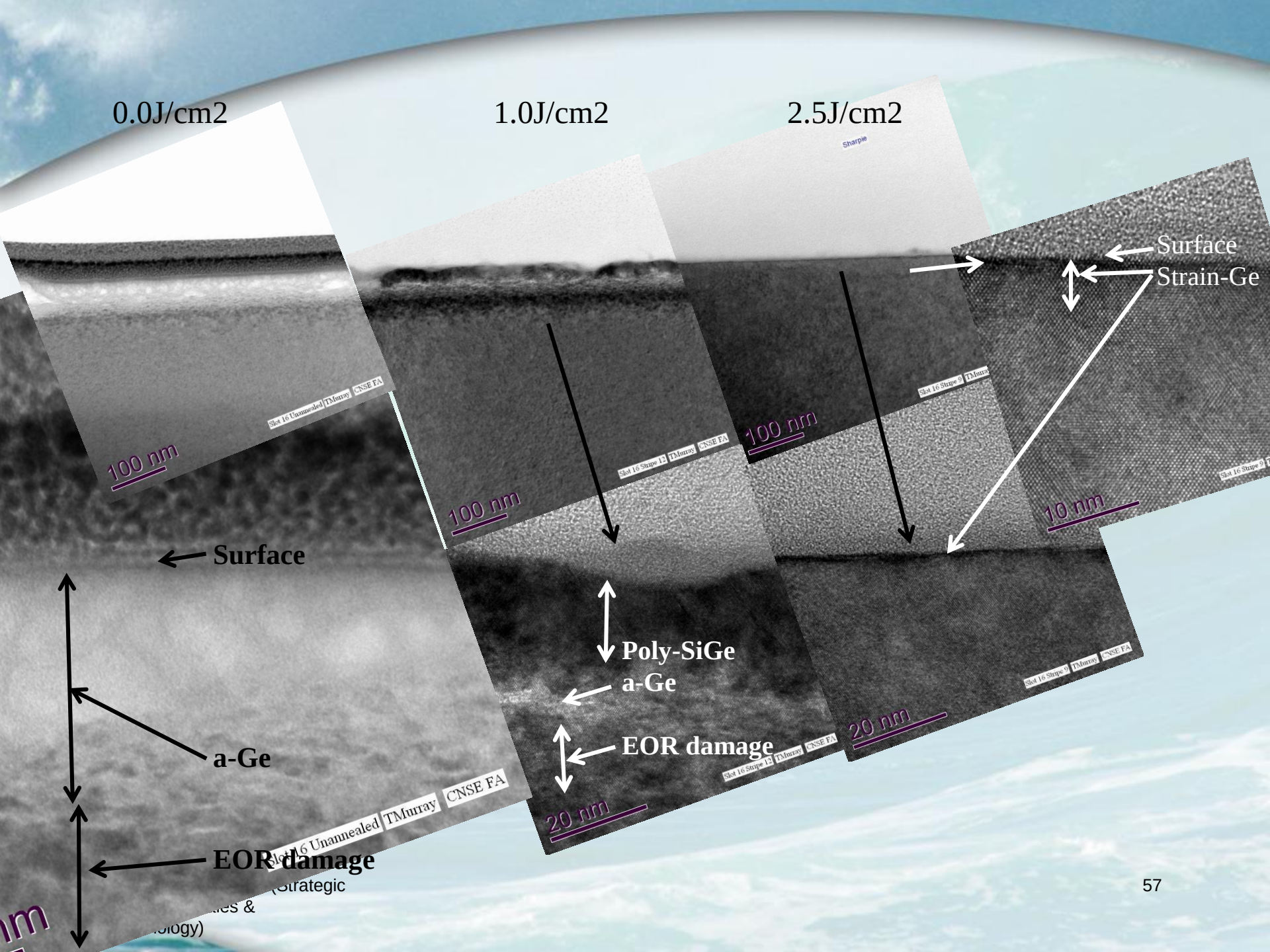
Ge 3keV at 1E16/cm2 (Ge=20%) & 1E17/cm2 (Ge=55%)

B2H6 500V at 4E15/cm2 & 4E16/cm2

Ge+B Plasma Implanted Wafers Provided by Micron
Laser Melt Annealing Provided by Innovavent & Excico

# Why is Plasma Ge=1E17/cm2 only 55% Ge while Ge=1E16/cm2 20% Ge?

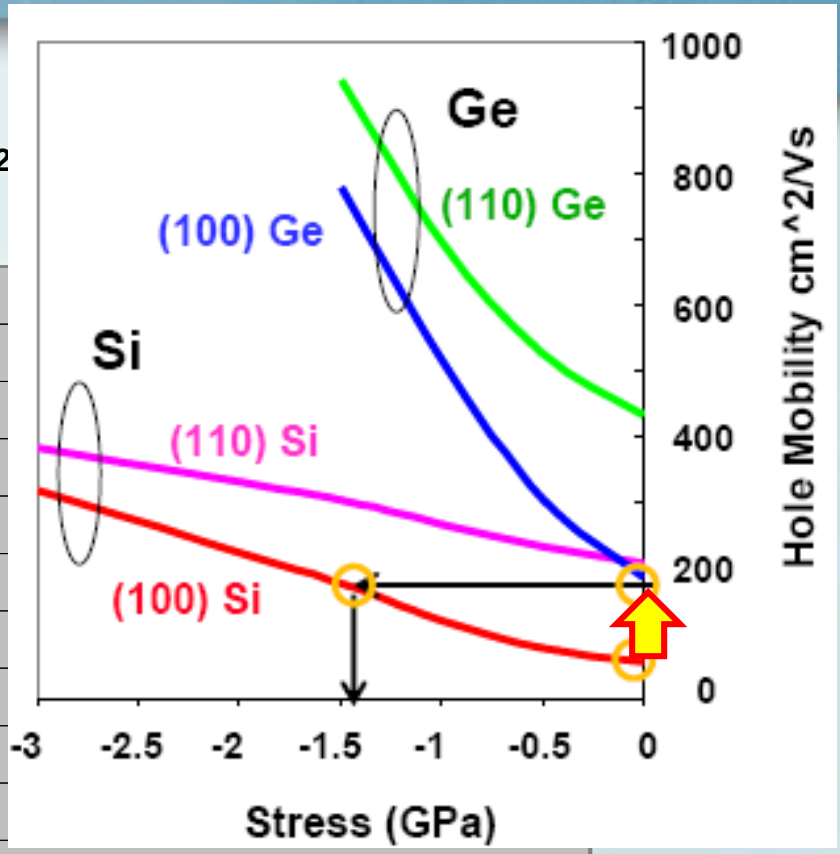



0.0J/cm2
1.0J/cm2
2.5J/cm2
Surface
a-Ge
EOR damage
Poly-SiGe
a-Ge
EOR damage
Surface
Strain-Ge
100 nm
100 nm
100 nm
10 nm
20 nm
20 nm
Slot 16 Unannealed TMurray CNSE FA

# UCLA Hall Analysis of 308nm

Slot#14:Ge=1E16+B=4E15

Slot#18: Ge=1E17+B=4E16



# Liquid Phase Epitaxy (LPE) Formation of Localized High Quality/Mobility Ge & SiGe by High Dose Ge-Implantation with Laser Melt Annealing for 10nm and 7nm Node

## Oct 6, 2014 ECS Conference on SiGe & Ge Technology

John Borland[1,2], Michiro Sugitani[3], Peter Oesterlin[4], Walt Johnson[5], Temel Buyuklimanli[6], Robert Hengstebeck[6], Ethan Kennon[7], Kevin Jones[7] & Abhijeet Joshi[8]

**[1]JOB Technologies, Aiea, Hawaii**

**[2]AIP, Honolulu, Hawaii**

**[3]SEN, Shinagawa, Tokyo, Japan**

**[4]Innovavent, Gottingen, Germany**

**[5]KLA-Tencor, Milpitas, California**

**[6]EAG, East Windsor, New Jersey**

**[7]University of Florida, Gainsville, FL**

**[8]Active Layer Parametrics, LA, CA**

# JOB Sample 3 Si Sb+Ge 3E15 5E16 No Anneal (Sb, Ge)

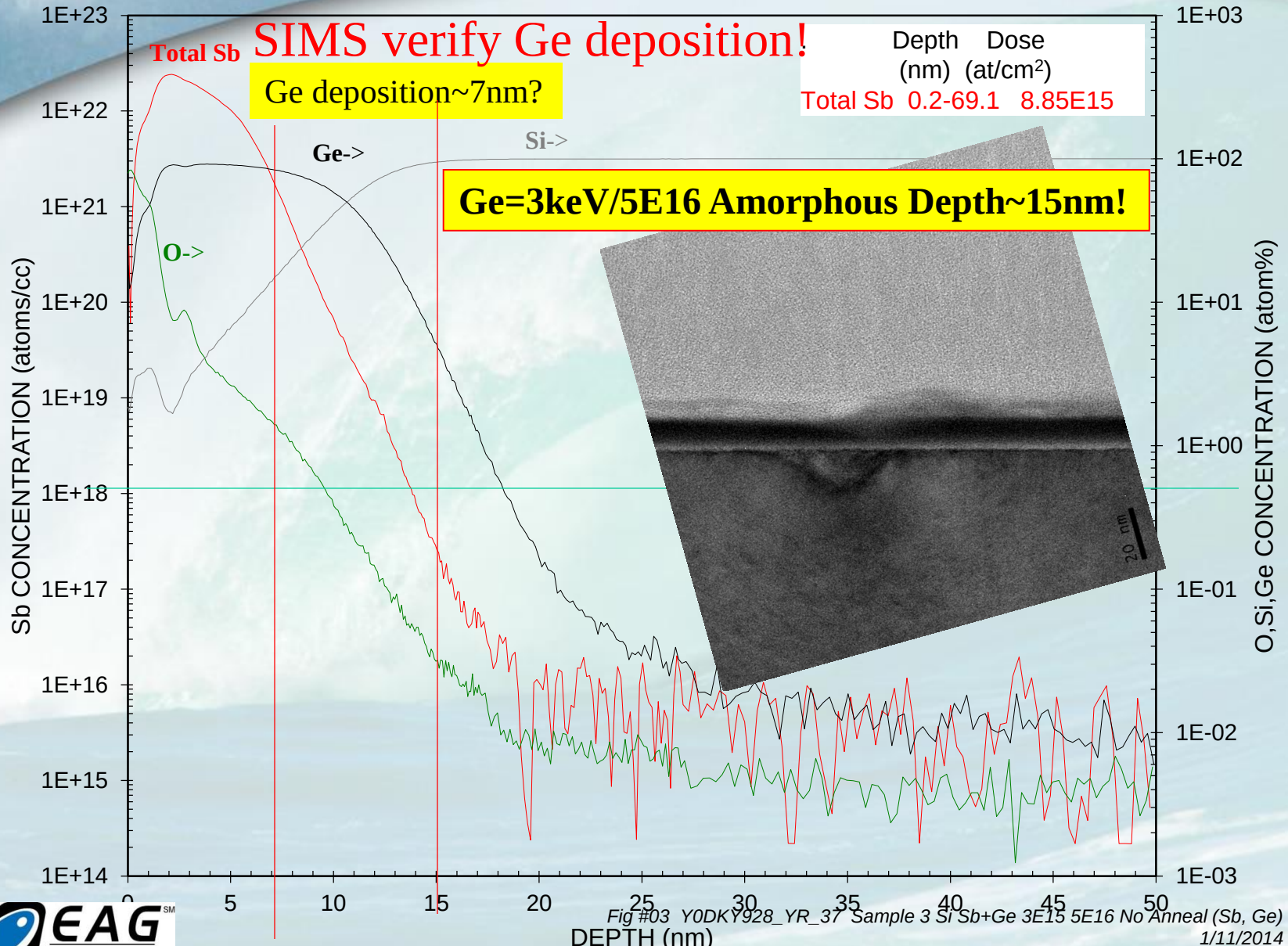
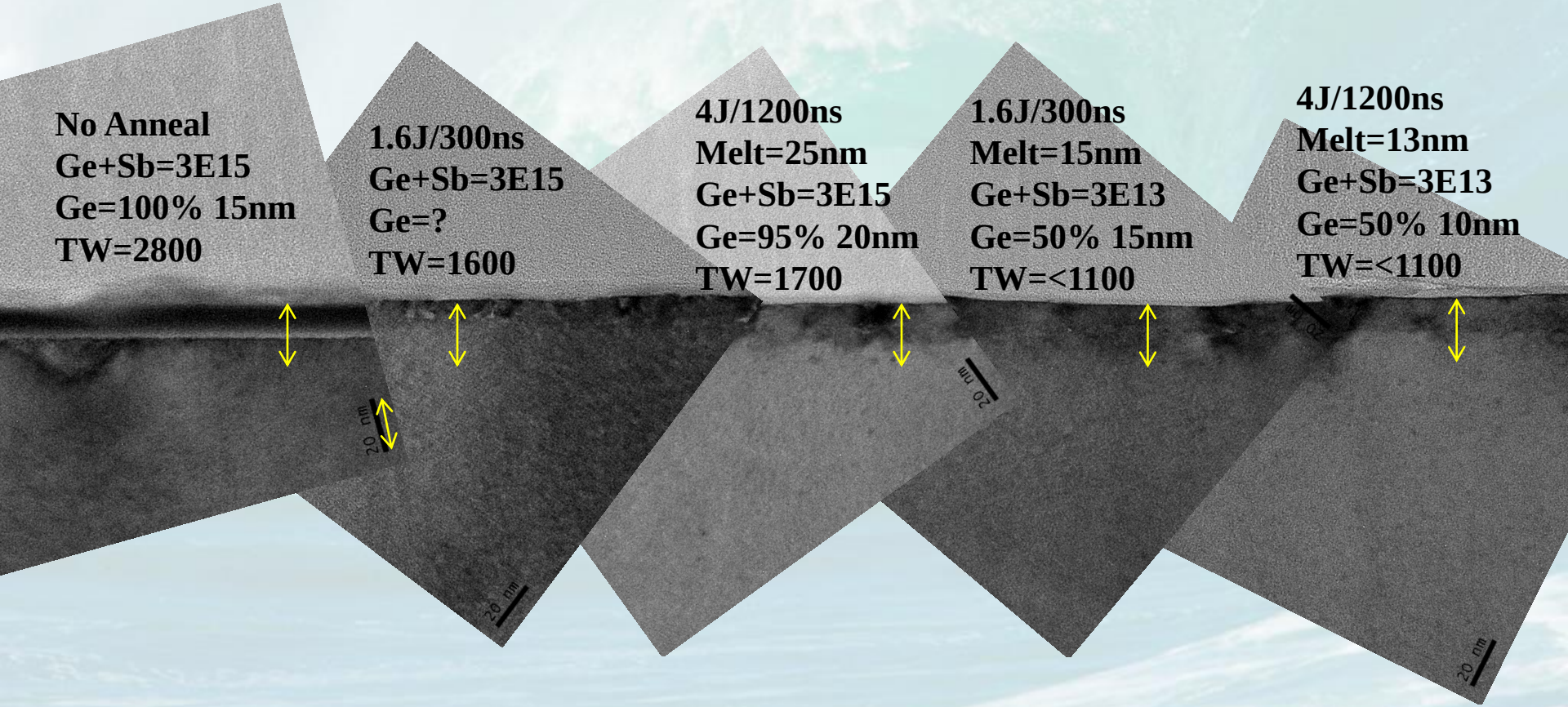



*Fig #03 Y0DKY928_YR_37 Sample 3 Si Sb+Ge 3E15 5E16 No Anneal (Sb, Ge) 1/11/2014*

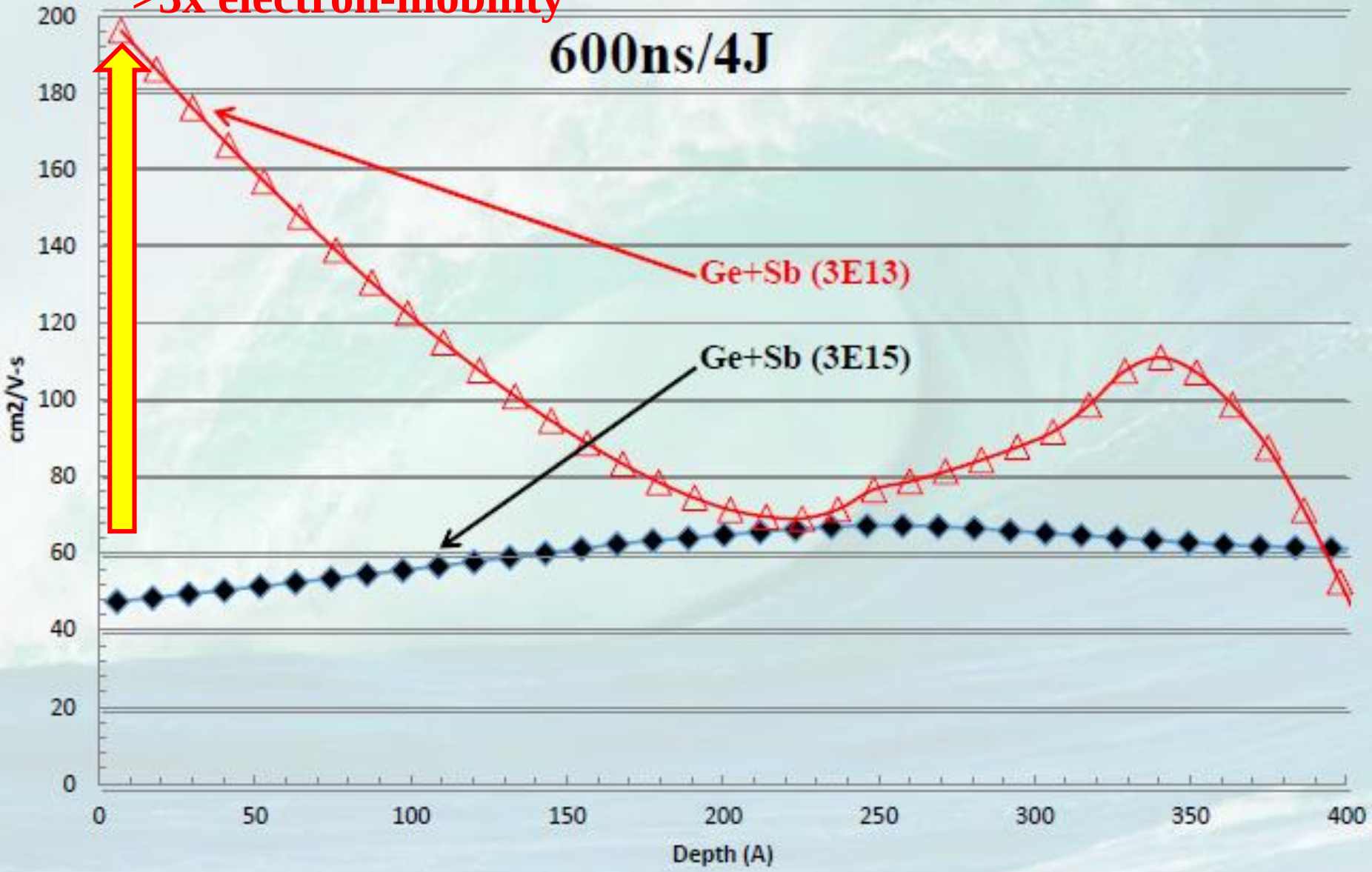
EAG Evans Analytical Group

...ogies (Strategic Marketing, Sales & Technology)

# X-TEM For Ge+Sb 3E13 & 3E15



# >3x electron-mobility



Si-Photonics paper K-1-1 on "Ge Active Photonic Devices on Si for Optical Interconnects" was a invited review paper so no new data only a review. In Fig.2 below he showed a 800°C Ge-Epi post anneal can reduce TDD from $10^9/cm^2$ to $<10^7/cm^2$. Fig.4 shows the Si-cap for n+ doping of the PIN.

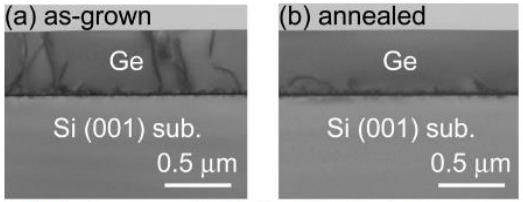



Fig. 2 Typical cross-sectional transmission electron microscope images for (a) as-grown Ge (600°C) and (b) annealed Ge (800°C).

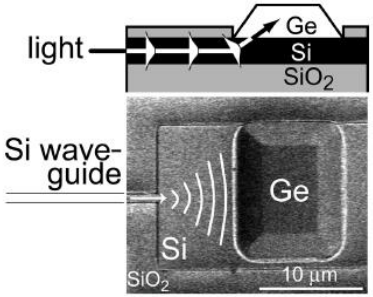



Fig. 3 A typical scanning electron microscope images for Ge selectively grown on an SOI layer.

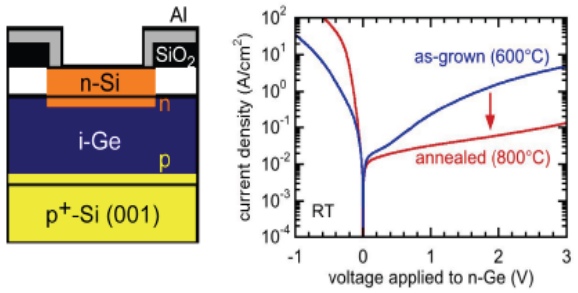
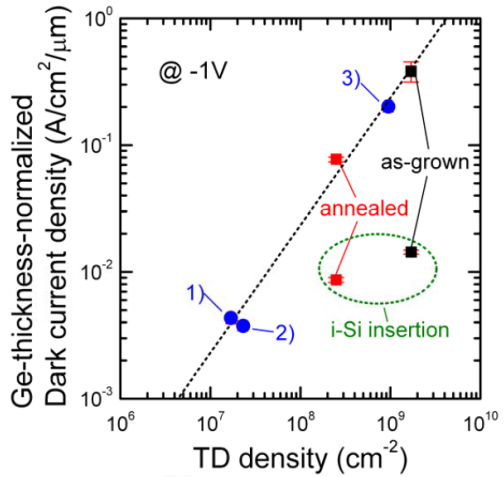
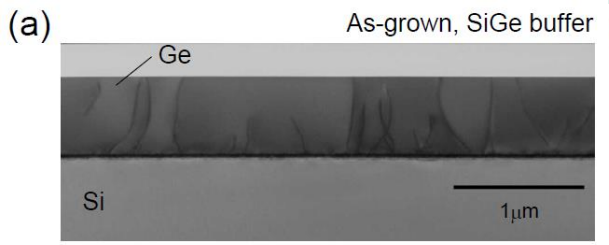
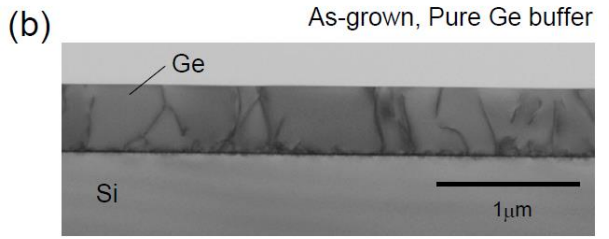


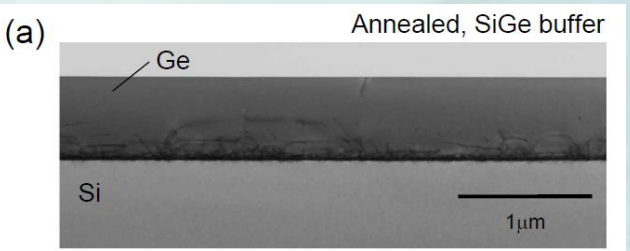

Fig. 4 (a) Schematic structure of Ge *pin* diode on Si and (b) typical *I-V* curves.

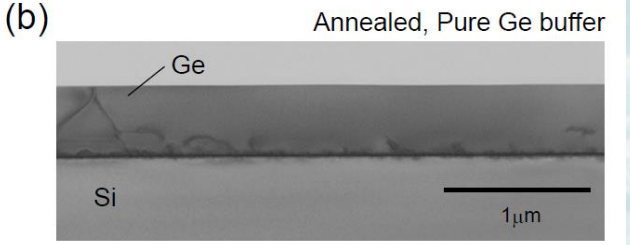
Univ of Tokyo, SSDM-2013



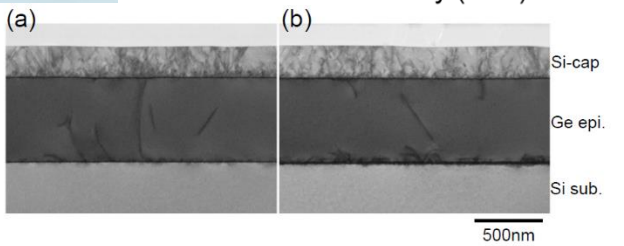
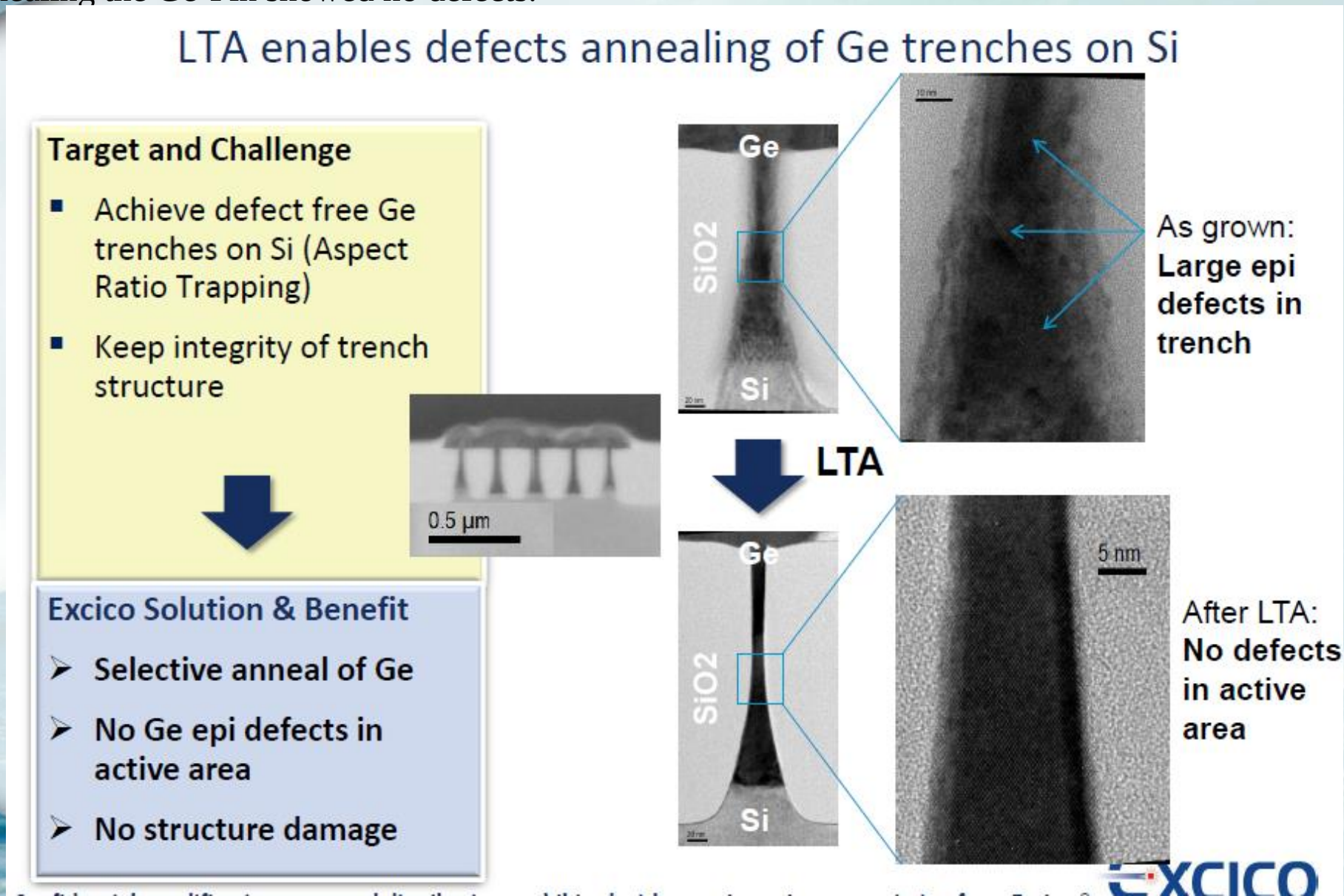



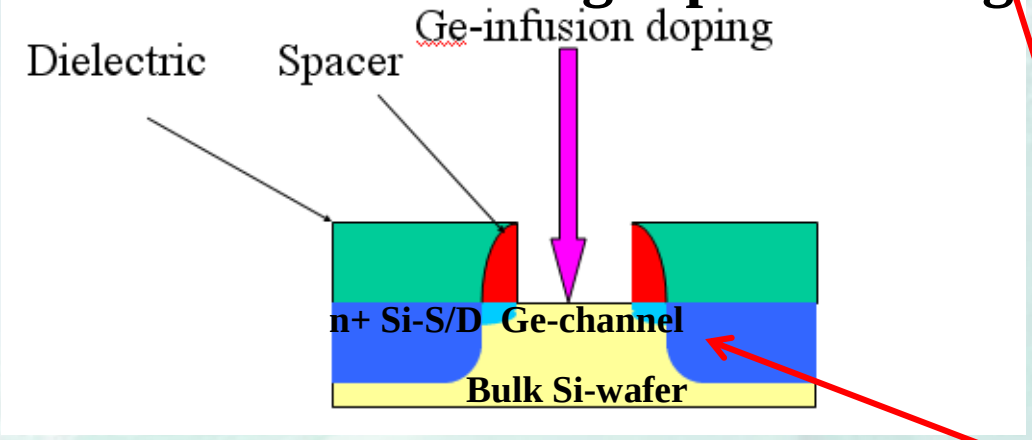

**Fig. 4.3** Cross-sectional TEM images of as-fabricated photodiodes using (a) as-grown Ge and (b) annealed Ge.

**IWJT-2014 Paper S1-02**: Wang of Excico on "Laser Thermal Annealing: A low thermal budget solution for advanced structures and new materials". In his presentation material he showed an interesting slide of a Ge-Fin structure after Ge-epi it had large epi Fin defects but after laser melt annealing the Ge-Fin showed no defects.



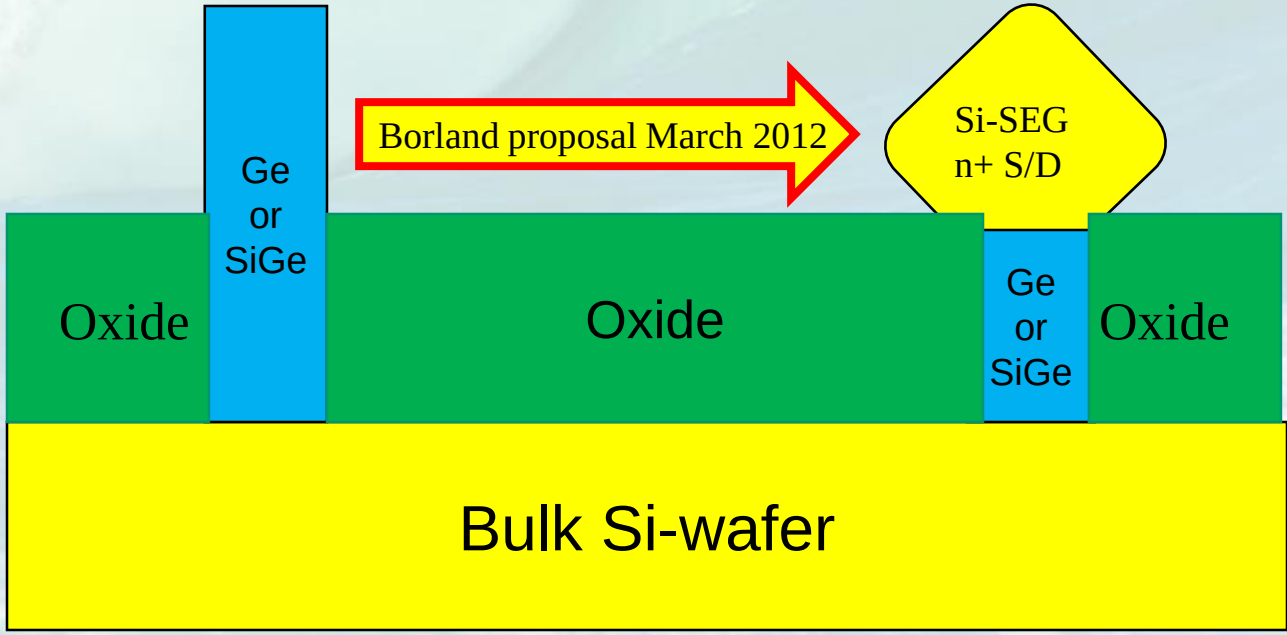
# Ge-channel Formation by Ge implant, plasma or GCIB doping (n+Si-cap S/D doping)

## nMOS Ge-channel formation using replacement gate process flow




Borland et al., SST July 2005 & US Patent #7,259,036 Aug 22, 2007

**nMOS Ge-Fin/channel** **nMOS n+ Si-S/D**



# Outline

- Introduction
- 22nm Node:
- 14/16nm Node:
- 10nm Node:
- Summary
  - High tilt 35-45 degrees bi-mode or quad-mode implantation will continue to be used for FinFET SDE & S/D doping for 14nm, 10nm and 7nm node.
    - Amorphous implantation of the Fin is Good as it leads to highest dopant activation and stacking fault stressor formation.
  - Ge or SiGe-FinFET at 10nm or 7nm node will require Ge-epi first approach for low defects by CVD or LPE and mesa etch sidewalls.
    - Low Ge-Fin n+ junction leakage will require <625C activation, Si-capping layer or mesa etch sidewalls.
    - Implant damage also creates acceptors so amorphization is preferred for p+ & n+ junctions in Ge
    - Laser melt annealing best for localized shallow n+ USJ.