Laser Spike Annealing for FinFETs

Jeff Hebb, Ph.D.
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Outline

- LSA Overview and Key Features
- FinFET Process Flow
- LSA Applications for FinFET
- Summary
LSA Overview

Key Attributes

Within-die Uniformity
- CO2 Laser: $\lambda \sim 10\mu m$
- P-polarized, brewster angle

Within-wafer & Wafer-to-wafer
- Temperature feedback control

Dwell time $= \frac{w}{v_x}$
Pattern Effects: Thin Film Interference

**FLA & DL**
- Short $\lambda$
- Normal incidence

**LSA**
- Long $\lambda$
- Brewster angle
- $p$-polarization

- Pattern effects caused by thin film interference variations $\rightarrow$ severe at short $\lambda$
- Long $\lambda$ insensitive to device film variations
Pattern Effects: Scattering and Light Trapping

High aspect ratio fins

Total Integrated Scattering:

\[ TIS = \frac{P_s}{RP_i} \approx \left( \frac{4\pi \sigma}{\lambda} \right)^2 \]

\( \sigma \) is rms surface roughness

- Height is still << 10.6\text{um}, so:
  - Scattering/light trapping is minimal for LSA
  - No shadowing effects

LSA pattern effect advantage extends to FinFETs
LSA with Full Wafer Ambient Control

Dual-beam LSA201

- Patented microchamber approach allows ambient control in a scanning system
- Enables applications which involve interface control and film modification, which will become more critical with smaller devices and new materials
Hypothetical FinFET Process Flow

- **Fin/STI formation**
  - Implant N-ext
  - Implant P-ext
  - Spike RTP (low temp)
  - LSA

- **Fin formation**

- **Extension**
  - LSA

- **Source/Drain**
  - LSA

- **Gate Stack**
  - LSA

- **Silicide**

- **Interfacial layer**
  - High K
  - Post dep anneal (LSA)
  - Metal gate

- **Silicide metal dep**
  - LSA

- **Backend**

* FinFET Renditions from Threshold Sytems (2103)
There are multiple LSA applications for FinFET:

1. Extension anneal
2. S/D activation anneal
3. HK anneal
4. Re-activation
5. Silicide formation

* FinFET rendition from V. Moroz (2013)
LSA for Extension Anneal


As implanted 600C/60s 1050C RTA

Twin defects

As 5keV 1e15 quad implant @ 45deg

• LSA offers higher activation and a different time regime for SPE to potentially improve defectivity
LSA for S/D Anneal

Improved process results:
(ext doping + epi + LSA)

Offset spacer RIE
Native oxide removal
Conformal doping for NFET/PFET Extension
Extension anneal
Epi pre-clean
ISBD SiGe Epi grow on PFET/ISPD Epi grow on NFET
Spacer2 formation
Multi-Steps S/D Implantation (MSI)
SD Activation anneal
Silicide
Contact/M1

T. Yamashita et al (IBM), VLSI 2011
LSA for NMOS Epitaxial eSiC

XRD of epi film

Total series resistance of NMOS

Spike RTA: \( C_{\text{sub}} \rightarrow C_{\text{int}} \)

LSA: \( C_{\text{int}} \rightarrow C_{\text{sub}} \) !!

Activation increases with LSA

- For epitaxial eSiC, LSA increases the concentration of substitutional C, enhancing NMOS mobility, while simultaneously increasing Phosphorous activation

P. Grudowski et al. (Freescale), IEEE SOI (2007)
Advantages of LSA for HK Anneal

- Lower gate leakage
- Smoother film
- Higher k value due to higher concentration of tetragonal phase
- Lower thermal budget can give thinner interfacial layer
- Fast ramp-down avoids dopant deactivation

Gilmer et al., ESSDERC (2006)
High k Anneal: LSA vs. FLA Cooling Comparison

- LSA ramps down quickly by cooling by 3D conduction to the bulk Si
- FLA cool-down limited by radiation loss
- FLA cools slowly by radiative cooling to the ambient (1D)
- Device performance is improved with LSA compared to Flash Anneal because fast ramp-down avoids dopant de-activation
- RTP will also have slow ramp-down and possible de-activation
Intel Study on Dopant De-activation during Flash Anneal

Too much Exposure after Flash Peak can also Deactivate!

The half-Spike anneal that follows the FLA pulse should not be too hot. Too much Dt will deactivate dopants on the way down!

H. Kennel / IEEE RTP 2010
Advantages of LSA for Advanced Silicides

- **Within-die uniformity**
  - Pattern effects much higher on diode laser system due to interference effects and higher silicide reflectivity

- **Temperature measurement and control**
  - Real time measurement of temperature of wafer surface and closed loop feedback

- LSA (10.6µm)  
  \[ \Delta T \sim 10^\circ C \]

- Diode Laser (0.8µm)  
  \[ \Delta T > 100^\circ C \]
Laser Annealing for Advanced Silicides

\[ \rho_c \propto \exp \left( \frac{\phi_B}{\sqrt{N_D}} \right) \]

Advantages of LSA for Ti silicide

- Higher temperature than RTA \( \rightarrow \) lower contact resistance
- Minimal interdiffusion of gate stack layers
- Process control
  - Minimal pattern effects
  - Closed loop temperature control
  - Becomes critical for Ti silicide where process window is smaller than Ni silicide

Source: V. Moroz (Synopsys), 2013

Chipworks Xray of Intel 22nm FinFET
Process Window: Ni vs. Ti Silicide

- For Ti silicide, process window becomes narrower → benefits of tighter temperature distribution from LSA becomes more critical.
Summary

• Long-wavelength LSA retains fundamental advantages (minimal pattern effects and closed loop control) for FinFETs

• LSA applications summary:
  • Extension anneal: Higher activation, potential for reduced defects
  • S/D anneal: Higher activation, improved NMOS strain
  • High k anneal: Lower leakage, no de-activation
  • Ti Silicide: Low thermal budget, tight process control

• Expect millisecond annealing to play an increasing role in IC manufacturing as devices are scaled to 10nm and below