Laser Spike Annealing for FinFETs

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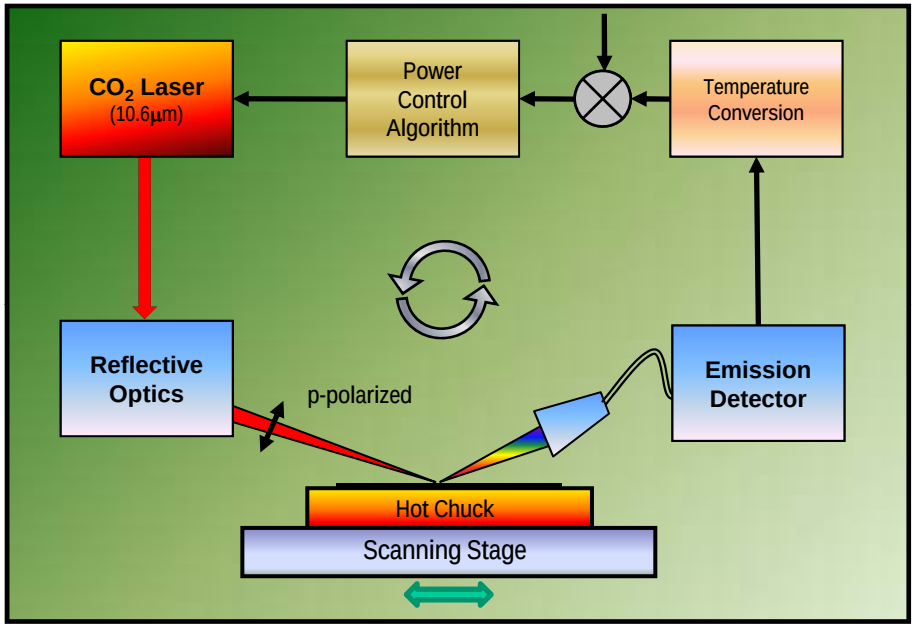
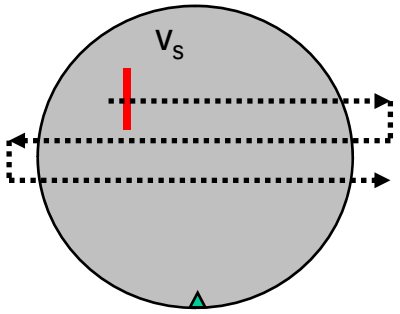
Outline

- LSA Overview and Key Features
- FinFET Process Flow
- LSA Applications for FinFET
- Summary

LSA Overview





$$\text{Dwell time} = \frac{w}{V_x}$$

Key Attributes

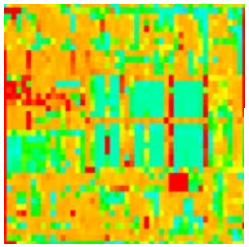
Within-die Uniformity
- CO_2 Laser: $\lambda \sim 10\mu m$
- P-polarized, brewster angle

Within-wafer & Wafer-to-wafer
- Temperature feedback control

Pattern Effects: Thin Film Interference

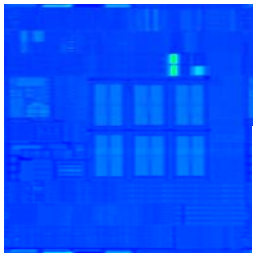
FLA & DL

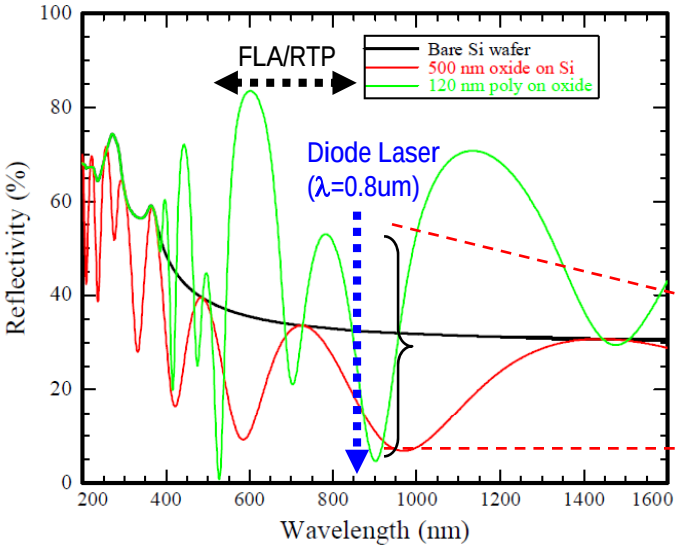
- Short λ
- Normal incidence

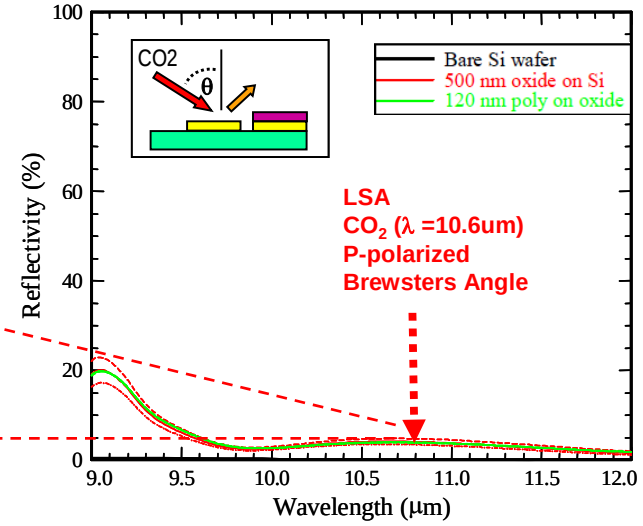


LSA

- Long λ
- Brewster **angle**
- p-polarization



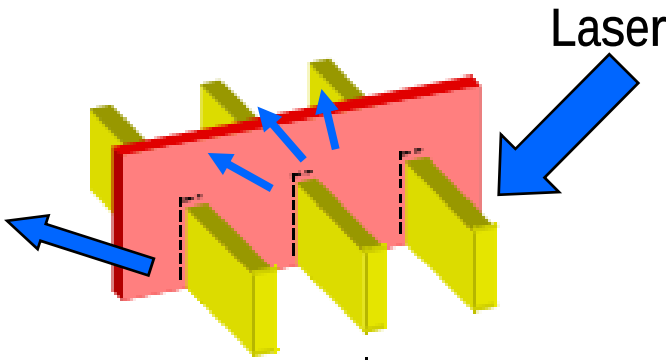




- Pattern effects caused by thin film interference variations → severe at short λ
- Long λ insensitive to device film variations

Pattern Effects: Scattering and Light Trapping

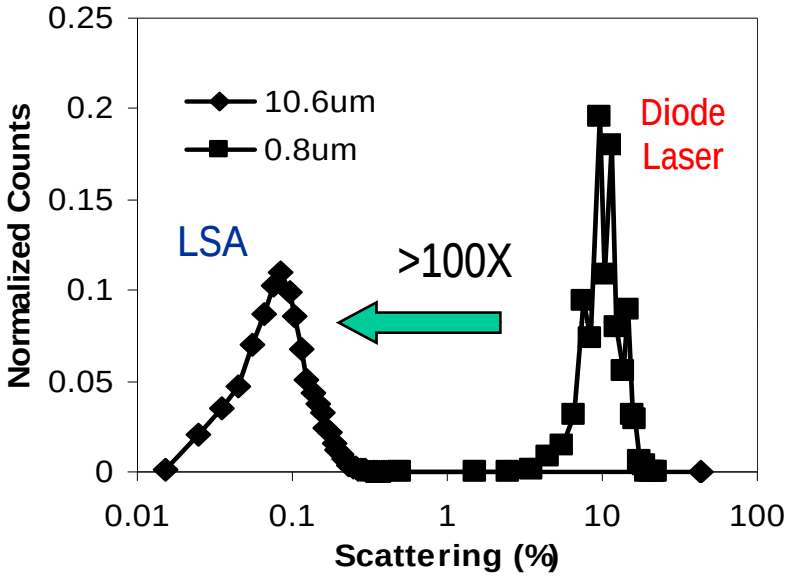
High aspect ratio fins



Total Integrated Scattering:

$$TIS = \frac{P_s}{RP_i} \approx \left(\frac{4\pi\sigma}{\lambda}\right)^2$$

σ is rms surface roughness

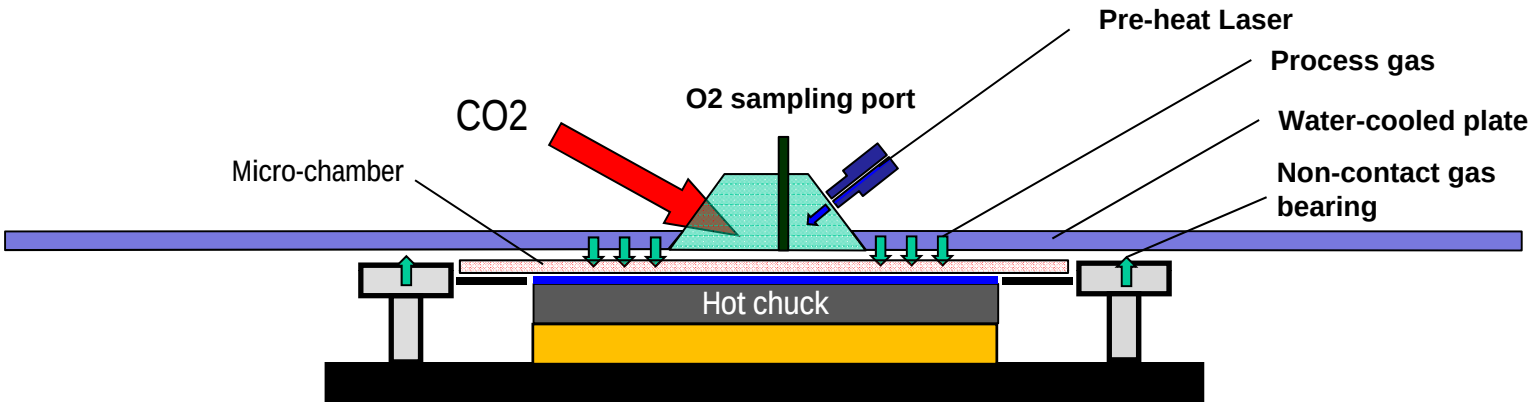


- Height is still << 10.6um, so:
  - Scattering/light trapping is minimal for LSA
  - No shadowing effects

LSA pattern effect advantage extends to FinFETs

LSA with Full Wafer Ambient Control

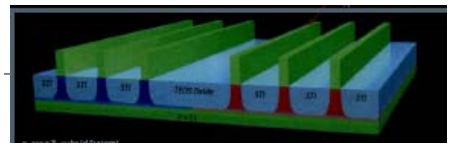
Dual-beam LSA201



- Patented microchamber approach allows ambient control in a scanning system
- Enables applications which involve interface control and film modification, which will become more critical with smaller devices and new materials

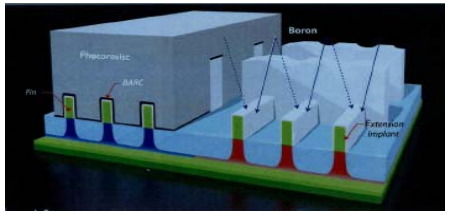
Hypothetical FinFET Process Flow

Fin/STI formation



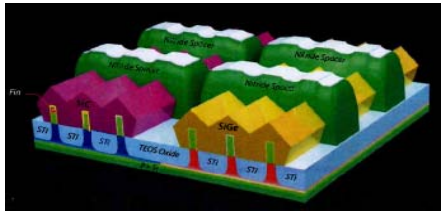
Fin formation*

Implant N-ext
Implant P-ext
Spike RTP (low temp)
LSA



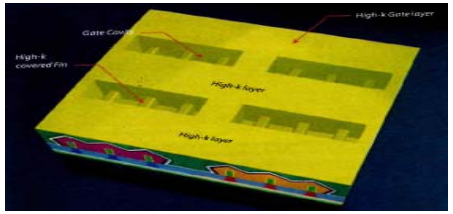
Extension

Spacer
NMOS epi (in-situ doped Si:C)
PMOS epi (in situ doped SiGe)
LSA



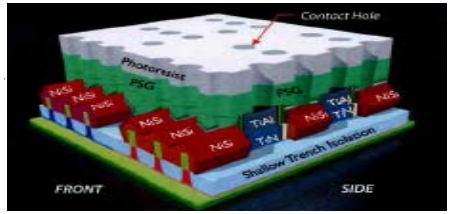
Source/
Drain

Interfacial layer
High K
Post dep anneal (LSA)
Metal gate



Gate
Stack

Silicide metal dep
LSA

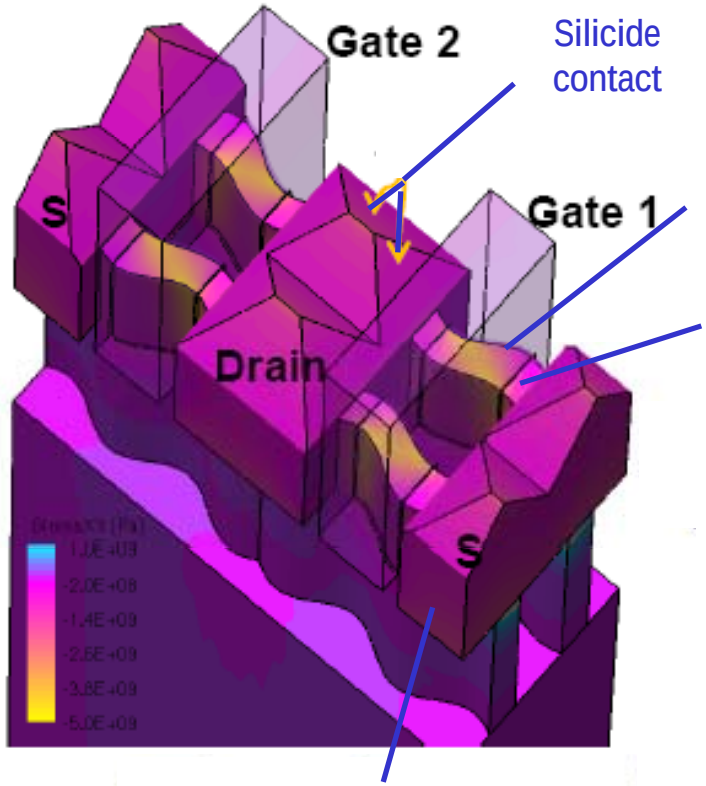


Silicide

Backend

* FinFET Renditions from Threshold Sytems (2103)

LSA Applications for FinFET



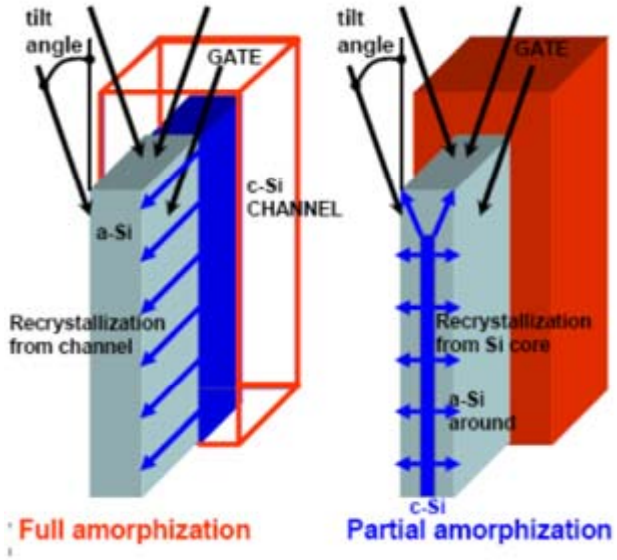
LSA Applications

1. Extension anneal
2. S/D activation anneal
3. HK anneal
4. Re-activation
5. Silicide formation

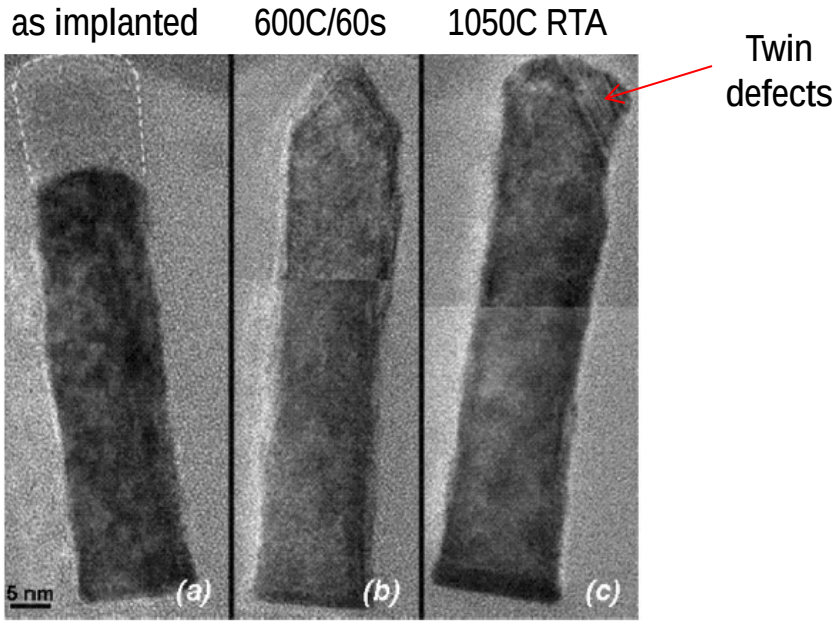
- There are multiple LSA applications for FinFET

* FinFET rendition from V. Moroz (2013)

LSA for Extension Anneal



R. Duffy, APL (2007)



As 5keV 1e15 quad implant @ 45deg

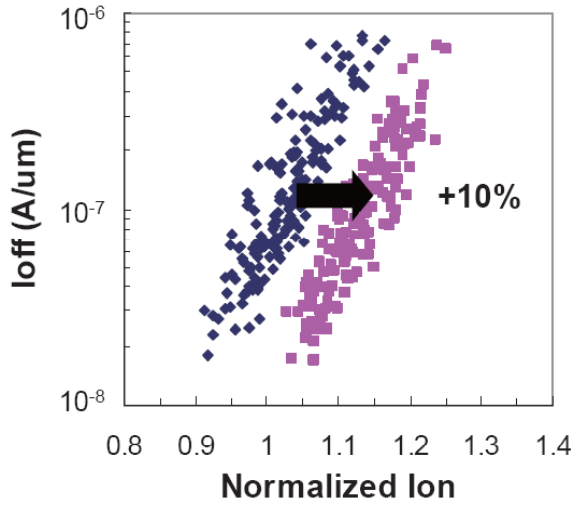
- LSA offers higher activation and a different time regime for SPE to potentially improve defectivity

LSA for S/D Anneal

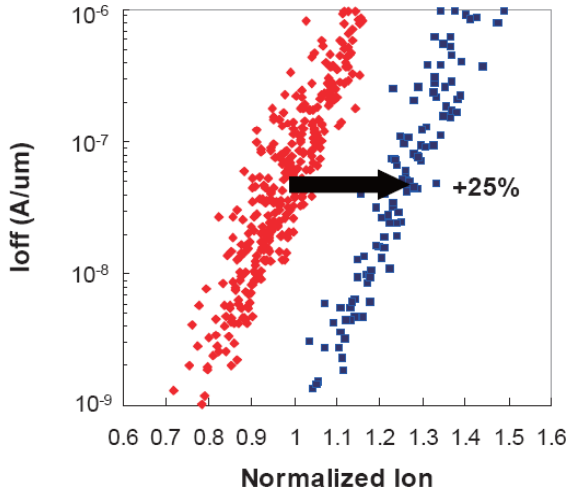
- Offset spacer RIE
- Native oxide removal
- Conformal doping for NFET/PFET Extension
- Extension anneal
- Epi pre-clean
- ISBD SiGe Epi grow on PFET/ISPD Epi grow on NFET
- Spacer2 formation
- Multi-Steps S/D Implantation (MSI)
- SD Activation anneal
- Silicide
- Contact/M1

LSA

Improved process results:
(ext doping + epi + LSA)



NFET

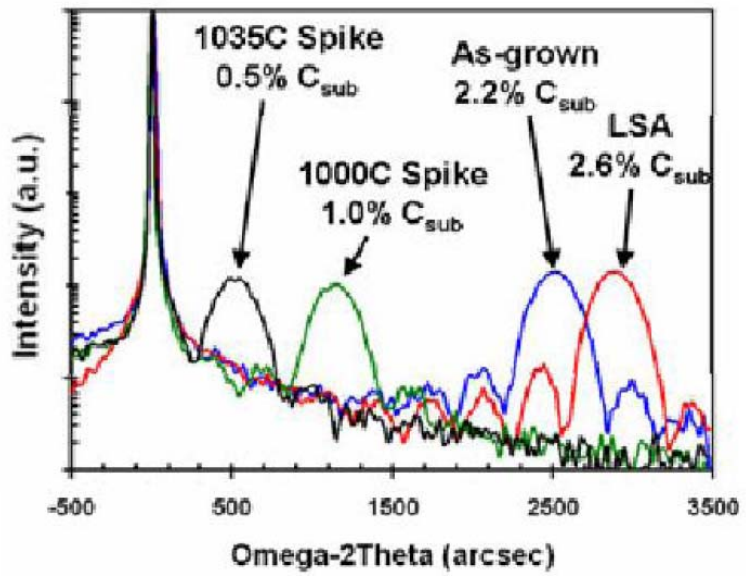


PFET

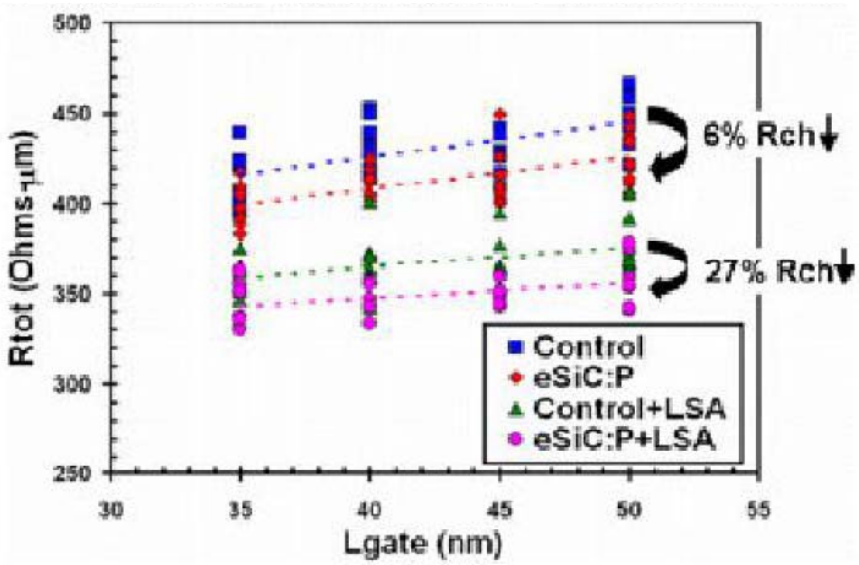
T. Yamashita et al (IBM), VLSI 2011)

LSA for NMOS Epitaxial eSiC

XRD of epi film



Total series resistance of NMOS



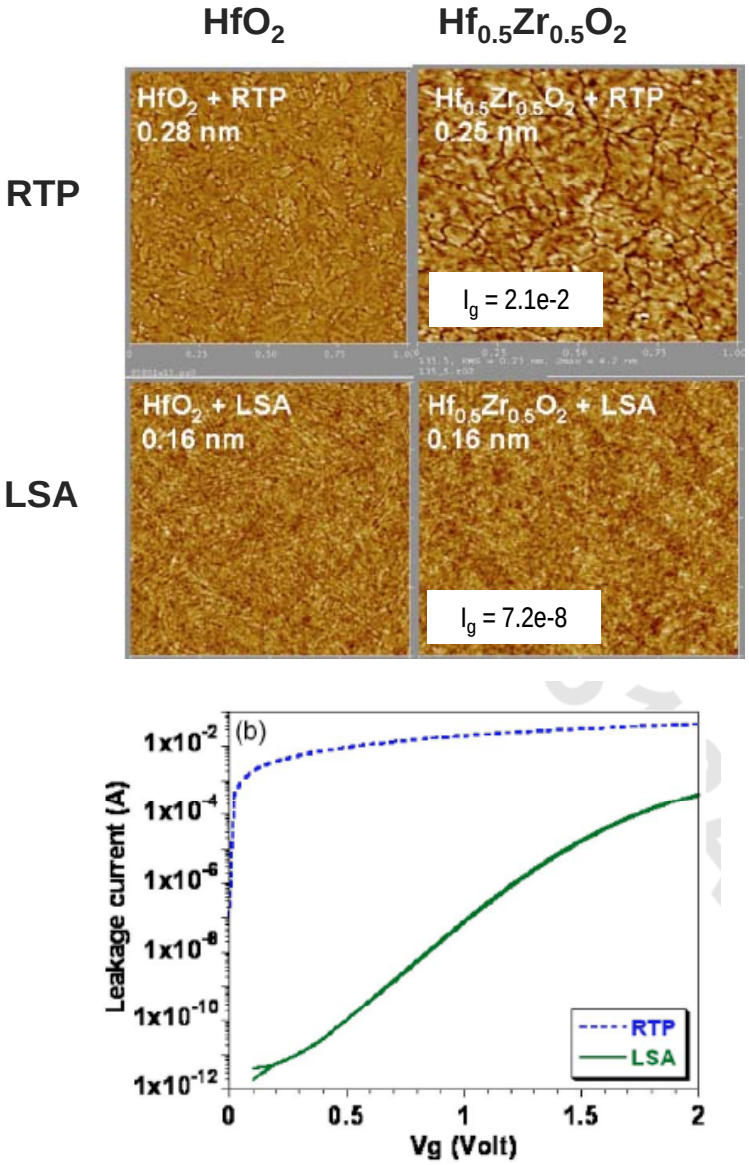
Spike RTA: C_{sub} → C_{int}
LSA: C_{int} → C_{sub} !!

Activation increases with LSA

- For epitaxial eSiC, LSA increases the concentration of substitutional C, enhancing NMOS mobility, while simulataneously increasing Phosphorous activation

P. Grudowski et al. (Freescale), IEEE SOI (2007)

LSA For High-k Post-Depostion Anneal



Advantages of LSA for HK Anneal

- Lower gate leakage
- Smoother film
- Higher k value due to higher concentration of tetragonal phase
- Lower thermal budget can give thinner interfacial layer
- Fast ramp-down avoids dopant de-activation

***Sources: Triyoso et al., Appl. Phys. Letters (2008)**
Gilmer et al., ESSDERC (2006)

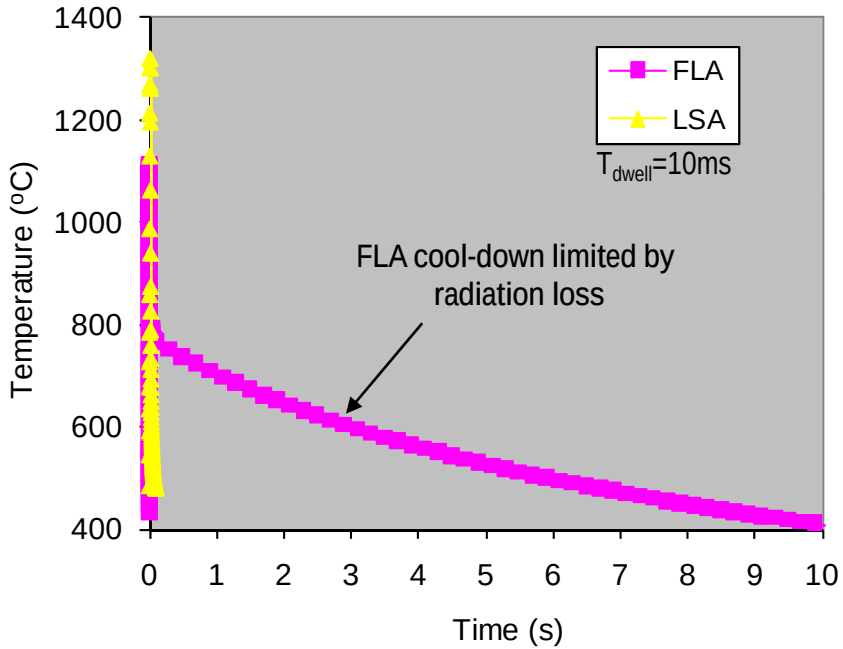
High k Anneal: LSA vs. FLA Cooling Comparison

Laser

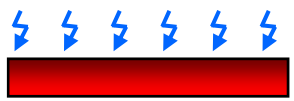
Backside chucked

- LSA ramps down quickly by cooling by 3D conduction to the bulk Si

Simulated Temperature Profiles



Flash Lamp



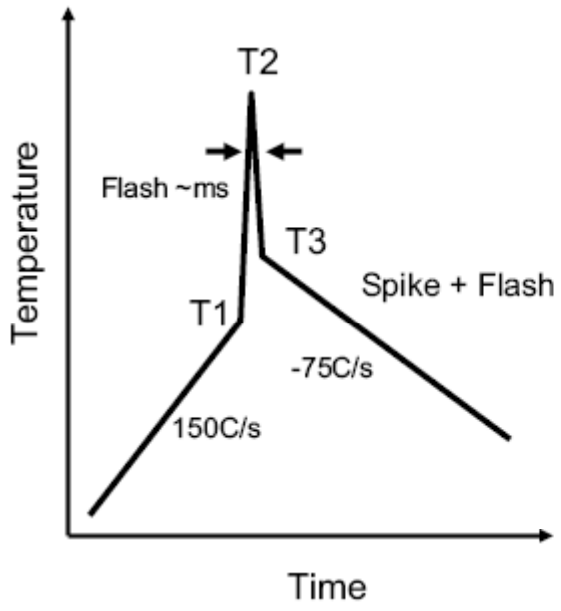
Backside float

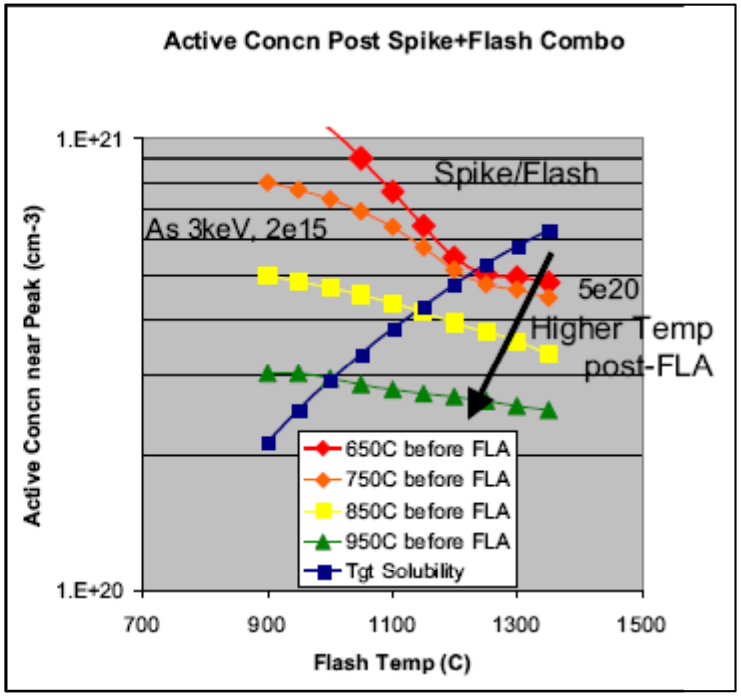
- FLA cools slowly by radiative cooling to the ambient (1D)

- Device performance is improved with LSA compared to Flash Anneal because fast ramp-down avoids dopant de-activation
- RTP will also have slow ramp-down and possible de-activation

Intel Study on Dopant De-activation during Flash Anneal

Too much Exposure after Flash Peak can also Deactivate!





The half-Spike anneal that follows the FLA pulse should not be too hot. Too much Dt will deactivate dopants on the way down!

H. Kennel / IEEE RTP 2010 38

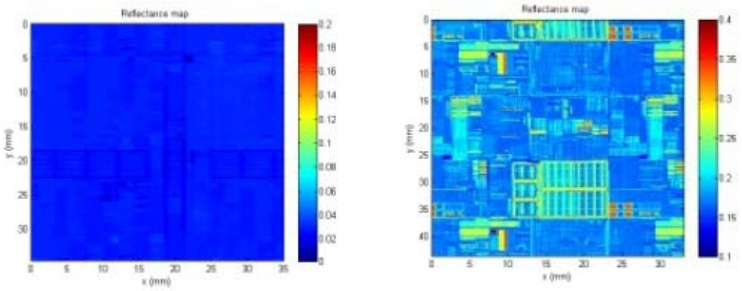
Intel slide

Advantages of LSA for Advanced Silicides

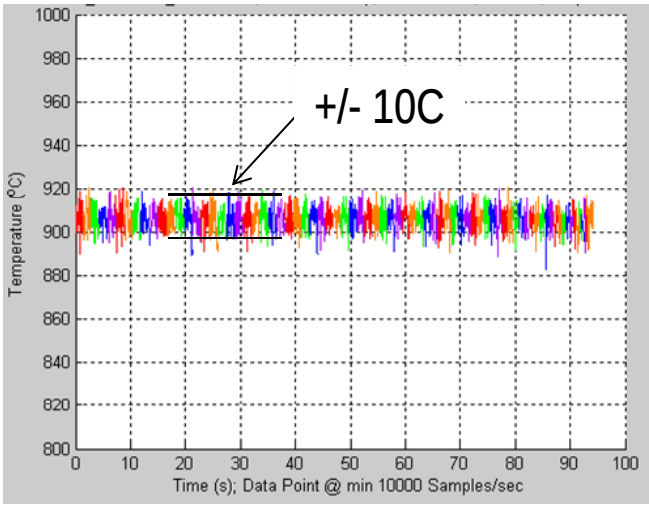
- **Within-die uniformity**
  - Pattern effects much higher on diode laser system due to interference effects and higher silicide reflectivity
- **Temperature measurement and control**
  - Real time measurement of temperature of wafer surface and closed loop feedback

LSA (10.6um)
$\Delta T \sim 10^{o}C$

Diode Laser (0.8um)
$\Delta T > 100^{o}C$



Closed loop control:
Advanced Silicide Device Wafer

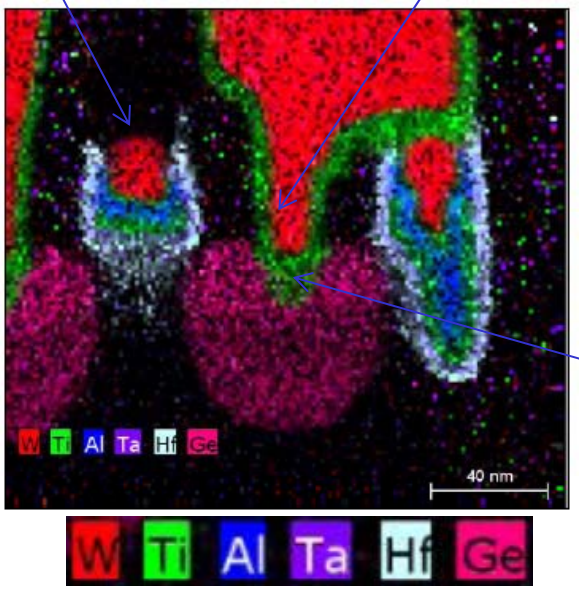


Laser Annealing for Advanced Silicides

$$\rho_c \propto \exp\left(\frac{\phi_B}{\sqrt{N_D}}\right)$$

Gate Contact

Source/Drain Contact



Ti

Chipworks Xray of
Intel 22nm FinFET

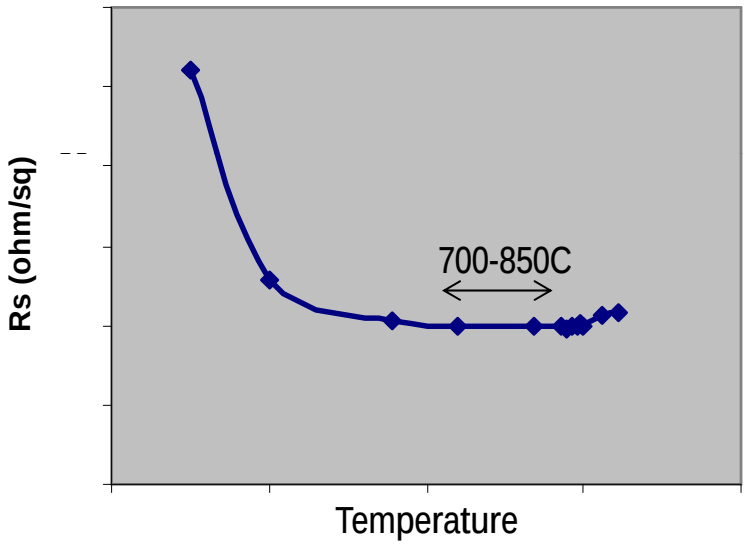
Source: V. Moroz (Synopsys), 2013

Advantages of LSA for Ti silicide

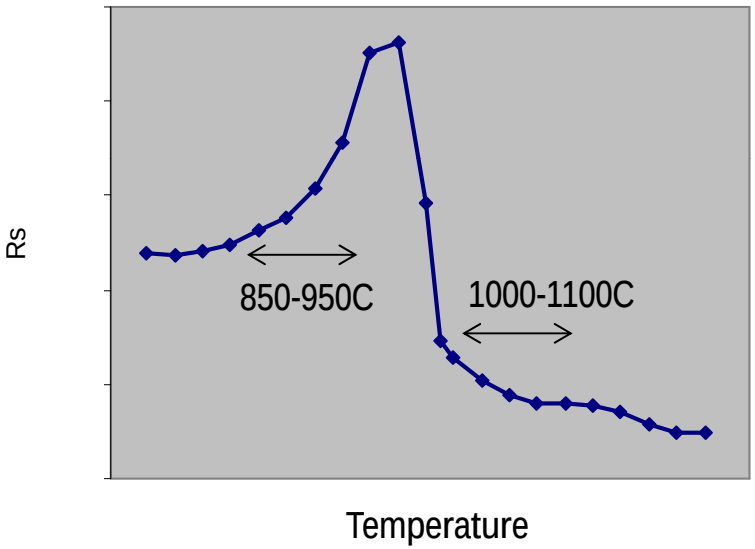
- Higher temperature than RTA → lower contact resistance
- Minimal interdiffusion of gate stack layers
- Process control
  - Minimal pattern effects
  - Closed loop temperature control
  - Becomes critical for Ti silicide where process window is smaller than Ni silicide

Process Window: Ni vs. Ti Silicide

Ni silicide transition



Ti silicide transition (Ti on SiGe)



- **For Ti silicide, process window becomes narrower → benefits of tighter temperature distribution from LSA becomes more critical.**

Summary

- **Long-wavelength LSA retains fundamental advantages (minimal pattern effects and closed loop control) for FinFETs**
- **LSA applications summary:**
  - **Extension anneal: Higher activation, potential for reduced defects**
  - **S/D anneal: Higher activation, improved NMOS strain**
  - **High k anneal: Lower leakage, no de-activation**
  - **Ti Silicide: Low thermal budget, tight process control**
- **Expect millisecond annealing to play an increasing role in IC manufacturing as devices are scaled to 10nm and below**