Low-Temperature Oxidation/Nitridation Processes enabling Advanced Junctions

.PLASMOX^{LT}

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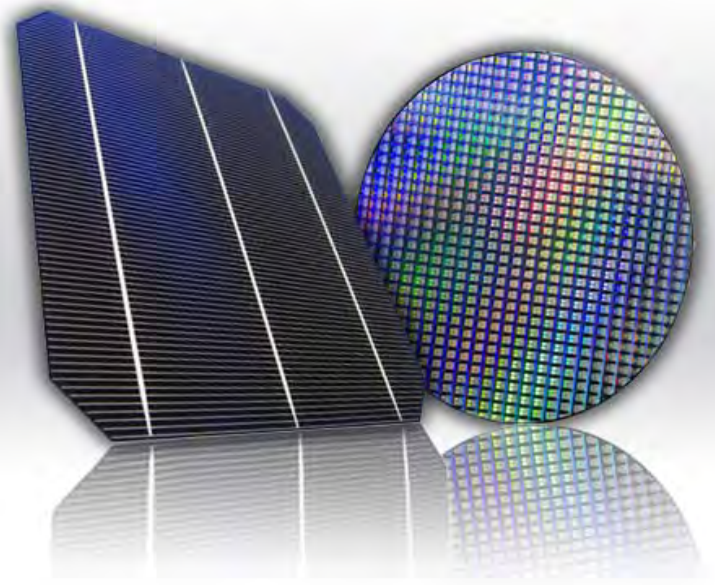
centrotherm photovoltaics

Photovoltaics

Semiconductor

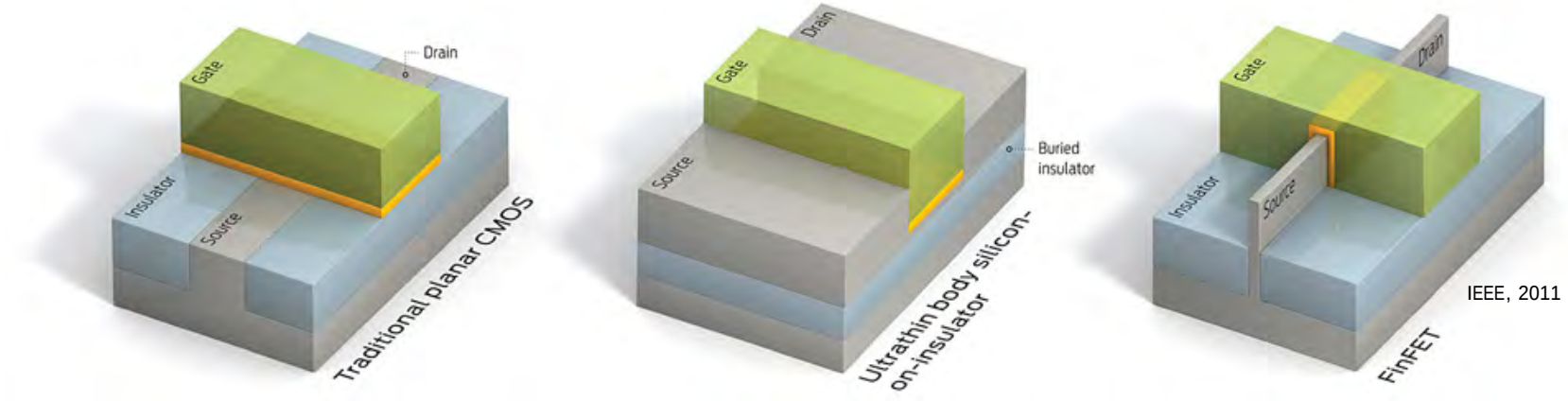


Contents

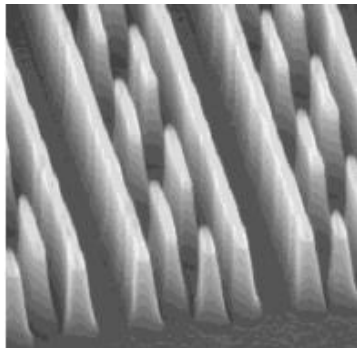
- Motivation for low-temperature oxidation
  - Ambient control during annealing
  - Dopant outdiffusion in novel 3D FIN structures
  - Temeprature causes deactivation
- The Plasmox^{LT} hardware concept
- Microwave plasma generation and oxidation mechanism
- Summary

Motivation

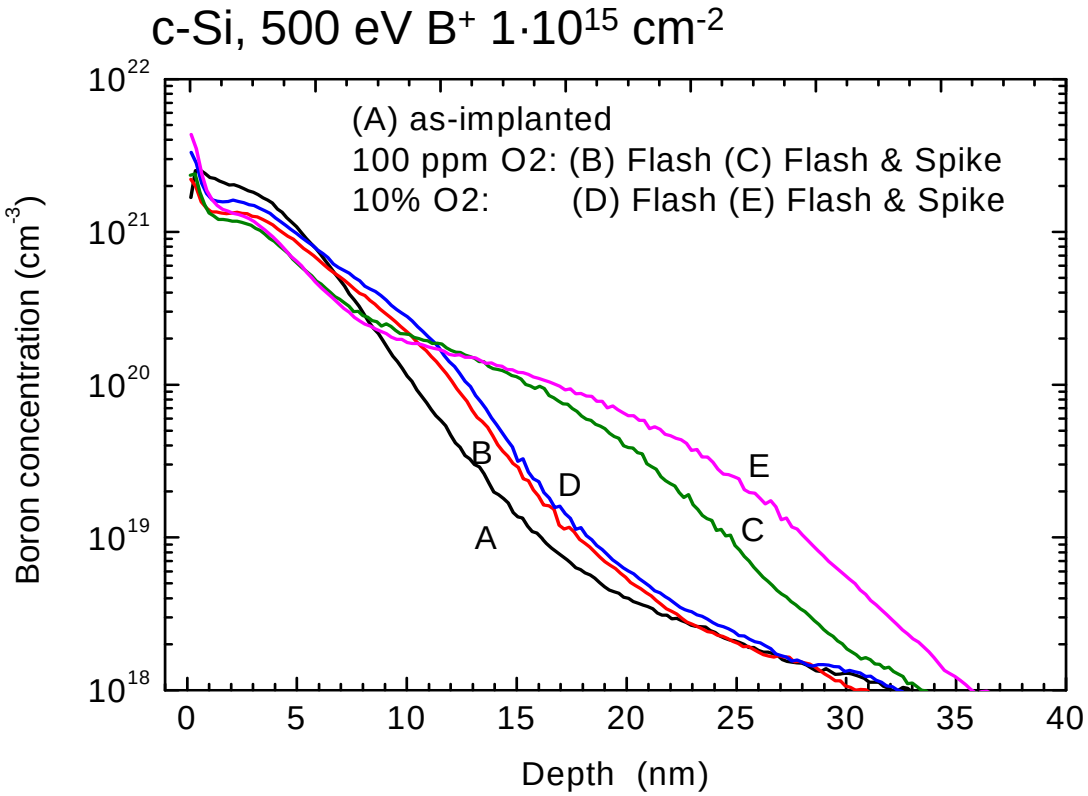
- Geometrical Scaling in 2D: (More Moore, comes to a physical end)
  - Thermal budget reduction for smaller feature size and for deactivation reduction: RTP and ms-annealing (MSA)
  - Plasma-assisted technologies for process temperature reduction



- Transistion planar to 3D Gate Structures: (technology challenges occurring)
  - Extreme conformality required
  - Excellent dopant activation



Oxidation Enhanced Diffusion during Flash Annealing, pMOS



Flash: 750°C / 1300°C
Spike: 950°C

B: 448 Ω/sq.
D: 395 Ω/sq.
C: 453 Ω/sq.
E: 463 Ω/sq.

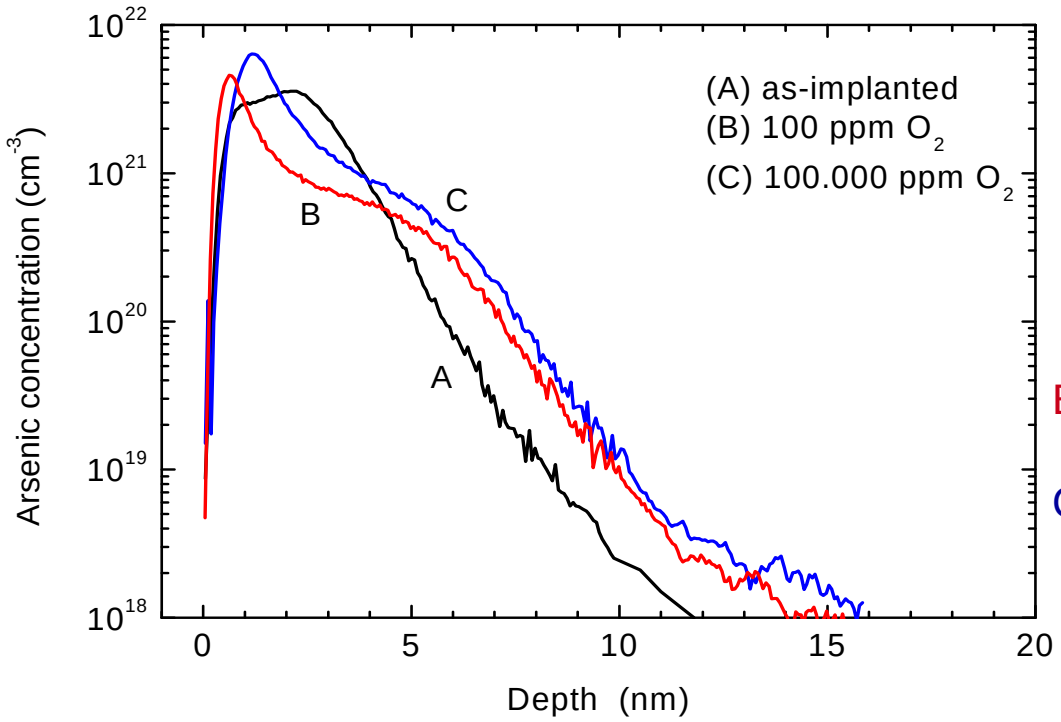
- For (D) less dissolution of immobile peak compared to (B). In case of 100 ppm O_2 ~20 % reduced retained dose.
- Ideal case: 10% O_2 during Flash and 100 ppm O_2 during Spike to avoid outdiffusion (dopant loss).

Advanced Activation Trends for Boron and Arsenic by Combinations of Single, Multiple Flash Anneals and Spike Rapid Thermal Annealing
W. Lerch, S. Paul, J. Niess, S. McCoy, J. Gelpey, F. Cristiano, F. Severac, P. F. Fazzini, A. Martinez-Lima, P. Pichler, H. Kheyrandish, D. Bolze
Materials Science and Engineering B 154-155 (2008) 3-13

Dose Protection during “Oxidizing” Flash Annealing, nMOS

c-Si, 1 keV As^+ $1 \cdot 10^{15}$ cm^{-2}

Flash: 750°C / 1300°C



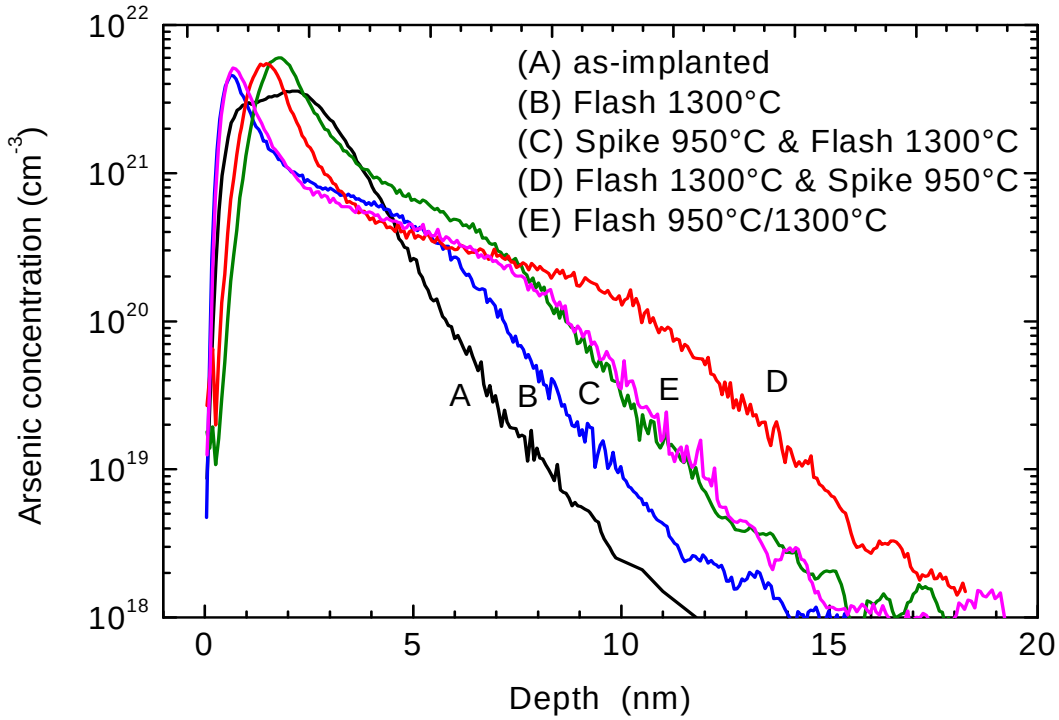
B: 649 Ω/sq.,
R_s^{Hall} = 660 Ω/sq.,
C: 649 Ω/sq.,
R_s^{Hall} = 663 Ω/sq.

- Dopant loss reduced by 30%, similar mobility values of 40 $cm^2V^{-1}s^{-1}$.
- In case of (B) the activation is 44 % and 30 % for (C).
- No impact on profile due to use of oxidizing ambient except reduced outdiffusion (reduction of dopant loss).

W. Lerch, et al. *Materials Science and Engineering B* 154-155 (2008) 3-13

Dopant Activation by Annealing Strategies, nMOS

c-Si, 1 keV As^+ $1 \cdot 10^{15}$ cm^{-2}



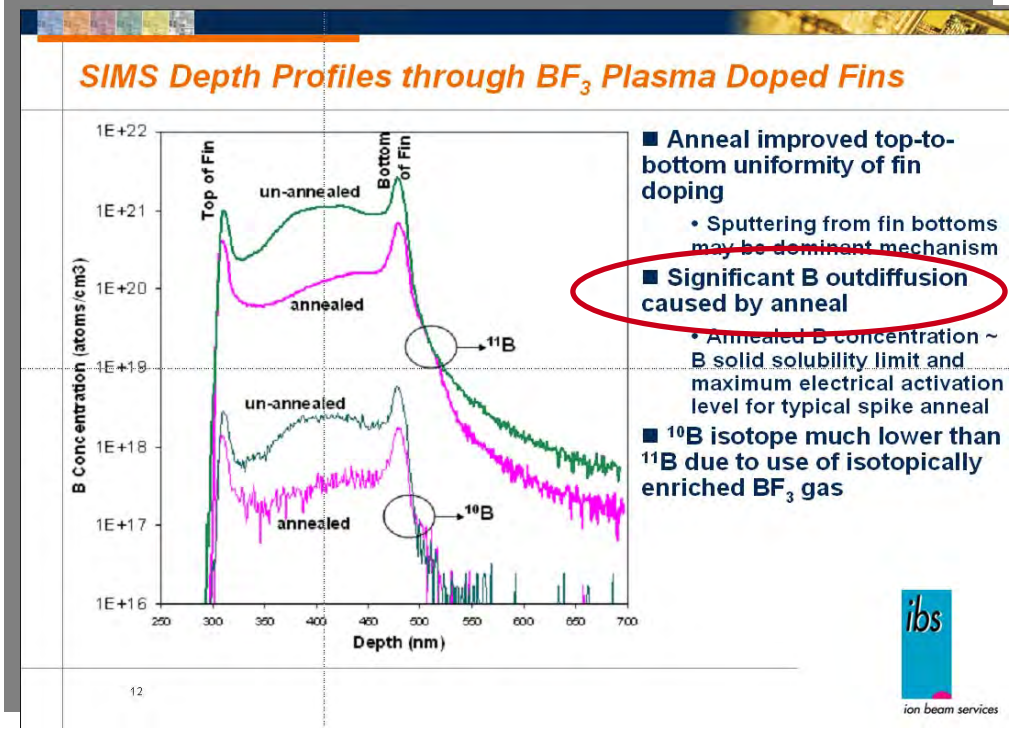
B: 648 Ω/sq., C: 591 Ω/sq.,
D: 694 Ω/sq., E: 693 Ω/sq.

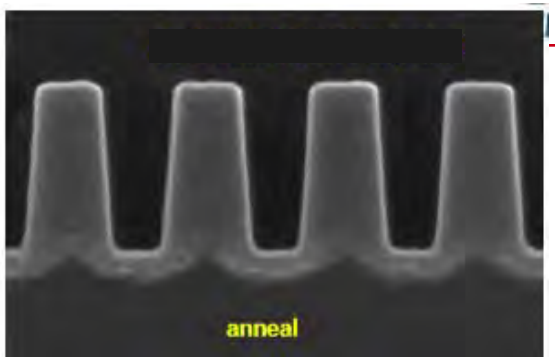
For arsenic implants in c-Si the defect density after flash and spike + flash is below TEM-WBDF detection limit.

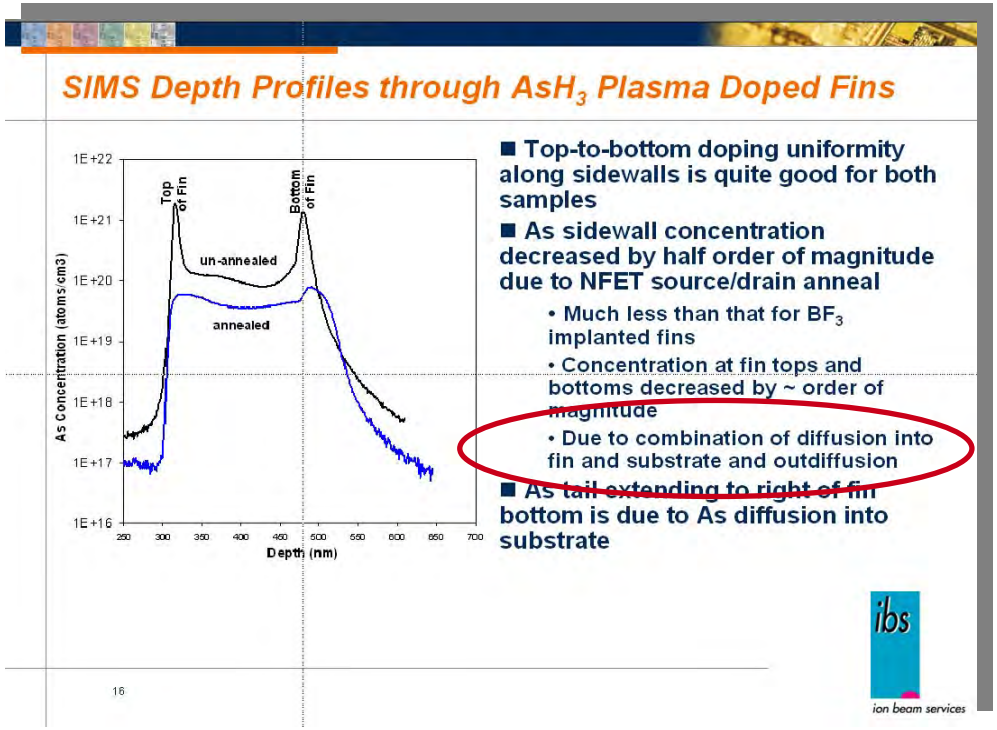
- Spike + Flash optimum strategy regarding Xj and Rs
- Annealing ambient of paramount importance or a low-T oxide capping layer to avoid As evaporation

W. Lerch, et al. *Materials Science and Engineering B* 154-155 (2008) 3-13

Felch et al., IWJT Kyoto (Jp) and Semicon 2011



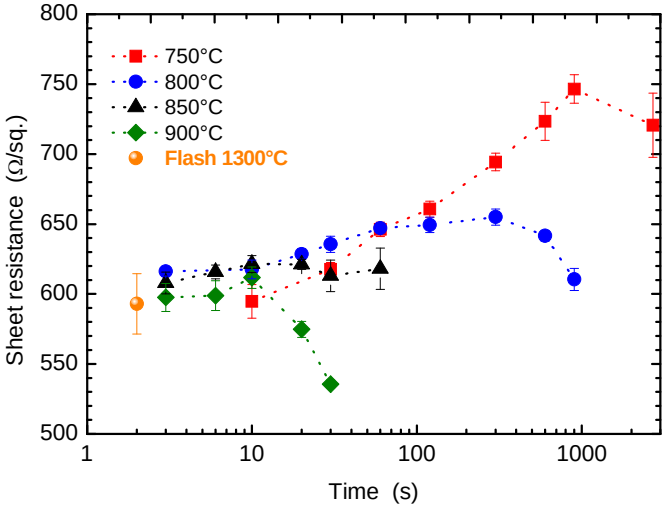


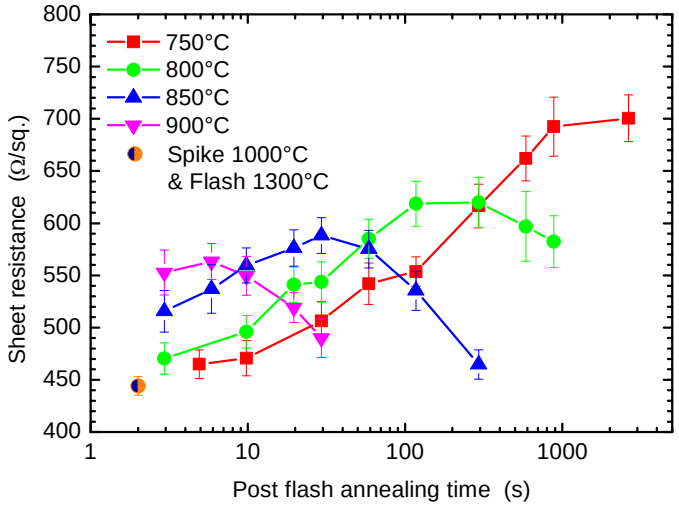


The difficulty for the activation and anneling process is that plasma doping profiles of either B and As reside directly under the surface and it is of paramount importance to deposit a capping layer at low-temperature to avoid massive dopant out-diffusion during the suitable annealing condition for controlled dopant redistribution and activation.

Deactivation a Driver for Low-Temperature Oxidation

R_s-Evolution (t / T) for highly activated
500 eV Boron, 1 keV Arsenic Profiles





- Deactivation / “reactivation” process for t / T regime
- Time dependent increase in R_s followed by marked drop
- Max. R_s decrease with T suggesting a thermally activated process
- Probably SiAs clusters and As-V cluster formation cause R_s increase within 3 s

W. Lerch, S. Paul, J. Niess, S. McCoy, T. Selinger, J. Gelpey, F. Crisitiano, F. Severac, M. Gavelle, S. Boninelli, P. Pichler, D. Bolze *Materials Science and Engineering B* **124-125** 24-31 (2005)

W. Lerch, S. Paul, J. Niess, S. McCoy, J. Gelpey, D. Bolze, F. Cristiano, F. Severac,P.F. Fazzini, A. Martinez, P. Pichler *15th IEEE EDS International Conference on Advanced Thermal Processing of Semiconductors, RTP 2007, Catania, Italy,* **15** 191-196 (2007)

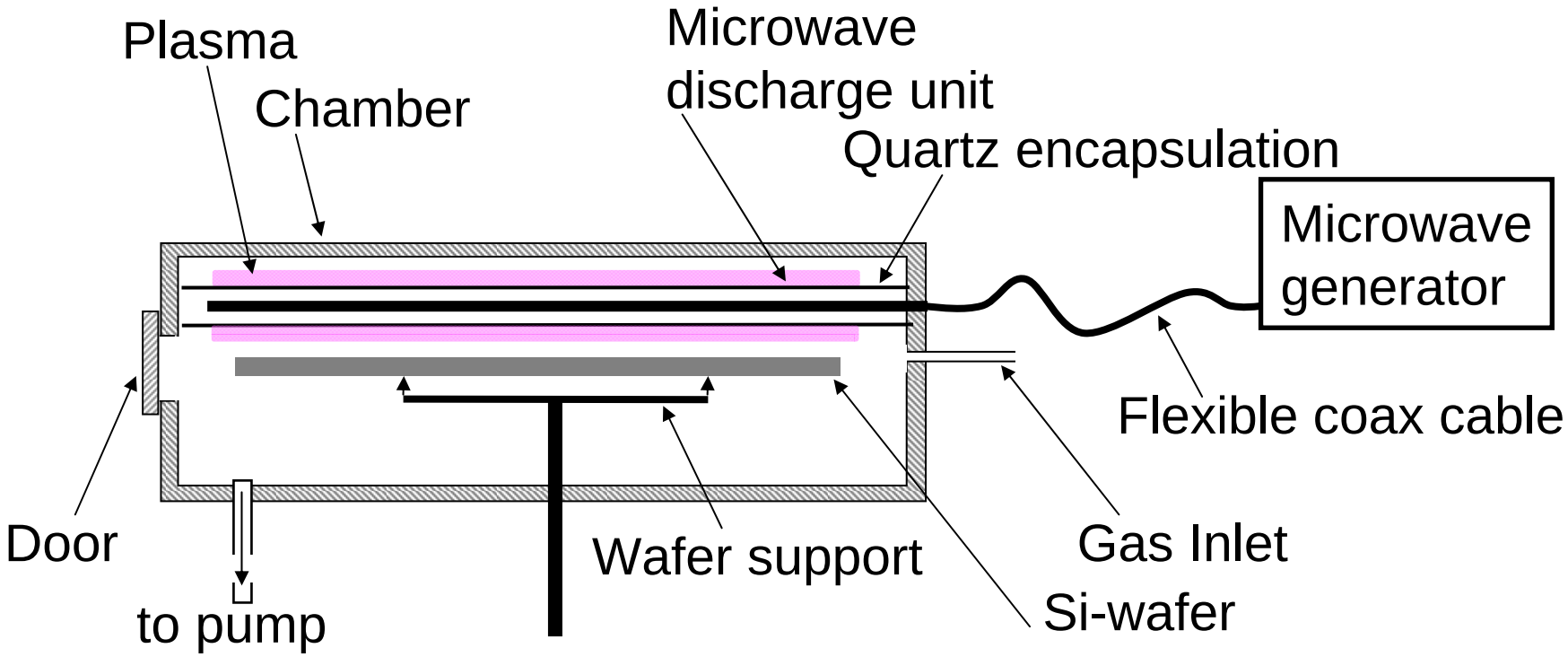
Interim Conclusions

- Outdiffusion needs to be controlled in shallow junctions
  - Use of higher oxygen concentration during anneal
  - Use a low temperature cap layer
- Post anneal process temperatures must be limited to prevent deactivation

HEAT: A Blunt Instrument for Device Fabrication?

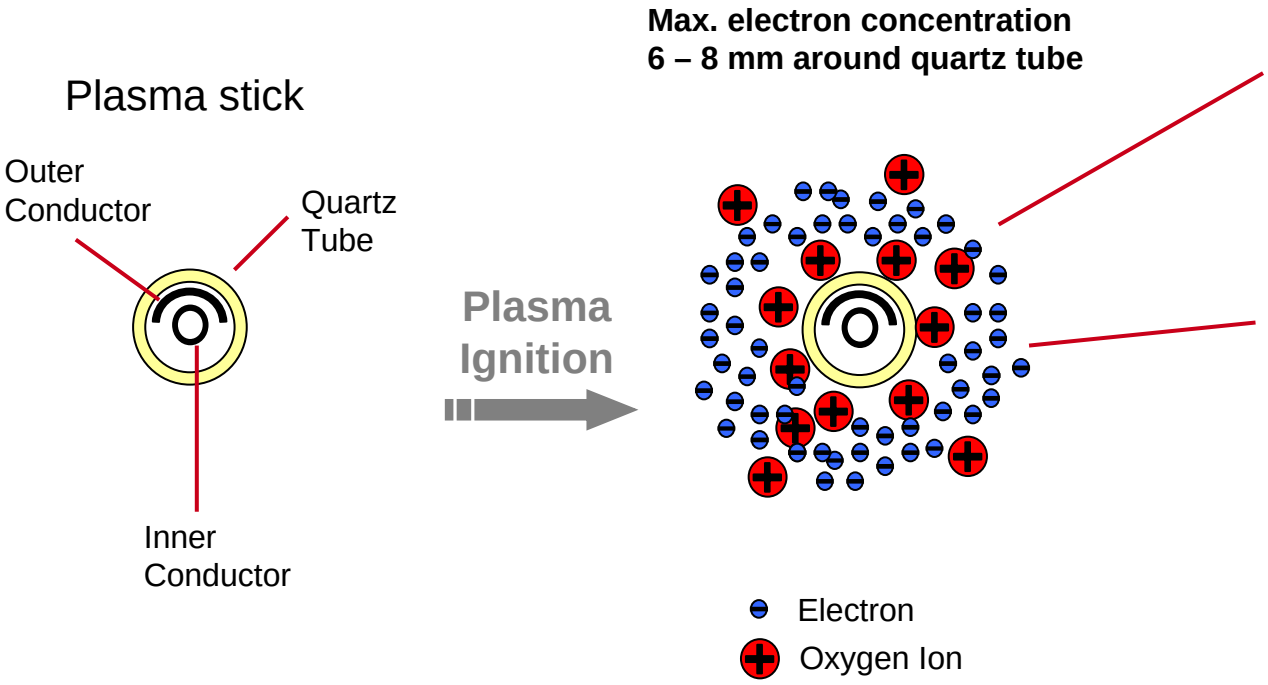
- Historically HEAT enabled:
  - Reaction
  - Phase change
  - Bond rearrangement
  - Atomic diffusion
- Sometimes we want these changes, sometimes not
- But HEAT alone is not the only possible driver
- Kinetics & reaction path must be optimized by design of thermal cycle and ambient conditions
- Non-thermal energy (photons, PLASMA, particle beams) provide desirable alternative reaction paths

Plasma Apparatus Schematic



Concept of a plasma chamber with microwave plasma generation and possible wafer preheating by lamps

Advantages of Microwave Plasma Generation



Neutral atoms/molecules and radicals are not shown, number of particles are adjusted for the sketch and do not represent real situation!

A ~100x higher frequency than RF results in a ~10^4 times higher degree of dissociation

High electron concentration around the plasma source

⇩

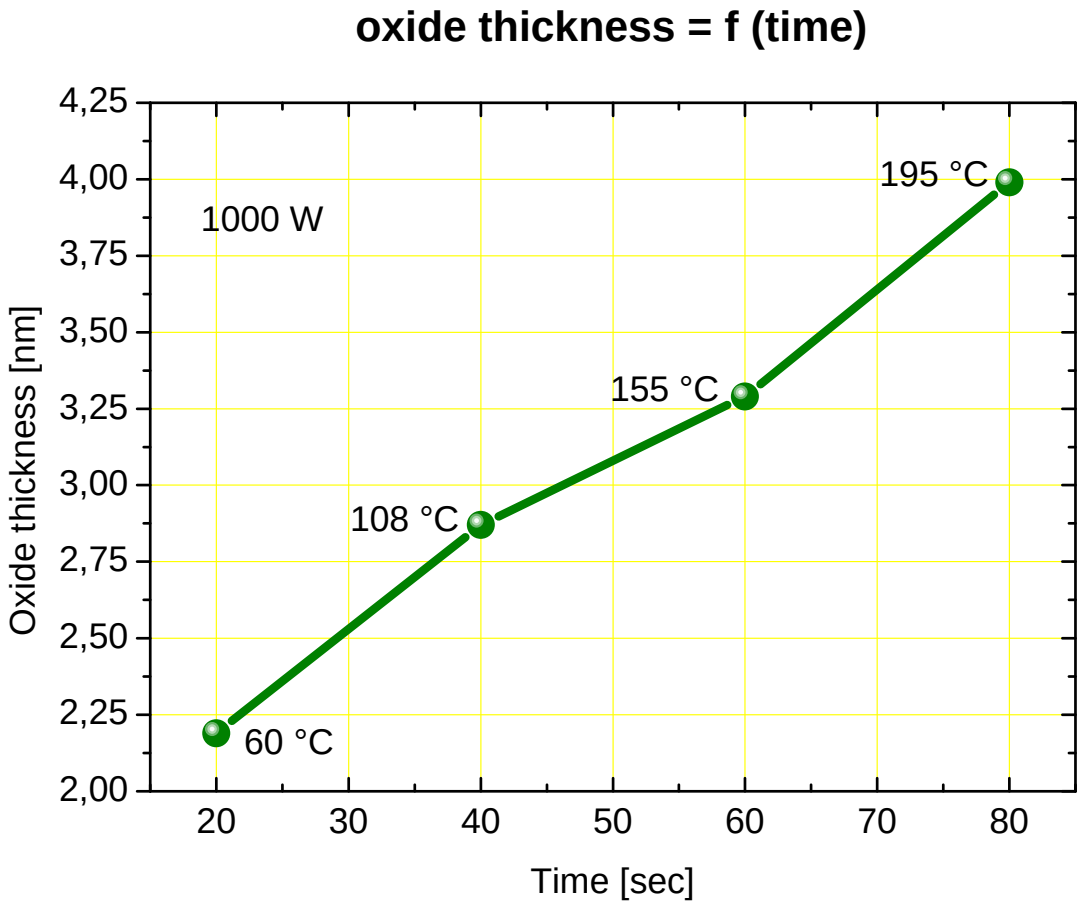
Shielding of microwave radiation by this high electron concentration

⇩

Plasma damage is greatly reduced, even near the plasma sticks

Less heating of the wafer

Growth Curves

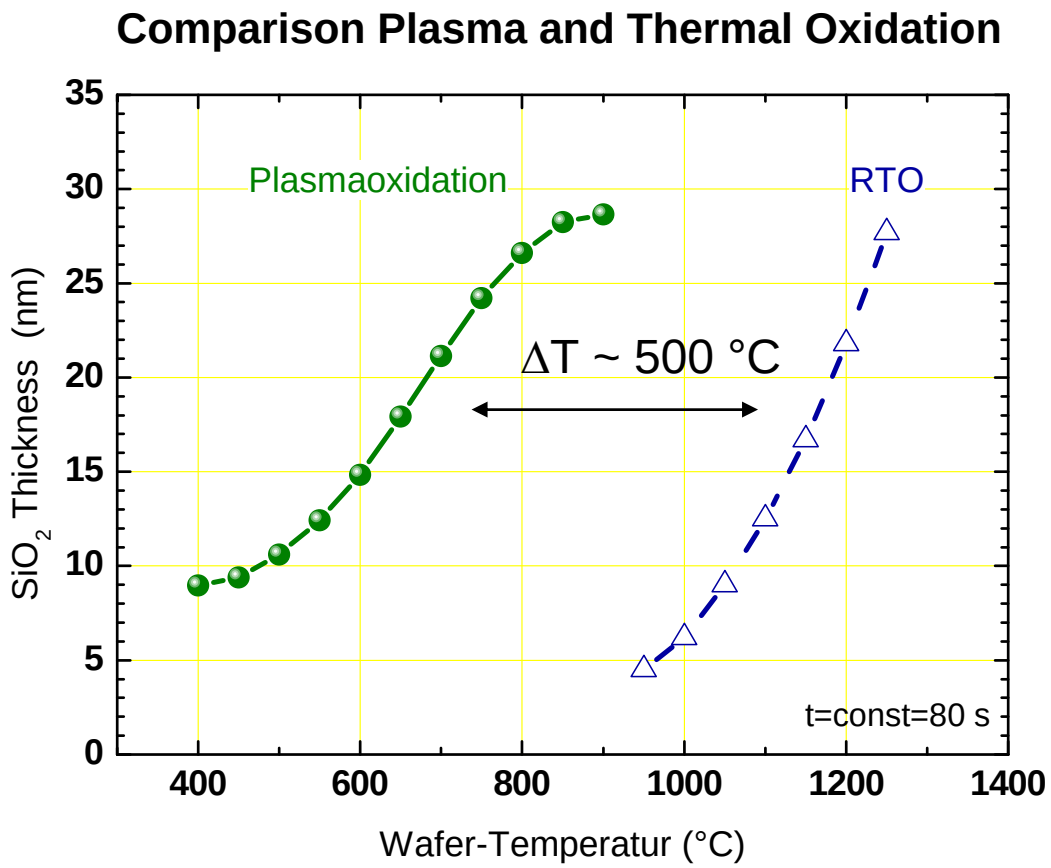


Oxide growth up to 4 nm with wafer temperature below 200 °C

(wafer heated up by plasma, no preheat by lamps)

W. Lerch, W. Kegel, J. Niess, A. Gschwandtner, J. Gelpey and Fuccio Cristiano (Invited) Scaling Requires Continuous Innovation in Thermal Processing; *ECS Trans.* (2012) Vol. 45, Issue 6, Pages 151-161

Comparison Plasma and Thermal Oxidation

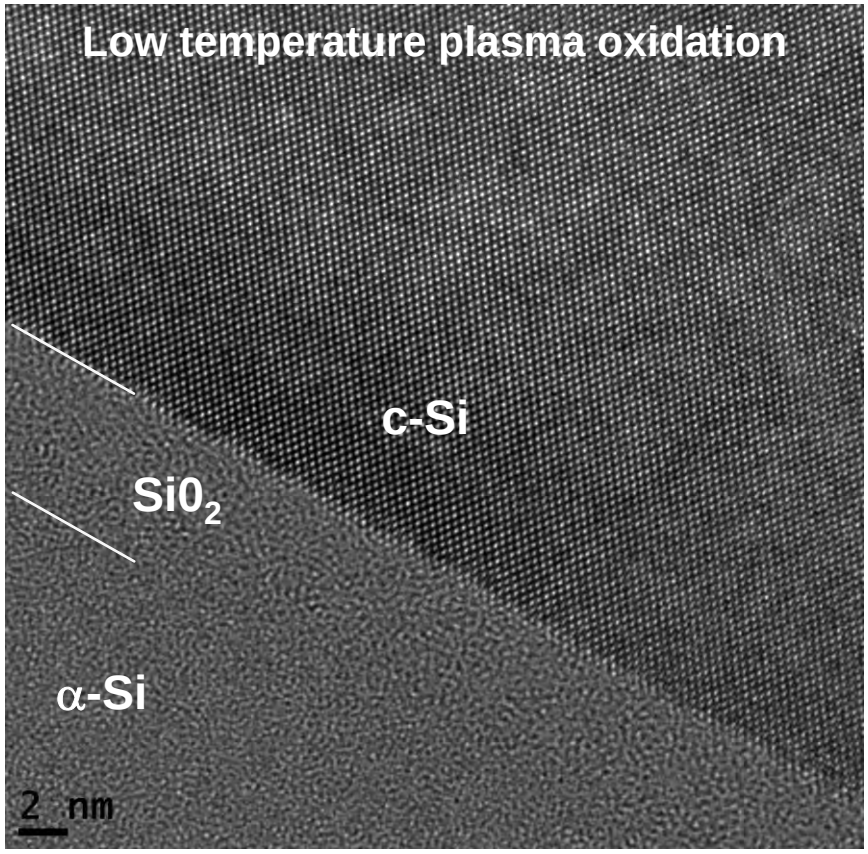


Oxide growth up to 30 nm with elevated wafer temperature up to 800 °C

(wafer preheated by lower lamp field, gaseous ambient O_2 and H_2)

J. Niess W. Kegel, W. Lerch, to be published in *phys. stat. solidi* 2013

TEM Interface Characterization



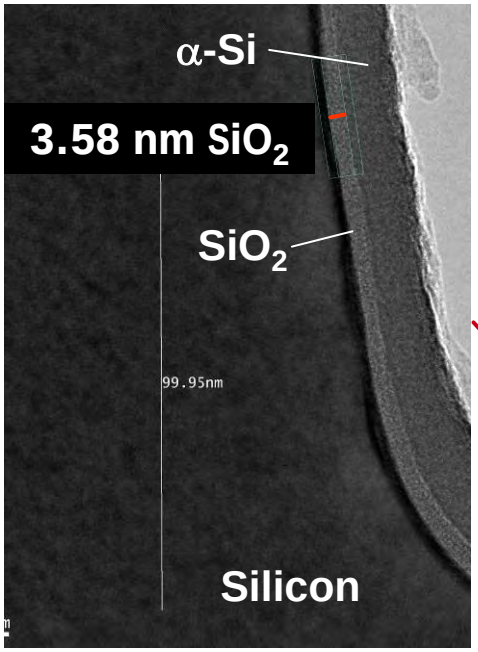
Temperature < 400 °C
Time: 80 s in O_2
t_{ox} = 5.1 nm

Si-SiO_2interface roughness on atomic scale. Equivalent to high-T furnace
No plasma- /microwave-damage observed!

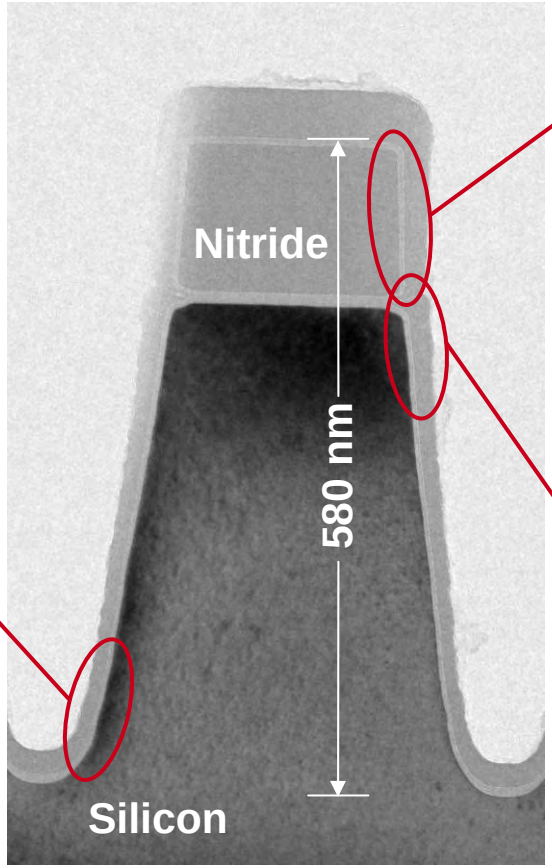
W. Lerch, W. Kegel, J. Niess, A. Gschwandtner, J. Gelpey and Fuccio Cristiano (Invited) Scaling Requires Continuous Innovation in Thermal Processing; *ECS Trans.* (2012) Vol. 45, Issue 6, Pages 151-161

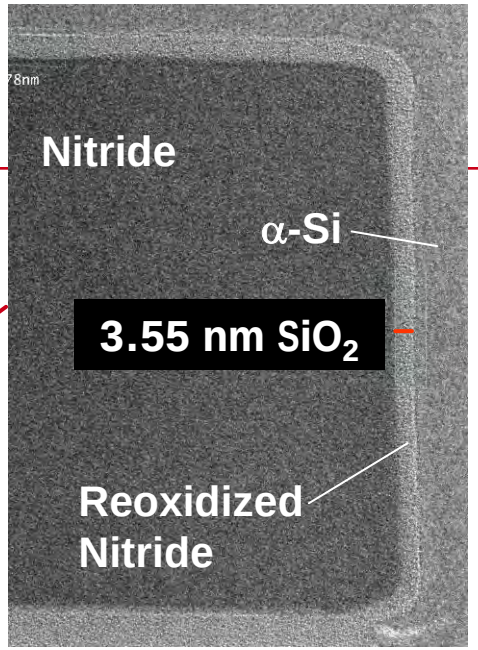
TEM Oxide Growth Characterization

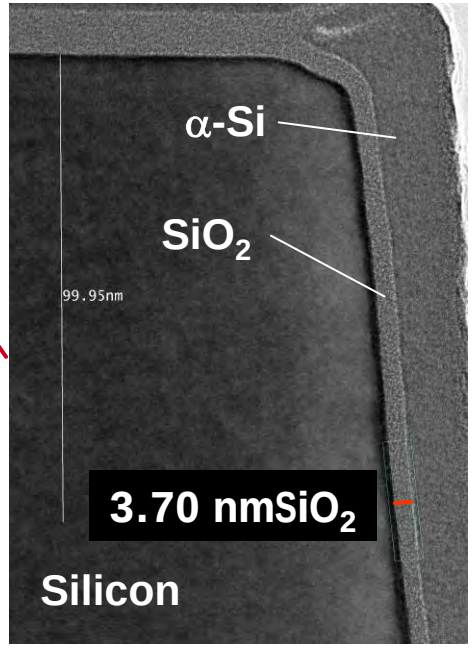
O_2 Plasma
t: 80 sec
p: 260 mTorr



STI structure (AR 3.2:1) with CAP nitride



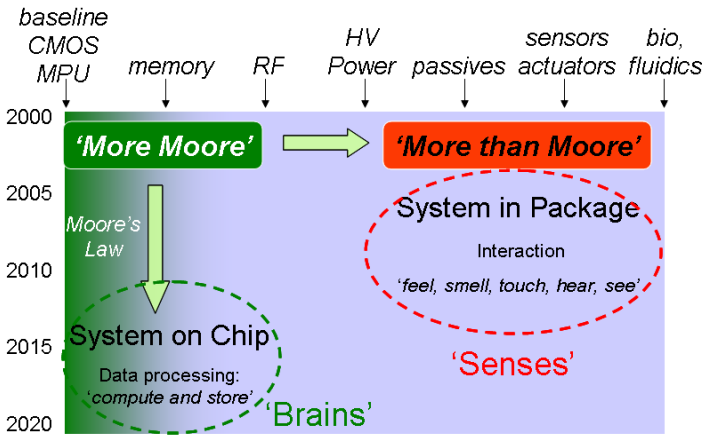




Conformal oxide growth on the sidewall for both oxidation of silicon and reoxidation of nitride

Conclusions

- CMOS device scaling will require extremely low-temperature processing (close to room temperature) or very high temperature/very short time processing as an enabling technology
- Interface engineering, gaseous ambient control, dopant outdiffusion control, topography control and reduction of parasitic resistances will become increasingly important as new device structures, especially 3D, and new materials are integrated
- Non-thermal energy sources and new reactive species provide enabling capabilities like the low-T plasma oxidation apparatus
  - Excellent corner rounding
  - Atomically flat interface
  - Nearly orientation independent oxidation
  - Low thermal budget processing
  - Excellent electrical isolation characteristic
- More-Moore, More-than-Moore and especially 3D devices will be enabled by low thermal budget processing



Acknowledgments

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Thank you very much for your attention!

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