



Leading Edge Si Devices: an Update

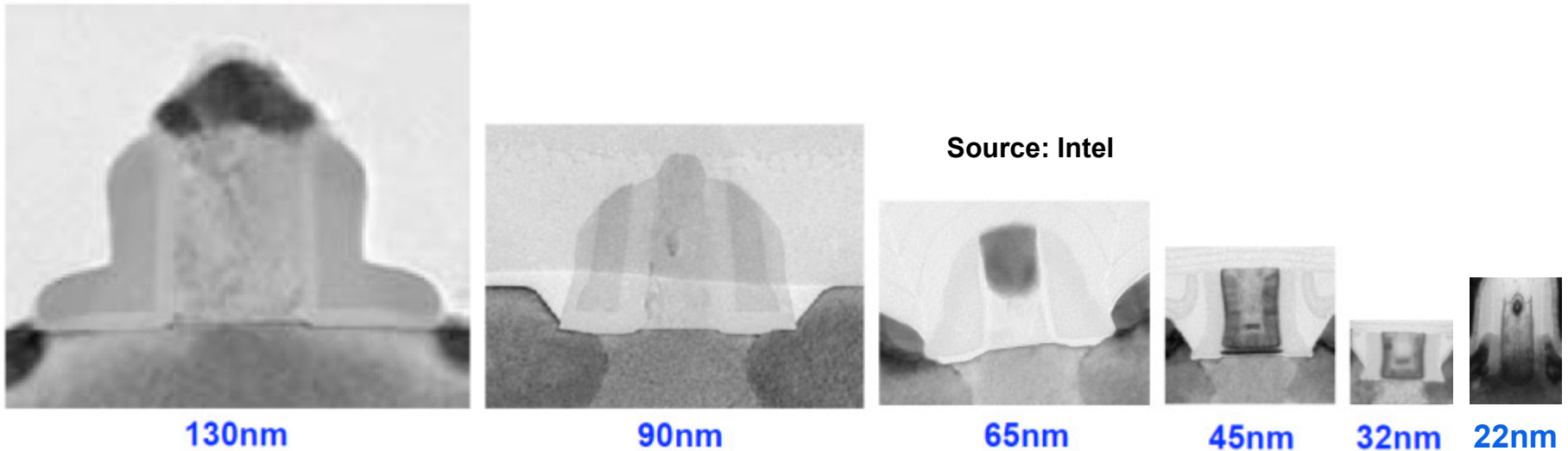
**Dick James, Senior Technology Analyst,
Chipworks**

Outline

- Logic transistors
 - GLOBALFOUNDRIES/AMD 32-nm Llano (HKMG, gate-first)
 - Samsung/Apple 32-nm A5 APL2498 (HKMG, gate-first)
 - Intel 22-nm Ivybridge (HKMG, gate-last, tri-gate)

The Last Few Generations

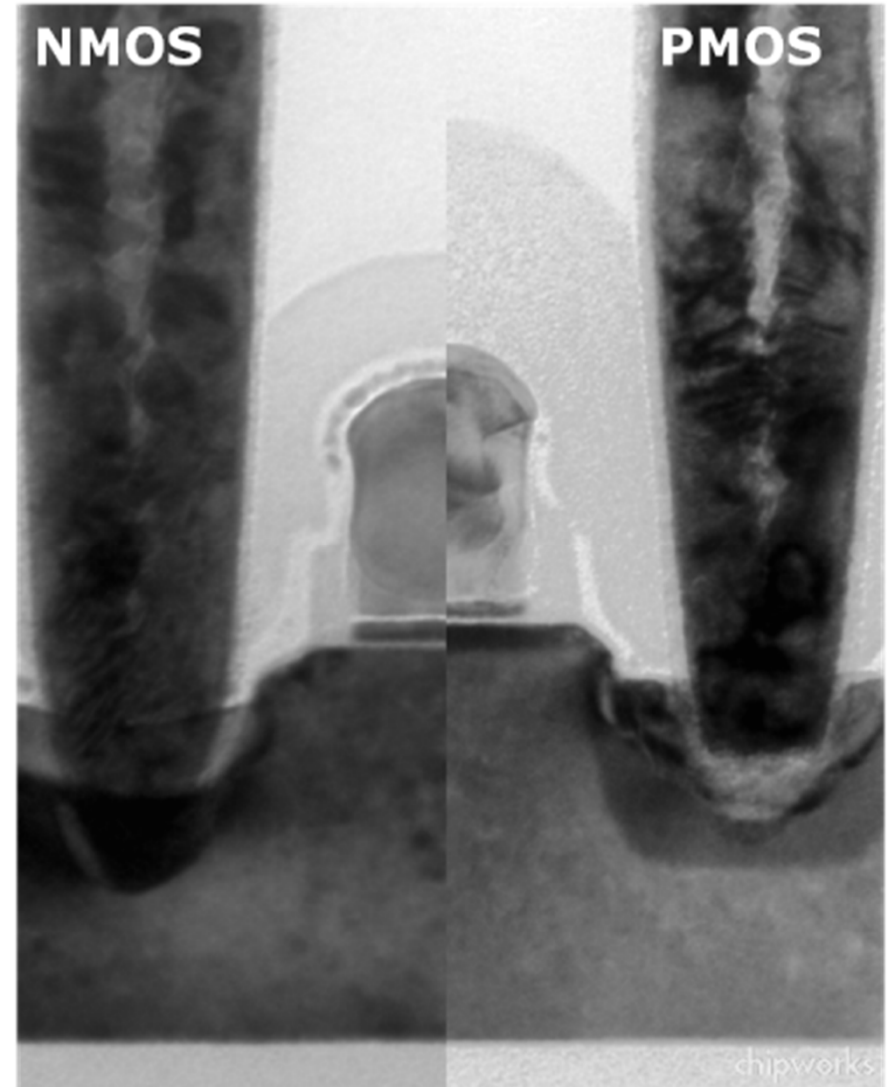
And the changes we've seen..



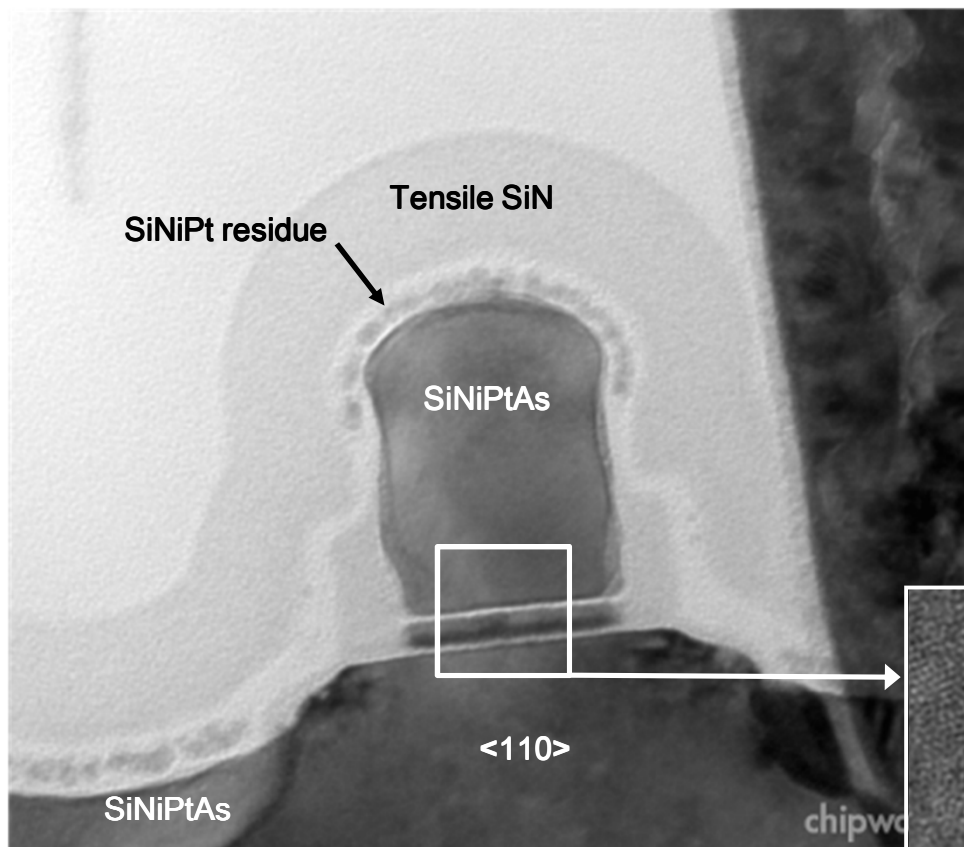
Lithography 248 nm -----> 193 nm -----> 193 nm wet
 Copper metallization ----->
 Low-k dielectrics (1st generation) ----->(2nd gen) ----->(3rd gen)
 Strained channels ----->
 High-k, metal-gate ----->
 Tri-gate FET

GLOBALFOUNDRIES/AMD A8-3850 Llano 32-nm HKMG

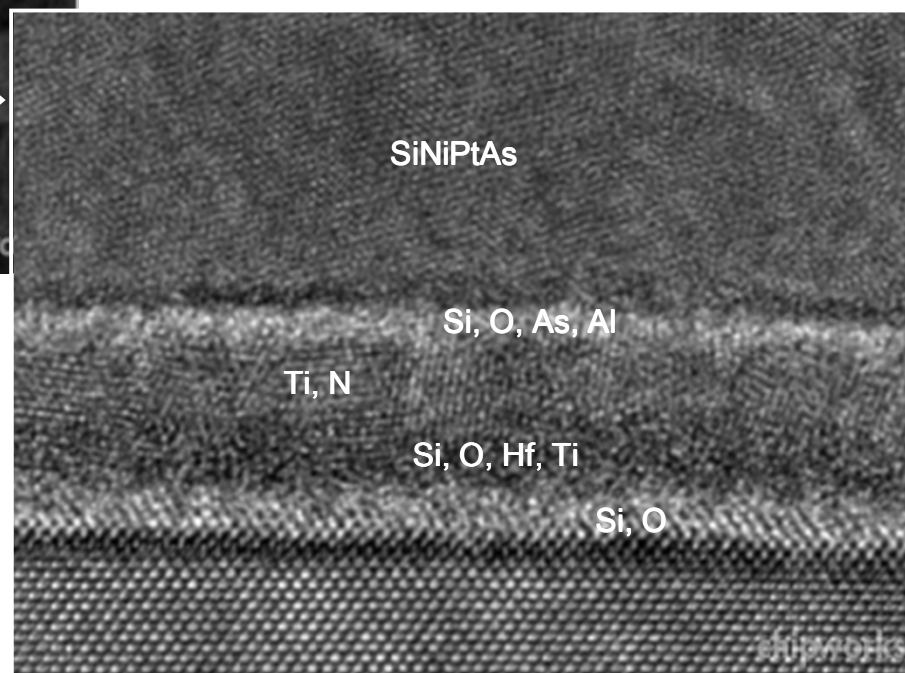
- Gate-first process on SOI substrate
- $T_{ox} \sim 1.2$ nm, Hf-based hi-k ~ 1.5 nm
- Dual-stress nitride liner for NMOS & PMOS channel stress
- Conventional $\langle 110 \rangle$ channel direction
- Epitaxial SiGe channel for PMOS performance
- Epitaxial SiGe source/drains for PMOS channel stress



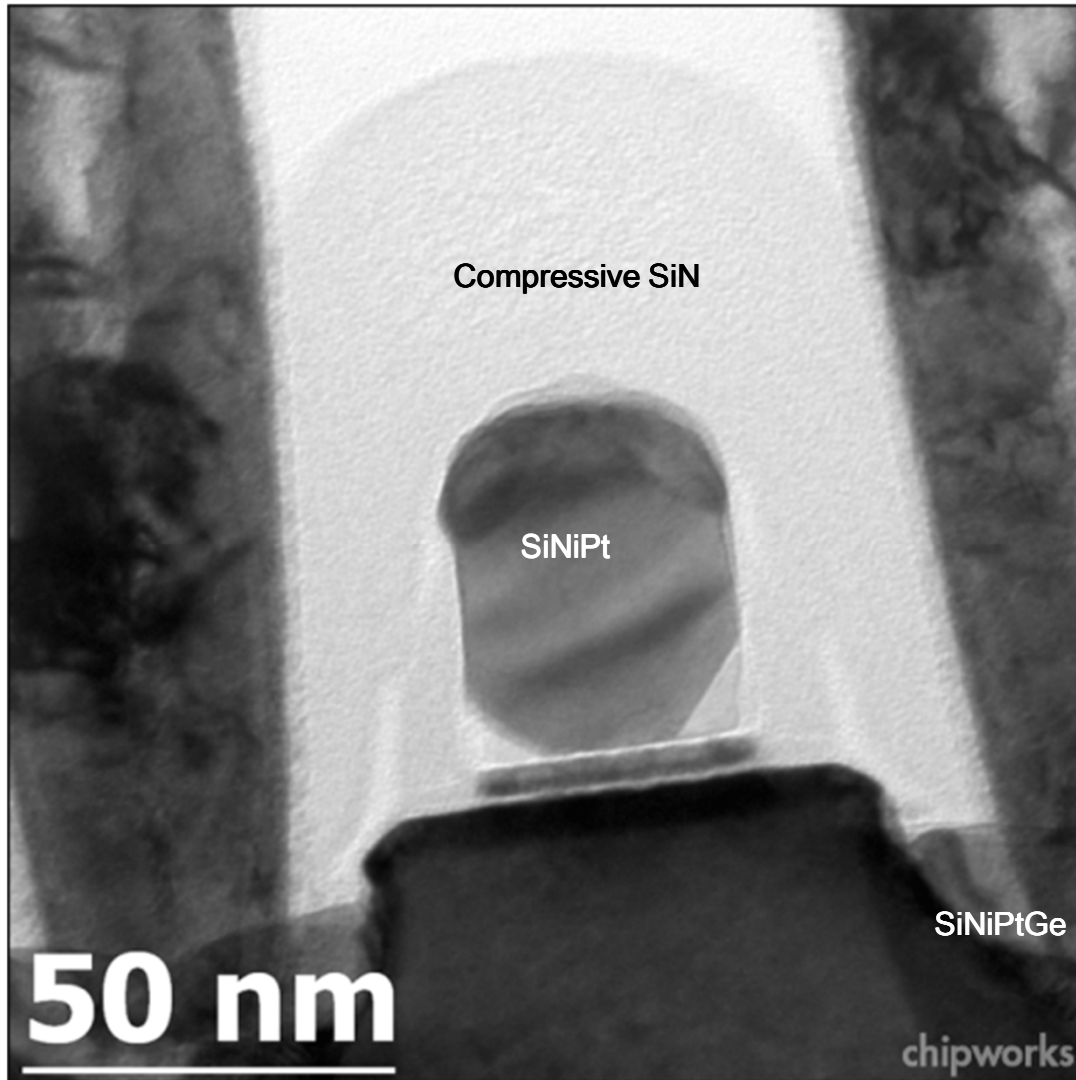
AMD/GLOBALFOUNDRIES 32-nm NMOS Transistor



- Minimum gate length observed ~33 nm
- Gates almost fully silicided
- Si-O-Al interface (barrier?) layer above TiN work function layer
- Tensile nitride liner for channel stress
- Dual stress-memorization cited

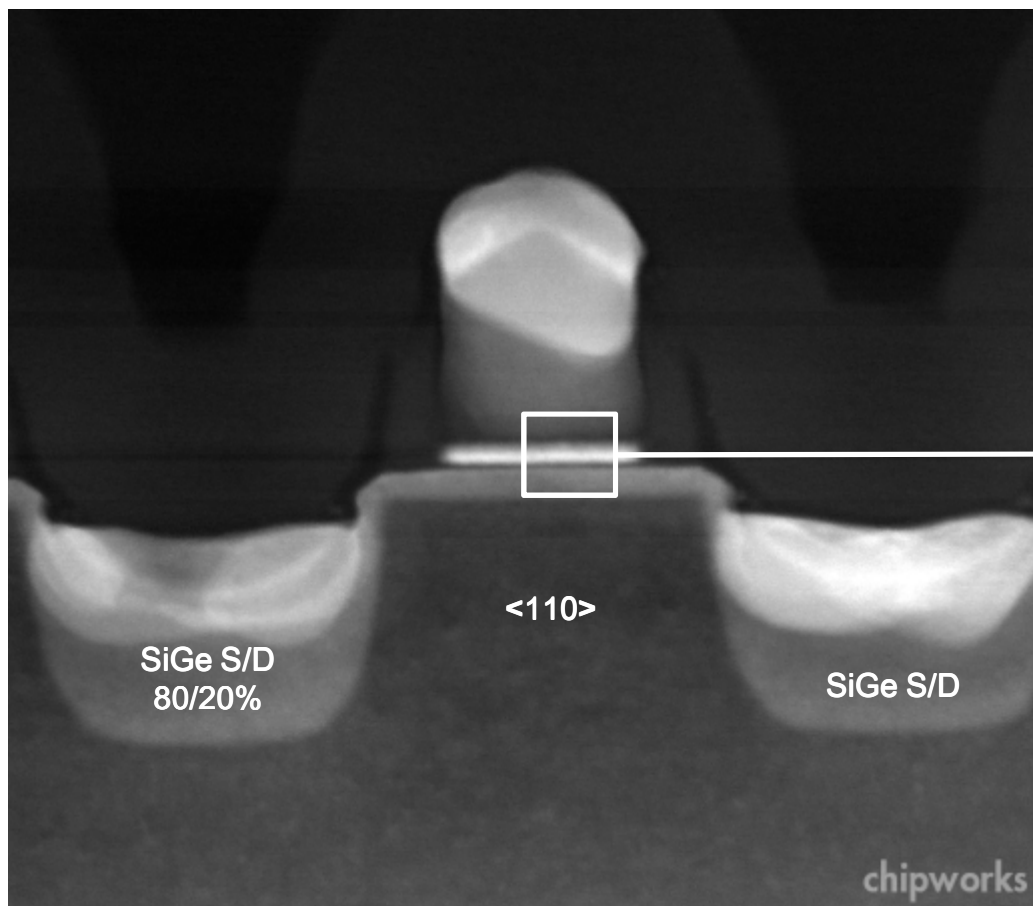


AMD/GLOBALFOUNDRIES 32-nm PMOS Transistor



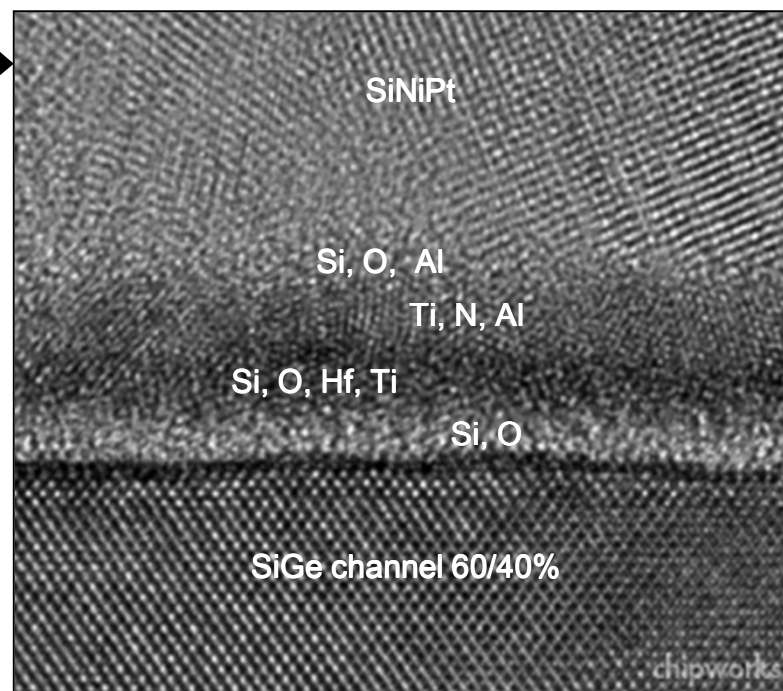
- Minimum gate length observed ~36 nm
- Gates almost fully silicided
- Si-O-Al interface (barrier?) layer above hi-k stack
- Compressive nitride liner for channel stress
- NMOS/PMOS gate stacks the same

AMD/GLOBALFOUNDRIES 32-nm PMOS Transistor



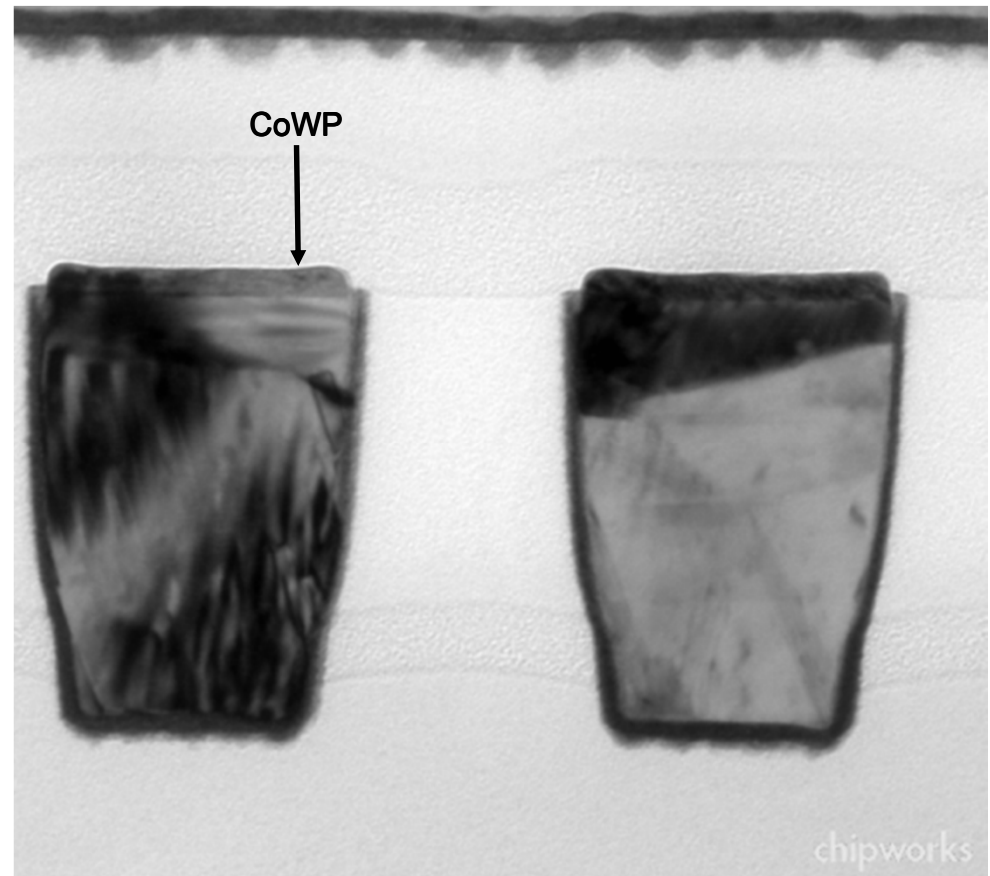
Dark-field image

- No dopant seen in stack for V_t shift
- SiGe channel shifts V_t , improves mobility
- SiGe source/drains for channel stress



AMD/GLOBALFOUNDRIES 32-nm Metal 1

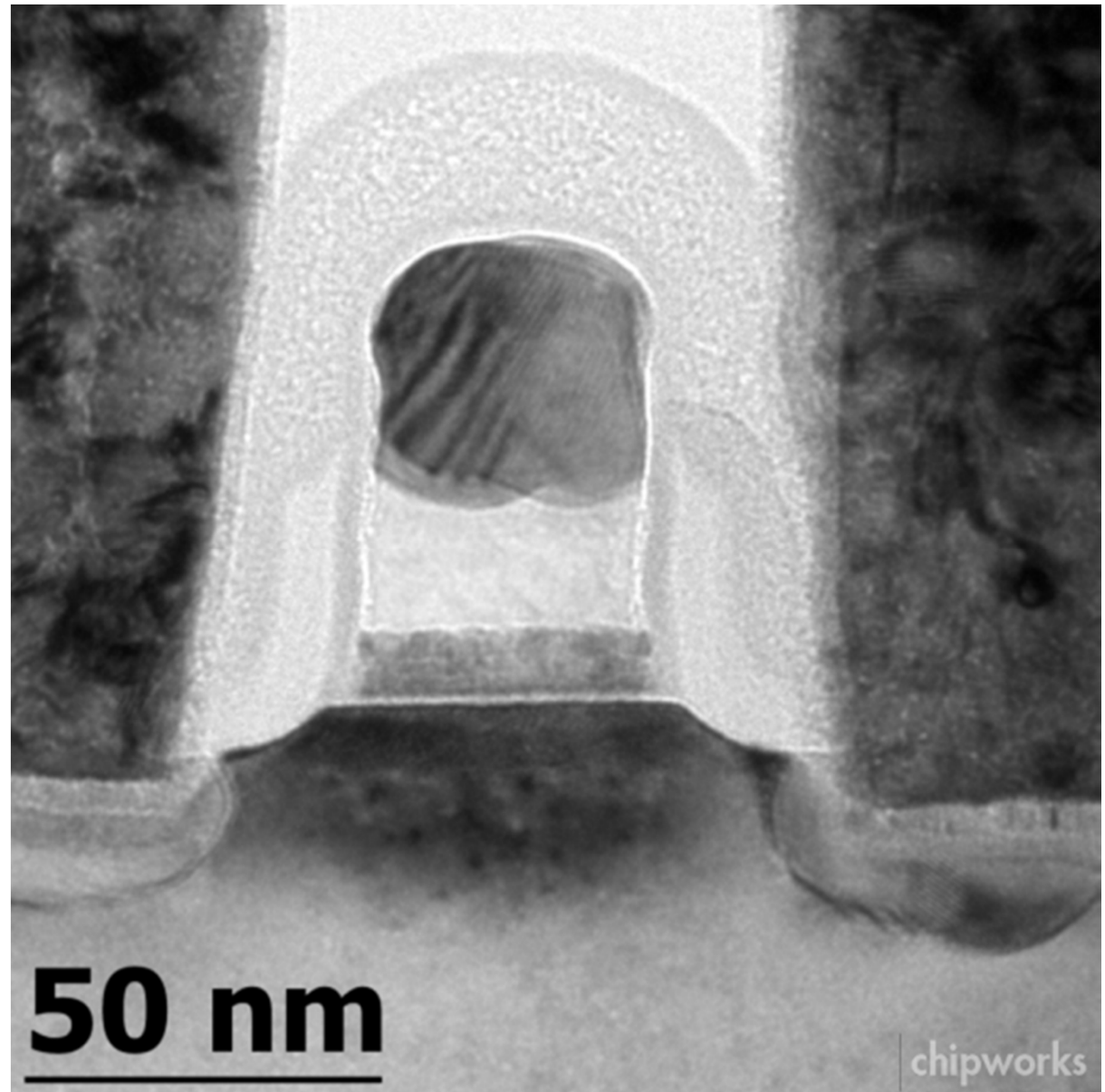
- Minimum metal pitch ~130 nm
– similar to Intel 32-nm
- CoWP layer on top of Cu lines to reduce electromigration



Apple A5 APL2498 (Samsung 32 nm HKMG gate-first LP process)

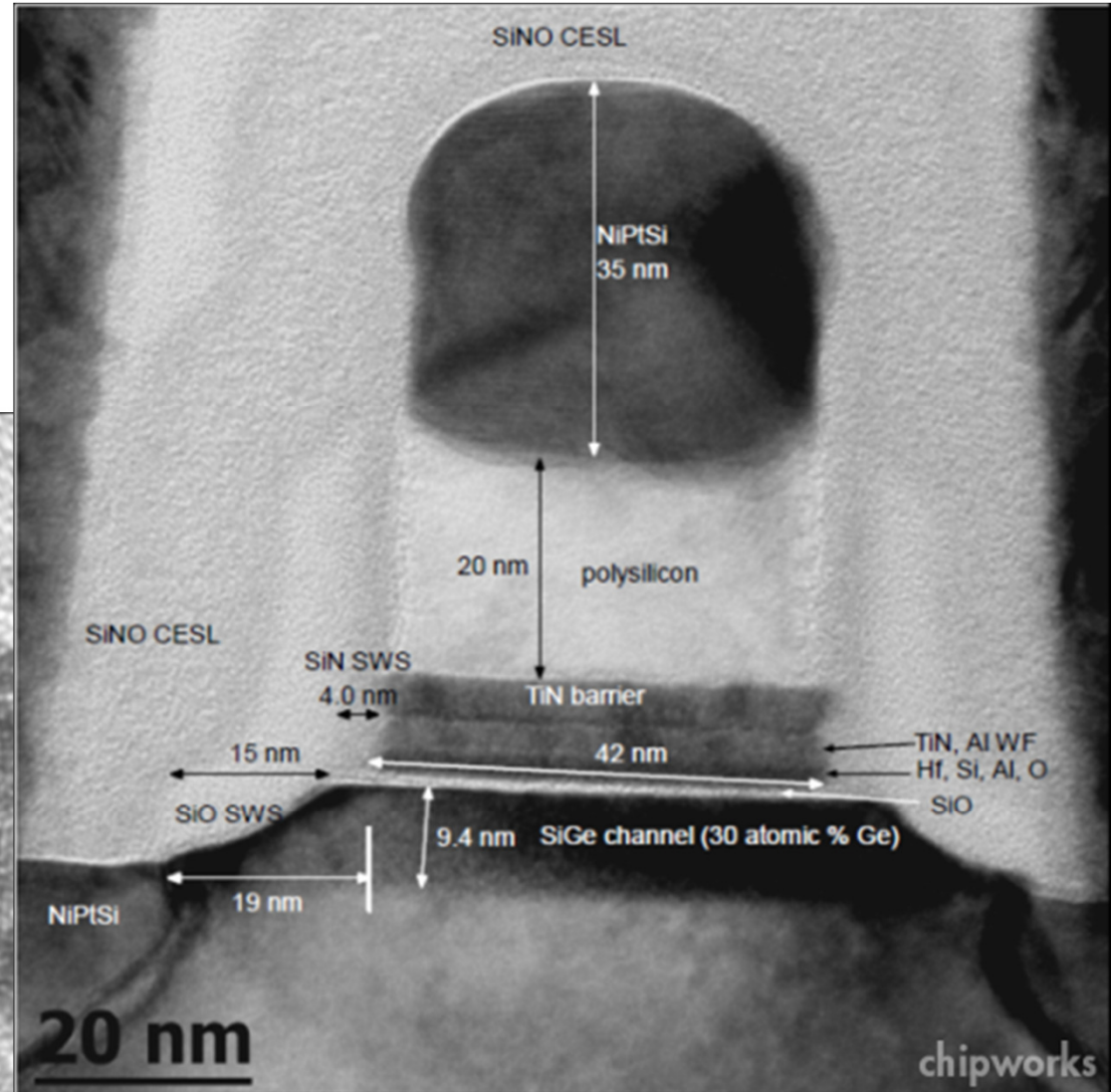
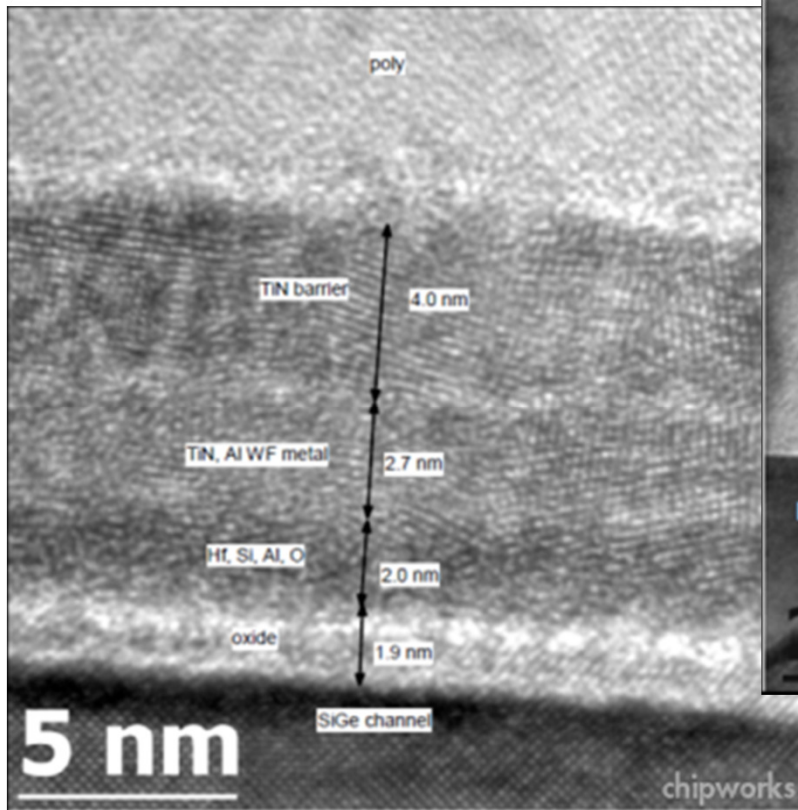
Apple/Samsung APL2498 PMOS Transistor

- Minimum gate length observed ~36 nm
- Gate-silicide ~19 nm
- Differential oxide spacer
- SiGe channel, $\langle 100 \rangle$
- No dual-stress liner
- Normal silicidation, Pt-doped NiSi (GF was almost fully silicided)



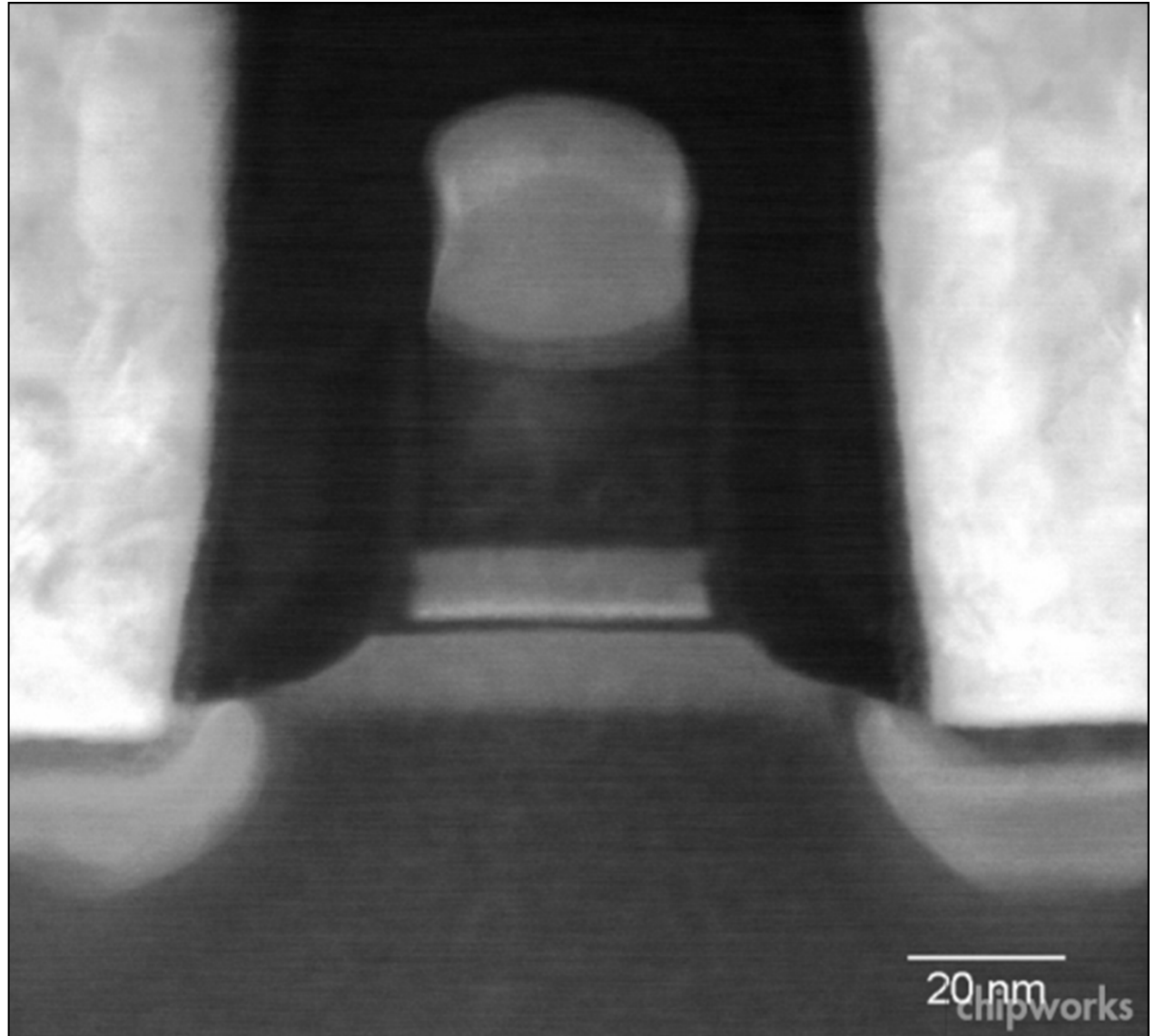
Apple/Samsung APL2498 PMOS Transistor

- SiGe channel ~30% Ge
- TiN, Al WF source layer
- 2nd TiN layer is NMOS WF layer deposited on PMOS WF layer

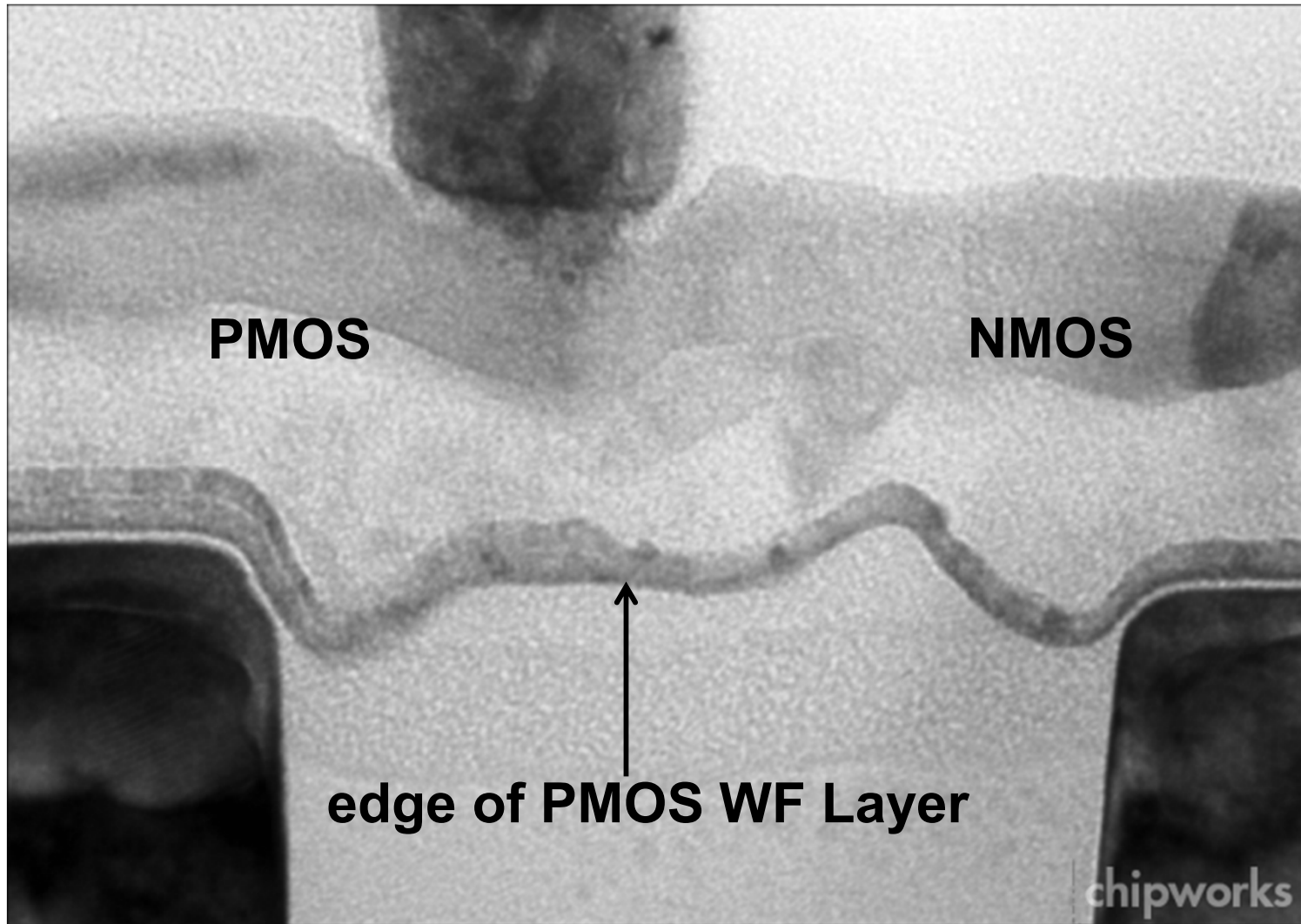


Apple/Samsung APL2498 PMOS Transistor

- STEM dark-field image

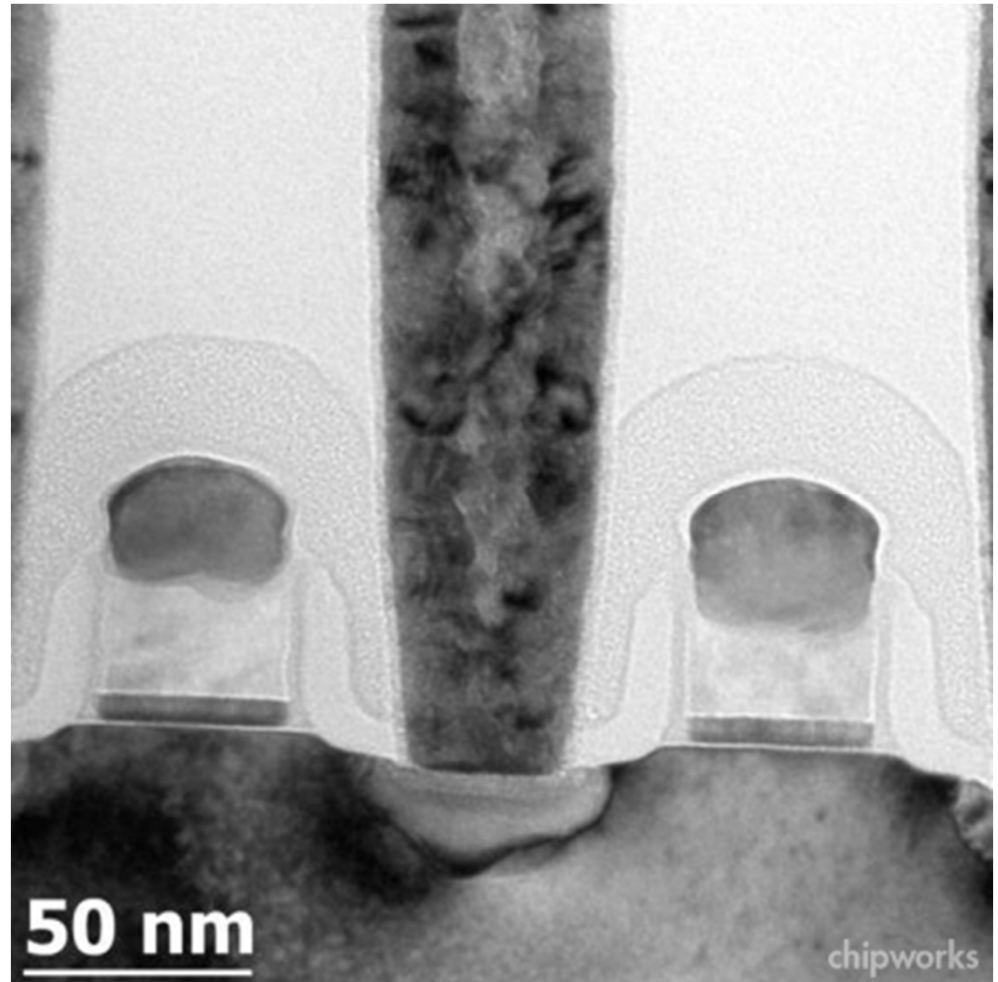


APL2498 PMOS/NMOS Transition



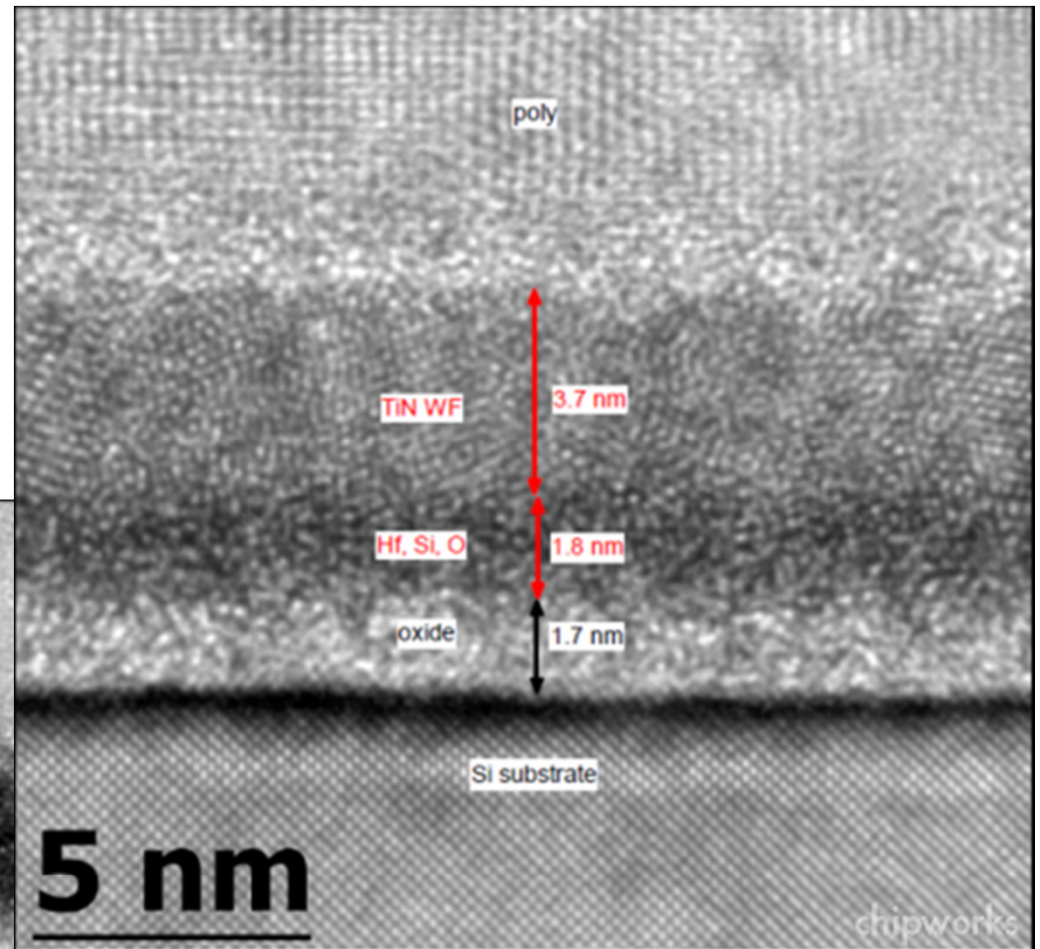
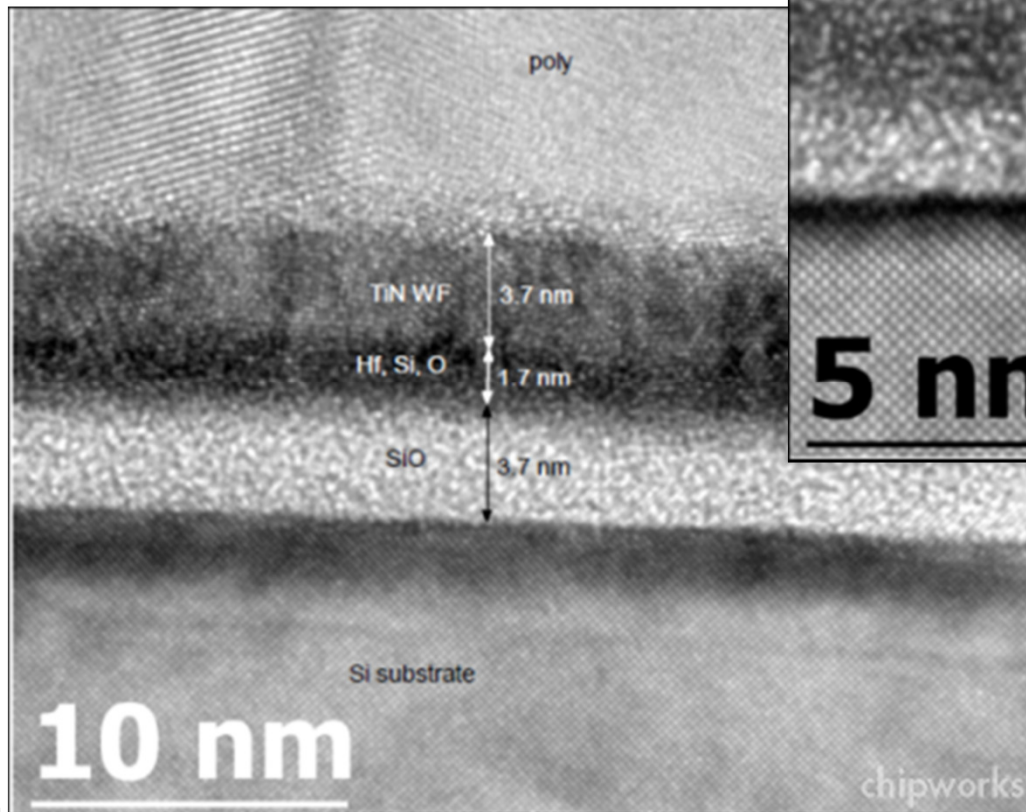
Apple/Samsung APL2498 NMOS Transistor

- Minimum gate length observed
~38 nm
- Gate-silicide ~17 nm
- Differential oxide spacer
- Stress memorization & tensile CESL?
- Normal silicidation, Pt-doped NiSi (GF was almost fully silicided)



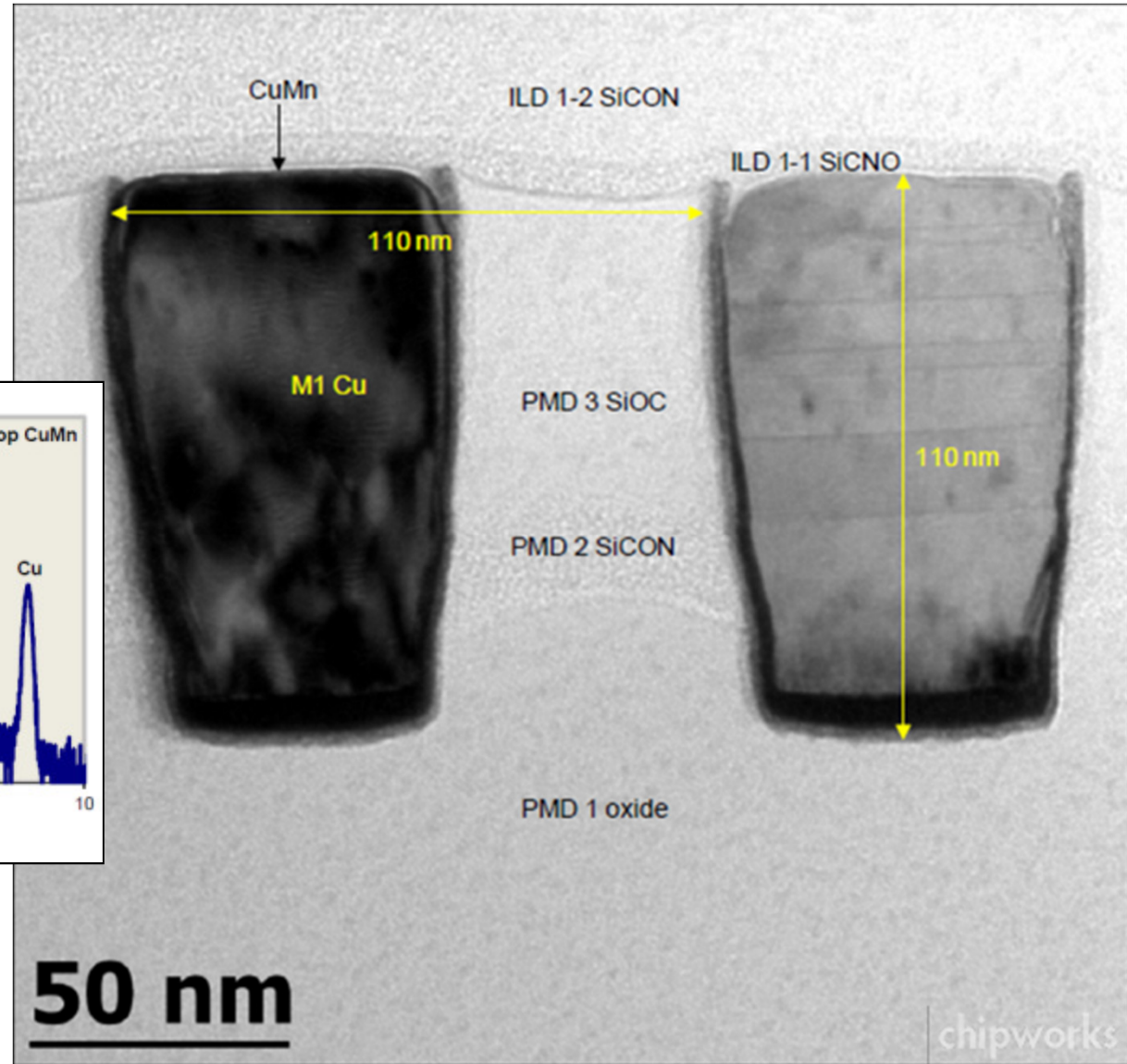
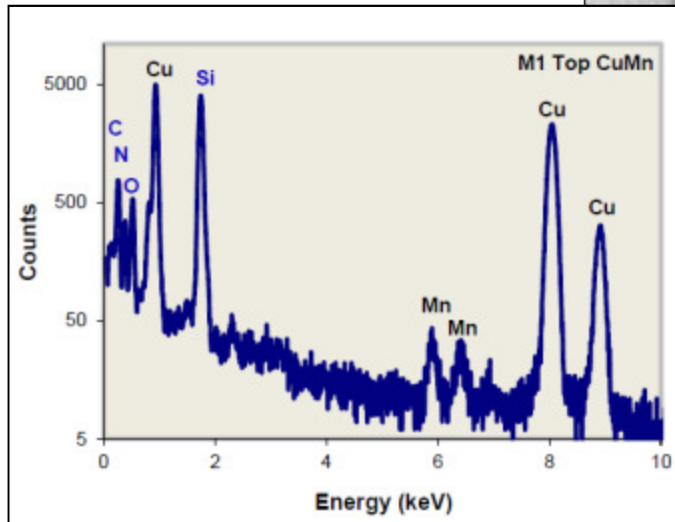
Apple/Samsung APL2498 NMOS Transistor

- $T_{\text{diel}} \sim 1.8$ nm nitrided oxide + 1.8 nm HfSiO
- 3.7 nm TiN WF layer, no dopant identified
- Thick ~ 3.7 nm t_{ox} NMOS noted

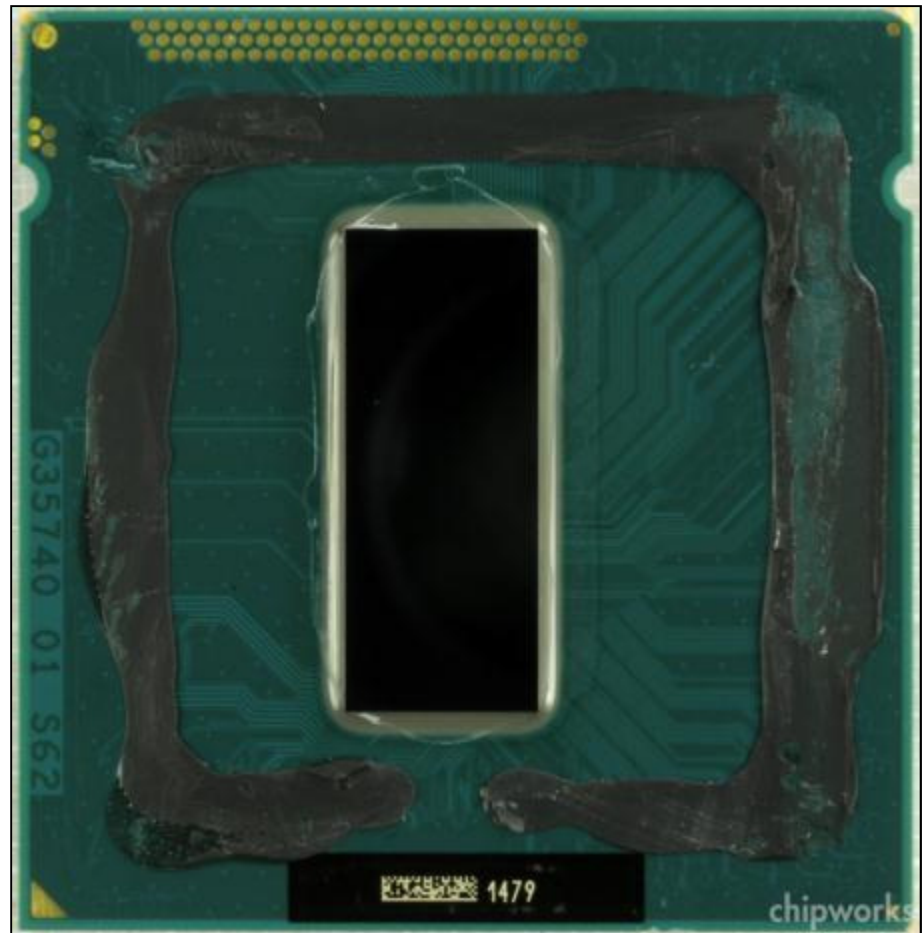


Apple/Samsung APL2498 Metals

- Cu is Mn-doped to reduce EM in M1 – M6

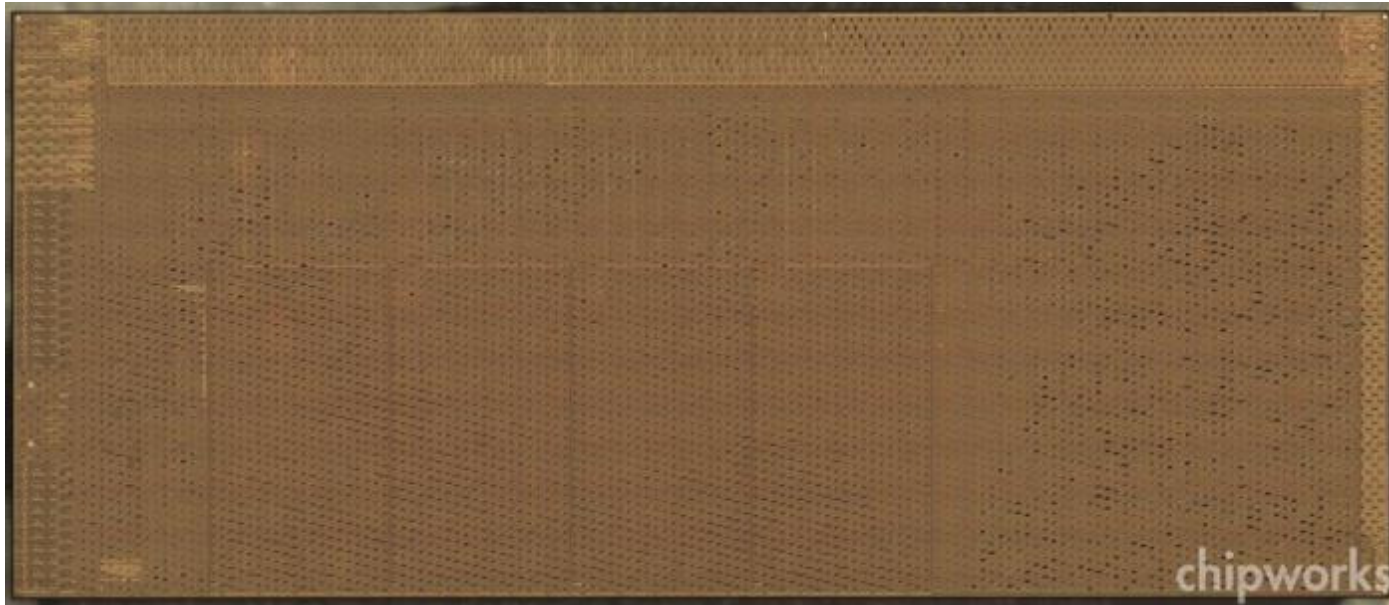


Intel Xeon E3-1230V2

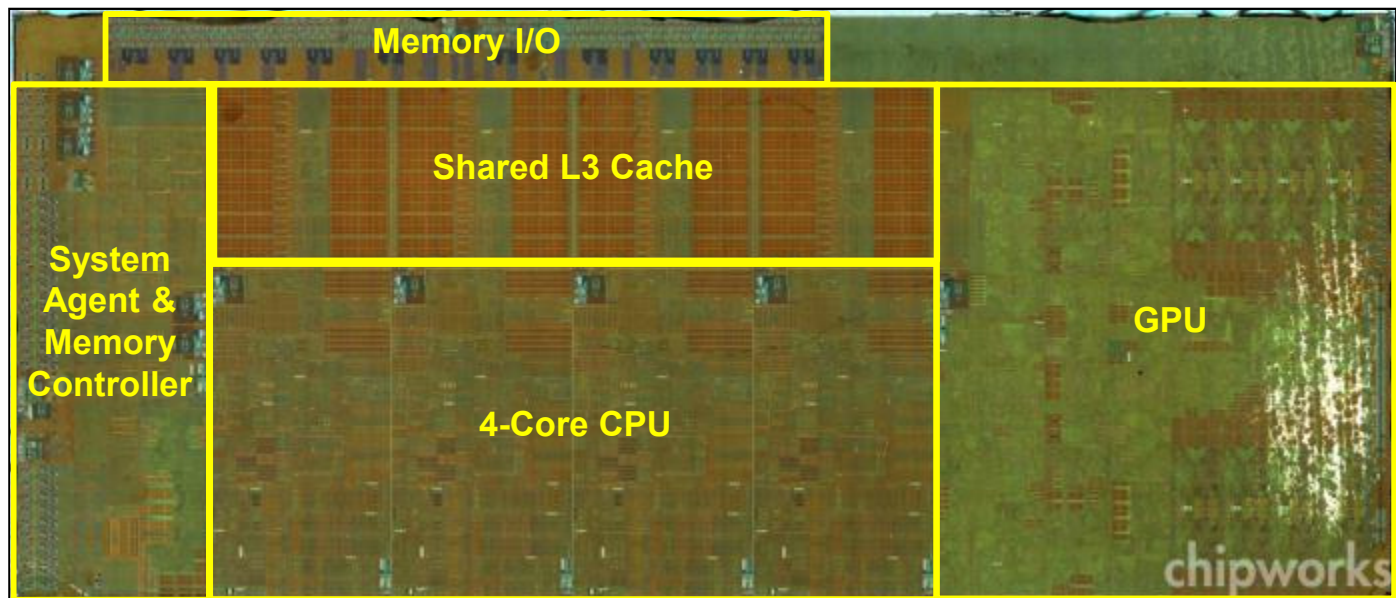


- Die size 8.06 x 19.52 mm (157 mm²)
- Eight-layer (2 + 6) build-up substrate

Intel Xeon E3-1230V2

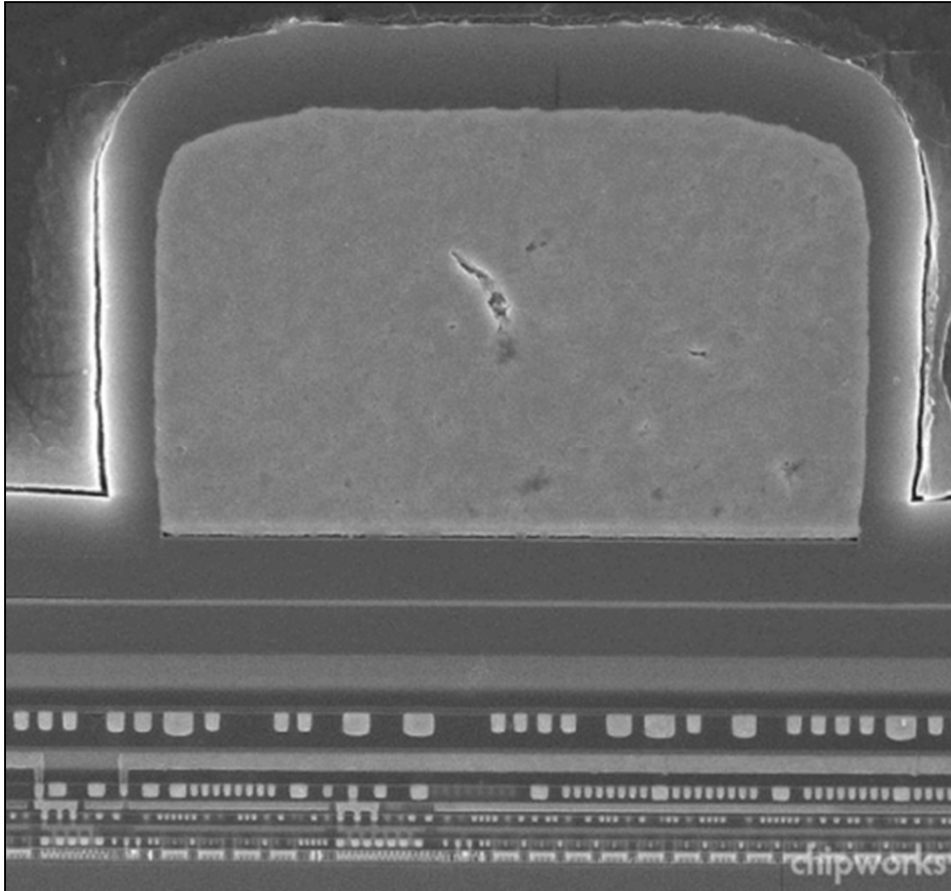


Top metal

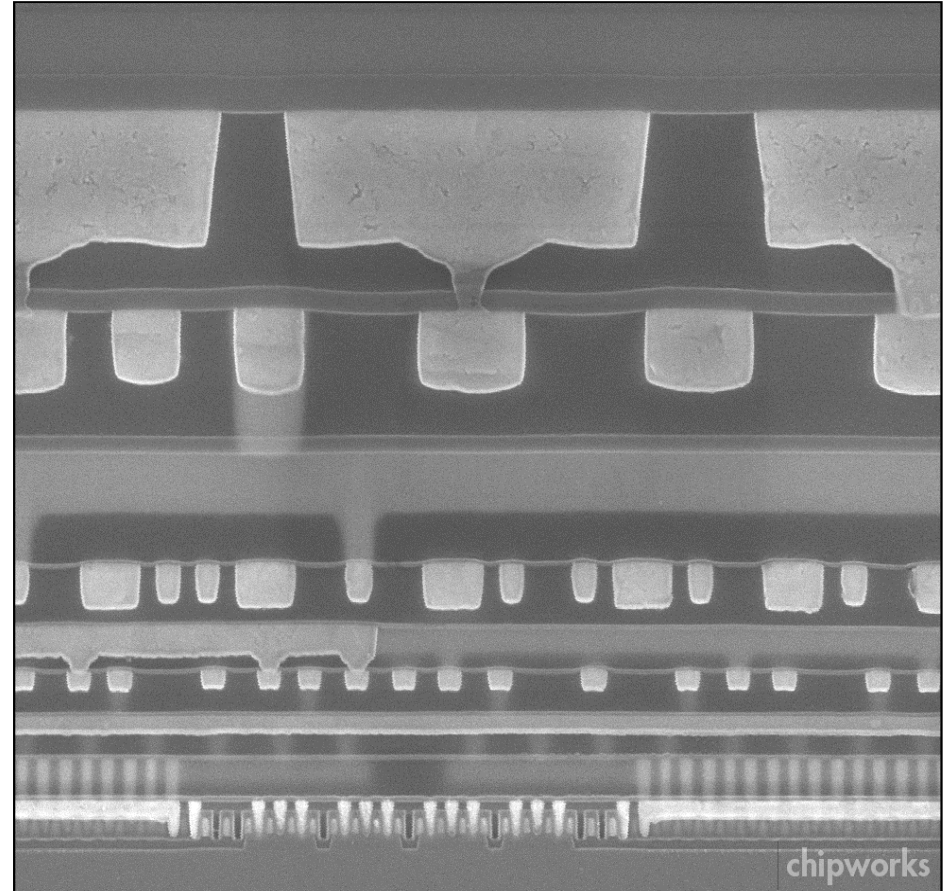


Delayed to gate level

General Structure



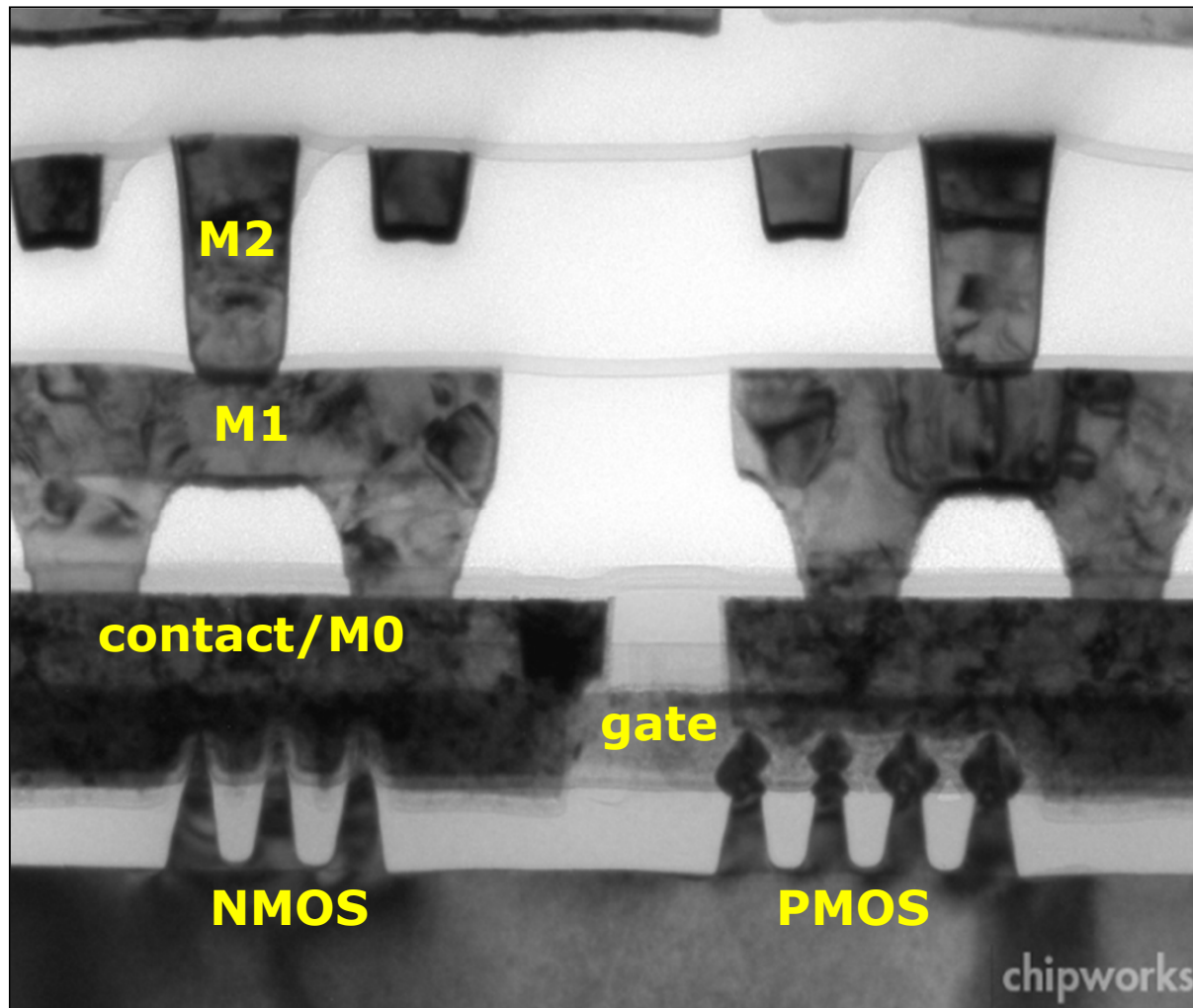
Full stack



M0 – M8

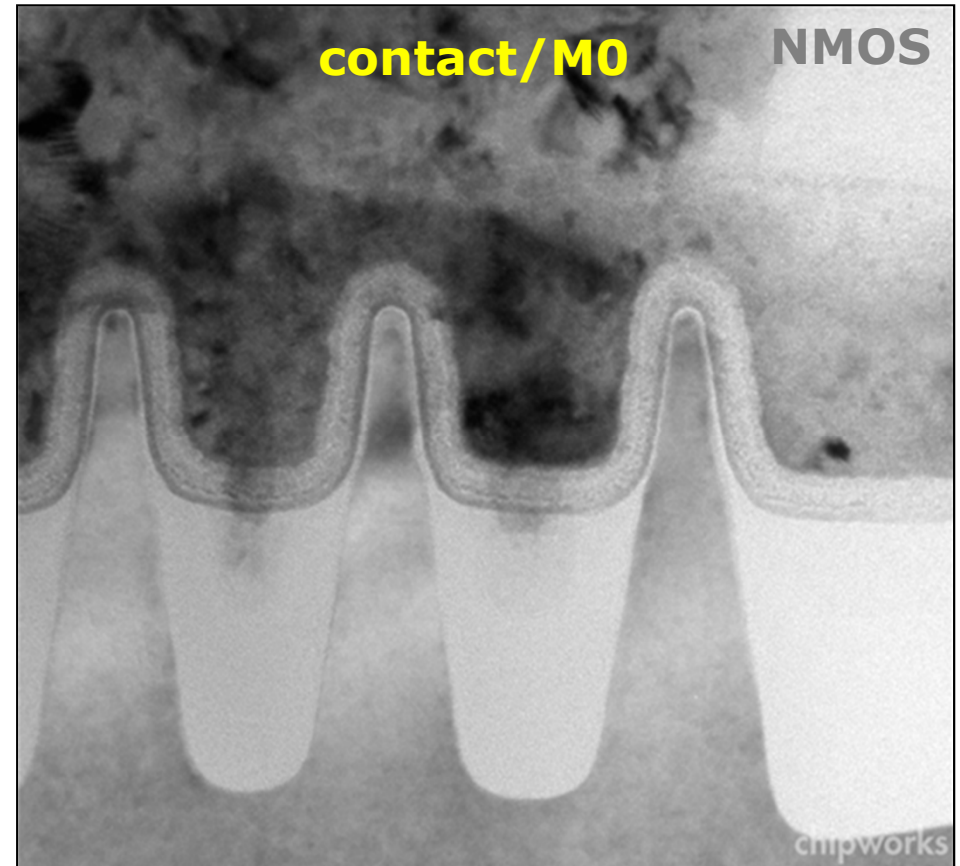
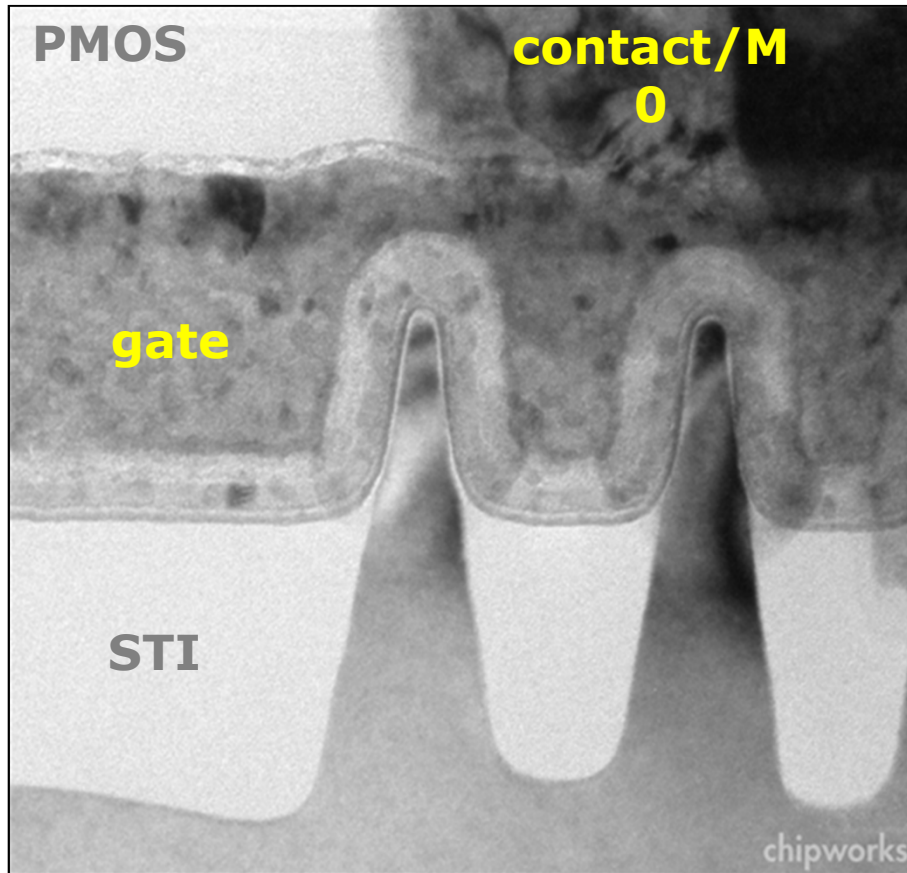
- Nine copper metal layers + tungsten M0 + MIM capacitor

FinFETs



- Common replacement gate trench for NMOS/PMOS
- Contacted gate pitch ~ 90 nm
- Tungsten trench contacts and M0

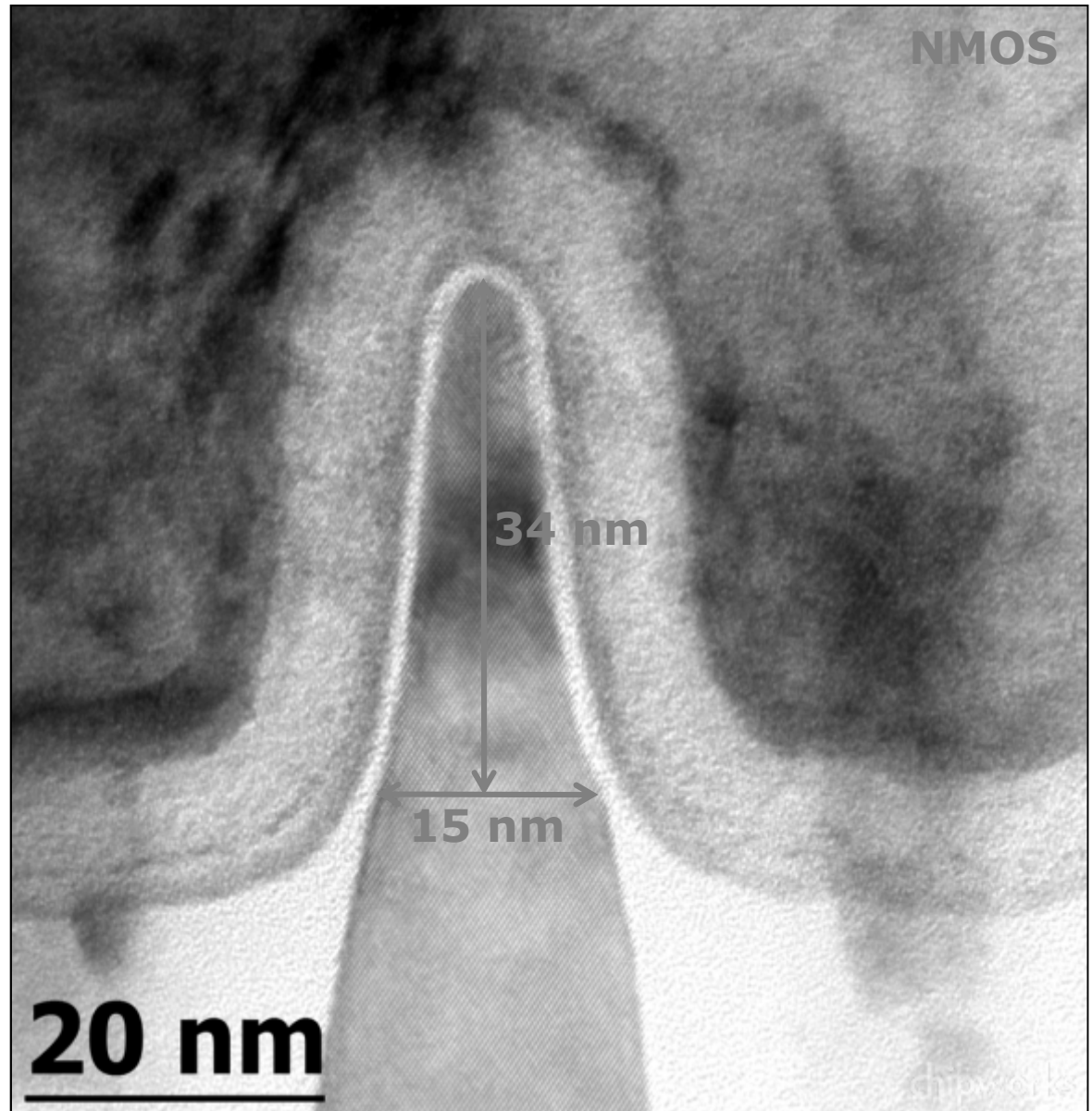
FinFETs – Fins



- Tapered fins, rounded tops for reliability
- Fin height ~100 nm, fin pitch ~60 nm

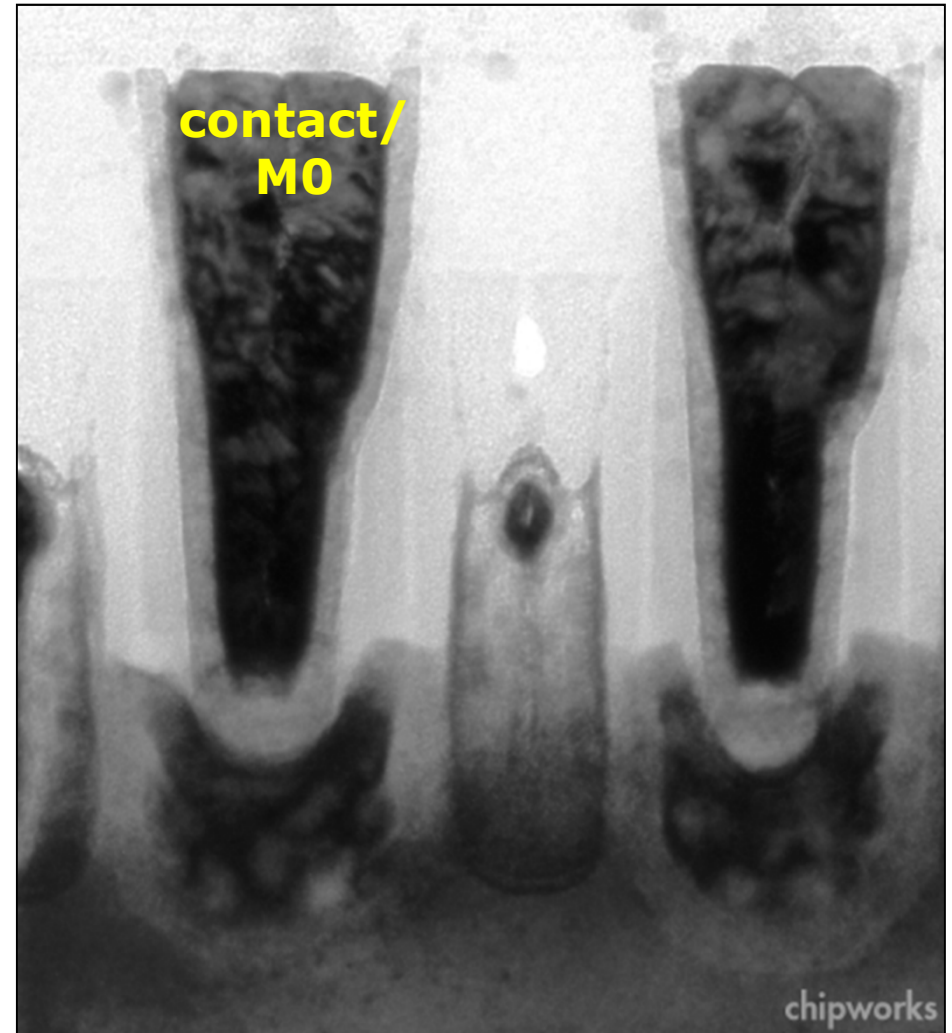
FinFETs – Fin Details

- NMOS/PMOS fins similar
- Top radius ~ 2.5 nm
- Functional fin width 5 – 15 nm top/bottom
- Gate width ~ 70 nm
- $\langle 110 \rangle$ channel direction



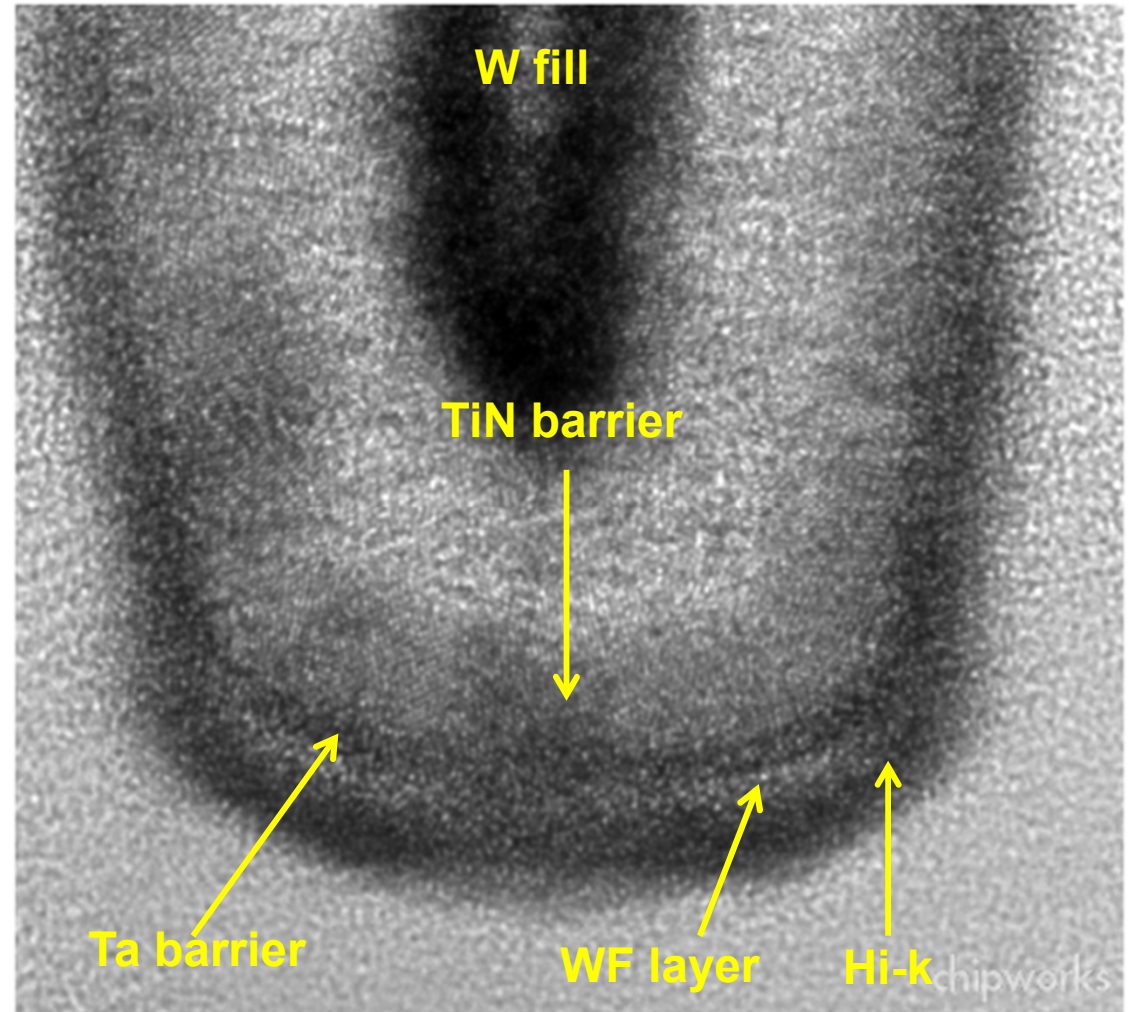
FinFETs – PMOS Gates

- Minimum gate length observed ~ 25 nm
- Epi SiGe in PMOS source-drains, isotropic cavity etch
- Ti silicide, not Ni
- Gates back-etched and filled with dielectric, allows self-aligned contacts



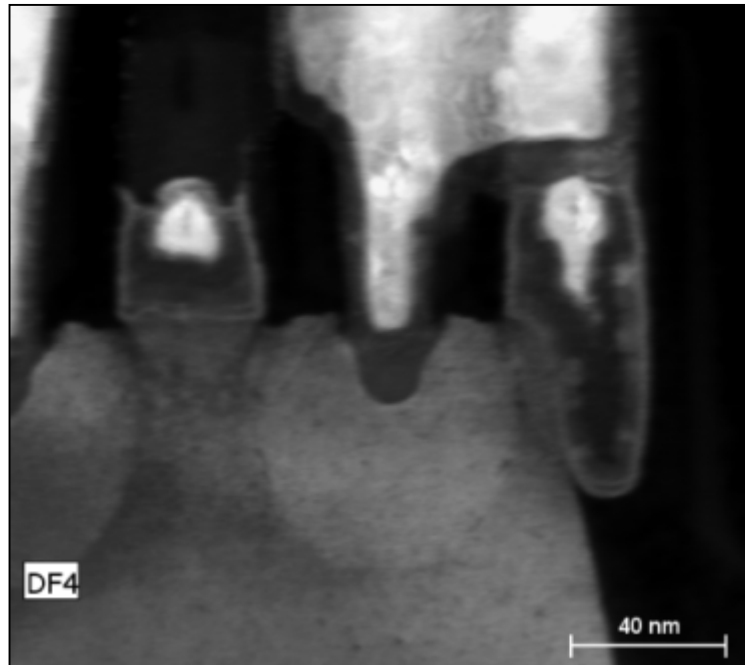
FinFETs – PMOS Gate

- Similar gate stack to 32-nm, 45-nm generations
- TiN work-function metal, ~1 nm Hf-based hi-k, ~1 nm SiO
- Gate fill changed from Ti-Al to tungsten/TiN

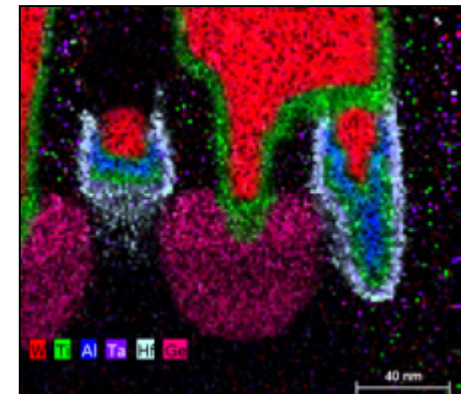
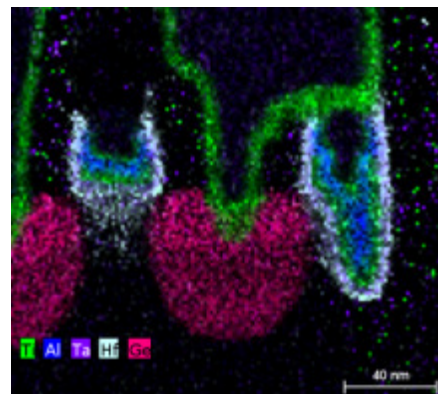
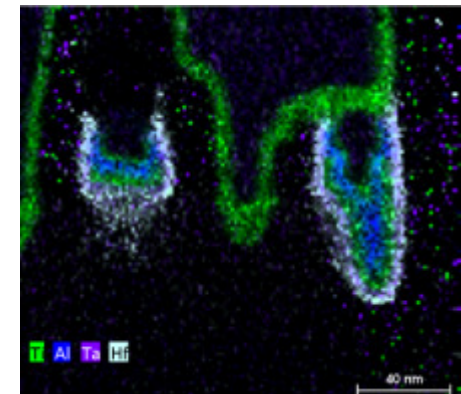
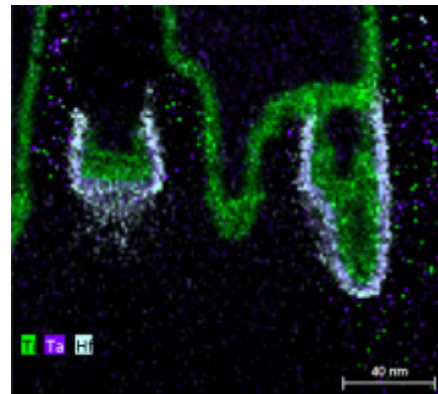
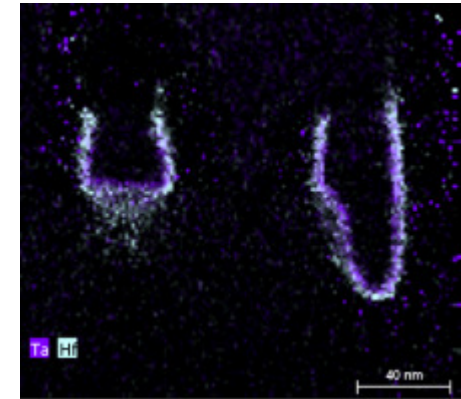
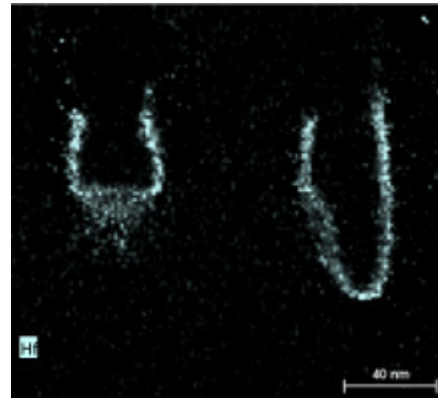


Bottom of PMOS gate

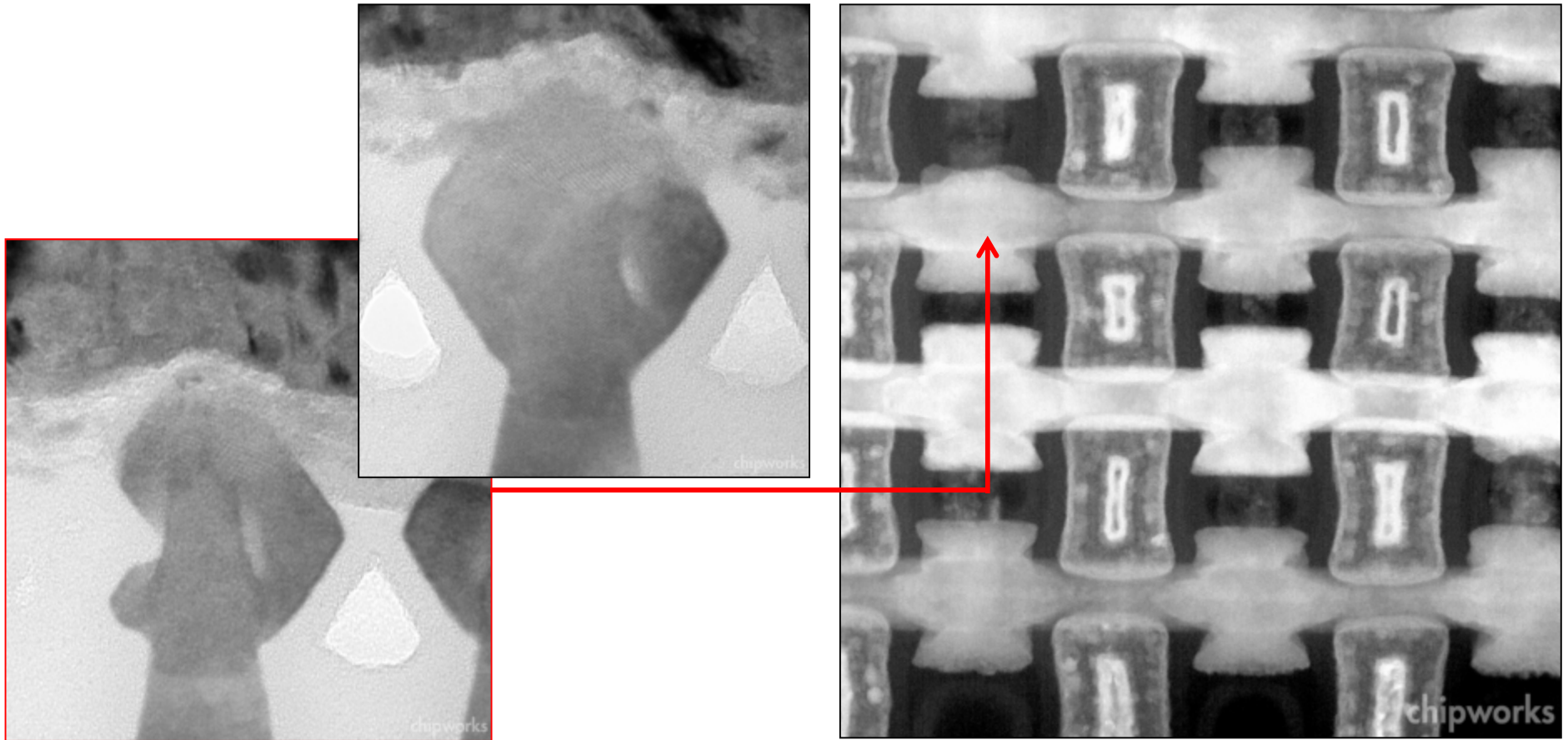
EDS Mapping of PMOS Gates



- 10-nm thin sample
- Shows the complex sequence of depositions in the gate stack



FinFETs – PMOS Source/Drains

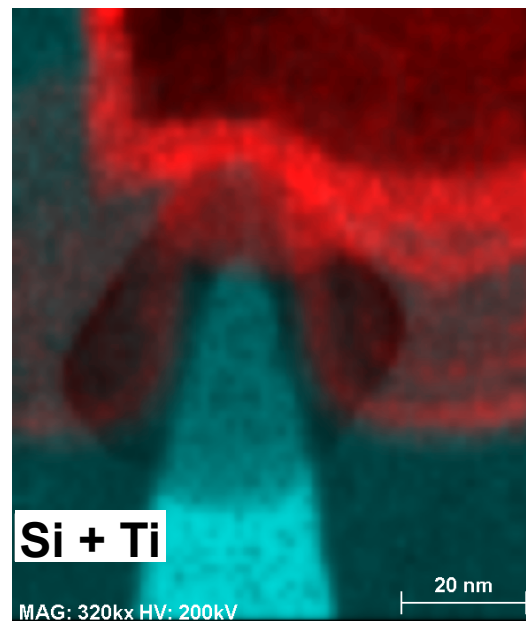
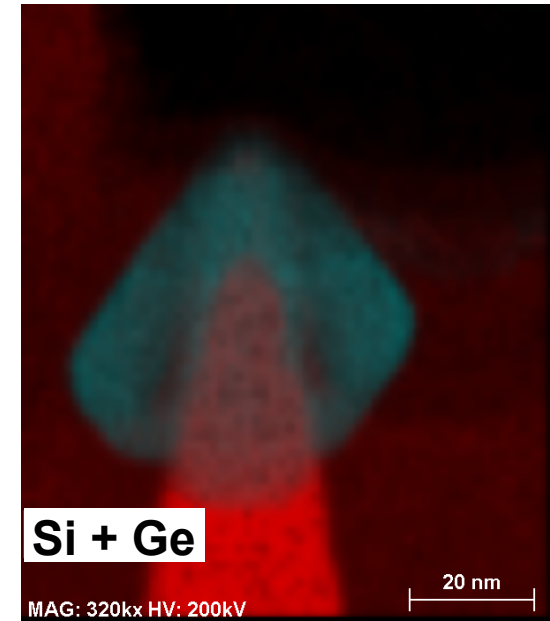
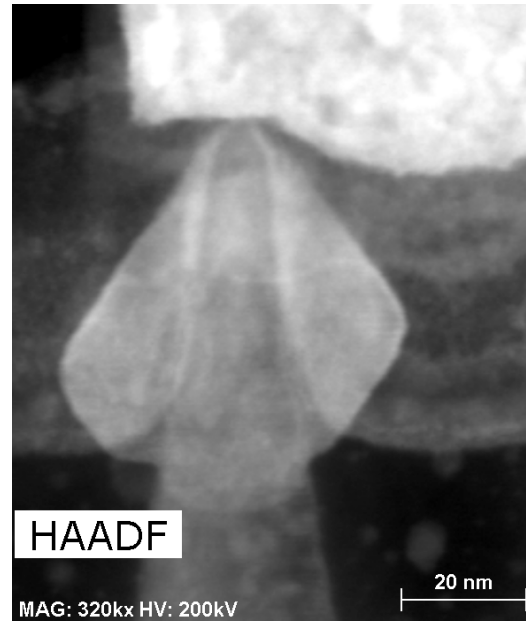


Plan-view STEM image

- ~50% SiGe, defects in epi growth on some fins
- E-SiGe appears to penetrate slightly under gate
- Epi lateral growth limited by sidewall spacer (SWS)

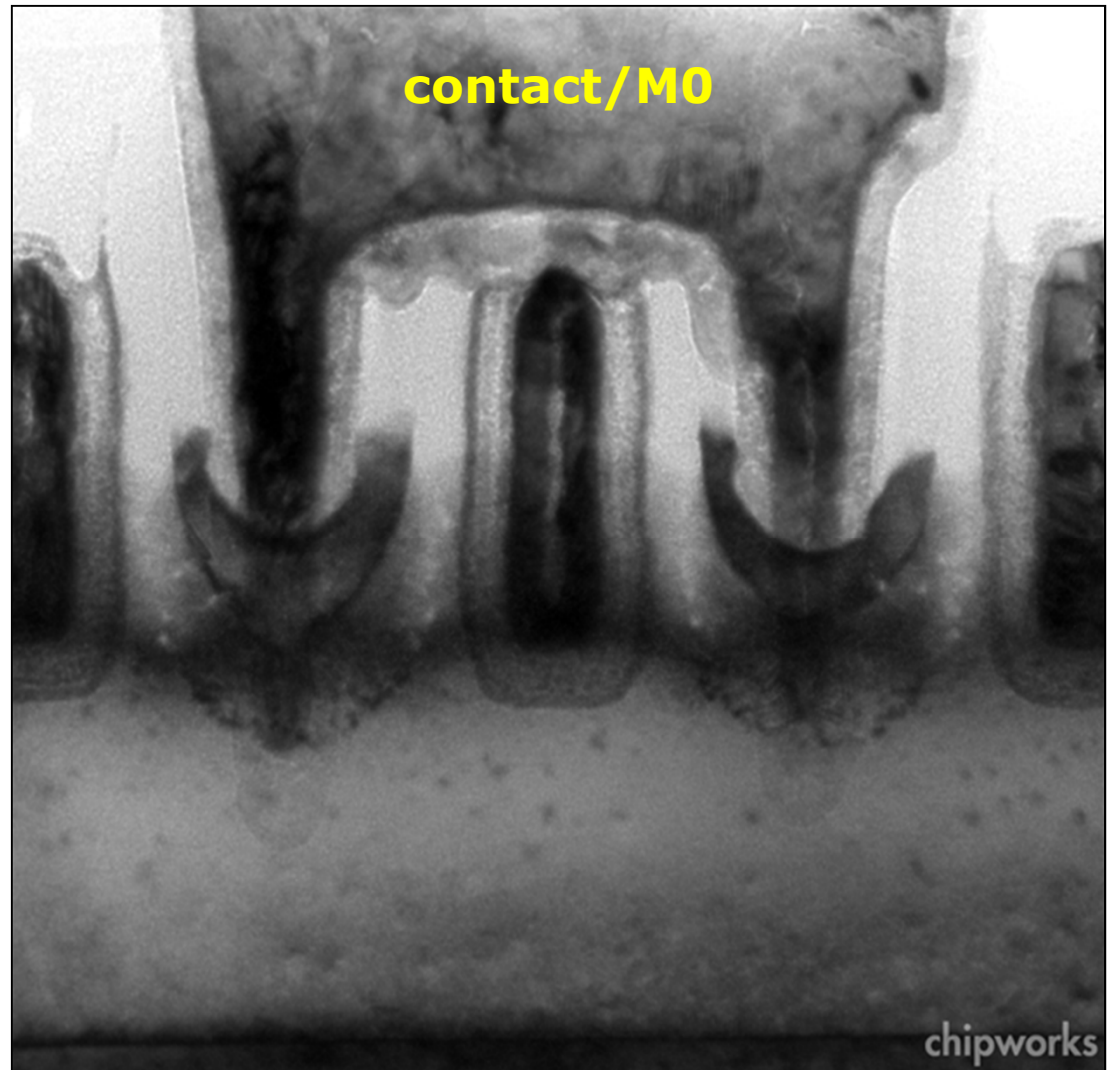
PMOS Source/Drains EDS Maps

- Clearly shows Ti silicide in epi



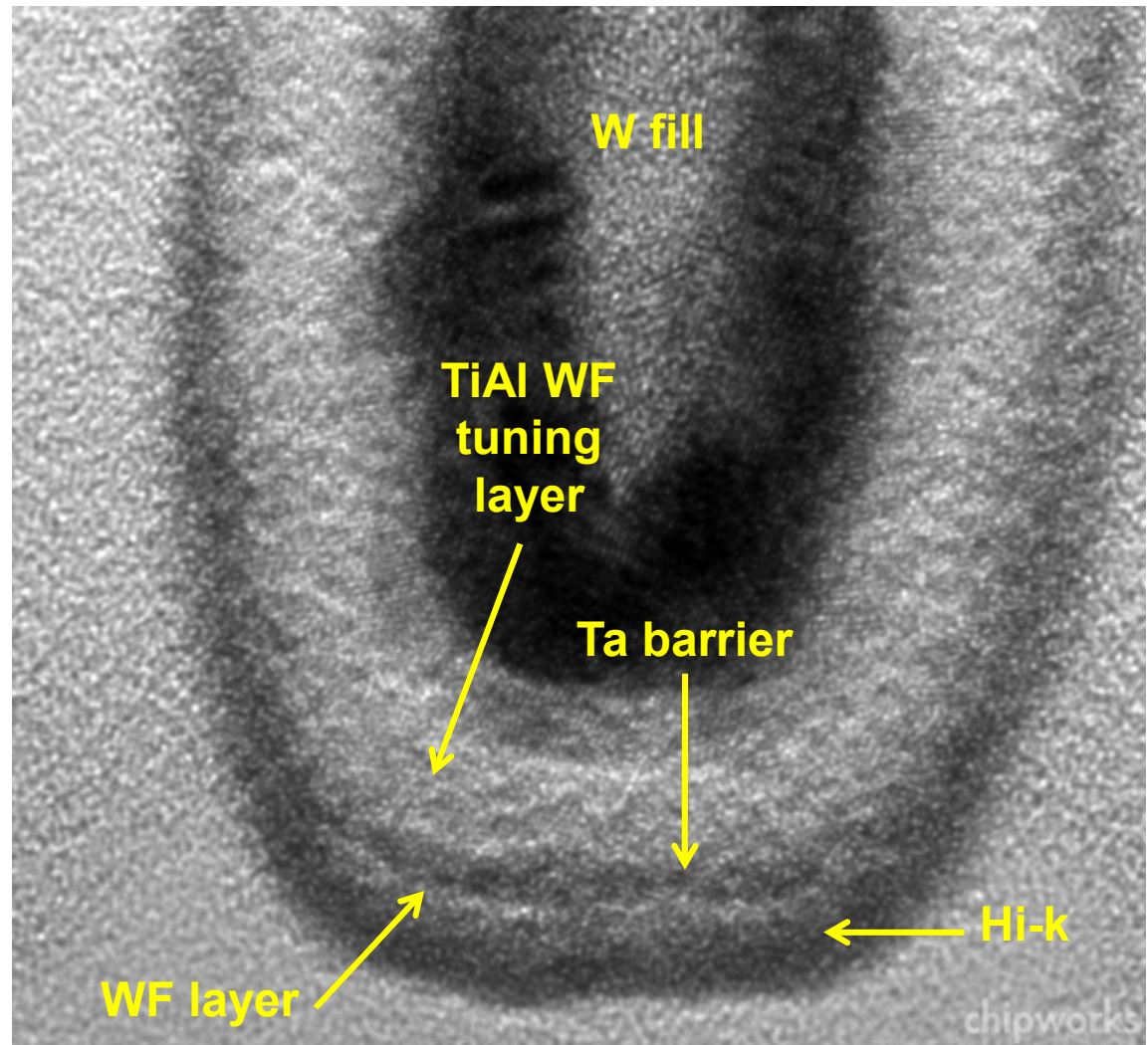
FinFETs – NMOS Gates

- Min gate length observed ~ 25 nm
- Isotropic cavity etch(?)
- Ti silicide, not Ni



FinFETs – NMOS Gate

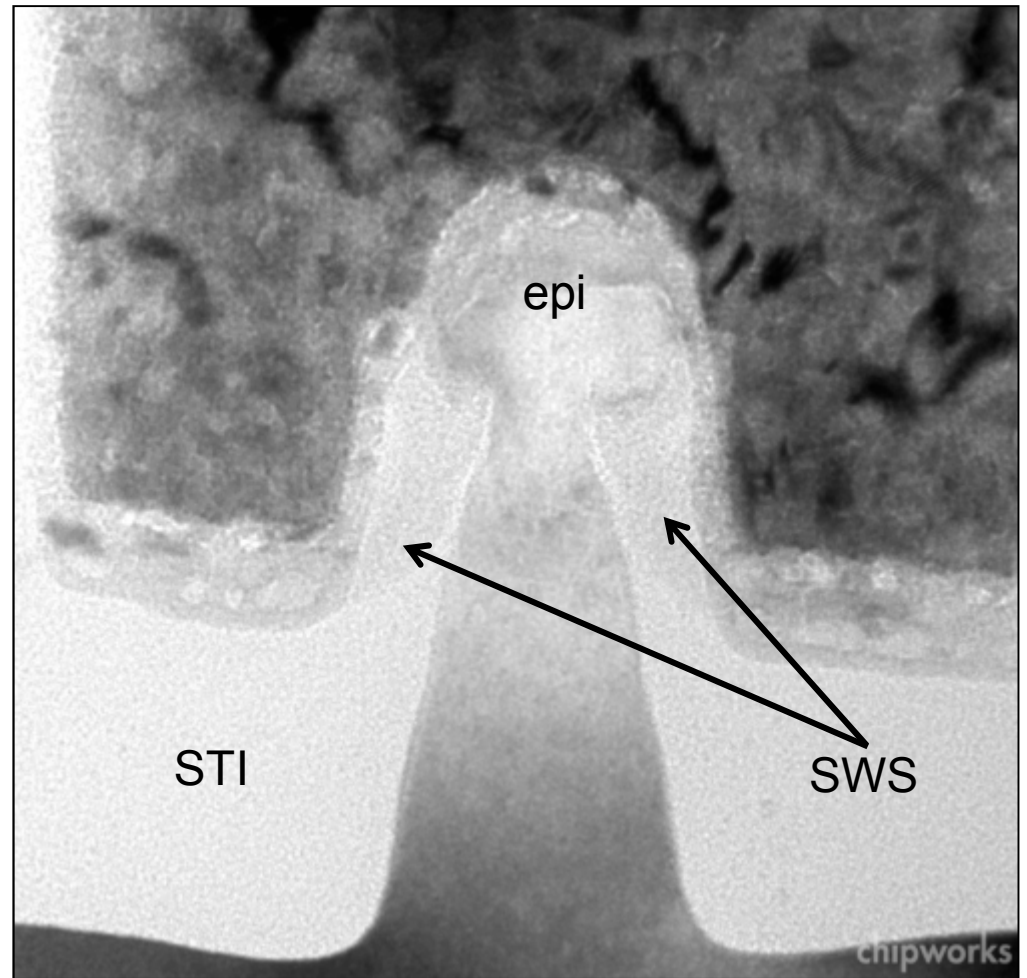
- Similar gate stack to 32-nm, 45-nm generations
- TiAlN work-function metal, ~1 nm Hf-based hi-k, ~1 nm SiO
- Gate fill changed from Ti-Al to tungsten/TiN



Bottom of NMOS gate

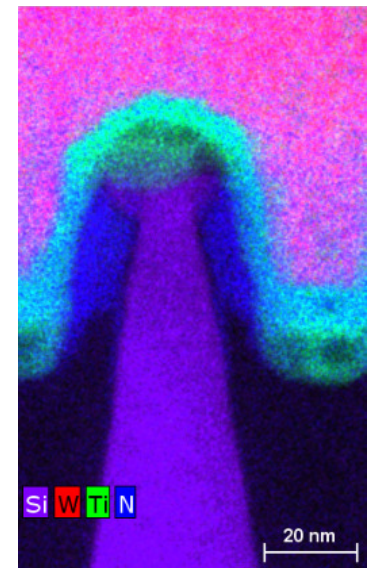
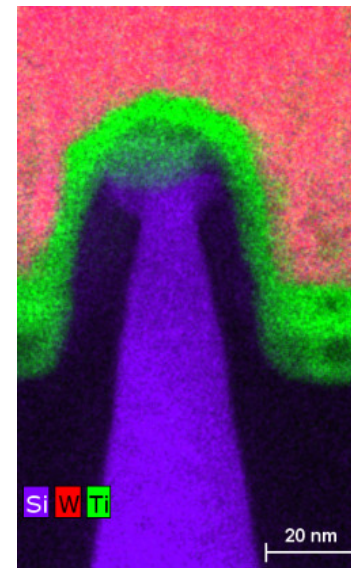
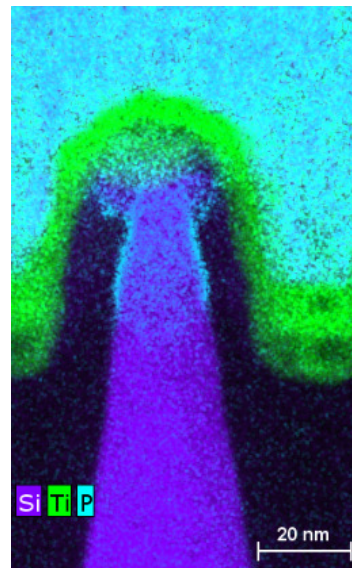
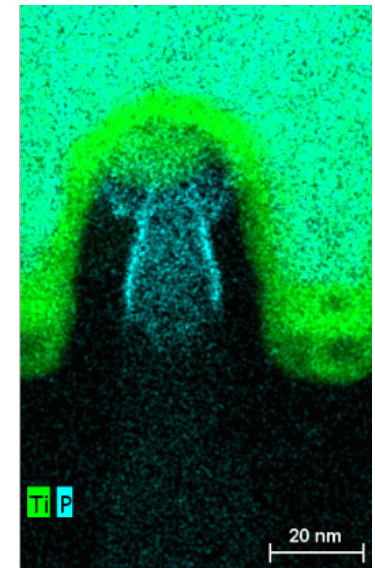
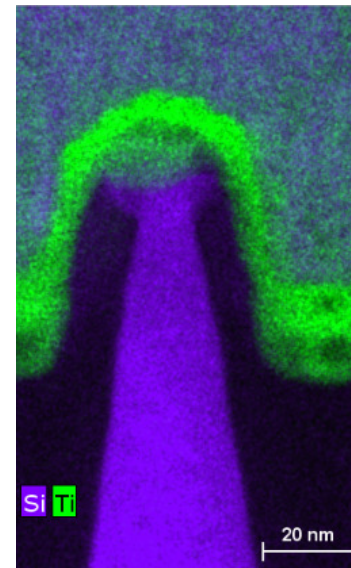
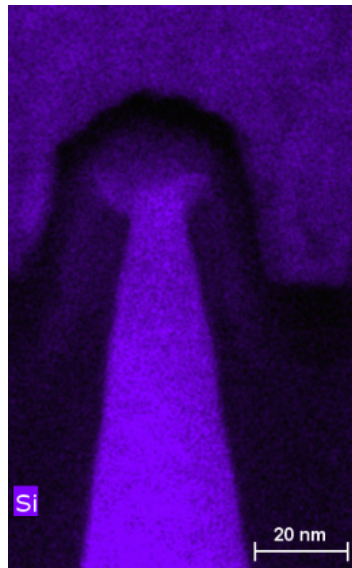
FinFETs – NMOS Source/Drains

- ‘Mushroom’ profile epi, no facets
- SWS nitride left on fin sides
- Epi lateral growth limited by SWS



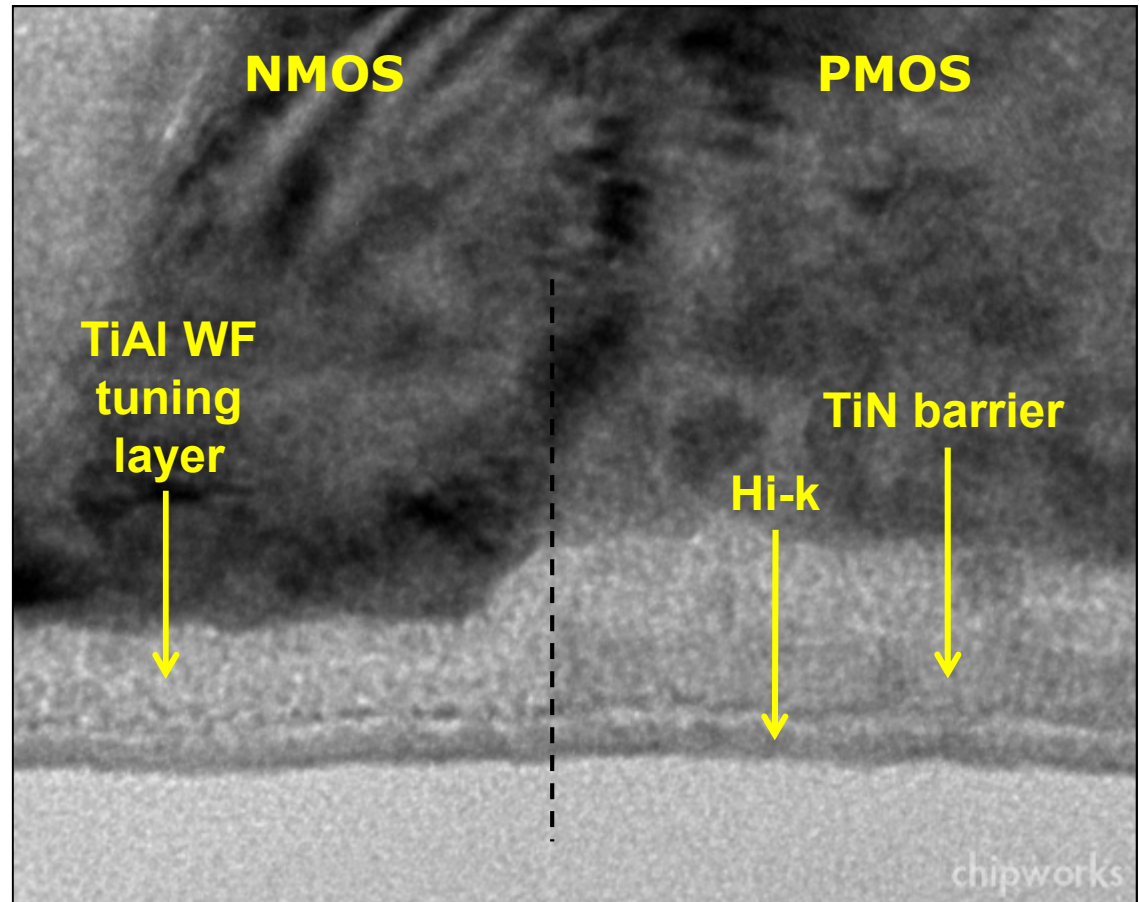
NMOS Source/Drains – EDS Mapping

- Clearly shows Ti silicide in epi
- P diffusion can be seen



FinFETs – Gate Transition

- Gate transition indicates PMOS WF stack is defined first



Summary

- Five high-k, metal-gate devices described
- The two Common Platform parts are similar but not the same
 - SiGe channel, nitride stress
- First example of a tri-gate/finFET part in high-volume commercial production
 - FinFET gate work-function materials are similar to those used for the previous 45- and 32-nm generations
 - Embedded SiGe is still used as a PMOS stressor
 - Gate fill has changed from TiAl to tungsten
 - Al-doped copper is used for electromigration improvement
 - Effective k-value of the dielectric has been reduced to help minimize intermetal parasitic capacitances
 - Integrated MIM capacitors

Acknowledgements

I would like to thank Chipworks' laboratory staff and process analysts for all the hard work of analyzing these complex devices. They did a great job!

Thank you for your attention!