Applications of Cluster Carbon – a Review

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Nissin Ion Equipment Inc., and **SemEquip Inc**

Carbon in Silicon

- Carbon is electrically inactive and substitutionally dissolved impurity in Silicon
- Implanted carbon forms strong gettering sites in Silicon and can act as sink for implantation-induced excess Si interstitials and thus avoids formation of dislocation loops.

Scheme of the Talk

- Cluster Carbon Properties and Applications
- Self-amorphization
- Cold implants
- Diffusion barrier
- Si:C stressor layer
- Silicide stabilization

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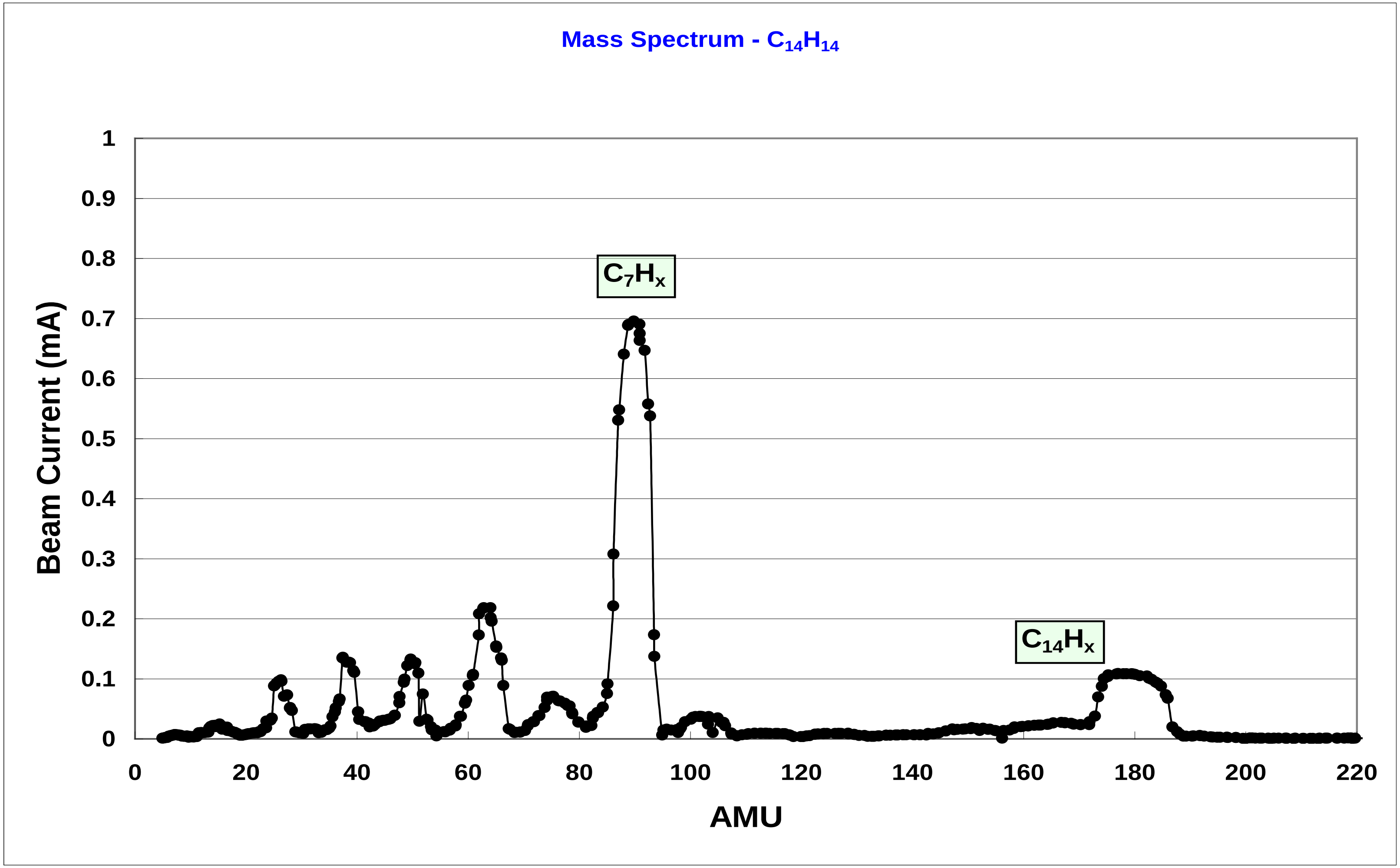
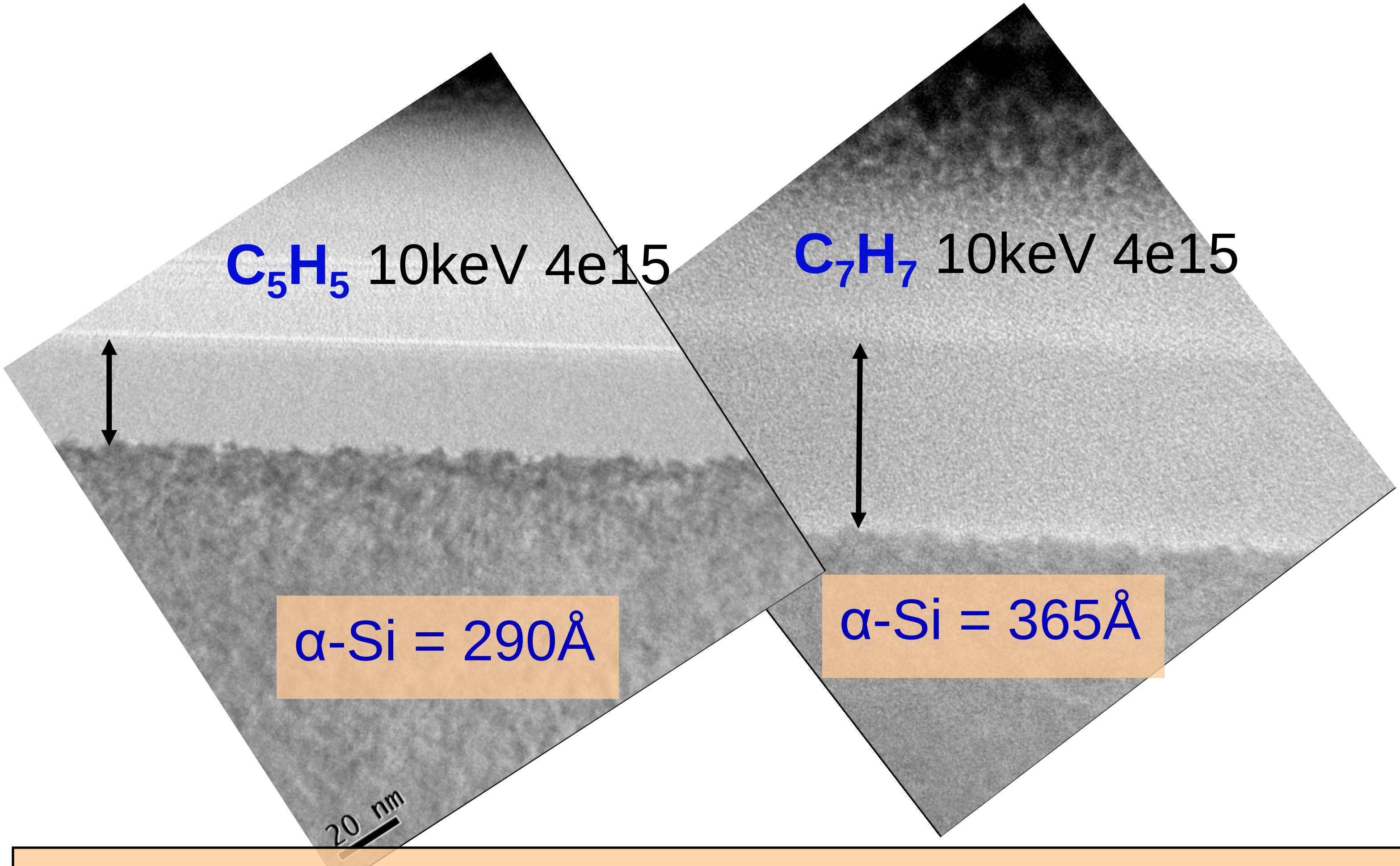
Mass Spectrum of $C_{14}H_{14}$ molecule



ClusterCarbon Self-amorphization - C_5H_5 vs C_7H_7



- **Going to a higher mass (from C_5 to C_7) at same implant condition yields about 25% increase in α-Si layer thickness**

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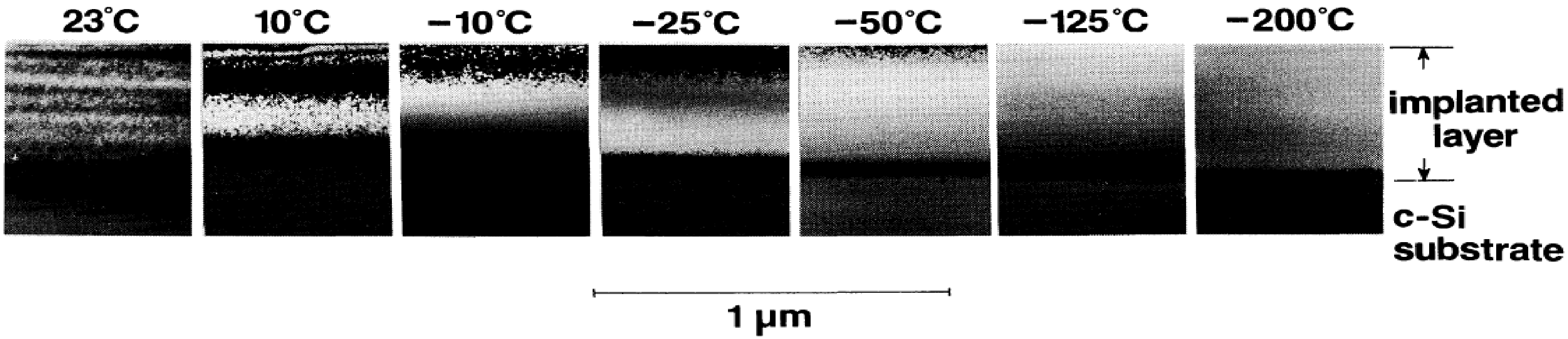
XTEM – Si^+ implanted Si(100) - 200keV, 5e14 atoms/cm^2



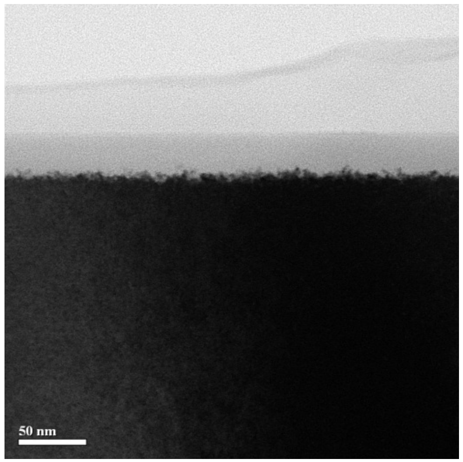
- **Even at -50°C, almost complete amorphization takes place.**
- **At low Ts, accumulation of small defects causes amorphization**
- **At high Ts, larger defect complexes are formed leading to defective amorphization**

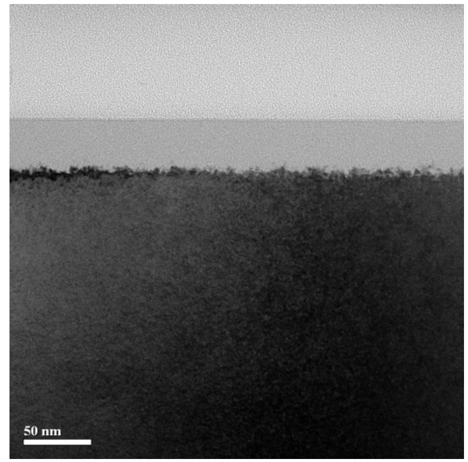
JAPANESE JOURNAL OF APPLIED PHYSICS
VOL. 30, NO. 12B, DECEMBER, 1991, pp. 3617–3620

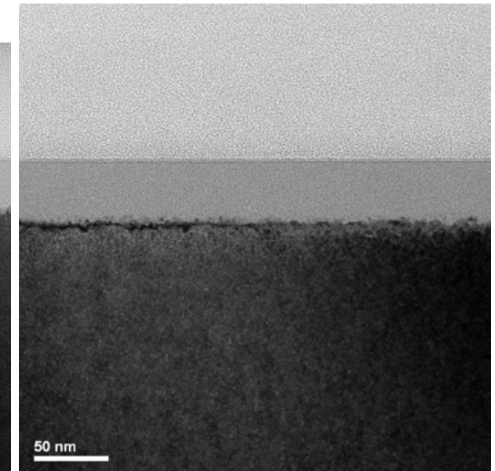
α- Si formation at 25, -30, -60 ℃ 10keV , 5E14 and 1E15

@25ºC @-30ºC @-60ºC

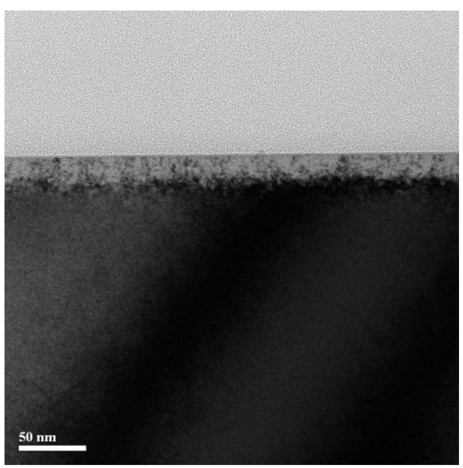
C_7 10keV 1E15/cm²

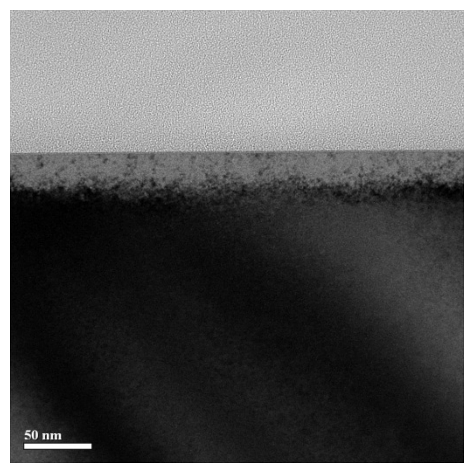


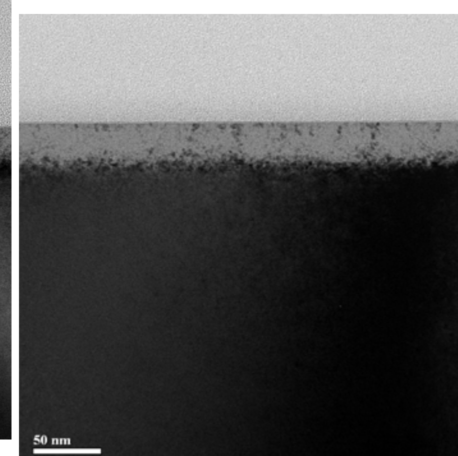




C_7 10keV 5e14/cm²



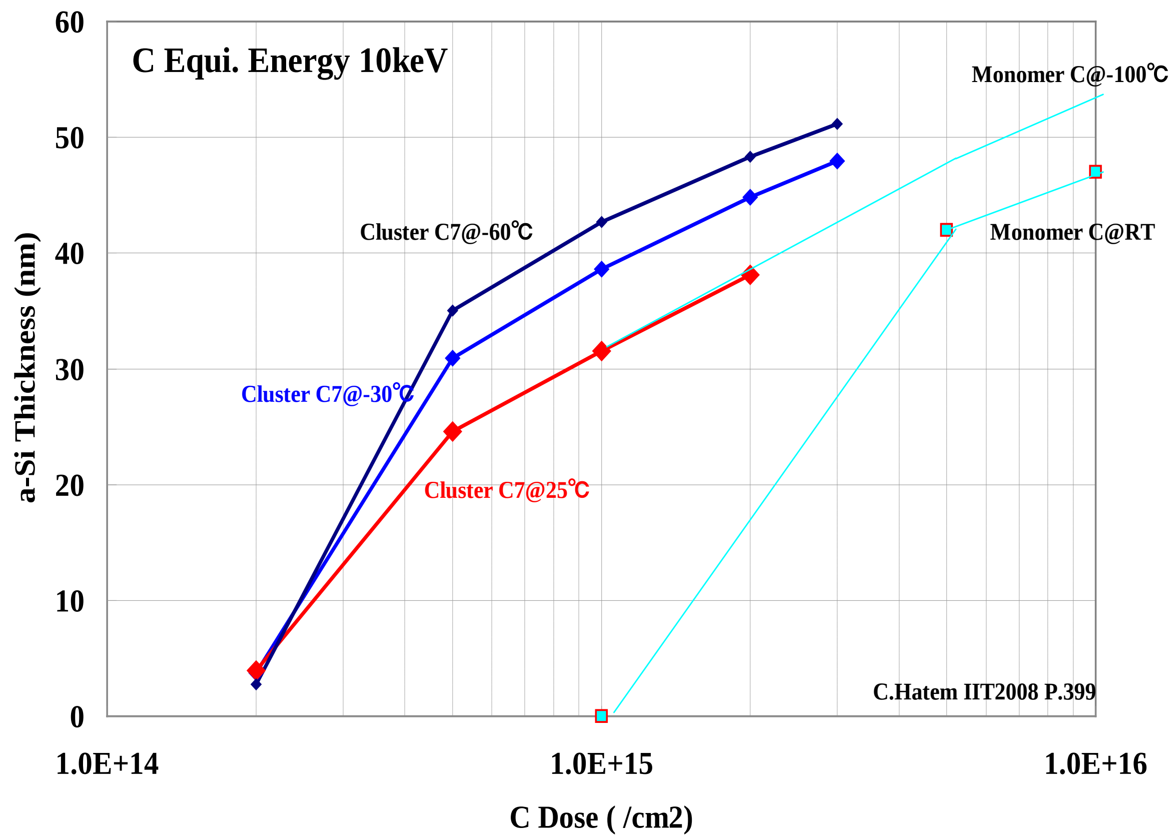




Amorphous Si Formation by Cluster Carbon at Low Temp.

❑ Amorphous Si thick formed by Cluster C_7 implant at 25℃ is almost the same as that of monomer C implant at "–100℃".

❑ With lowering the substrate temperature, a-Si thickness increases well beyond the a- Si thickness by monomer carbon implant.



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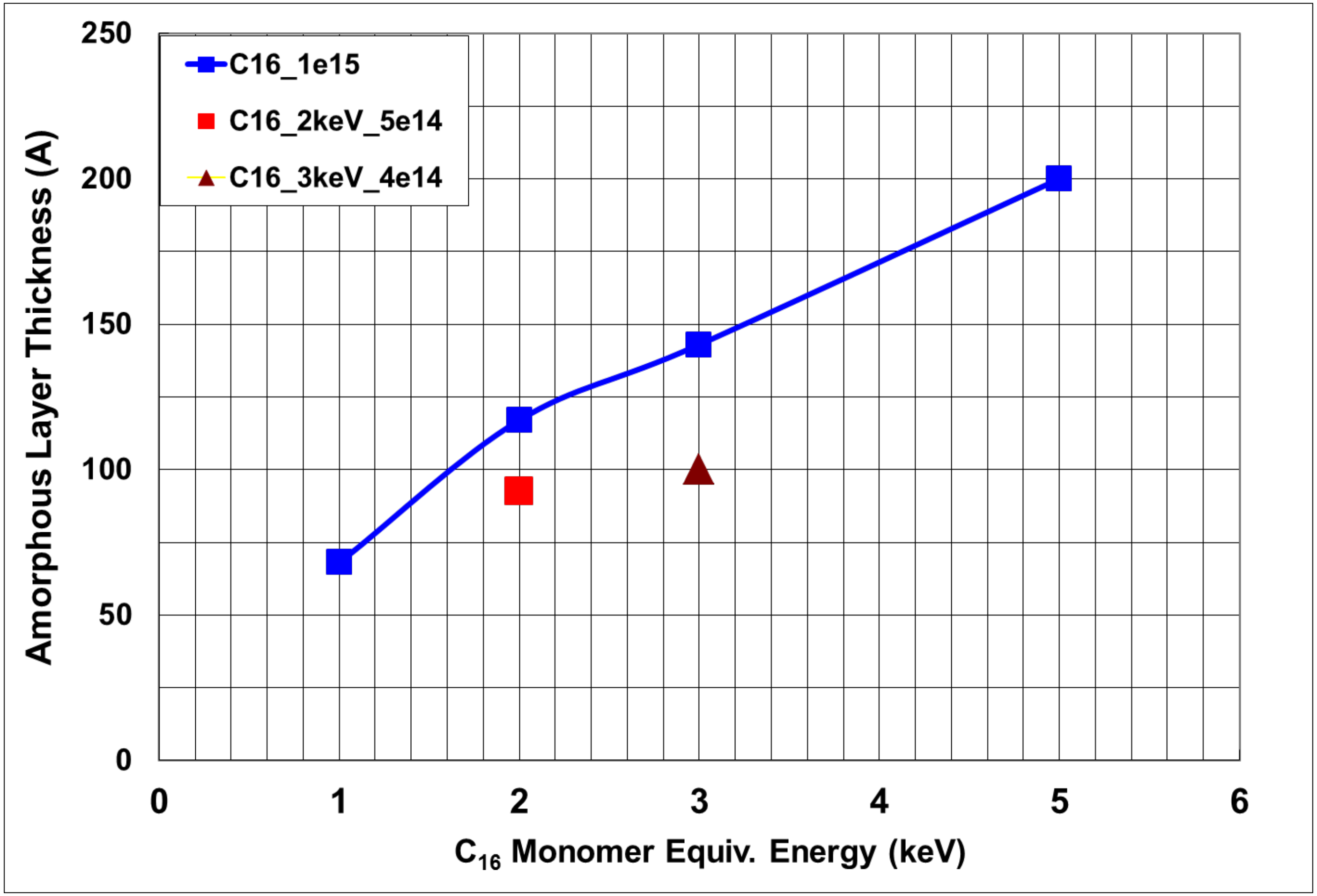
Amorphous Si Formation by Heavier Cluster Carbon – (Halo, SDE Applications)



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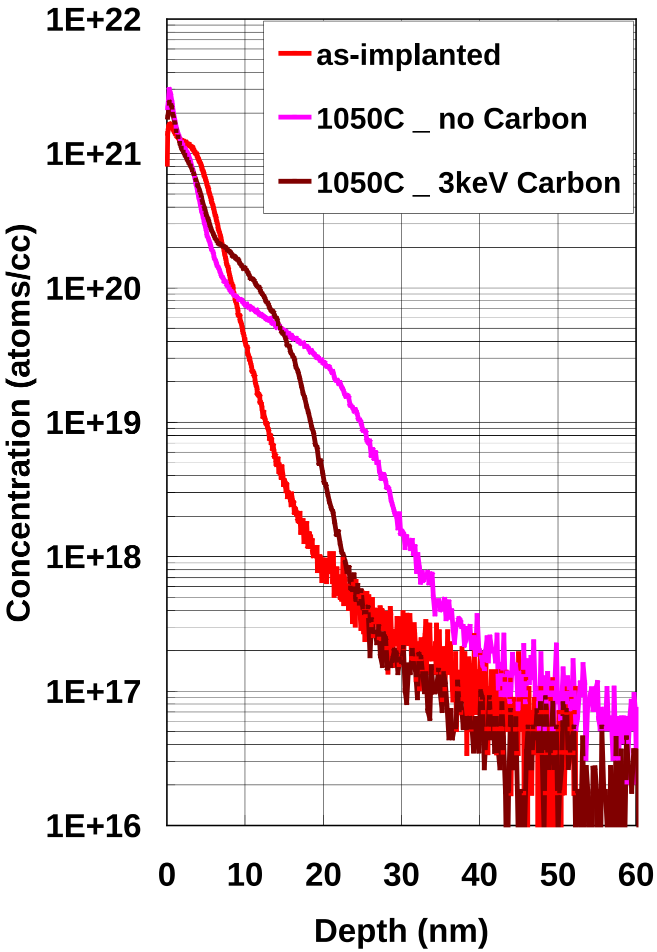
- Silicide stabilization,

ClusterCarbon™ Co-Implant



Carbon co-implant provides the following:

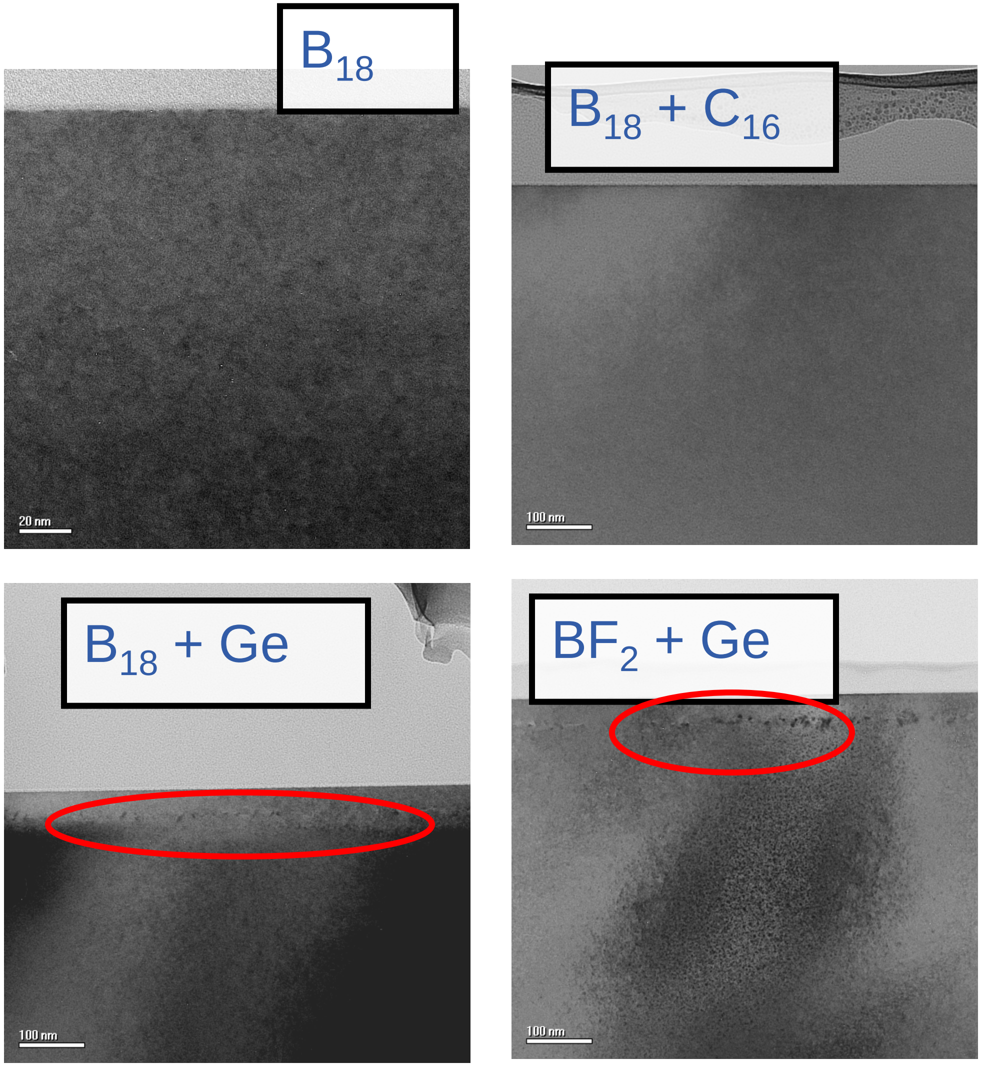
- Shallower Junctions
- Higher Solid Solubility
- Improved Junction Abruptness

(Cluster Boron 500eV, 1e15
– Spike anneal 1050^{o}C with and without Carbon)

EOR Defect Elimination : iRTP @ 900^{o}C

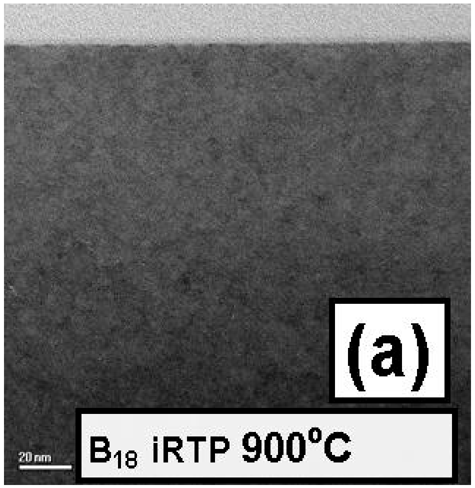
20 nm scale

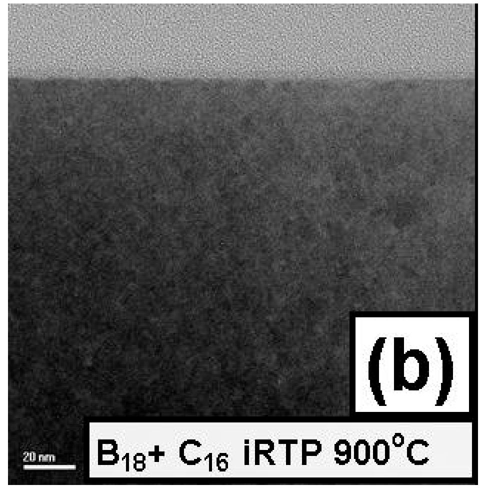
100 nm scale

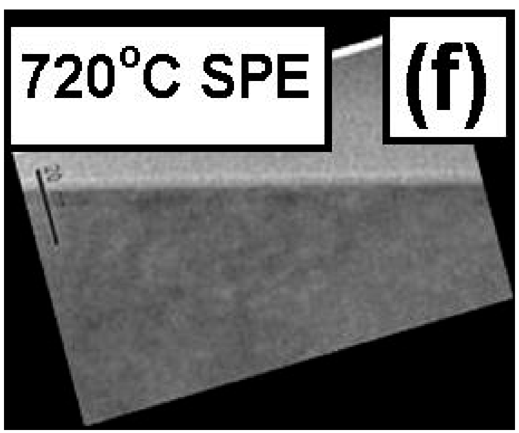


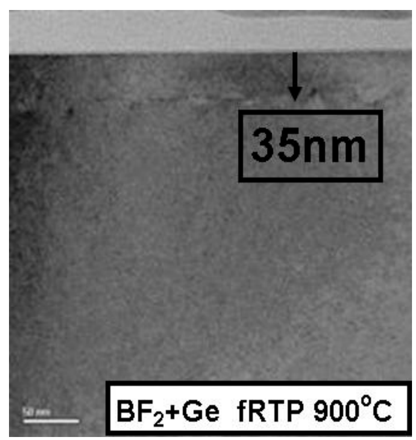
Ge co-implants produce EOR defects that remain following iRTP @900^{o}C

XTEM: iRTP 900^{o}C Diffusionless Anneal



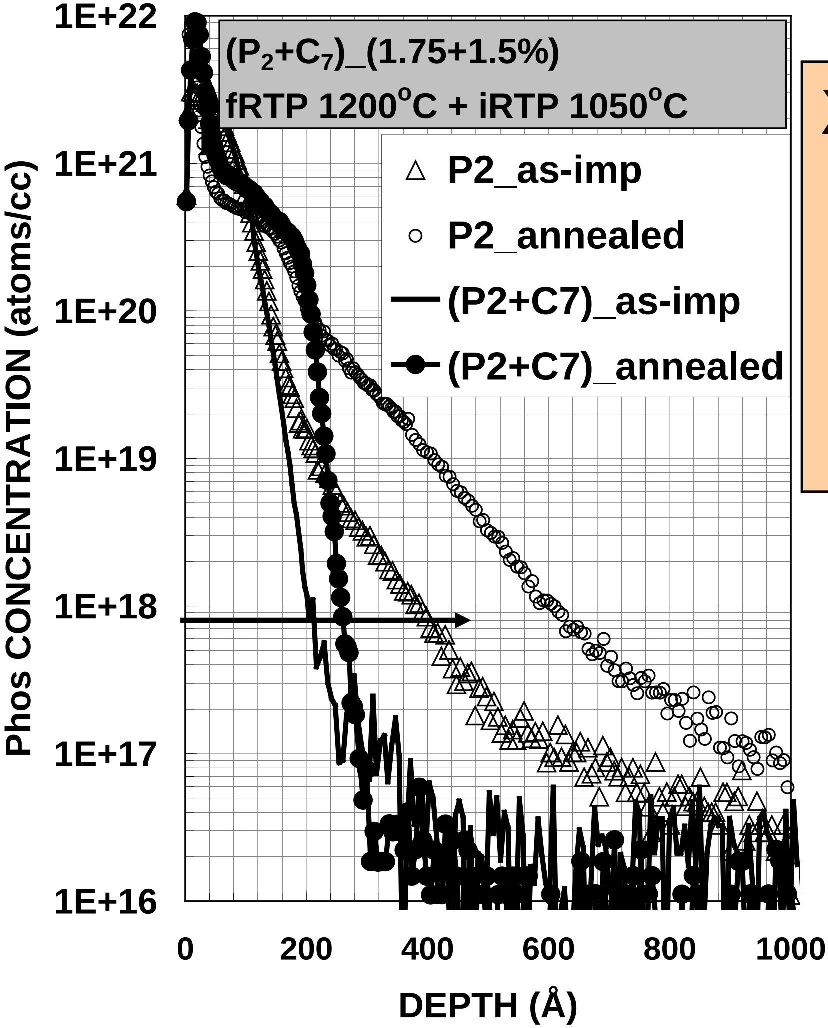






With diffusionless anneal, no EOR defects with $B_{18}H_{22}$ and $B_{18}H_{22}$ + $C_{16}H_{10}$.

C_7 as PAI implant and diffusion barrier (RT)



Xj ~ 280Å with C_7 co-implant
~ 480Å without C_7 co-implant

ΔXj ~ 200Å

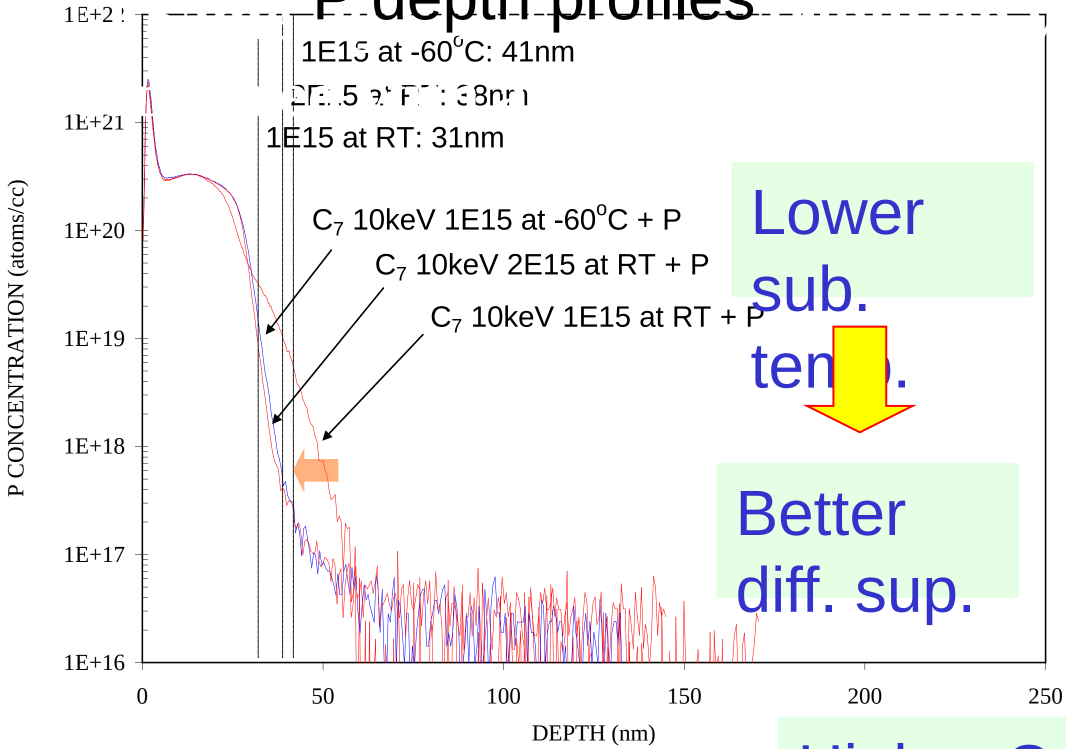
- **Reduced Xj**
- **Abrupt junction**

- **Nagayama et al, IWJT 2010**
- **K. Sekar et al, Mat. Sci. Eng. B 154-155 (2008) 122-125**

Diffusion control, low temp effect (IIT 2012)

- **Thick amorphous layer – efficient P diffusion suppression**
- **Even with tighter distribution, almost same Rs because of higher activation**

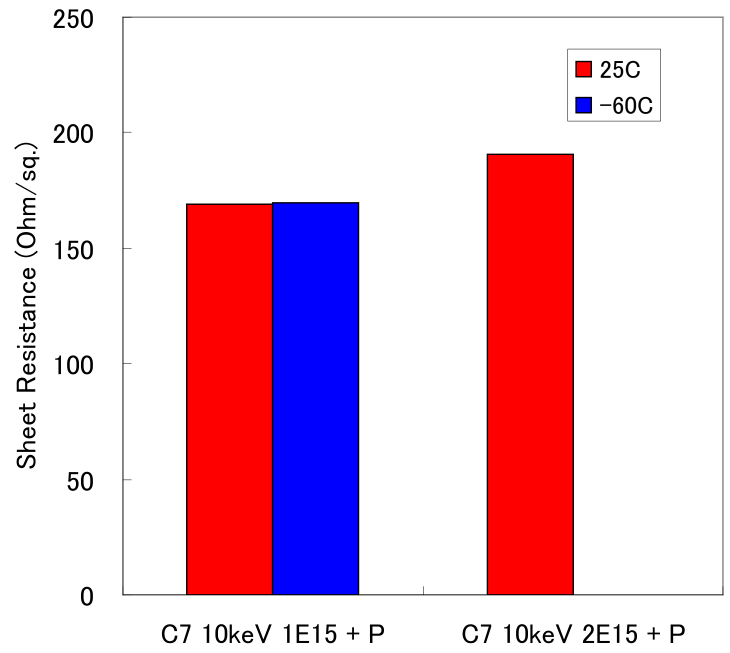
P depth profiles



Lower sub. temp.

Better diff. sup.

Rs



Higher C dose → Higher Rs

Lower sub. temp. → Same Rs

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Nickel Silicide – advantages and issues

Advantages :

- One step low temp. formation
- Low resistivity
- Low Si consumption
- Does not suffer from resistivity degradation on narrow lines or gates

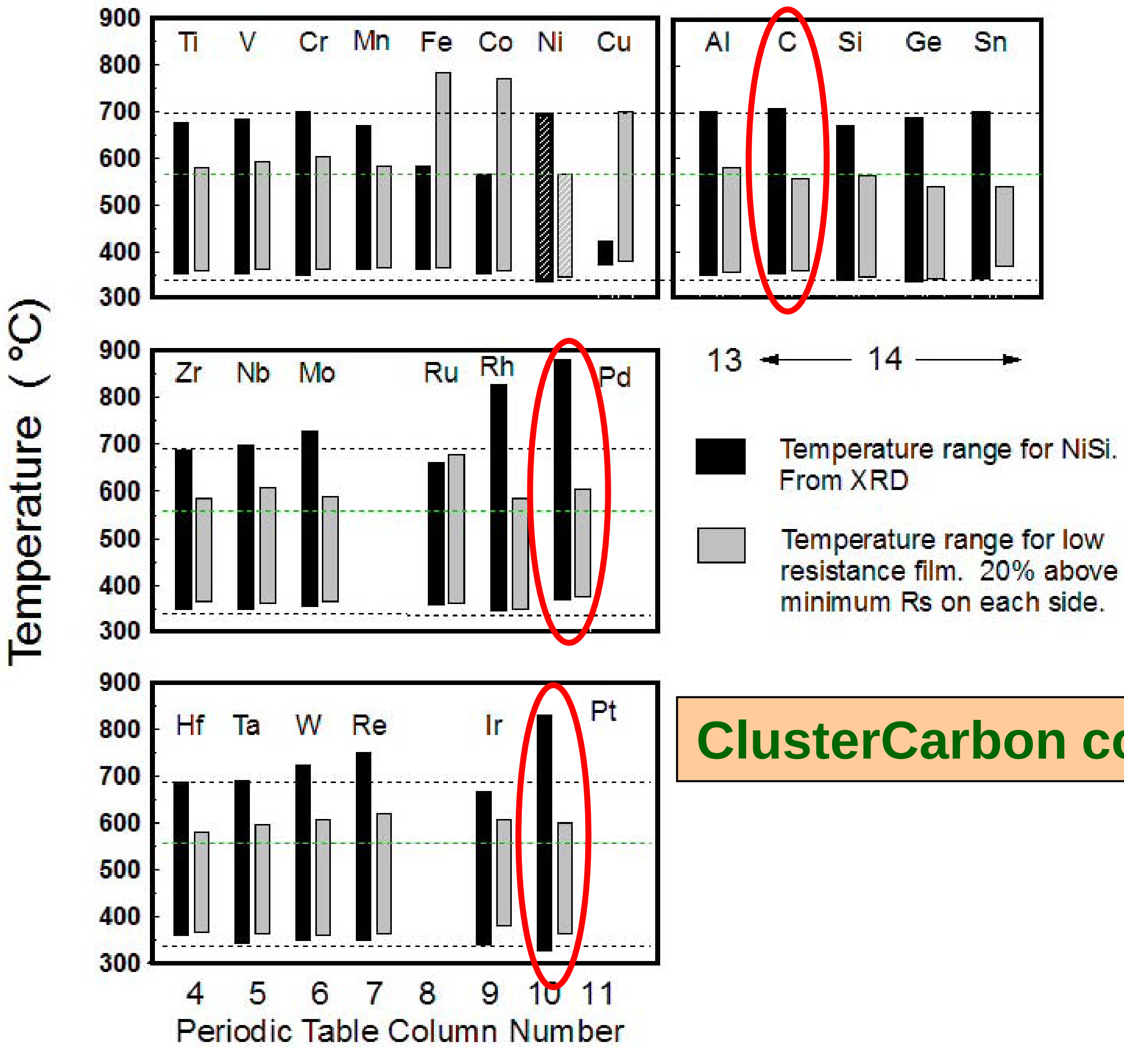
Issues :

- Rough interface between NiSi and Si
- NiSi phase is not thermodynamically stable in contact with excess Si
- NiSi films are morphologically unstable and prone to agglomeration
- Large junction leakage current
- Sheet resistance degradation due to oxygen contamination

One of the existing Solutions :

- Use of metals as an alloying element to stabilize Nickel Silicide

Choice of elements :



ClusterCarbon could be a choice!

ECS 210th Meeting – Abstract 1010

Electron Device Letters, Vol. 29 (2008) 89-92
ECS Transactions , 13 (2008) 397-404 (IMEC)
Microelectronic Engineering, 88 (2011) 578-582

- NiSi:C as contact technology for MOSFETS with silicon-carbon (Si:C) source/drain (S/D) regions.
- Presence of carbon at NiSi:C grain boundaries and NiSi:C/Si interface modify the grain boundary and interfacial energies and thus influence the kinetics of NiSi:C silicidation.
- NiSi:C silicidation suppresses deep-level defects leading to better n+/p junction characteristics

Experimental Process flow: Ni silicide (bulk wafer)

- wafer (N-type silicon: Implant C_{16},$B_{18}H_{22}$,BF_2,B_{11})
- Native oxide removal (HF 1 : 100)
- Metal deposition
  (splits :Ni/TiN (15/10nm), Ni-Pd(5%)/TiN , Yb/Ni/TiN (1.5/13.5/10nm), ..)
- 1st Rapid thermal process
  (splits : 400℃ ~ 800℃, 30s)
- Selective wet etching (H_2SO_4 : H_2O_2 = 4 : 1)
- 2nd Rapid thermal process
- Post-silicidation annealing (550°C ~ 700°C, 30min)

(collaboration study between SemEquip and CNU)

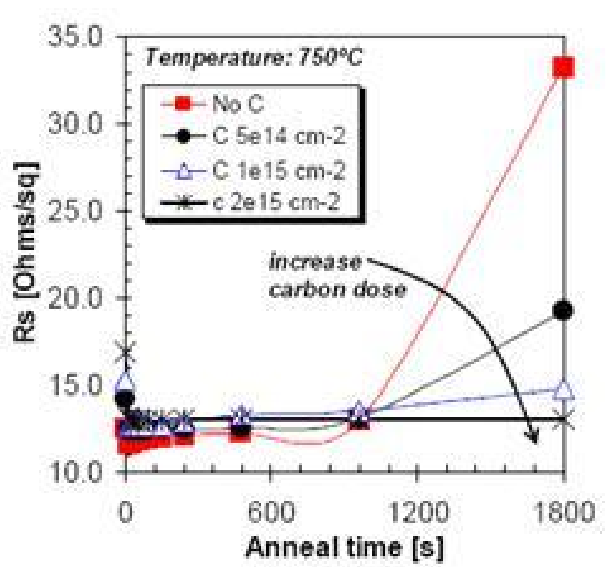
Experimental Process flow: Ni silicide (diode pattern)

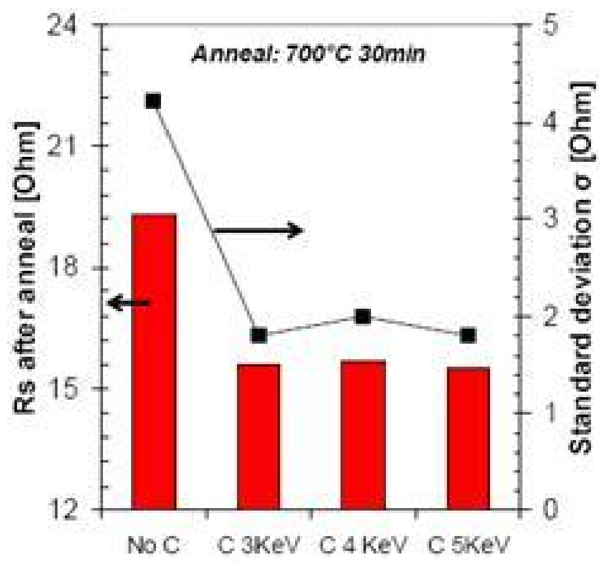
- Pattern wafer (N-type silicon: Implant C_{16},$B_{18}H_{22}$,BF_2,B_{11})
- Native oxide removal (HF 1 : 100)
- Metal deposition

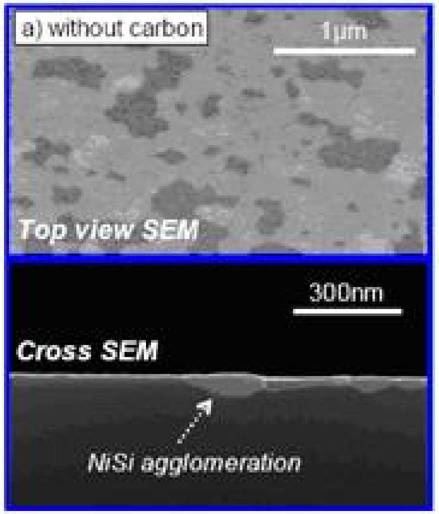
  (splits : Ni/TiN (15/10nm), Ni-Pd(5%)/TiN , Yb/Ni/TiN (1.5/13.5/10nm)…..)
- Rapid thermal process (600 ℃, 30s)
- Selective wet etching (H_2SO_4 : H_2O_2 = 4 : 1)
- Measure I-V characteristics (junction leakage current)

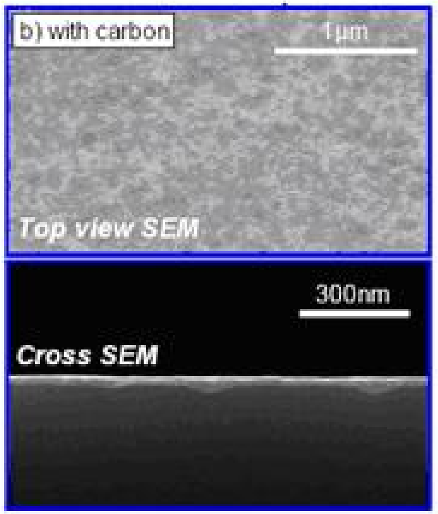
(collaboration study between SemEquip and CNU)

Impact of Carbon co-implants on silicide stability





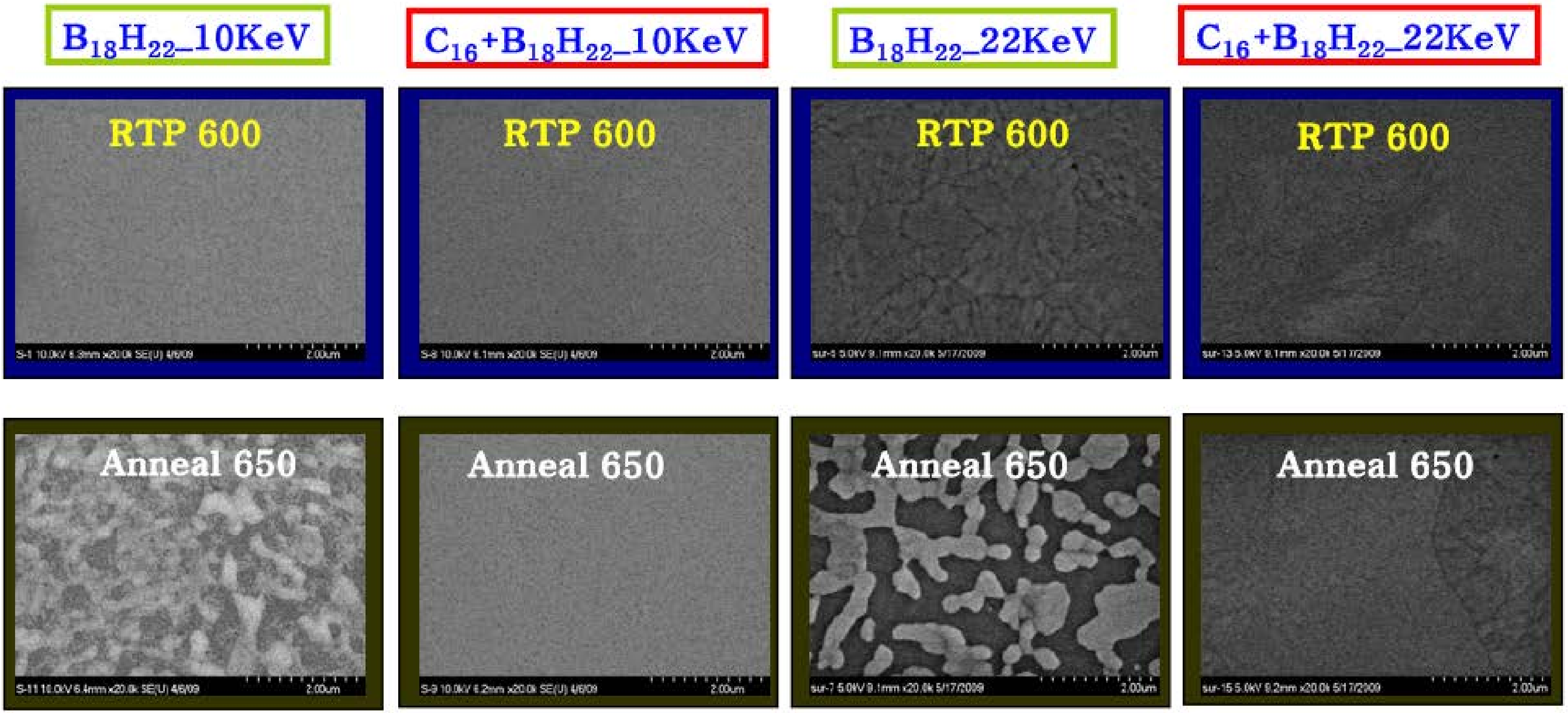




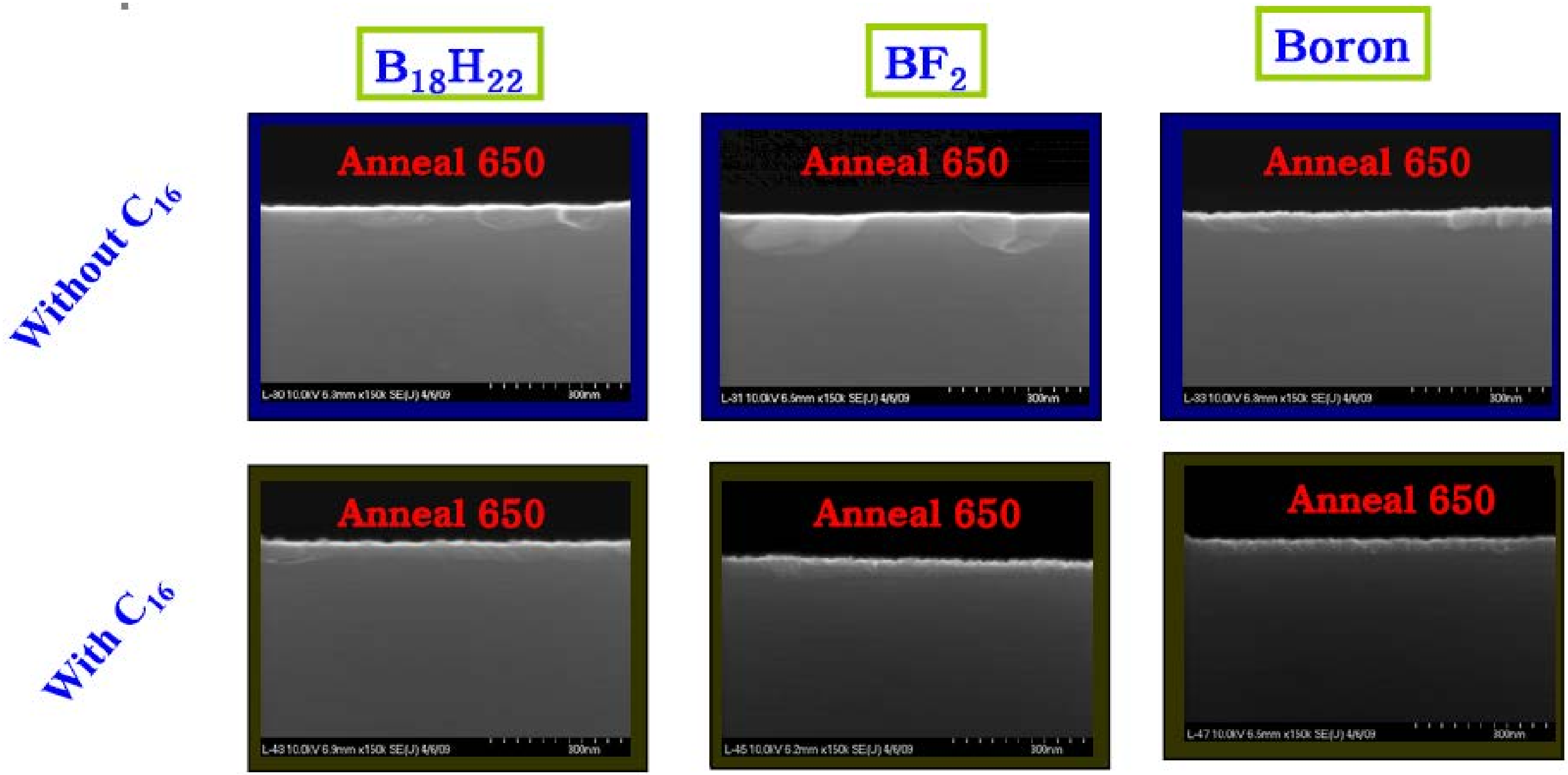
- Clear advantages in Ni silicide resistance and stability with thermal anneals.
- This gain comes from the fact that a lower agglomeration effect is observed on both surface and depth when carbon is present in the silicide

(IMEC web site)

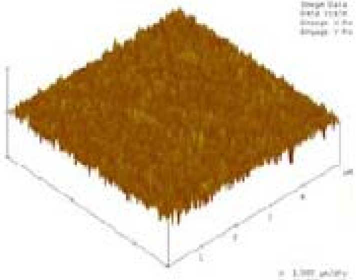
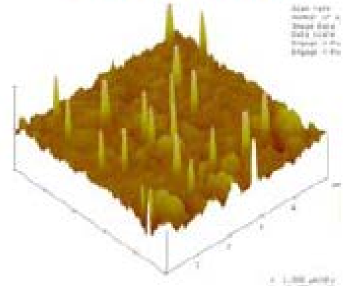
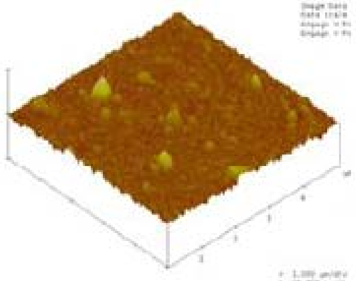
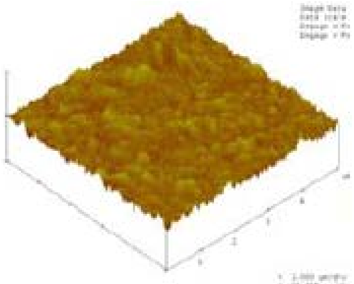
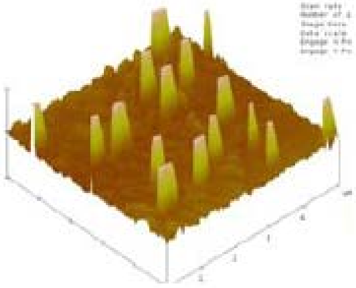
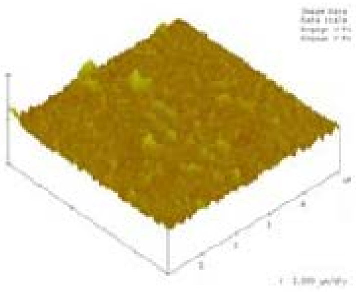
NICKEL SILICIDE :
Plan view SEM: Carbon effect – Lower agglomeration



X-SEM: Carbon effect

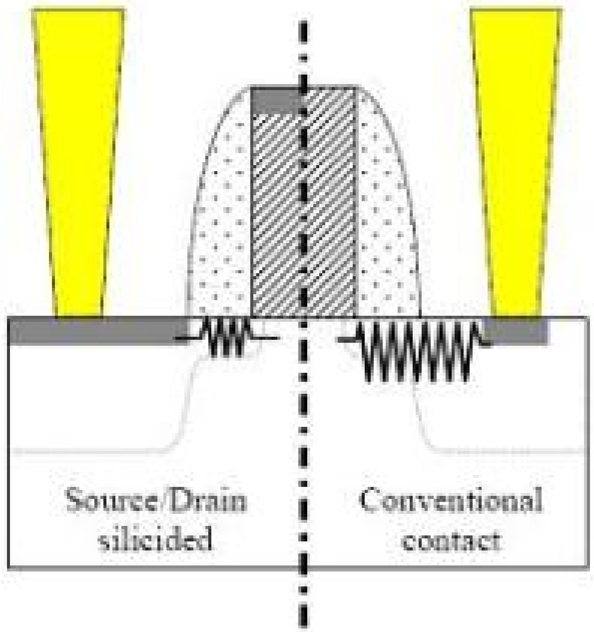


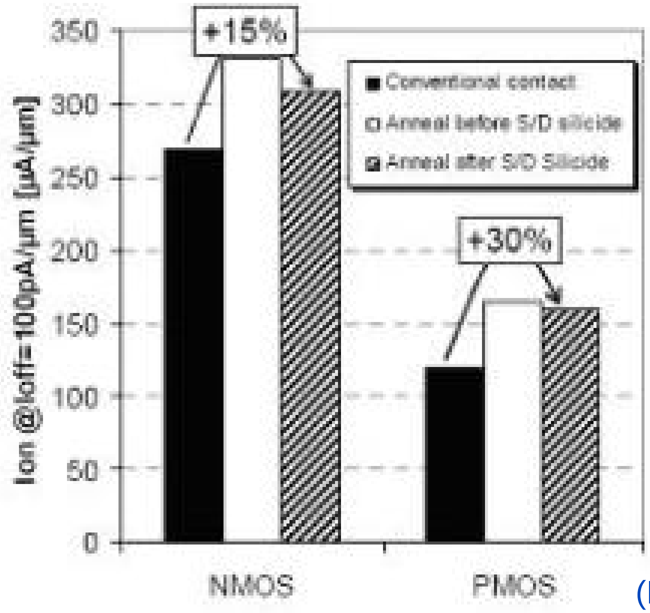
AFM Surface roughness: carbon effect

	$B_{18}H_{22}$	BF_2	Boron
	Anneal 650	Anneal 650	Anneal 650
Without C_{16}	 Roughness=2.045nm	 Roughness=5.141nm	 Roughness=1.559nm
With C_{16}	 Roughness=1.515nm	 Roughness=5.064nm	 Roughness=1.280nm

- C_{16} lower surface roughness

Thermally stable Ni silicide for DRAM applications





(IMEC web site)

- Thermal budget constraints during the DRAM BEOL, Ni silicide is not stable and not usable unless its thermal stability is improved.
- Carbon implantation techniques to stabilize the ultra-shallow junction and S/D silicides to withstand the DRAM BEOL to improve the overall peripheral CMOS performance.
- Ref : IMEC website, CNU Korea , SemEquip Collaboration

CMOS periphery devices in Memory Applications

Carbon-based thermal stabilization techniques to improve the performance of CMOS periphery devices in memory application.

- Substantial current drive improvement,
- contact resistance lowering
- RO delay improvement

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NMOS Device Performance

Strain (Si:C Layer) => high % $[C]_{subs}$

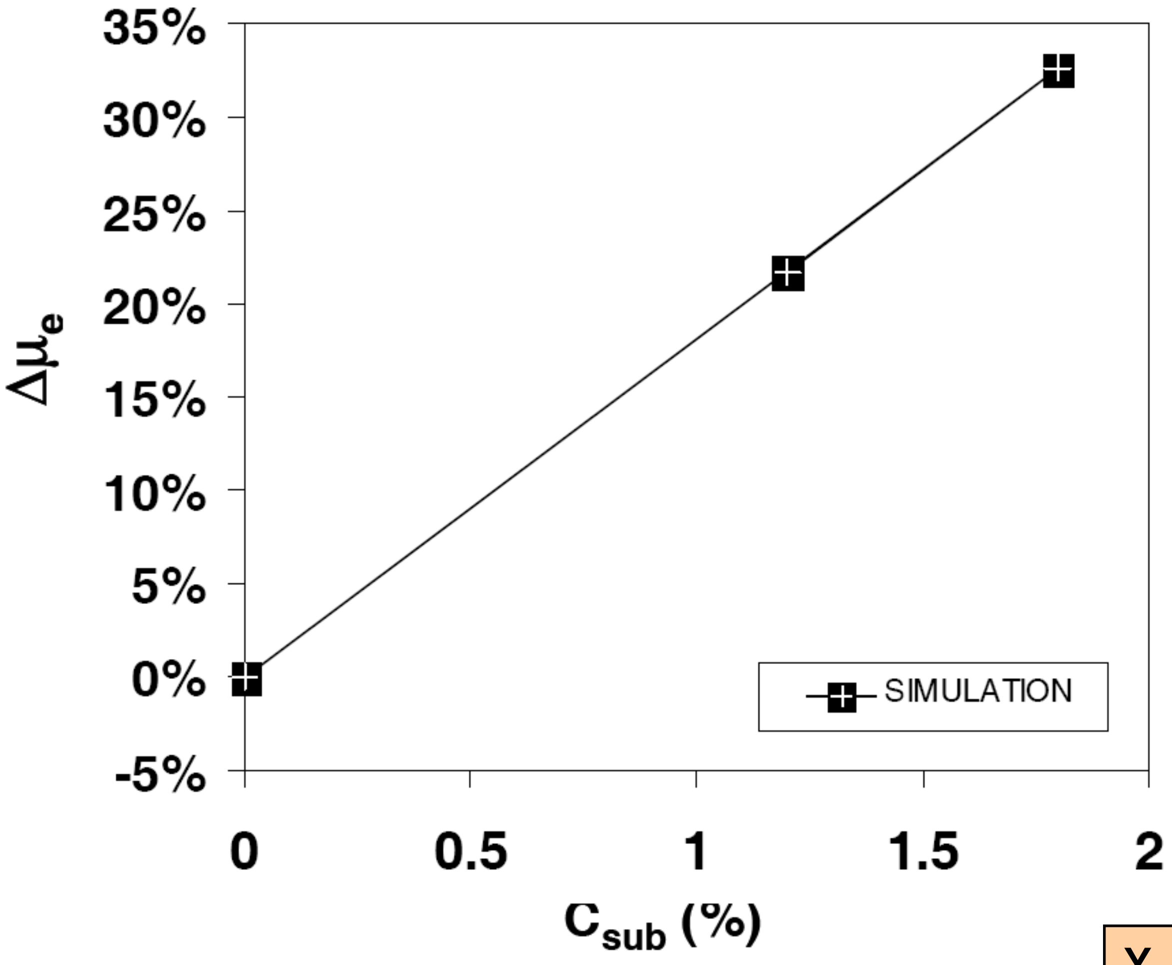
↓

Mobility enhancement

↓

Device Speed

Mobility Enhancement vs % of $[C]_{subs}$

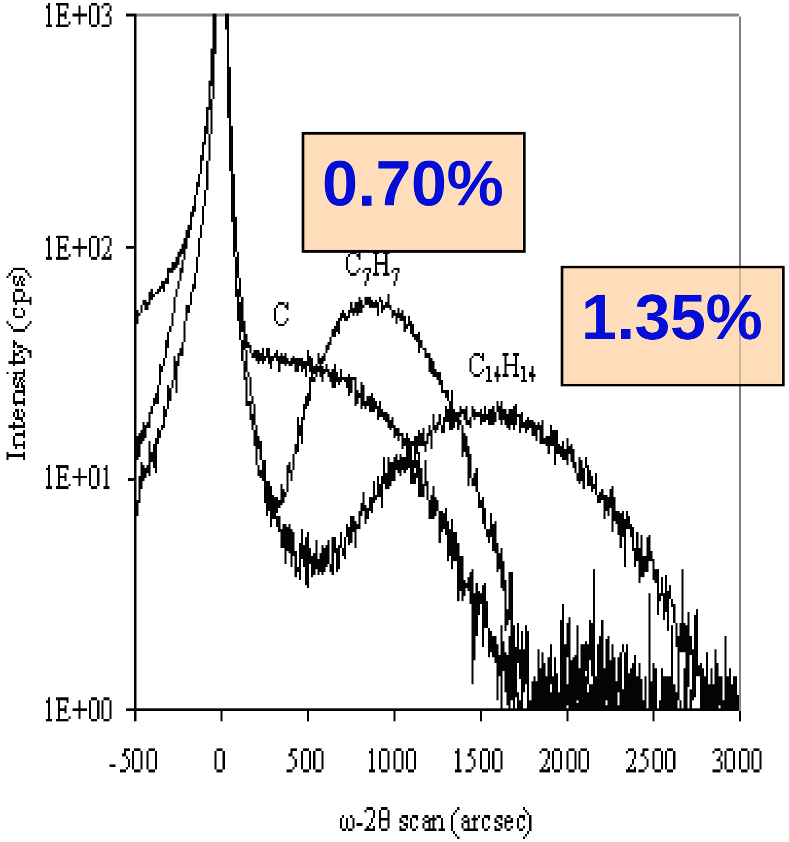


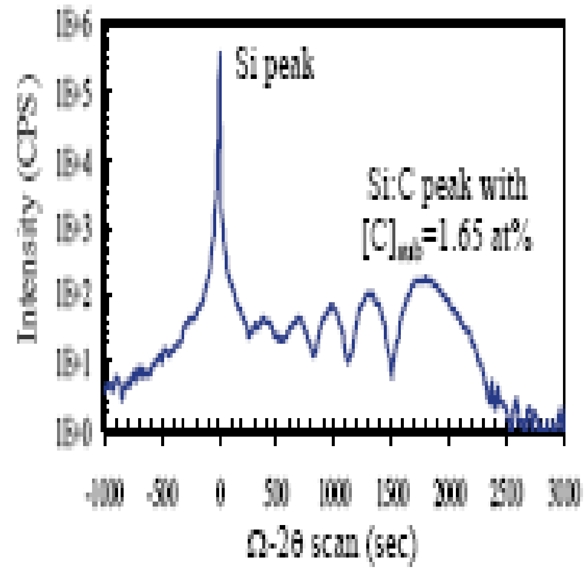
Y. Cho et al, EMRS, 2008

[C]$_{subs}$ from HRXRD - 6keV, 2e15 atoms/cm^2 (Laser Annealing)

ECS 2007 – TI, Axcelis, SemEquip

VLSI 2007 – pg 44



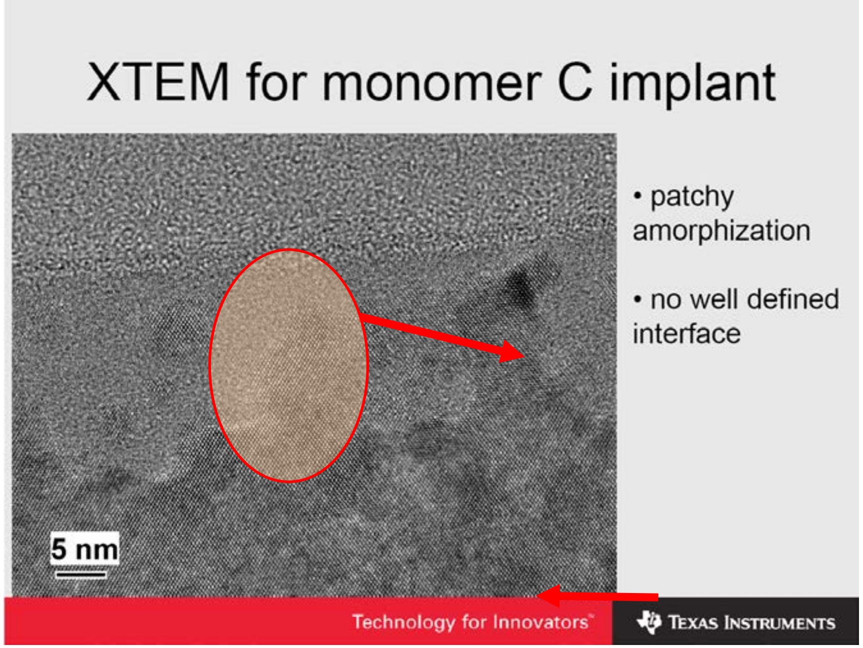


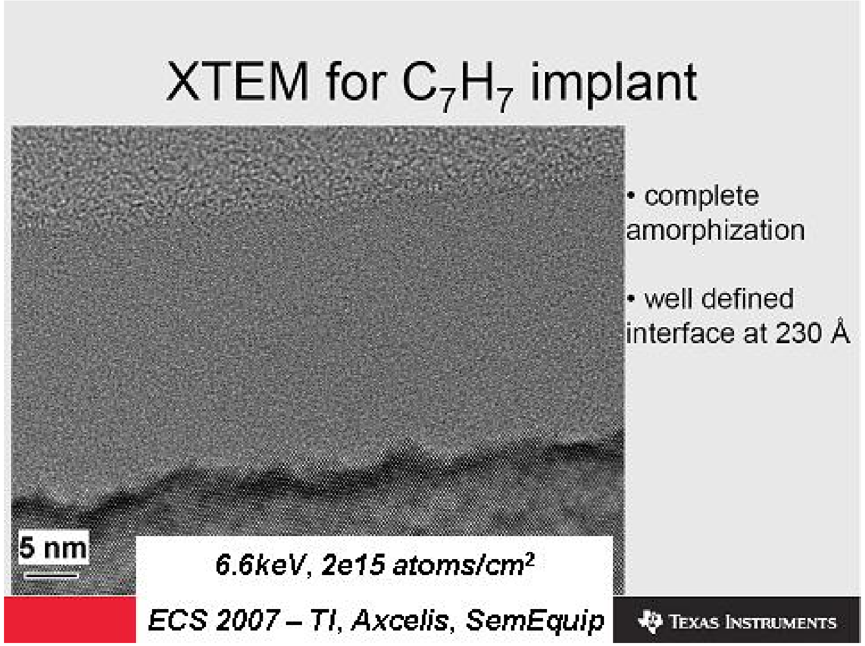
1.65%

Fig. 2 HRXRD rocking curve of the SPE Si:C film ([C]$_{sub}$=1.65 at.%) grown on (100) Si substrate. The well defined Si:C peak and fringes indicate that the Si:C film is high-quality single crystal.

TEM – Monomer vs C_7H_7 - 6keV, 2e15 atoms/cm^2

ECS 2007





Patchy amorphization

Well defined interface

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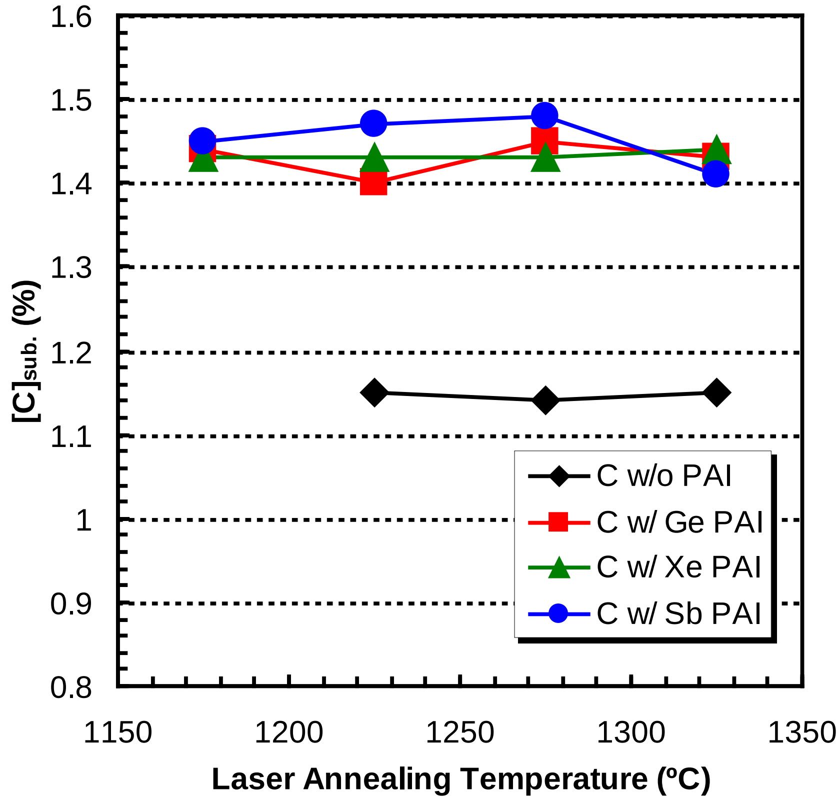
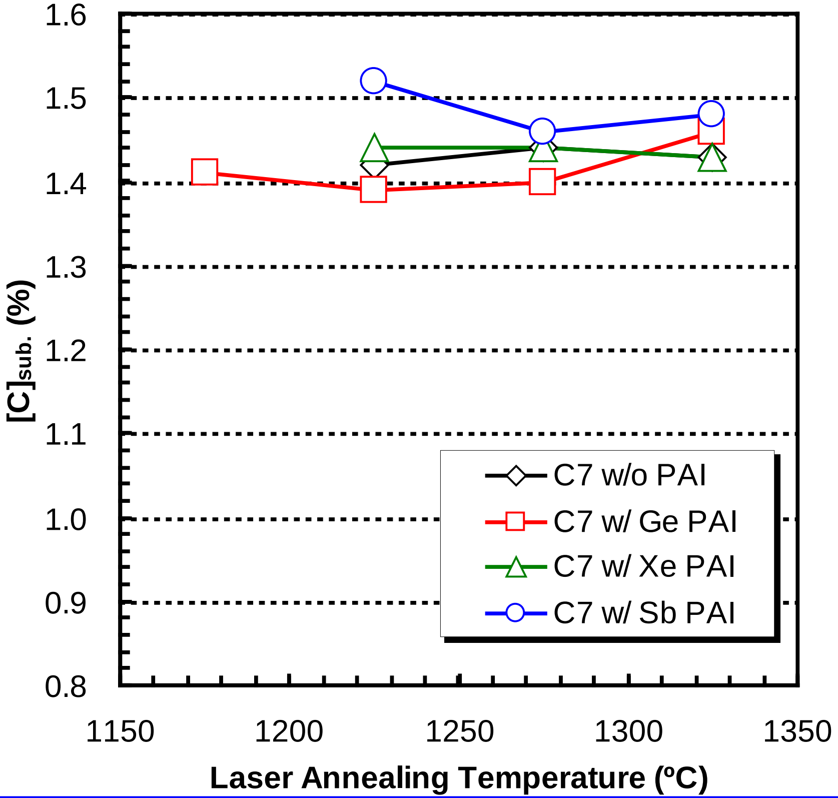
P + C_7H_7 - HRXRD - $[C]_{subs}$ (Borland et al RTP 2009)

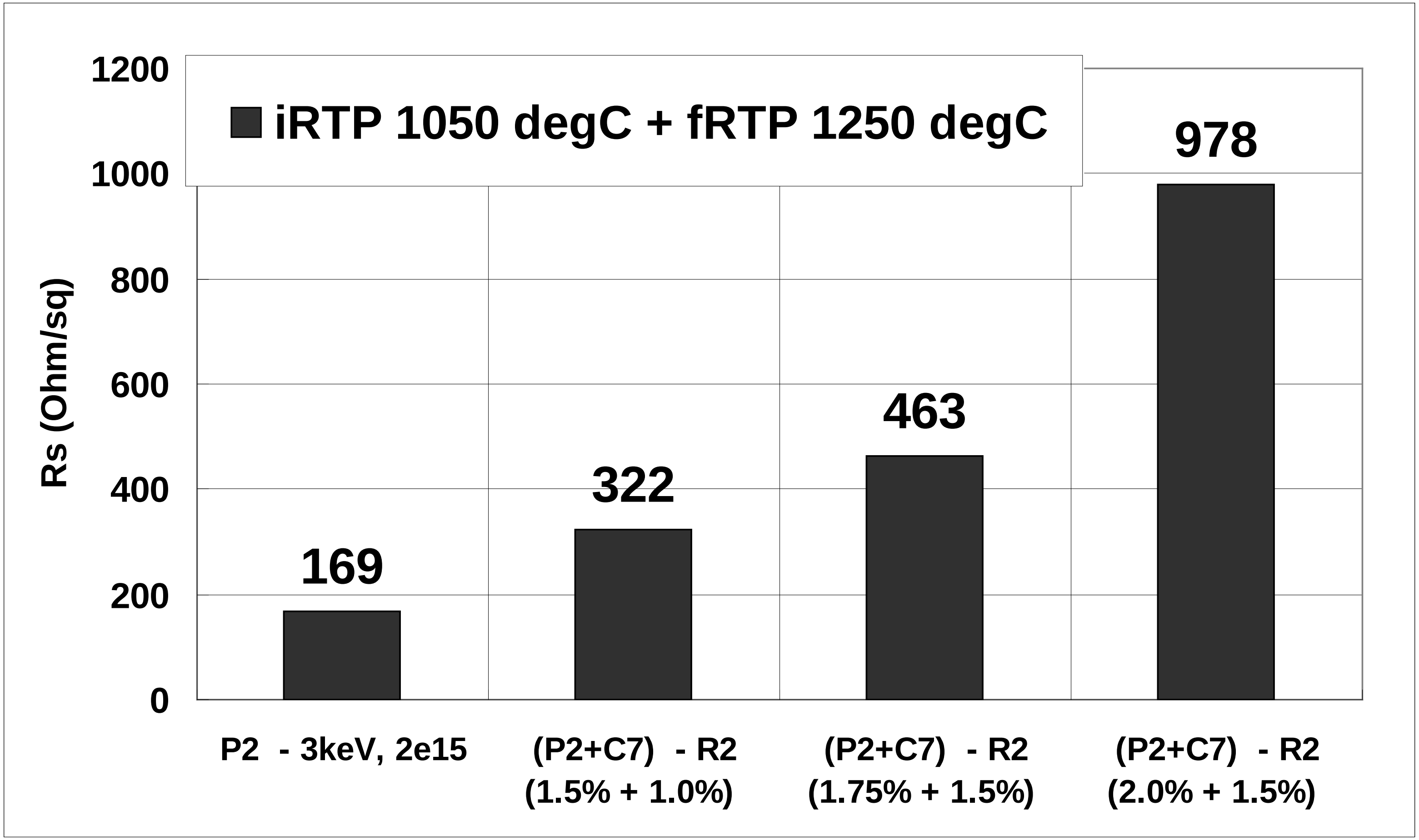




- Monomer C w/o PAI ➔ low[C]sub➔ P4 on [C]sub is small.
- Cluster C7: High [C]sub independent on PAI conditions.
- There is no clear dependence on LSA temperature.

$P_2 + C_7H_7$ Rs results

(iRTP 1050°C + fRTP 1200°C)

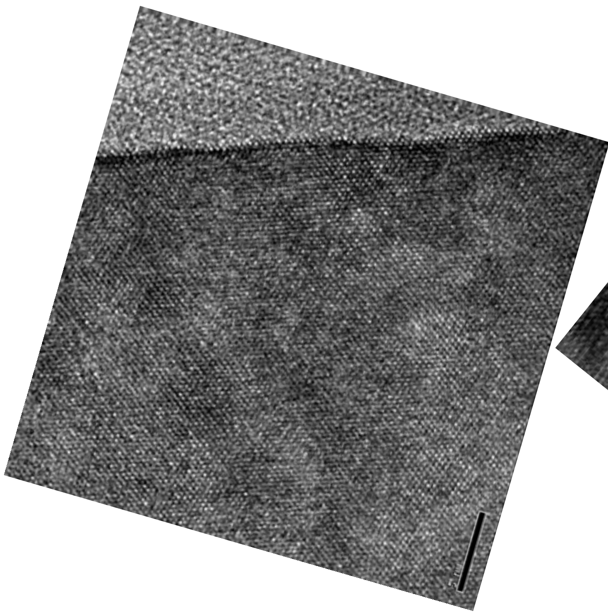


Dramatic increase in Rs beyond 1.75% atomic carbon. Precipitation of carbon beyond 1.75%

XTEM 400 kV

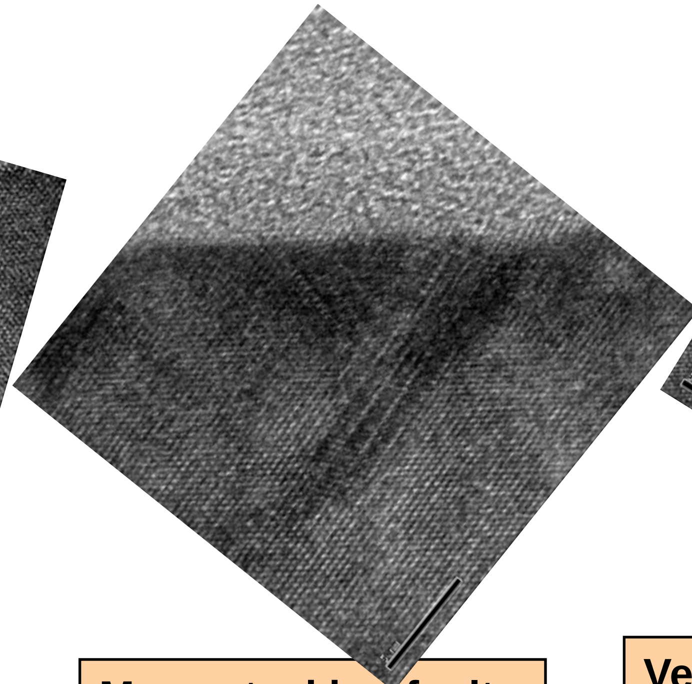
$P_2 + C_7H_7$ (iRTP 1050^{o}C + fRTP 1250^{o}C)

1.5% + 1.0%



Very few stacking faults with a couple of EOR loops

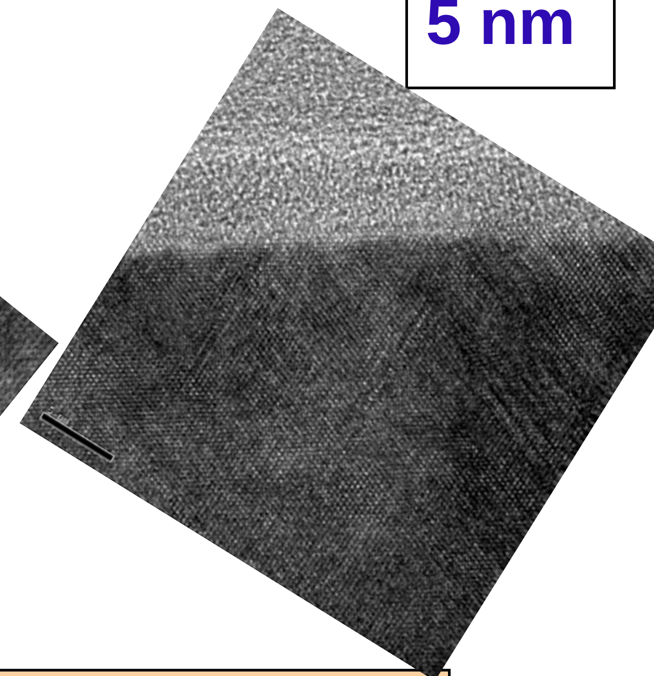
1.75% + 1.5%



Many stacking faults with a couple of EOR loops

2.0% + 1.5%

5 nm

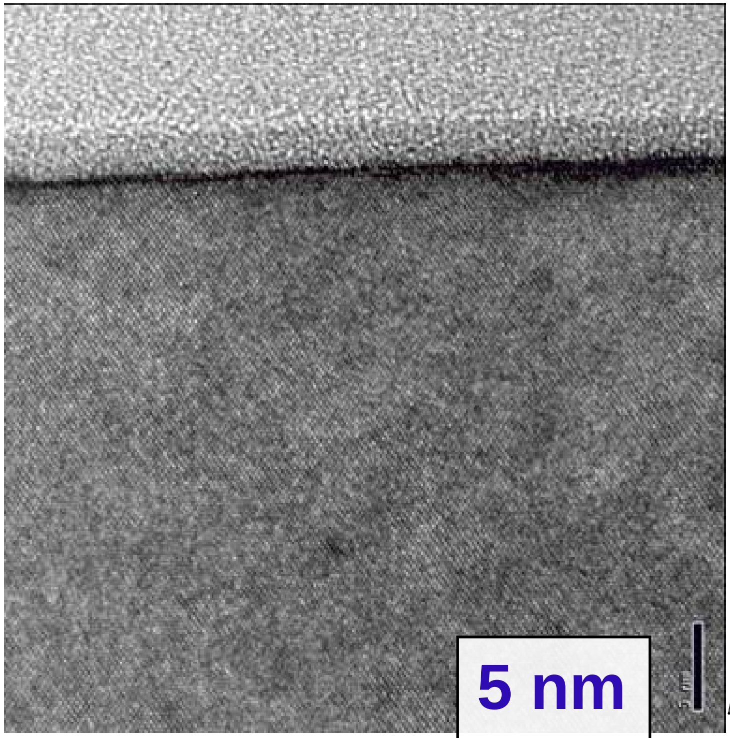


Very many stacking faults with a couple of EOR loops

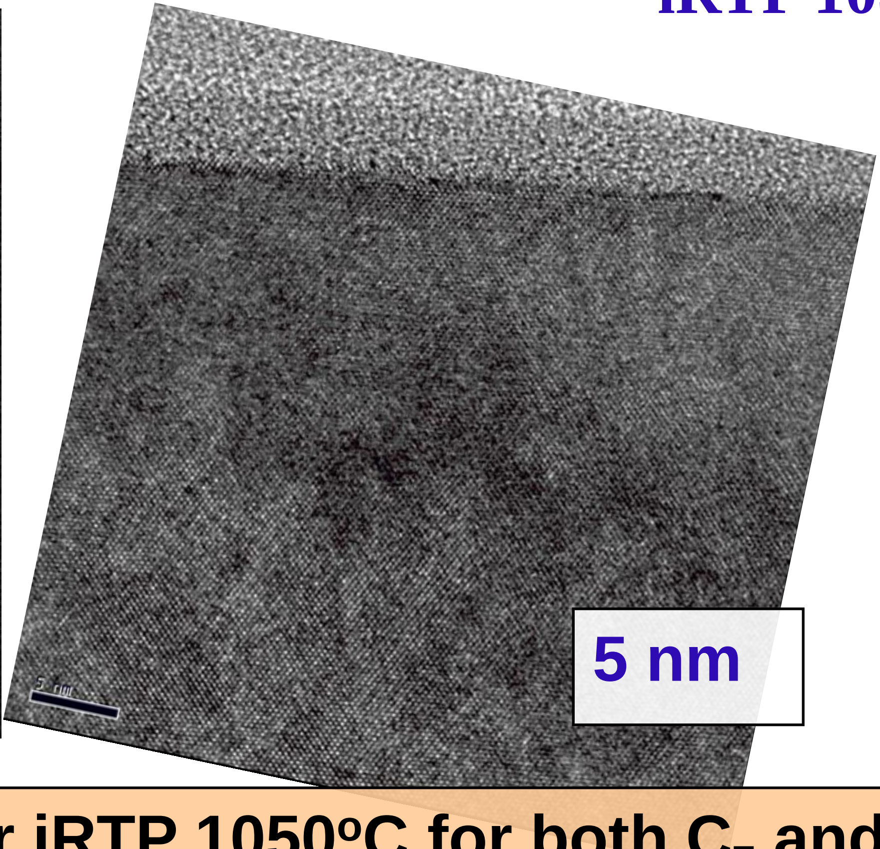
XTEM

1.5% atomic carbon - C_7H_7 vs (P_2 + C_7H_7)

C_7H_7 fRTP 1200ºC + iRTP 1050ºC



$P_2 + C_7H_7$ fRTP 1200ºC + iRTP 1050ºC



No regrowth defects after iRTP 1050ºC for both C_7 and P_2+C_7 cases.

Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp677-678

Analytical Approach for Enhancement of nMOSFET Performance with Si:C Source/Drain Formed by Molecular Carbon Ion Implantation and Laser Annealing

Tadashi Yamaguchi[1], Yoji Kawasaki[1], Tomohiro Yamashita[1], Noriko Miura[1], Mariko Mizuo[2], Jun-ichi Tsuchimoto[1], Katsumi Eikyu[1], Kazuyoshi Maekawa[1], Masahiko Fujisawa[1], and Koyu Asai[1]

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[2]Renesas Semiconductor Engineering Corporation, 4-1, Mizuhara, Itami, Hyogo, 664-0005, Japan

SSDM 2010 - RENESAS : Si:C – S/D formation

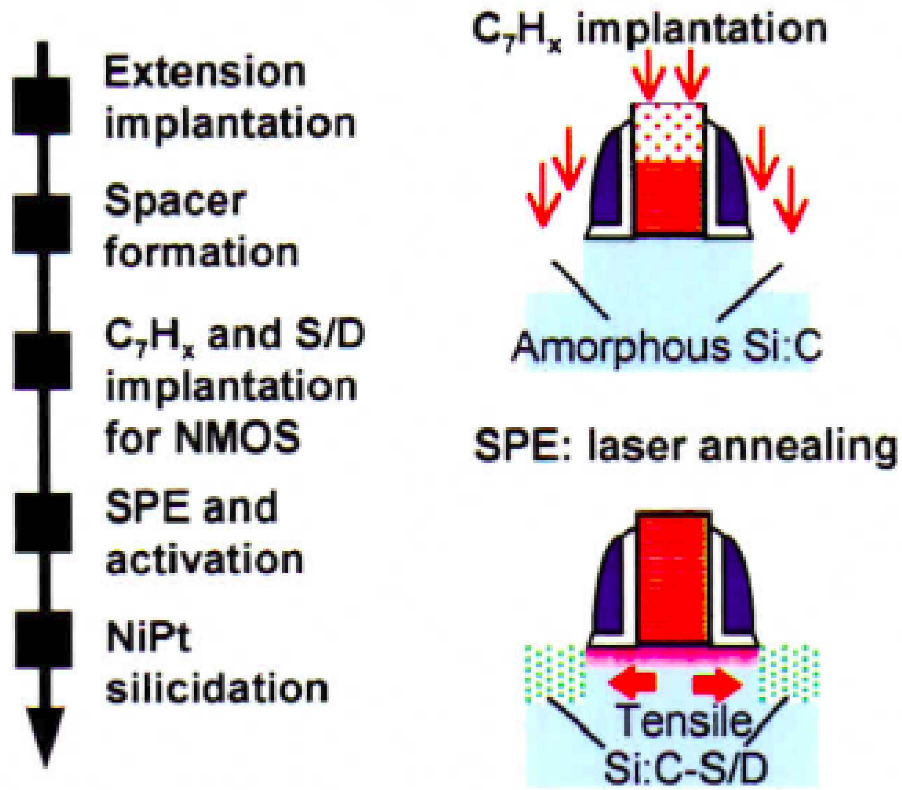


Fig. 1. Process flow of Si:C-S/D formation in nMOSFETs using C_7H_x implantation.

➢

SSDM 2010 - RENESAS : Si:C – S/D formation

Raman-test pattern

(a) Cross-sectional view

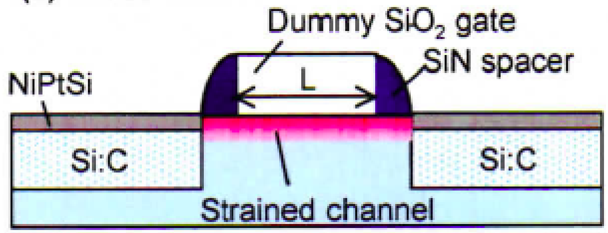
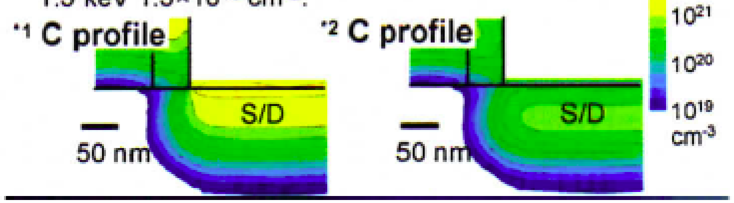


Table I. Process conditions and junction properties of nMOSFETs with Si:C-S/D.

	Process-A	Process-B
C_7H_x	Multi step*1	Single step*2
P	2 keV 3×10^{15} cm^{-2}	2 keV 3×10^{15} cm^{-2}
RTA/Laser [°C]	1000/1200	1000/1200
$C_{Si:C}$ [%]	N.D.	0.33
SIMS X_j [nm]	52	52
$T_{Si:C}$ [nm]	44	44
JL nFETs [A]	0.8×10^{-3}	1.0×10^{-3}

*1 10 keV 3×10^{15} cm^{-2}, 6 keV 3×10^{15} cm^{-2}, 1.5 keV 1.5×10^{15} cm^{-2}.
*2 10 keV 3×10^{15} cm^{-2}.



➢ Multi-step implant vs Single step implant

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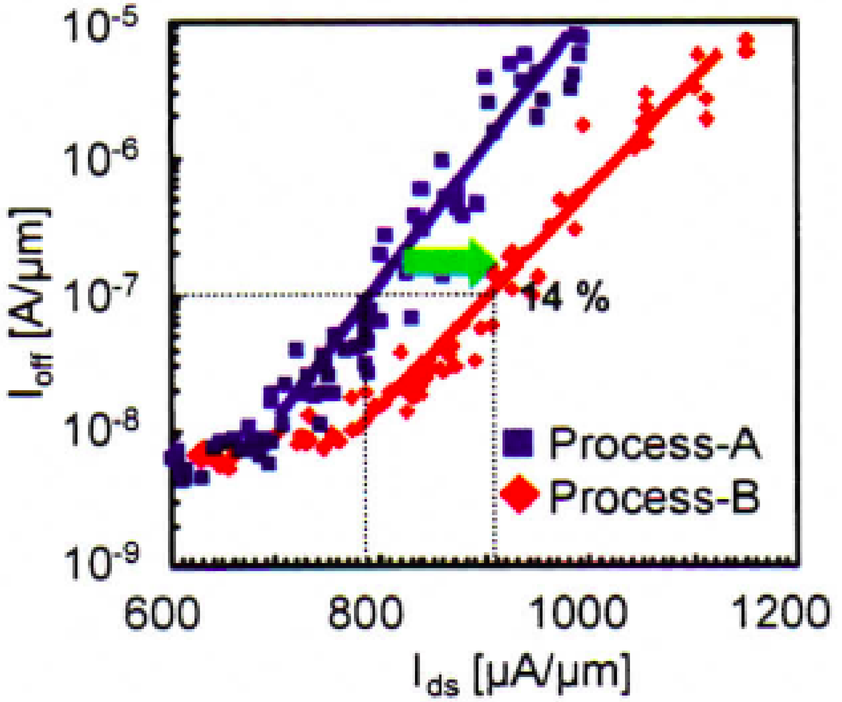

Fig. 10. I_{ds}-I_{off} characteristics of nMOSFETs with Si:C-S/D using process-A and -B.

- Single Step implant showed better Ioff characteristics

Other applications

- Carbon implant for Photoresist stripping (carbon-implanted etch stop)
- Materials Modification
- Gettering implants
- Carbon implants in other materials….

SUMMARY

- Cluster Carbon and Applications
- Amorphization, Cluster Carbon (S/D, SDE, Halo implants)
- Cold implants (Shallow Junctions, Diffusion barrier, CMOS sensors etc)
- Si:C stressor layer
- Silicide stabilization (n-MOSFET and Memory Applications)
- Carbon implant for Photoresist stripping
- Other applications….