Applications of Cluster Carbon – a Review

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Nissin Ion Equipment Inc., and SemEquip Inc
Carbon in Silicon

- Carbon is electrically inactive and substitutionally dissolved impurity in Silicon

- Implanted carbon forms strong gettering sites in Silicon and can act as sink for implantation-induced excess Si interstitials and thus avoids formation of dislocation loops.
Scheme of the Talk

- Cluster Carbon Properties and Applications
  - Self-amorphization
  - Cold implants
  - Diffusion barrier
  - Si:C stressor layer
  - Silicide stabilization
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Mass Spectrum of $C_{14}H_{14}$ molecule

Mass Spectrum - $C_{14}H_{14}$

Beam Current (mA)

AMU
ClusterCarbon Self-amorphization - $C_5H_5$ vs $C_7H_7$

- Going to a higher mass (from $C_5$ to $C_7$) at same implant condition yields about 25% increase in $\alpha$-Si layer thickness
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Even at -50°C, almost complete amorphization takes place.

At low Ts, accumulation of small defects causes amorphization.

At high Ts, larger defect complexes are formed leading to defective amorphization.
$\alpha$-Si formation at 25, -30, -60 °C 10keV, 5E14 and 1E15

@25°C

@-30°C

@-60°C

C$_7$ 10keV
1E15/cm$^2$

C$_7$ 10keV
5e14/cm$^2$
Amorphous Si Formation by Cluster Carbon at Low Temp.

- Amorphous Si thick formed by Cluster C\textsubscript{7} implant at 25°C is almost the same as that of monomer C implant at “–100°C”.
- With lowering the substrate temperature, a-Si thickness increases well beyond the a-Si thickness by monomer carbon implant.

![Graph showing the relationship between C dose and a-Si thickness for different implant conditions.](https://example.com/graph.png)
Amorphous Si Formation by Heavier Cluster Carbon – (Halo, SDE Applications)
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ClusterCarbon™ Co-Implant

Carbon co-implant provides the following:

- Shallower Junctions
- Higher Solid Solubility
- Improved Junction Abruptness

(Cluster Boron 500eV, 1e15
- Spike anneal 1050°C with and without Carbon)
EOR Defect Elimination: iRTP @ 900ºC

Ge co-implants produce EOR defects that remain following iRTP @900ºC
With diffusionless anneal, no EOR defects with $B_{18}H_{22}$ and $B_{18}H_{22} + C_{16}H_{10}$. 
C₇ as PAI implant and diffusion barrier (RT)

Xj ~ 280Å with C₇ co-implant
~ 480Å without C₇ co-implant

ΔXj ~ 200Å

- Reduced Xj
- Abrupt junction

- Nagayama et al, IWJT 2010
**Diffusion control, low temp effect (IIT 2012)**

- Thick amorphous layer – efficient P diffusion suppression
- Even with tighter distribution, almost same Rs because of higher activation

P depth profiles:

- 1E15 at -60°C: 41nm
- 1E15 at RT: 31nm
- C7 10keV 1E15 at -60°C + P
- C7 10keV 2E15 at RT + P
- C7 10keV 1E15 at RT + P

Sheet Resistance (Ohm/sq.)

- Lower sub. temp.
- Better diff. sup.

- Higher C dose → Lower Rs
- Higher Rs → Same Rs
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Nickel Silicide – advantages and issues

Advantages:
- One step low temp. formation
- Low resistivity
- Low Si consumption
- Does not suffer from resistivity degradation on narrow lines or gates

Issues:
- Rough interface between NiSi and Si
- NiSi phase is not thermodynamically stable in contact with excess Si
- NiSi films are morphologically unstable and prone to agglomeration
- Large junction leakage current
- Sheet resistance degradation due to oxygen contamination

One of the existing Solutions:
- Use of metals as an alloying element to stabilize Nickel Silicide
Choice of elements:

![Bar charts showing temperature ranges for different elements.](image)

ClusterCarbon could be a choice!

ECS 210th Meeting – Abstract 1010
NiSi:C as contact technology for MOSFETS with silicon-carbon (Si:C) source/drain (S/D) regions.

Presence of carbon at NiSi:C grain boundaries and NiSi:C/Si interface modify the grain boundary and interfacial energies and thus influence the kinetics of NiSi:C silicidation.

NiSi:C silicidation suppresses deep-level defects leading to better n+/p junction characteristics.
Experimental Process flow: Ni silicide (bulk wafer)

1. Wafer (N-type silicon: Implant C_{16}, B_{18}, H_{22}, BF_{2}, B_{11})
2. Native oxide removal (HF 1 : 100)
3. Metal deposition
   (splits: Ni/TiN (15/10nm), Ni-Pd(5%)/TiN, Yb/Ni/TiN (1.5/13.5/10nm), ..)
4. 1st Rapid thermal process
   (splits: 400 °C ~ 800 °C, 30s)
5. Selective wet etching (H_{2}SO_{4} : H_{2}O_{2} = 4 : 1)
6. 2nd Rapid thermal process
7. Post-silicidation annealing (550 °C ~ 700 °C, 30min)

(collaboration study between SemEquip and CNU)
Experimental Process flow: Ni silicide (diode pattern)

1. Pattern wafer (N-type silicon: Implant $C_{16}B_{18}H_{22}BF_2B_{11}$)
2. Native oxide removal (HF 1 : 100)
3. Metal deposition
   - (splits: Ni/TiN (15/10nm), Ni-Pd(5%)/TiN, Yb/Ni/TiN (1.5/13.5/10nm).....)
4. Rapid thermal process (600 °C, 30s)
5. Selective wet etching ($H_2SO_4 : H_2O_2 = 4 : 1$)
6. Measure I-V characteristics (junction leakage current)

(collaboration study between SemEquip and CNU)
Impact of Carbon co-implants on silicide stability

- Clear advantages in Ni silicide resistance and stability with thermal anneals.
- This gain comes from the fact that a lower agglomeration effect is observed on both surface and depth when carbon is present in the silicide.

(IMEC web site)
NICKEL SILICIDE:
Plan view SEM: Carbon effect – Lower agglomeration
X-SEM: Carbon effect

- Without C₁₆
  - B₁₈H₂₂
  - Anneal 650

- With C₁₆
  - BF₂
  - Anneal 650

- Boron
  - Anneal 650
AFM Surface roughness: carbon effect

- $B_{18}H_{22}$, Anneal 650
  - Without $C_{16}$: Roughness=2.045nm
  - With $C_{16}$: Roughness=1.515nm

- $BF_2$, Anneal 650
  - Roughness=5.141nm
  - Roughness=5.064nm

- Boron, Anneal 650
  - Roughness=1.559nm
  - Roughness=1.280nm

- $C_{16}$ lower surface roughness
Thermally stable Ni silicide for DRAM applications

- Thermal budget constraints during the DRAM BEOL, Ni silicide is not stable and not usable unless its thermal stability is improved.
- Carbon implantation techniques to stabilize the ultra-shallow junction and S/D silicides to withstand the DRAM BEOL to improve the overall peripheral CMOS performance.

Ref: IMEC website, CNU Korea, SemEquip Collaboration
CMOS periphery devices in Memory Applications

Carbon-based thermal stabilization techniques to improve the performance of CMOS periphery devices in memory application.

- Substantial current drive improvement,
- contact resistance lowering
- RO delay improvement
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  - Si:C stressor layer
Strain (Si:C Layer) $\Rightarrow$ high $\%$ $[C]_{subs}$

Mobility enhancement

Device Speed
Mobility Enhancement vs % of $[C]_{subs}$

Y. Cho et al, EMRS, 2008
$[C]_{\text{subs}}$ from HRXRD - 6keV, 2e15 atoms/cm$^2$ (Laser Annealing)

ECS 2007 – TI, Axcelis, SemEquip

VLSI 2007 – pg 44

Fig. 2 HRXRD rocking curve of the SPE Si:C film ($[C]_{\text{sub}}=1.65$ at.$\%$) grown on (100) Si substrate. The well defined Si:C peak and fringes indicate that the Si:C film is high-quality single crystal.
TEM – Monomer vs $C_7H_7$ - 6keV, 2e15 atoms/cm²

ECS 2007

XTEM for monomer C implant
- patchy amorphization
- no well defined interface

5 nm

XTEM for $C_7H_7$ implant
- complete amorphization
- well defined interface at 230 Å

6.6keV, 2e15 atoms/cm²

ECS 2007 – Ti, Axcelis, SemEquip

Patchy amorphization

Well defined interface
Monomer C w/o PAI ➔ low[C]sub ➔ P4 on [C]sub is small.
Cluster C7: High [C]sub independent on PAI conditions.
There is no clear dependence on LSA temperature.
$P_2 + C_7H_7$

(iRTP 1050°C + fRTP 1200°C)

Dramatic increase in Rs beyond 1.75% atomic carbon. Precipitation of carbon beyond 1.75%
XTEM

$P_2 + C_7H_7$ (iRTP 1050°C + fRTP 1250°C)

1.5% + 1.0%

Very few stacking faults with a couple of EOR loops

1.75% + 1.5%

Many stacking faults with a couple of EOR loops

2.0% + 1.5%

Very many stacking faults with a couple of EOR loops

5 nm
XTEM

1.5% atomic carbon - $C_7H_7$ vs $(P_2 + C_7H_7)$

No regrowth defects after iRTP 1050°C for both $C_7$ and $P_2 + C_7$ cases.
Analytical Approach for Enhancement of nMOSFET Performance with Si:C Source/Drain Formed by Molecular Carbon Ion Implantation and Laser Annealing

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SSDM 2010 - RENESAS: Si:C – S/D formation

Fig. 1. Process flow of Si:C-S/D formation in nMOSFETs using C$_7$H$_x$ implantation.
SSDM 2010 - RENESAS : Si:C – S/D formation

- Multi-step implant vs Single step implant

Table I. Process conditions and junction properties of nMOSFETs with Si:C-S/D.

<table>
<thead>
<tr>
<th></th>
<th>Process-A</th>
<th>Process-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{7}H_{x}</td>
<td>Multi step(^{1})</td>
<td>Single step(^{2})</td>
</tr>
<tr>
<td>P</td>
<td>2 keV</td>
<td>2 keV</td>
</tr>
<tr>
<td></td>
<td>3 \times 10^{15} \text{ cm}^{-2}</td>
<td>3 \times 10^{15} \text{ cm}^{-2}</td>
</tr>
<tr>
<td>RTA/Laser [^{\circ}C]</td>
<td>1000/1200</td>
<td>1000/1200</td>
</tr>
<tr>
<td>C_{Si:C} [%]</td>
<td>N.D.</td>
<td>0.33</td>
</tr>
<tr>
<td>SIMS X_{j} [nm]</td>
<td>52</td>
<td>52</td>
</tr>
<tr>
<td>T_{Si:C} [nm]</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>JL nFETs [A]</td>
<td>0.8 \times 10^{-3}</td>
<td>1.0 \times 10^{-3}</td>
</tr>
</tbody>
</table>

\(^{1}\) 10 keV. 3 \times 10^{15} \text{ cm}^{-2}, 6 \text{ keV.} 3 \times 10^{15} \text{ cm}^{-2}, 1.5 \text{ keV.} 1.5 \times 10^{15} \text{ cm}^{-2}.

\(^{2}\) 10 keV. 3 \times 10^{15} \text{ cm}^{-2}.
SSDM 2010 - RENESAS : Si:C – S/D formation

- Single Step implant showed better Ioff characteristics

Fig. 10. $I_{ds}$-$I_{off}$ characteristics of nMOSFETs with Si:C-S/D using process-A and -B.
Other applications

- Carbon implant for Photoresist stripping (carbon-implanted etch stop)

- Materials Modification

- Gettering implants

- Carbon implants in other materials....
SUMMARY

- Cluster Carbon and Applications
- Amorphization, Cluster Carbon (S/D, SDE, Halo implants)
- Cold implants (Shallow Junctions, Diffusion barrier, CMOS sensors etc)
- Si:C stressor layer
- Silicide stabilization (n-MOSFET and Memory Applications)
- Carbon implant for Photoresist stripping
- Other applications....