ULTRA LOW THERMAL BUDGET LASER THERMAL ANNEALING FOR 3D SEMICONDUCTOR AND PHOTOVOLTAIC APPLICATIONS

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Applications Development

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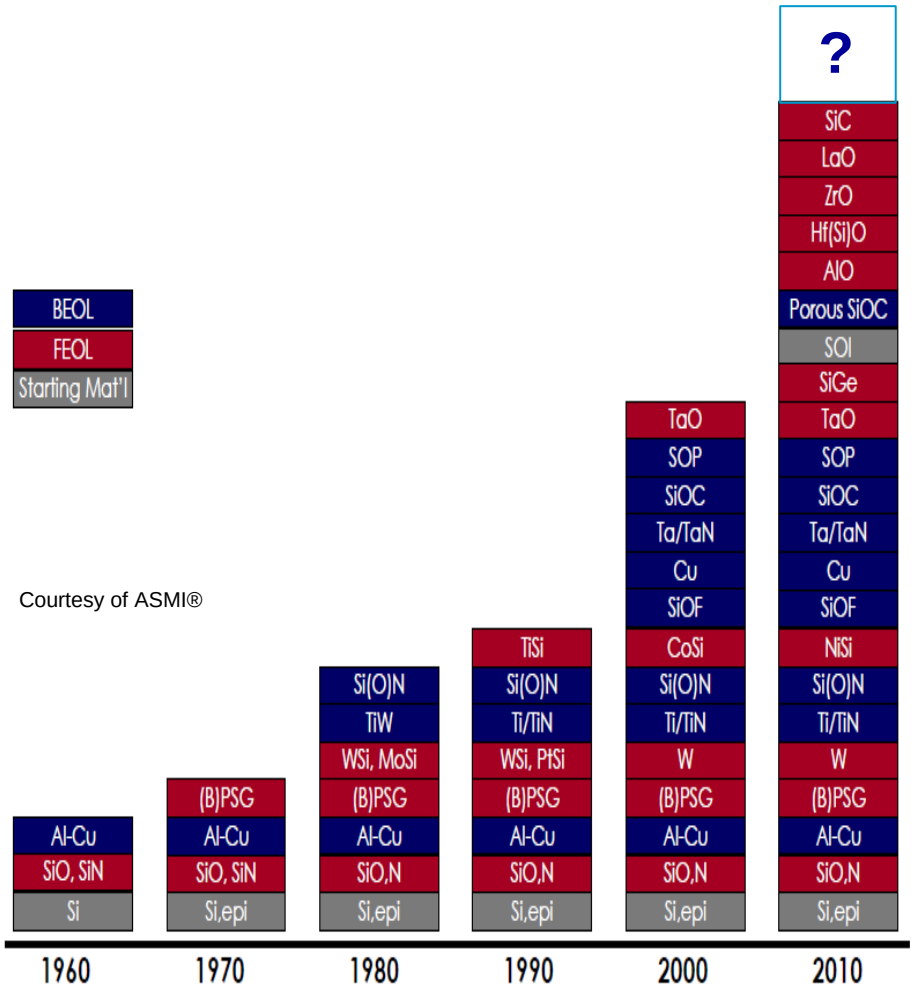
Excico Company Snapshot

- **Thermal processing solutions for semiconductor manufacturing using Ultrafast Annealing technologies and processes**

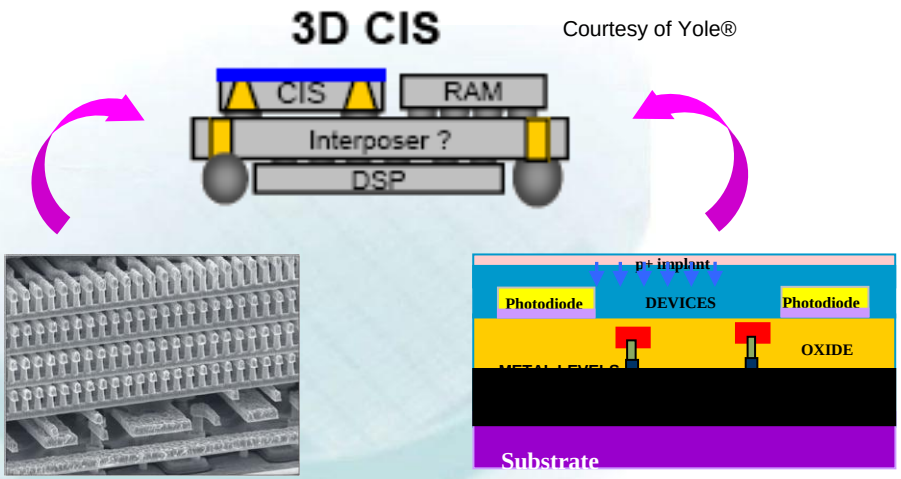
  - ❖ **strong Focus on SEMI Markets :**
    - ⇨ **Memory**
    - ⇨ **LOGIC**
    - ⇨ **CMOS Imagers**
    - ⇨ **Power Devices**

  - ❖ **Strong development of PV applications**
  - ❖ **Other: LED, MEMS,…**

More than Moore = More materials & 3D design



Courtesy of ASMI®



Courtesy of Yole®

CHALLENGES

- **Improve numerous material properties through annealing**
- **3D Localized process control**

Low thermal budget is mandatory

The 3D Thermal Processes Challenge

SEMI & PV trends

- -Cost reduction
- -Yield increase
- -New Material
- -2D to 3D

Process Flows

- -Minimize Steps
- -Process uniformity
- -Material Selectivity
- -Low Thermal Budget

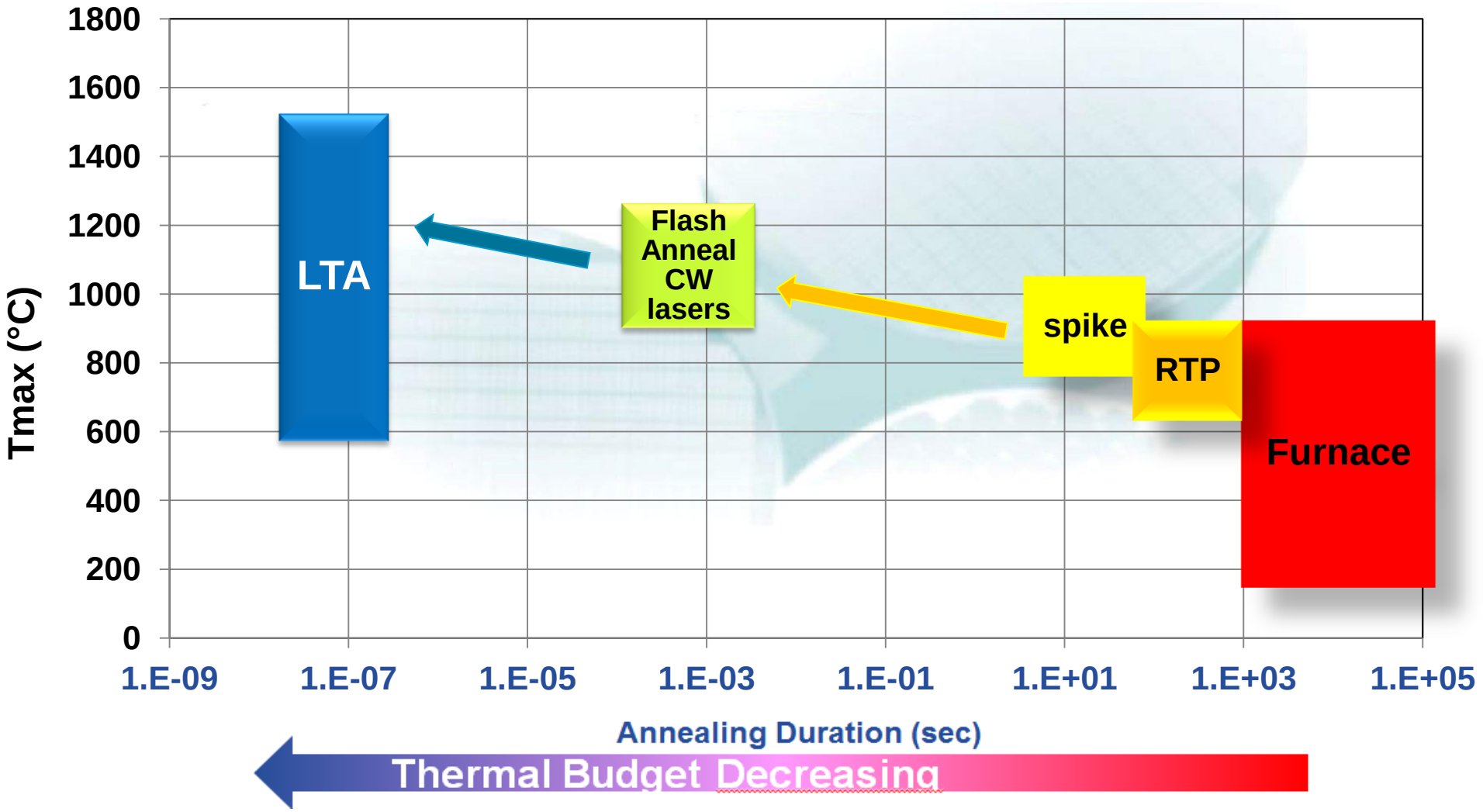
New Annealing Equipements

+Pulsed Lasers

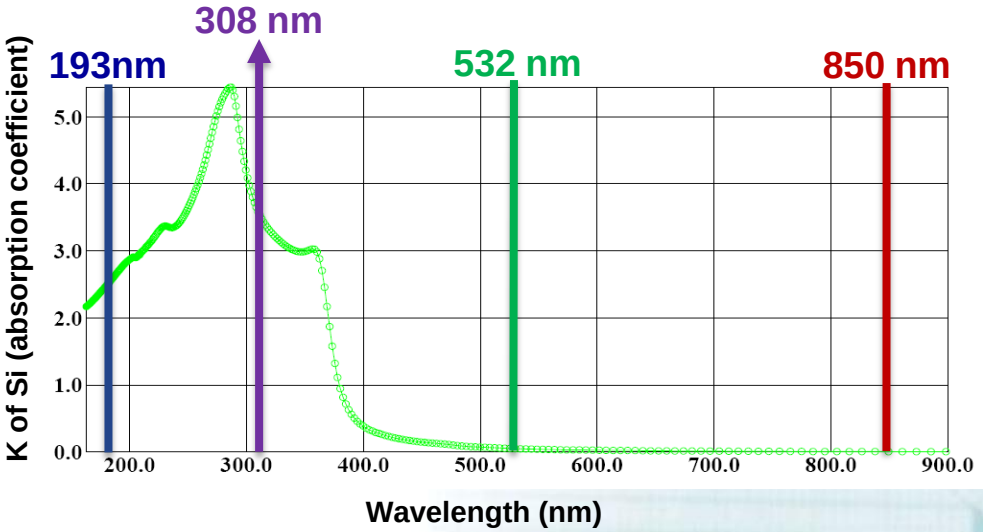
+Wavelength selectivity

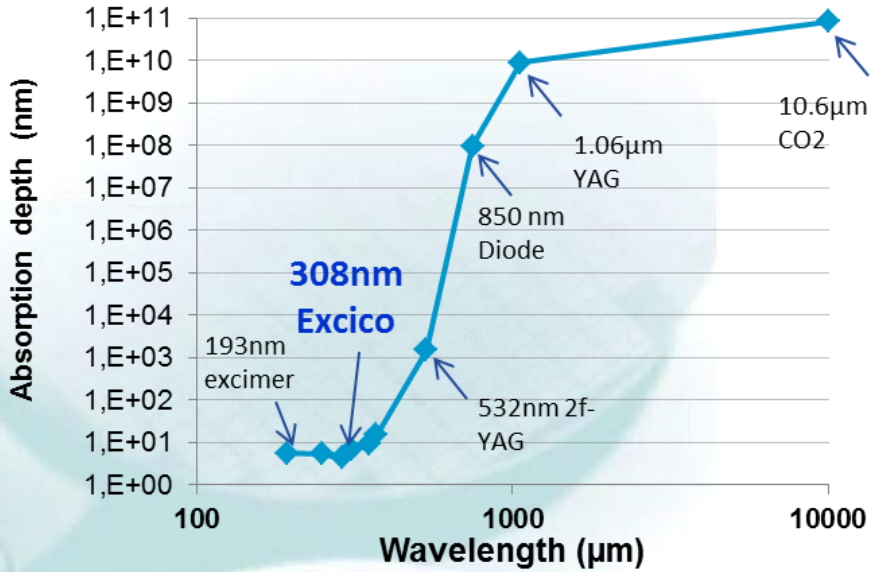
+Single Die Anneal

New devices are demanding shorter anneals and higher temperatures



Controlling process depth is key to rapid, high-precision anneal, and 3D anneal control





- **Selecting the right wavelength laser is key to getting nm Process Control**
  - ❖ Long wavelength lasers have penetration that is too deep which could makes hard-to-control anneal process
  - ❖ Controlling melt depth with long wavelength requires additional process steps adding cost and affecting yield

Today Controllable process depth requires a laser with wavelength of 200-350nm

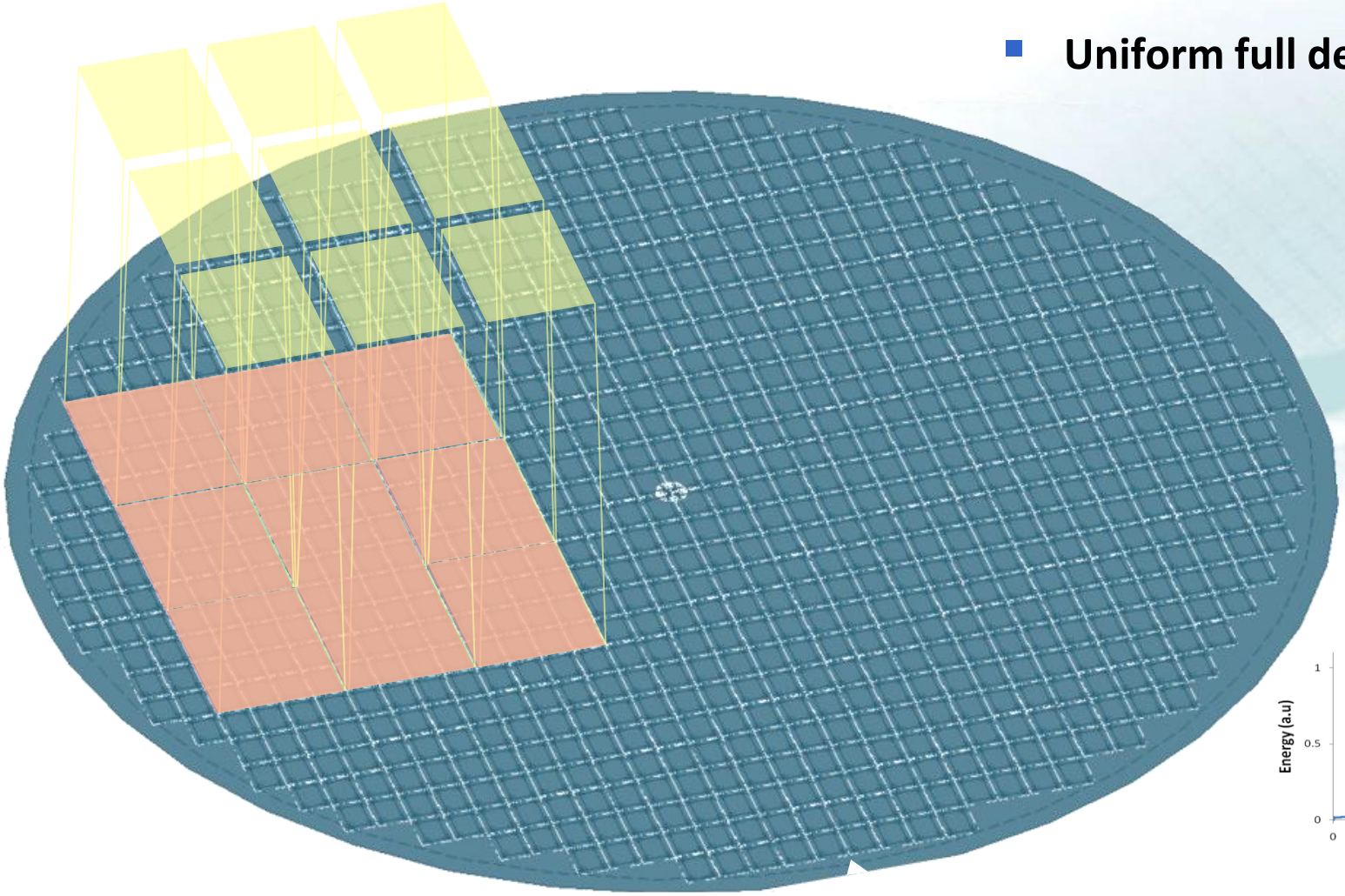
Excico LTA can anneal selectively 2D and 3D structures

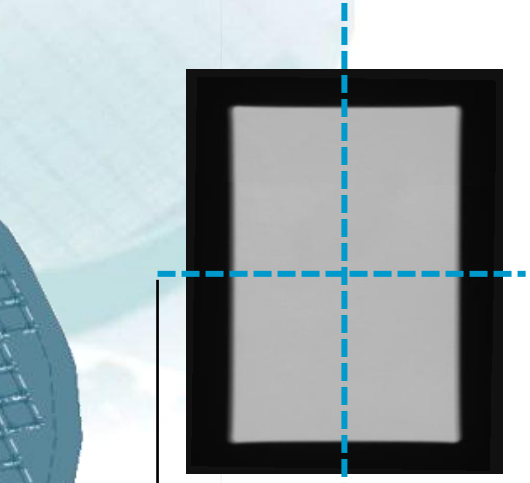
	Laser Thermal Annealing	Scanned ms-Anneal (Flash, Laser)	RTP
Temperature	From 300 to >1400 °C	700°C/ 1300°C	<1200 °C
Time at Temperature	< 1 µs	>1ms	> 1 s
Process Achievement	**Liquid phase epi + extreme activation + No diffusion**	solid phase + better activation + less diffusion	solid phase + limited activation
Depth Selective anneal	**~1 to 1000 nm depth**	Full Wafer depth	Full wafer depth
Material Selective anneal	**YES : single wavelength**	Full wafer surface	Full wafer surface

Process

Excico LTA – Full Die Exposure capability

- Excico LTA Step and Repeat process
- Uniform full device exposure (FDE)



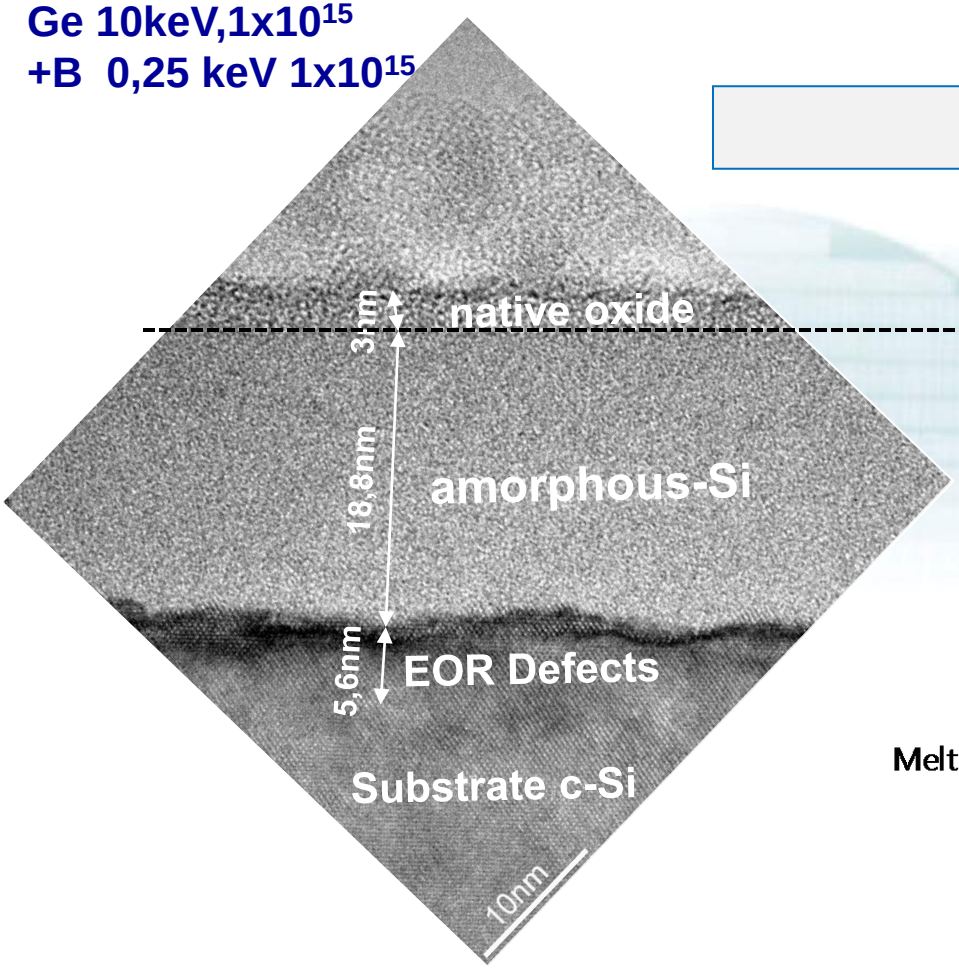


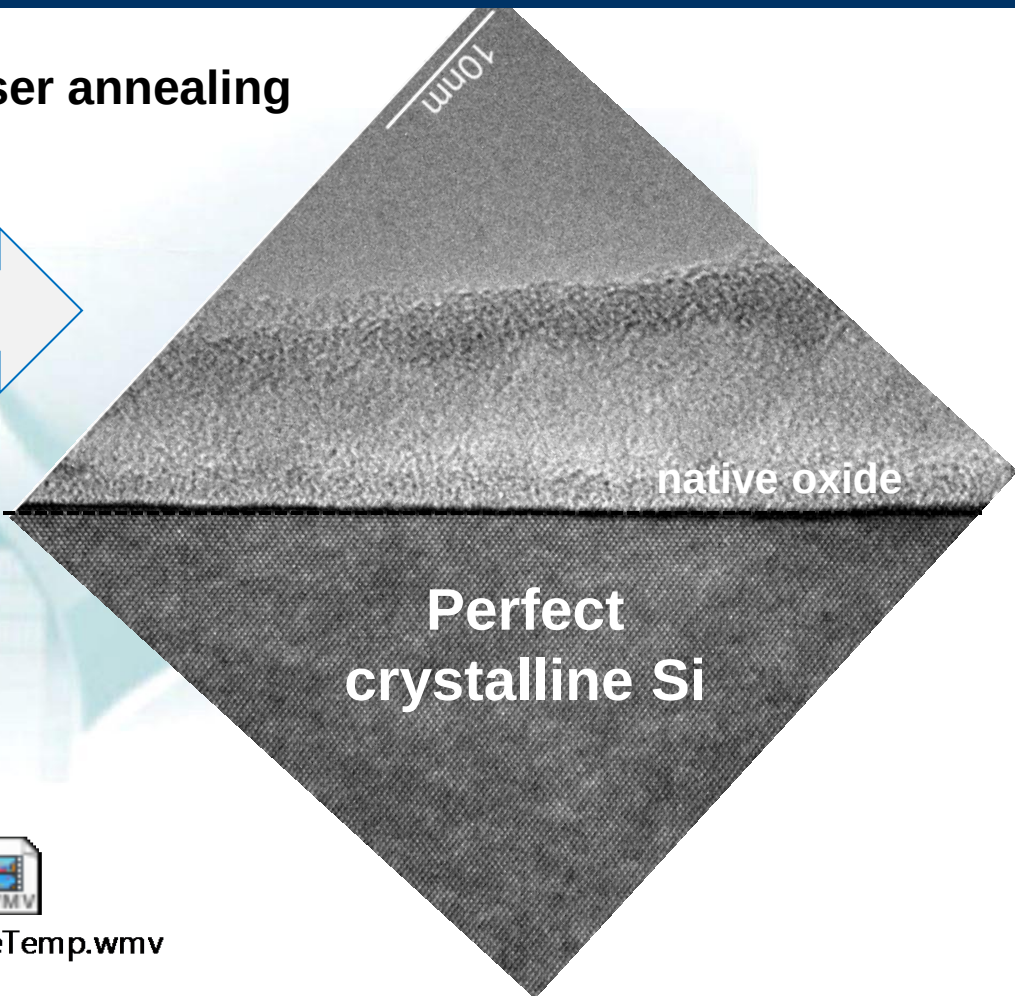
LTA Junction Recrystallization process

Before Laser annealing

Ge 10keV,1x10^{15}
+B 0,25 keV 1x10^{15}

After Laser annealing



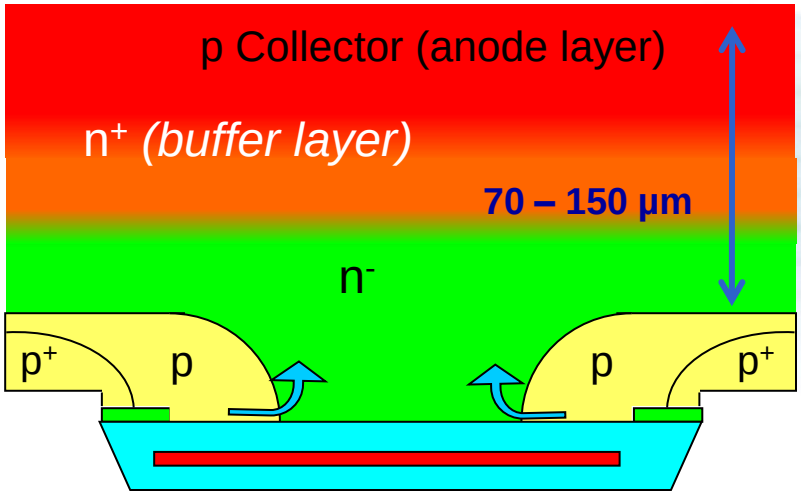


MeltPhaseTemp.wmv

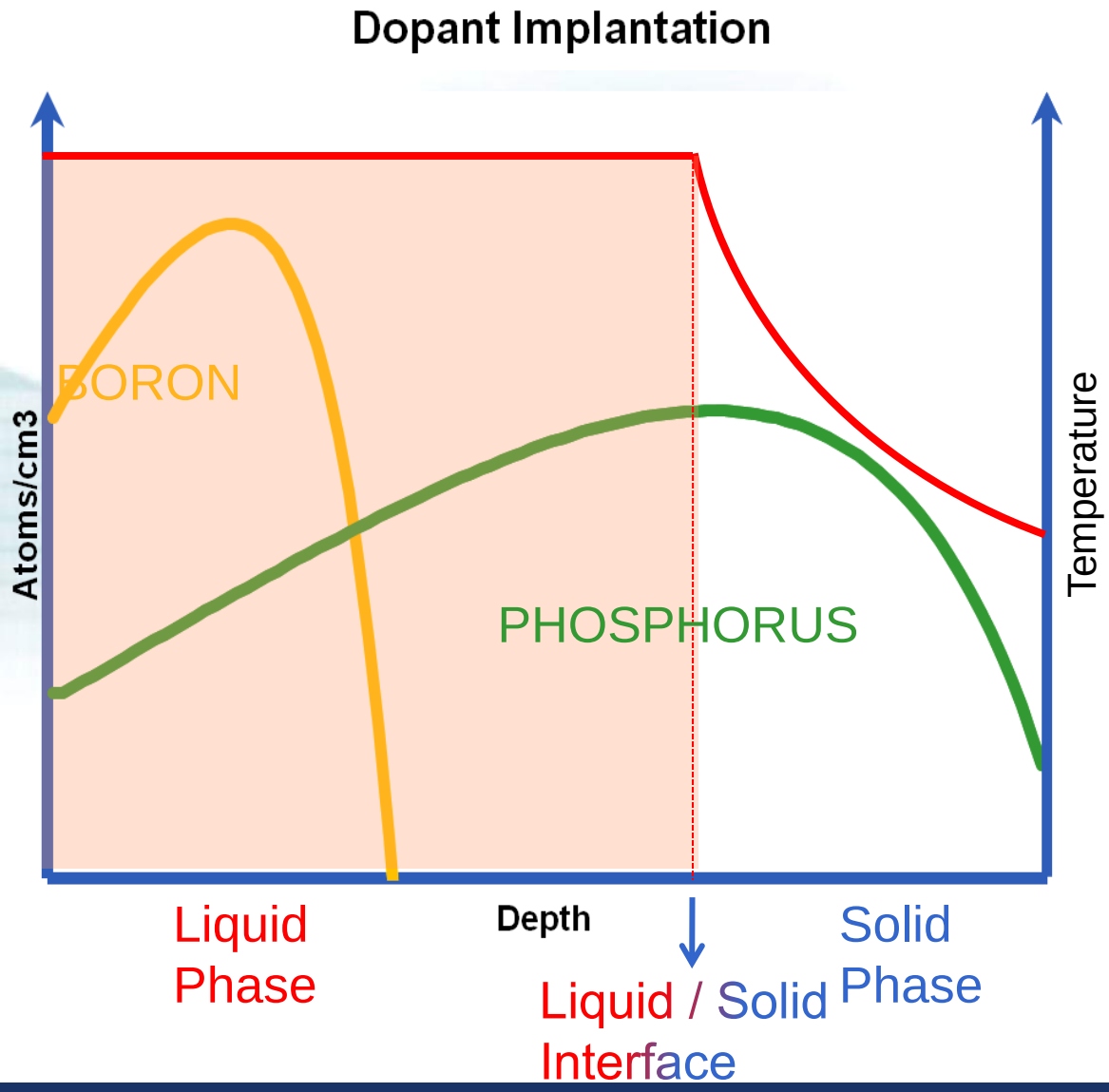
3D AND BACKSIDE PASSIVATION OF THINNED WAFERS

Double Implant IGBT for Power Devices

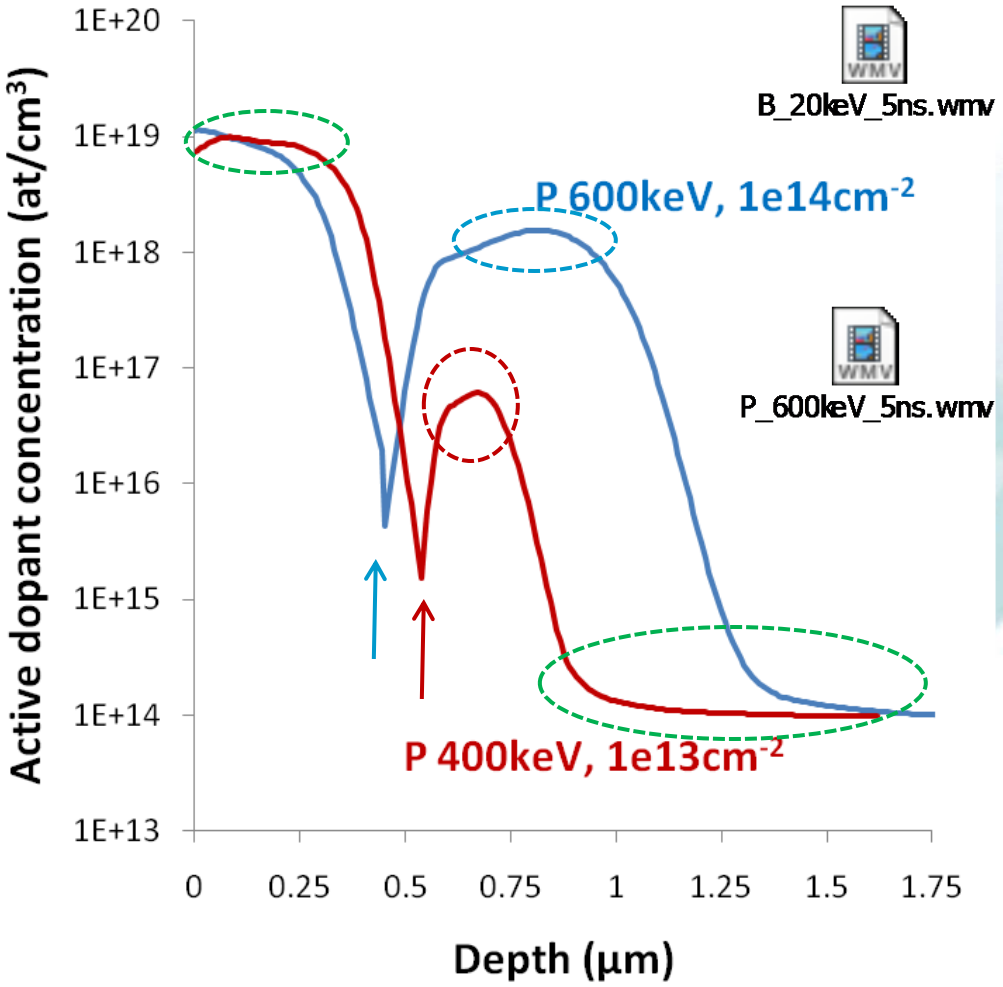
Laser Pulse



Goal : activate the backside (P+) *and* the buffer region (N+)



3D Multiple junction engineering



Activation: SRP results

- Full activation around Rp
- EOR Defects fully annealed
- Small dopant mixing zone

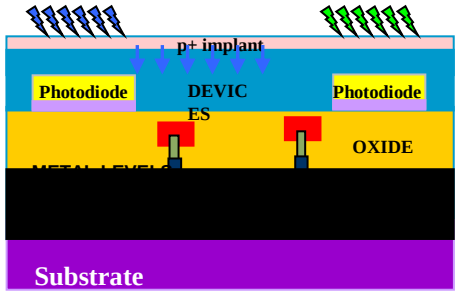
Good anode efficiency
Good buffer layer

[K. Huet et al., RTP 2010]

CMOS IMAGING SENSORS

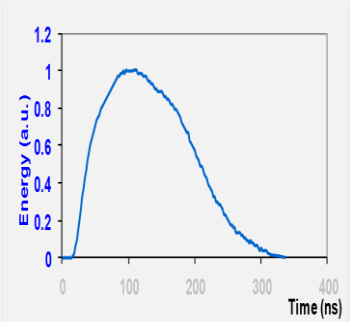
‘3D’ Backside Passivation/activation of CIS

Backside Imagers



- Keep buried collectors non damaged by passivation step

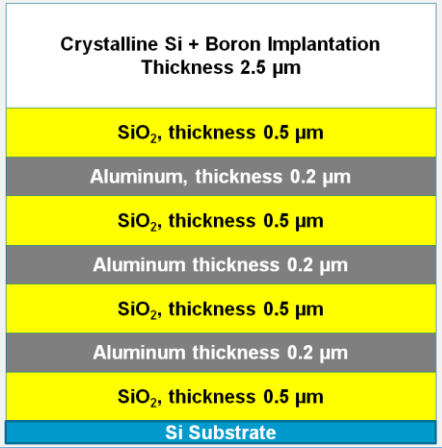
LTA pulse



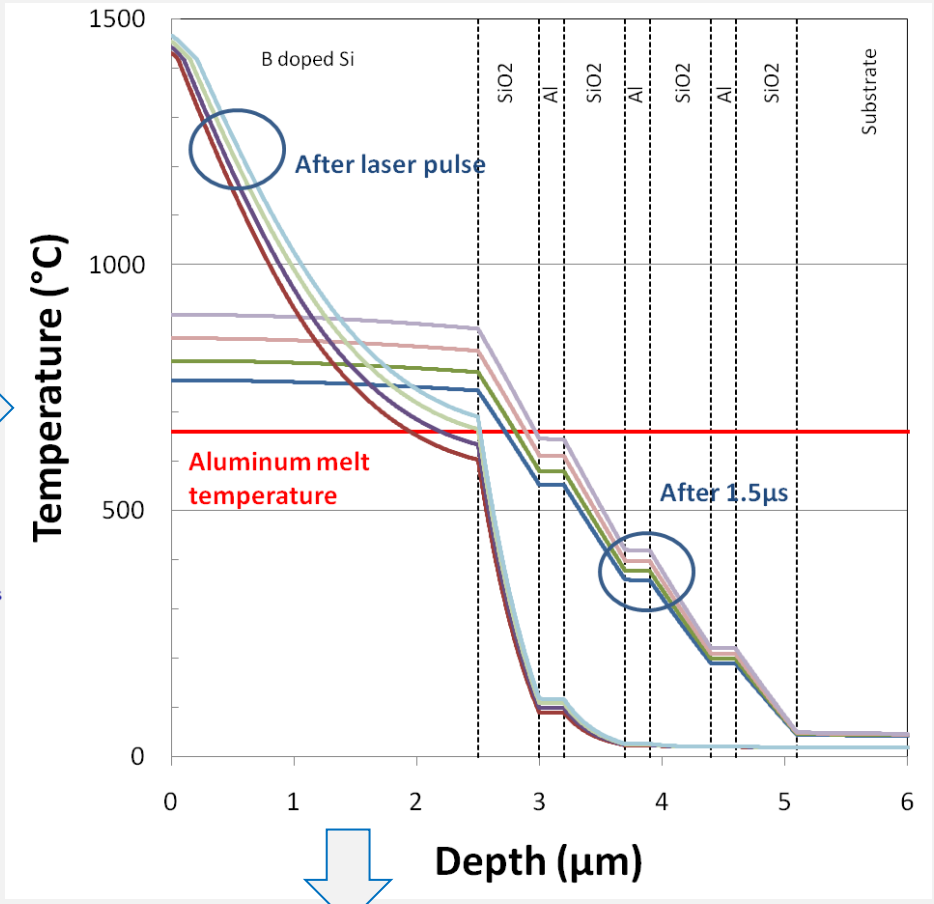
+

Structure

Laser irradiation
λ = 308 nm, 170ns

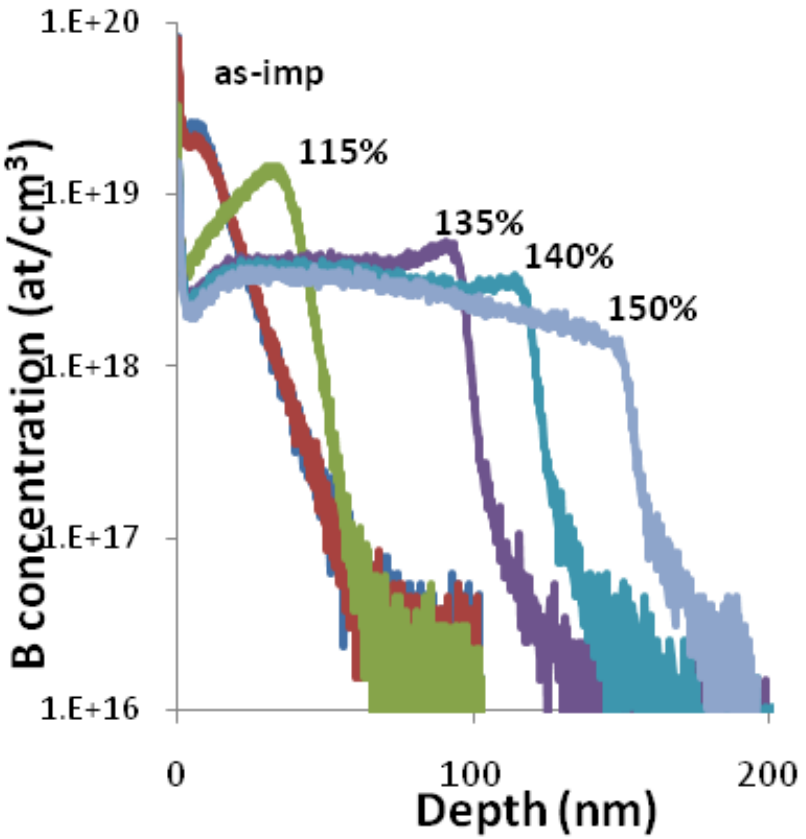


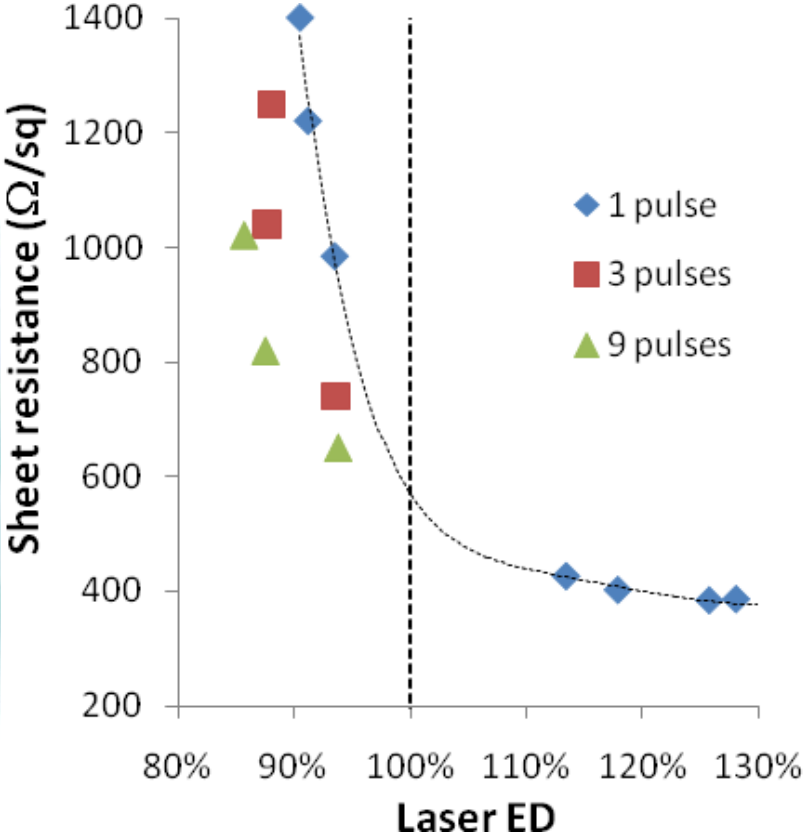
Temperature profiles



Process Window determination to avoid damage of metal layer

Junction dopant profiles for CMOS imagers



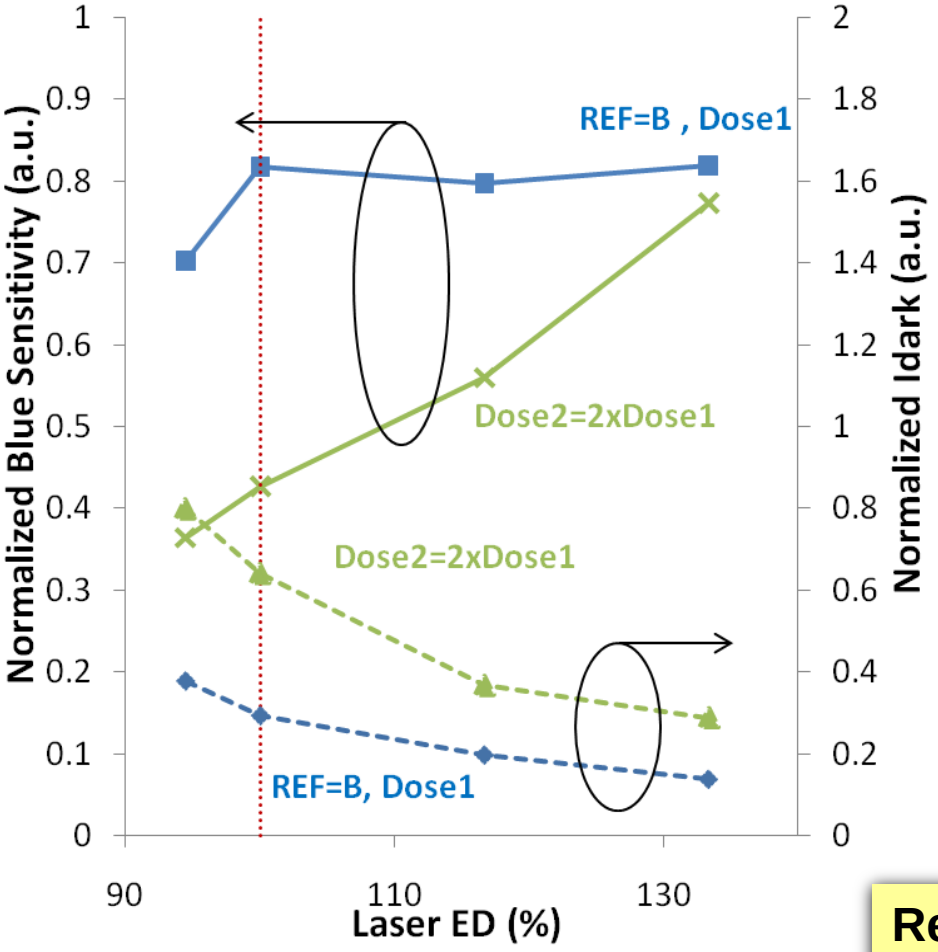


- **Shape controlled by Melt depth**
- **Diffusionless in Nonmelt**

- **Melt regime > 90% activ. rate**
- **Non melt regime > 50%**

[J. Venturini et al., IISW 2011 & Subtherm 2011]

Backside Single shot process: Imager Device performance



For same implanted depth 60 nm @ 1e17

- **Low B_{11} Dose**
  - ❖ Less imp-induced defects
  - ❖ Shallower dopant tail
  - ⇒ Excellent performance at low ED
- **High B_{11} dose (2X)**
  - ❖ More imp-induced defects & Deeper dopant tail
  - ⇒ Higher ED needed for optimal performance
- **Non-melt regime: Good backside passivation for low dose implant**

Residual defects are more contributing to device performance than the Junction thickness

[J. Venturini et al., IISW 2011 & Subtherm 2011]

NEXT GENERATION 3D MEMORIES

ITRS 2011 – NVM Technology Roadmap

Non-Volatile Memory Potential Solutions

First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
NAND Flash Poly 1/2 Pitch	22nm			17nm			13nm			10nm			8nm

NAND Flash

Floating gate device

Charge trapping device (CT)

3D stacking

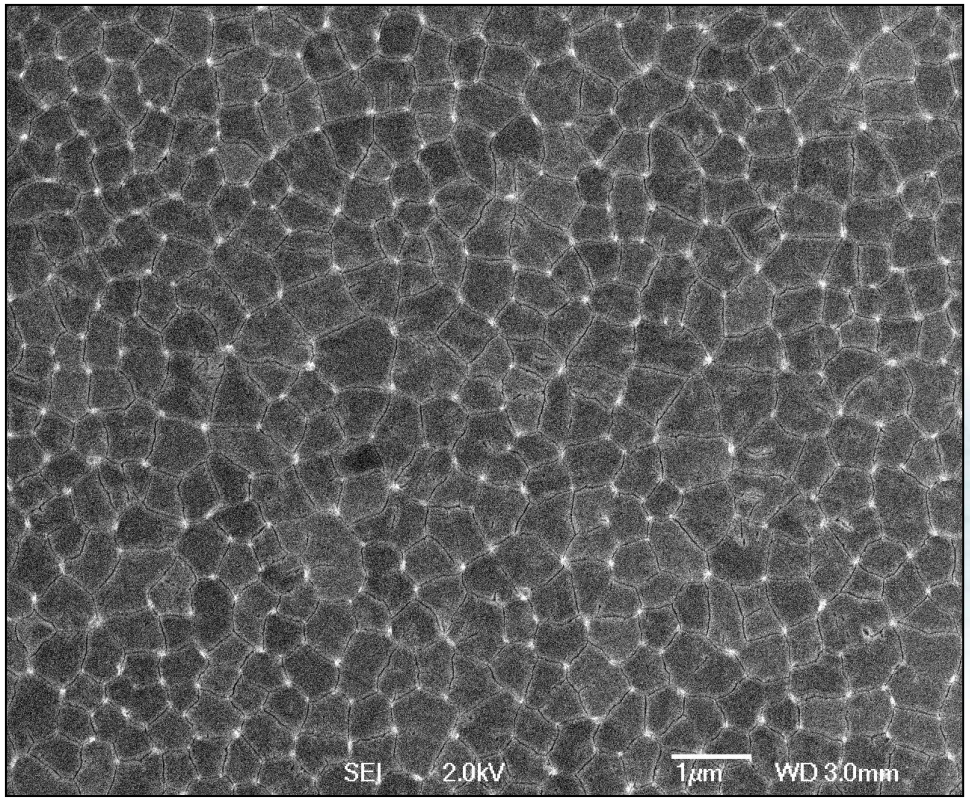
Research Required
Development Underway
Qualification / Pre-production
Continuous Improvement

NAND Flash scaling after 2015

Source: IMEC

- 3D Charge Trapping is the chosen path
- Non charged based cell (ReRAM, PCRAM) comes close behind

Excico LTA enables Low Thermal Budget Crystallization



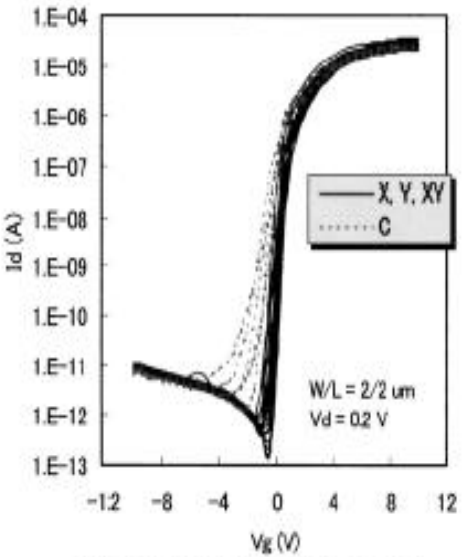


Fig. 3. Id-Vg characteristics of c-Si

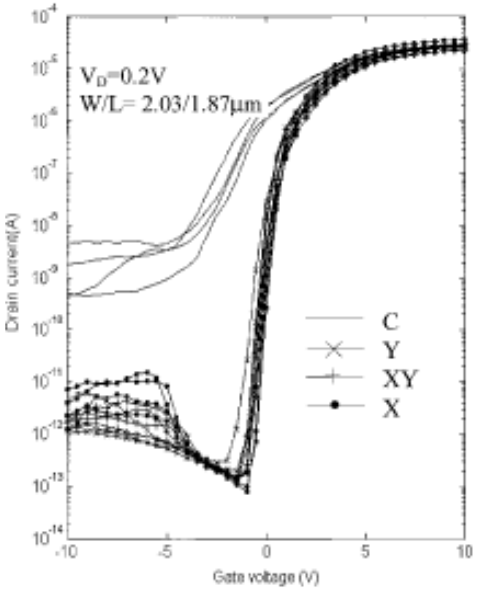


Fig.2. I_D-V_G characteristics of c-Si TFTs at various positions inside a grain-filter having ECR-PECVD SiO_2 as a gate insulator

180 ns anneal pulse

30 ns anneal pulse

[Y. Hiroshima & all, Seiko Epson and DIMES, in AMLCD'03]

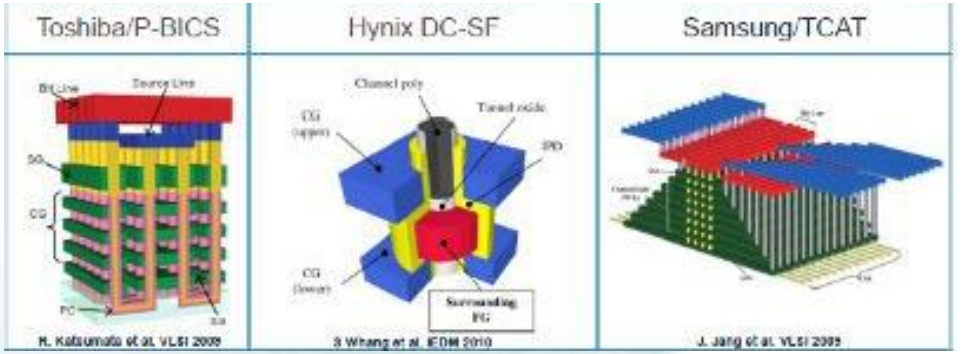
Longer anneal Pulse

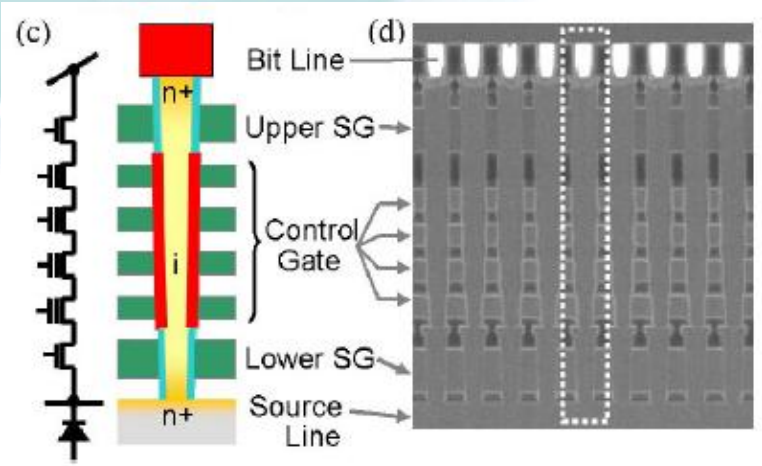
- Higher crystal quality and larger grains
- Higher mobility and better TFT performance uniformity

Excico LTA for 3D NAND Flash memory

3D NAND: Vertical channel crystallization challenges

- Large grains High Quality Si: Low defects and High mobility
- Localize thermal budget in Silicon channel region
- Low thermal budget mandatory
  - ⇨ Keep 3D patterned structure integrity
  - ⇨ Avoid dielectric layers mixing with poly Si





Aochi et al., IMW 2011

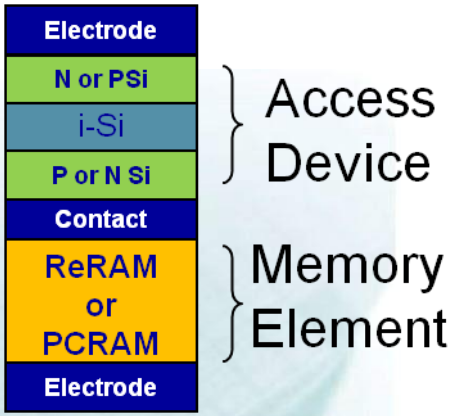
Excico Laser Thermal Annealing Solution

- Selective anneal of Upper Transistor Si channel
- Uniform poly Si with large grains
- Damage free low thermal budget process
- High select transistor performance: Low leakage and high ON current

Excico LTA for 3D NAND Flash memory 3D Emerging Memories

ReRAM & PCRAM: Access Device design challenges

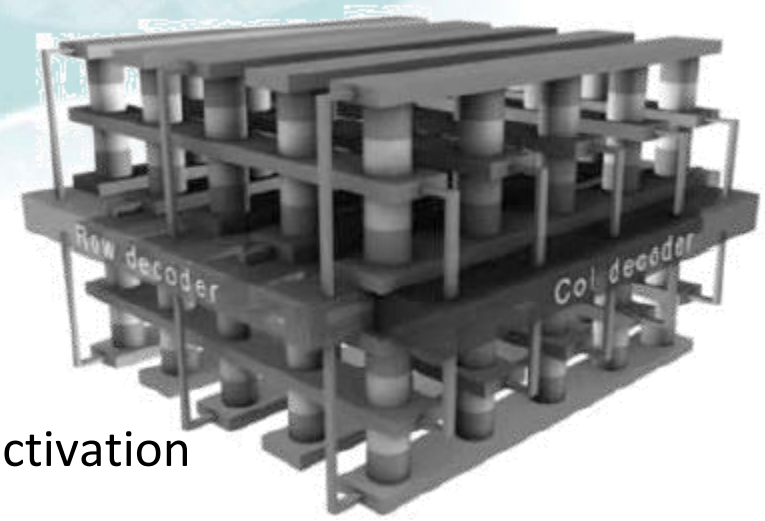
- Control Dopant Diffusion
- High dopant activation
- High Quality Si
- Low thermal budget mandatory
  - ⇨ Control dopant diffusion
  - ⇨ Avoid damaging fragile materials & 3D stacking



Excico Laser Thermal Annealing Solution

- Ultra low thermal budget and sub-µs process
- Melt process to achieve Large grain size and high activation
- UV Laser light for selective annealing of Si region

[K. Huet et al., IIT 2012, J. Venturini et al., IWJT 2012]



Lee et al., IEDM 2008

PHOTOVOLTAIC CELLS

Application strategy c-Si segment

Reduce $/W$_p$

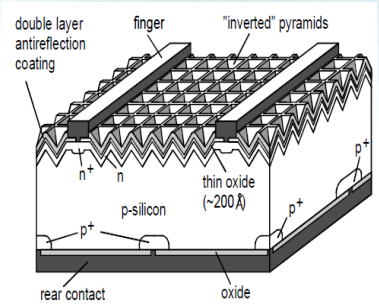
Enable panel price < 1$/Wp from 2012 & beyond

1. *Increase W_p by increasing cell/mod. efficiency*
2. *Lower $ by any cost reduction source enabled by laser processing*

Eff. ↑ road

High efficiency solar cell structures

- *Selective Emitters,*
- *PERC/PERL*
- *HJ/IT*
- *n-type, RCC/IBC*



PERL: η =25.0%

$ ↓ road

1. *Reduce equipment Cost-Of-Ownership*
2. *Reduce material costs (replace Ag by Cu)*
3. *Reduce No. of process steps*
4. *Lower c-Si wafer thickness*

✓ **both roads taken at the same time**

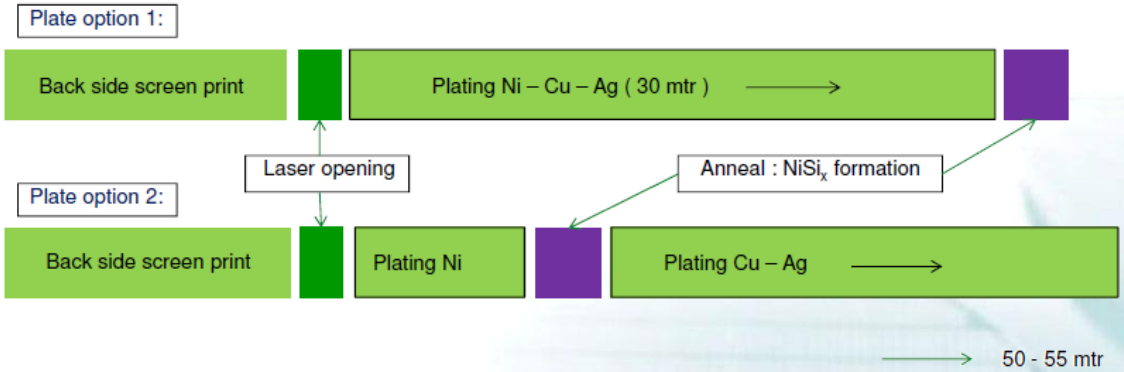
Applications details c-Si segment

high eff. cell type	Eff. %	LTA process
p-type PERL/PERC	19-20.5%	**Silicidation** for **front side copper contacts**
p-type PERL	19-20.5%	**Boron activation** for BSF
n-type PERT	19.5-21%	**Boron activation** emitter backside
Selective Emitters	17.5-19%	Laser **doping** front side (PSG)
SHJ (n-type)	19.5-23%	**TCO anneal** front &/or back side
IBC (n-type)	20-25%	**Boron & Phosph. activation** backside
SHJ-RCC (n-type)	21-25%	- **TCO anneal** front & rear - Laser **contacting**

✓ **several process paths for Excico on high efficiency c-Si cells**

NiSi formation for Cu contacts on c-Si cells

✓ NiSi for mechanical adhesion of Cu contacts

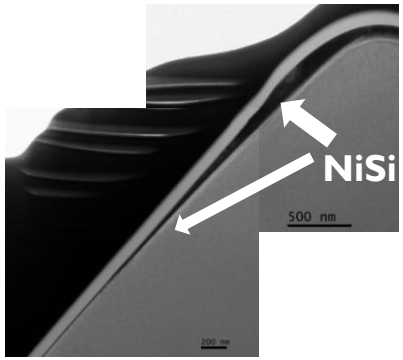


[L. Tous et al., Proc. of the 2nd Silicon PV, Belgium, 2012]

✓ ELA advantages vs. furnace vs. RTA :

- shallow emitter compatible (better control of thickness & composition)
- higher productivity + lower thermal budgets vs. furnace
- +0.6% abs. vs best RTA process
- in-line integration possible

✓ PERC cell results with NiSi formation by laser:

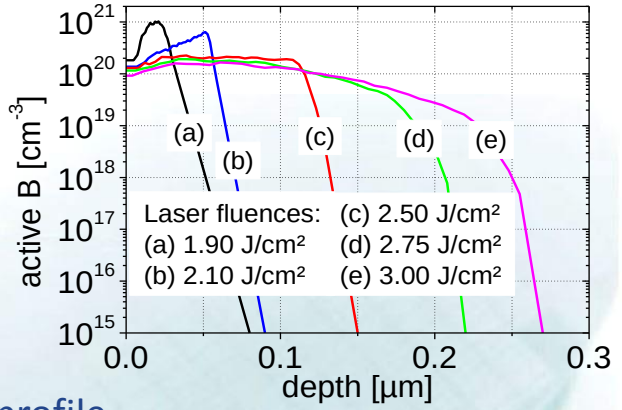


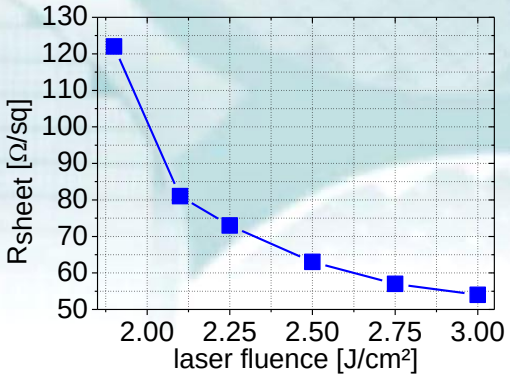
Cell type		Jsc [mA/cm2]	Voc [mV]	FF [%]	Eta [%]	Rseries [Ohm.cm2]	pFF [%]
85 Ω/sq SP Ag reference	Average (6 cells)	38.3 ±0.1	651.3 ±2.1	77.3 ±1	19.3 ±0.2	1.1 ±0.1	83.2 ±0.3
	best	38.4	653.5	77.8	19.5	1.0	83.4
85 Ω/sq ps-laser + Ni (ELA) /Cu	Average (5 cells)	39.1 ±0.3	649.2 ±1.1	77.7 ±1	19.7 ±0.2	0.8 ±0.2	82.2 ±0.1
	best	**39.3**	**649.8**	**78.3**	**20.0**	**0.7**	**82.1**

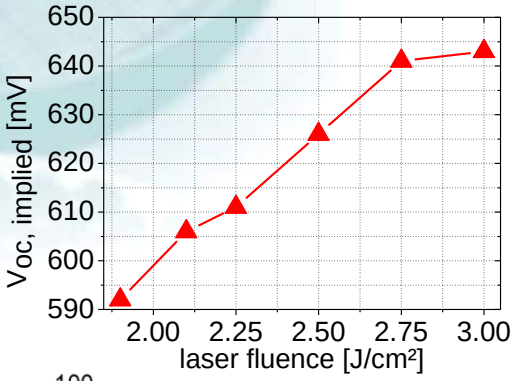
→ 20% efficiency & +0.4-0.5% absolute vs. SP Ag

Boron activation for rear junctions

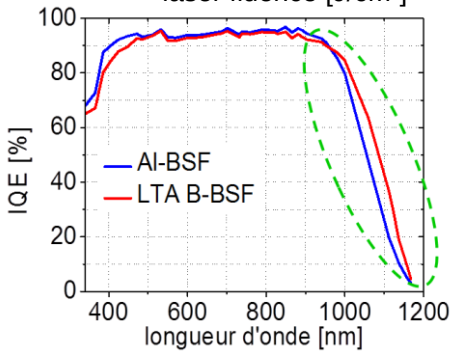
- ✓ **Engineering control of junctions**
  - Single side processing
  - Local XY doping capability
  - Independent optimization of different doped areas
- ✓ **Highly efficient p+ junctions**
  - Excellent activation rate (close to 100%) in box-shaped profile
  - High lifetime (no defects)







- ✓ **Low thermal budgets → no bulk degradation**
- ✓ **+0.3% efficiency achieved vs Al-BSF standard cell**



[B. Paviet-Salomon et al., Proc. of the 2nd Silicon PV, Belgium, 2012]

Summary – LTA : a 3D enabling annealing process

- **Cost and complexity of 2D scaling are moving devices design to 3D**
- **Ultra-fast annealing with the right duration is required**
- **Right wavelength selection is key to process integration success**
- **Successful integration of 3D Devices is today proven**
  - ❖ Vertical 3D IGBT and Power Diodes
  - ❖ Backside CMOS Imaging Sensors
  - ❖ 3D Memories (Vertical channel & Emerging)
  - ❖ Applicable to various More than Moore Semi applications
- **PV application development is promising**
  - ❖ Silicidation for front side copper contacts
  - ❖ Boron diffusion & activation for BSF or backside emitters
  - ❖ Phosphorus diffusion & activation for Selective emitters
  - ❖ TCO anneal

Thanks for your attention!

Supporting « More than Moore » processes