A Review of IBS-related Papers at IIT12

Michael Current: Current Scientific
(Frank Torregrossa: IBS)

1. PIII process for finFets, FDSOI, nano-wires
2. PIII for USJ in InGaAs
3. Formation of Si nano-crystals for EEPROM
4. PIII gettering for poly-Si PV cells

http://www.ion-beam-services.com/
IBS co-authored Papers at IIT12

9:00 Invited

Residual structural defects in highly activated implanted USJs by advanced processes: millisecond annealing and plasma implants
F. Cristiano1, Z. Essa2, Y. Qu1, Y. Spiegel1, F. Torregrosa4, P. Bouleuc2, C. Tavernier2, O. Cojocaru3, D. Blavette4, D. Mangelinck5, and P. F. Fazzini6
1CNRS-LAAS, University of Toulouse, France, 2STMicroelectronics, France, 3CEMES-CNRS, France, 4IBS, France, 5Max-Planck-Institut für Eisenforschung, Germany, 6GPM-UMR-CNRS, Université de Rouen, France, 7Université Paul Cézanne, France, 8LPCNO-INSIA, France

O16 Fabrication of Si nanocrystals in thin SiO2 layers by Plasma Immersion Ion Implantation followed by RTA, application to flash memories
Y. Spiegel1, C. Bonafos2, A. Siaoui1, F. Torregrosa4, J. Groenen2, S. Bhabani5, G. Ben-Assayag5, and P. Normand6
1IBS, France, 2CEMES-CNRS, France, 3InESS, France, 4IMEL/NCSR, Greece

O17 Low cost purification of multicrystalline silicon by Plasma Immersion Ion Implantation (PIII)
El Amin Kouadri Boudjeltia1, Hasnna Etienne2, Thomas Michel2, Marie-France Barthe2, Caroline Andreazza2, Roland Benoli3, Gabrielle Regula3, and Esidor Ntsozonok4
1CEMHIT, France, 2IBS, France, 3CRMO, France, 4IM2NP, France

O47 BF3 PIII modeling: implantation, amorphization and diffusion
Z. Essa1,2, F. Cristiano1, Y. Spiegel1, P. Bouleuc2, M. Quilec4, N. Taleb2, A. Burenkov5, M. Hackenberg5, E. Bedel-Pereira5, V. Mortet1, F. Torregrosa4, and C. Tavernier1
1STMicroelectronics France, 2LAAS-CNRS France, 3IBS, France, 4Proton Analysis, France, 5Fraunhofer IISB Germany

O57 Plasma immersion ion implantation for sub 22nm node devices: FD-SOI and Trigate Nano-wire
J. Duchang2, F. Milési2, S. Barraud2, F. Gonzatti1, S. Reboh1, F. Mazen1, and F. Torregrosa2
1CEA-LETI, France, 2Ion Beam Services, France

P1-16 Simulation of BF3 Plasma Immersion Ion Implantation into Silicon
A. Burenkov1, A. Hahn1, Y. Spiegel2, H. Etienne2, and F. Torregrosa2
1Fraunhofer Institute for Integrated Systems and Device Technology, Germany, 2Ion Beam Services, France

P2-30 Application of Plasma Immersion Ion Implantation for next generation devices: FinFet and III-V channel CMOS
F. Torregrosa4, Wei-Yip Loh2, Y. Spiegel1, Chris Hobbs2, H. Etienne1, Richard Hill2, Wei-e Wang6, and Paul Kirsch3
1IBS, France, 2SEMATECH, U.S.A.
IBS, Ion Beam Services

25 years of Ion Implant Expertise

• Created in 1987, HQ in France
  – Subsidiaries in UK, SG
  – Worldwide Offices and sales reps

• 3 Business Units
  – Doping & Components
  – Equipment & Services
  – PULSION
IMC-200/400 Ion Implanter

Options for hot (500 C) and cold (-150 C) implants

200 or 400 kV terminal
100, 125, 150 mm wafers
*Modern electronics*
Many options
IMC-200/400 : Easy to Use

- Intuitive and easy to use interface
  - Touchscreen, mouse or keyboard
  - Live error reports
  - Maintenance routines
  - Datalogging, mass spectrum, interlocks, ...
IMC-200/400 : Easy to Maintain

• Simple design, easy troubleshooting
  – Minimum cabling (networked communication)
  – Self-diagnosis electronics
  – Manufacturing documentation provided

• Very little dependence on IBS for spare parts !!
  – Electronics/Electrical parts available at any electronics dealer
  – Parts available for 15+ years, with ascending compatibility
  – Widely used PLC & electronics package

• Direct modem support for fast assessments
  – Remote troubleshooting
  – Uploads/Downloads/Updates
# PULSION® configurations

<table>
<thead>
<tr>
<th>PULSION nano</th>
<th>PULSION Auto-loading</th>
<th>PULSION HP Auto-loading</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
<tr>
<td>Manual loading 1 chamber</td>
<td>Auto loading 1-2 chambers</td>
<td>Auto loading 1-4 chambers</td>
</tr>
<tr>
<td>Labs</td>
<td>Device qualification</td>
<td>Production</td>
</tr>
</tbody>
</table>
PULSION®: Plasma Immersion Ion Implantation

High Pressure, very high density plasma:
Remote ICP plasma source

Dual Region Chamber Design (DRC)

Low Pressure, high density plasma

Wafer

Rotating chuck for better uniformity

Continuous or pulsed plasma

Features to Improve Uniformity

Longer distance to improve homogeneity

Plasma Sheath

PULSION® Versatile low-flow configuration, 0-30 kV standard (40kV option)
Pulsion PIII: High Throughputs

Low-cost, low-footprint tool for high-dose (>5e14) and low-energy (<30 kV) process.

Dopants: (B, As, P, etc.)
- Enhanced silicide contact Rc.
- Raised SD epi doping
- Shallow junctions
- PV cell doping
- Trench and fin doping

Non-dopants: (Ge, Si, N, F, S, Al, etc.)
- Amorphization for laser anneals, stain, etc.
- High-k dielectric Vth tuning
- Silicide phase stabilization
- Stress memorization
- PR “freezing” for dual-litho
- Si-nano crystals for EEPROM cells
Plasma Immersion Ion Implantation For Sub 22nm Node Devices: FD-SOI and Trigate Nano-Wire

J.Duchaine*, F. Milési+, R. Coquant†, S.Barraud+, F. Gonzatti+, S. Reboh+, F. Mazen+, F.Torregrosa*

* CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France
† IBS, ZI Peynier- Rousset, Avenue Gaston Imbert prolongée, 13 790 Peynier, France
‡ STMicroelectronics, 850, rue J. Monnet, 38926 Crolles, France
Fully-Depleted Channels

Planar FD-SOI

Double Gate

Tri Gate (Lg~H) / FinFET (H>>Lg)

Nano Wire

28nm  20nm  14nm  11nm  8nm
Planar FD-SOI: Direct transfer to PIII

Direct, non-optimized, transfer of SD implant for SDC and SDE matches beamline.

Isat as function of $\Delta V_t$ for different $L_g$ & $W=10 \mu m$
Tri-Gate finFET

Excellent CMOS transistor characteristics.

PIII give improves Ion; +11% for nMOS, +18% for pMOS
Low contact resistance, conformal fin doping.
PIII AsH₃ Doping of FinFETs

Pulsion PIII provides good sidewall doping.

Cap during anneal inhibits As outdiffusion.

Post anneal doping nearly uniform (conformal) in depth by poly-SIMS.
PIII for In$_{53}$Ga$_{47}$As Doping

Pulsion PIII process provides high-activation, shallow junction Si doping of InGaAs.
**Formation of Si nano-crystals for FLASH**

**Fabrication Of Si Nanocrystals In Thin SiO₂ Layers By Plasma Immersion Ion Implantation Followed By Thermal Annealing**

Y. Spiegel¹, C. Bonafos², A. Slaoui³, F. Torregrosa¹, J. Groenen², S. Bhabani³, G. BenAssayag², and P. Normand⁴

¹IBS, France,
²CEMES-CNRS, France,
³InESS, France,
⁴IMEL/NCSR, Greece
Nano-Si Floating Gates

Replace solid poly-Si floating EEPROM gate with *distributed* layer of Si nano-crystals.

Process needs (1) High Si⁺ dose (2) low energy. Ideal for Pulsion use.

- **Thin layers**: 5-10 nm
- **Ultra Low Energy**: 0.5-5 keV
- **Dose**: $5 \times 10^{15} - 2 \times 10^{16}$ ions/cm² $\rightarrow$ About 10 at. %
- **High temperature annealing** (conventionnal N₂ or RTA) $\rightarrow$ phase separation

Loss nearby the storage node

Local data loss

Si⁺

annealing
Process Optimization

• Si implantation with SiF$_4$ / SiH$_4$ / H$_2$ mixtures
• In Situ Mass spectrometry analysis

Ex. 0.75 SiF$_4$/0.25 H$_2$ mixture

Targets
- Maximization of Si/F ratio
- Minimization of H$_2$ and HF

Implantation conditions

<table>
<thead>
<tr>
<th></th>
<th>5$^E$-4 to 1$^E$-2 mBar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td></td>
</tr>
<tr>
<td>Gas flow</td>
<td>2 to 10 sccm</td>
</tr>
<tr>
<td>Aceleration voltage</td>
<td>0.5 to 5 kV</td>
</tr>
<tr>
<td>Dose</td>
<td>1E16 to 7E16 at/cm$^2$</td>
</tr>
</tbody>
</table>

Tuning oxide thickness to locate Si NCs near channel

10 nm SiO$_2$  7.5 nm SiO$_2$  6 nm SiO$_2$

NCs  TO

10 nm

TO=8.3 nm  TO=4 nm  TO=2.4 nm
Single memory cells for EEPROM-like applications

Excellent read/write and data retention characteristics.

• Long time extrapolation: 10 years retention at 85°C, 0.42V (RT, 0.6V)
Low cost purification of multicrystalline silicon by Plasma Immersion Ion Implantation (PIII)


Monocrystalline silicon
- Good quality
- Efficiency: 15-25%
- Expensive

Multicrystalline silicon
- Less expensive
- Intermediate quality
- Efficiency: 12-20%
PV Poly-Si is full of Metals

Multi-crystalline Si PV cells have high metal content.

High metal content kills carrier lifetime and limits PV efficiency.

How to reduce metal levels (raise mc-Si efficiency) at modest cost?
Hydrogen Implants for Voids

Implantation: PIII
20kV, $5 \times 10^{16}$ H/cm$^2$
Distributed voids

Implantation: Beamline
20keV, $5 \times 10^{16}$ H/cm$^2$
Delamination of Si
Metals are Gettered to Voids

Annealing at 1000 C getters Cu and Ni to the H-created voids.

Process concept:
- Implant high-dose H with PIII.
- Anneal at 800 C to form voids.
- Anneal at 1000 C to getter metals.
- Etch off top 100 nm surface layer.
- Process higher efficiency MC-PV.

Process less effective for Fe and Cr (??).
A Review of IBS-related Papers at IIT12

Michael Current: Current Scientific (Frank Torregrossa: IBS)

1. PIII process for finFets, FDSOI, nano-wires
2. PIII for USJ in InGaAs
3. Formation of Si nano-crystals for EEPROM
4. PIII gettering for poly-Si PV cells

http://www.ion-beam-services.com/