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the total ion implantation solution

A Review of IBS-related Papers at IIT12

Michael Current: Current Scientific
(Frank Torregrossa: IBS)

1.PIII process for finFets, FDSOI, nano-wires
2. PIII for USJ in InGaAs
3. Formation of Si nano-crystals for EEPROM
4. PIII gettering for poly-Si PV cells

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IIT2012

IBS co-authored Papers at IIT12

9:00 *Invited* I8 **Residual structural defects in highly activated implanted USJs by advanced processes: millisecond annealing and plasma implants**
F. Cristiano[1], Z. Essa[1,2], Y. Qiu[1,3], Y. Spiegel[4], F. Torregrosa[4], P.Boulenc[2], C. Tavernier[2], O. Cojocaru[5], D. Blavette[6], D. Mangelinck[7], and P. F. Fazzini[8]
[1]CNRS-LAAS, University of Toulouse, France, [2]STMicroelectronics, France, [3]CEMES-CNRS, France, [4]IBS, France, [5]Max-Planck-Institut für Eisenforschung, Germany; [6]GPM-UMR-CNRS, Université de Rouen, France; [7]Université Paul Cézanne, France; [8]LPCNO-INSA, France

O16 **Fabrication of Si nanocrystals in thin SiO_2 layers by Plasma Immersion Ion Implantation followed by RTA, application to flash memories**
Y. Spiegel[1], C. Bonafos[2], A. Slaoui[3], F. Torregrosa[1], J. Groenen[2], S. Bhabani[3], G. Ben-Assayag[2], and P. Normand[4]
[1]IBS, France, [2]CEMES-CNRS, France, [3]InESS, France, [4]IMEL/NCSRD, Greece

O17 **Low cost purification of multicrystalline silicon by Plasma Immersion Ion Implantation (PIII)**
El Amin Kouadri Boudjelthia[1], Hasnaa Etienne[2], Thomas Michel[2], Marie-France *Barthe[1], Caroline Andreazza[3], Roland Benoit[3], Gabrielle Regula[4], and Esidor Ntsoenzok[1]*
[1]CEMHTI, France, [2]IBS, France, [3]CRMD, France, [4]IM2NP, France

O47 **BF3 PIII modeling: implantation, amorphization and diffusion**
Z. Essa[1,2], F. Cristiano[2], Y. Spigel[3], P. Boulenc[1], M. Quillec[4], N. Taleb[4], A. Burenkov[5], M. Hackenberg[5], E. Bedel-Pereira[2] , V. Mortet[2] , F. Torregrosa[3], and C. Tavernier[1]
[1]STMicroelectronics France, [2]LAAS-CNRS France, [3]IBS, France, [4]Probion Analysis, France, [5]Fraunhofer IISB Germany

O57 **Plasma immersion ion implantation for sub 22nm node devices: FD-SOI and Trigate Nano-wire**
J. Duchaine[2], F. Milési[1], S. Barraud[1], F. Gonzatti[1], S. Reboh[1], F. Mazen[1], and, F. Torregrosa[2]
[1]CEA-LETI, France, [2]Ion Beam Services, France

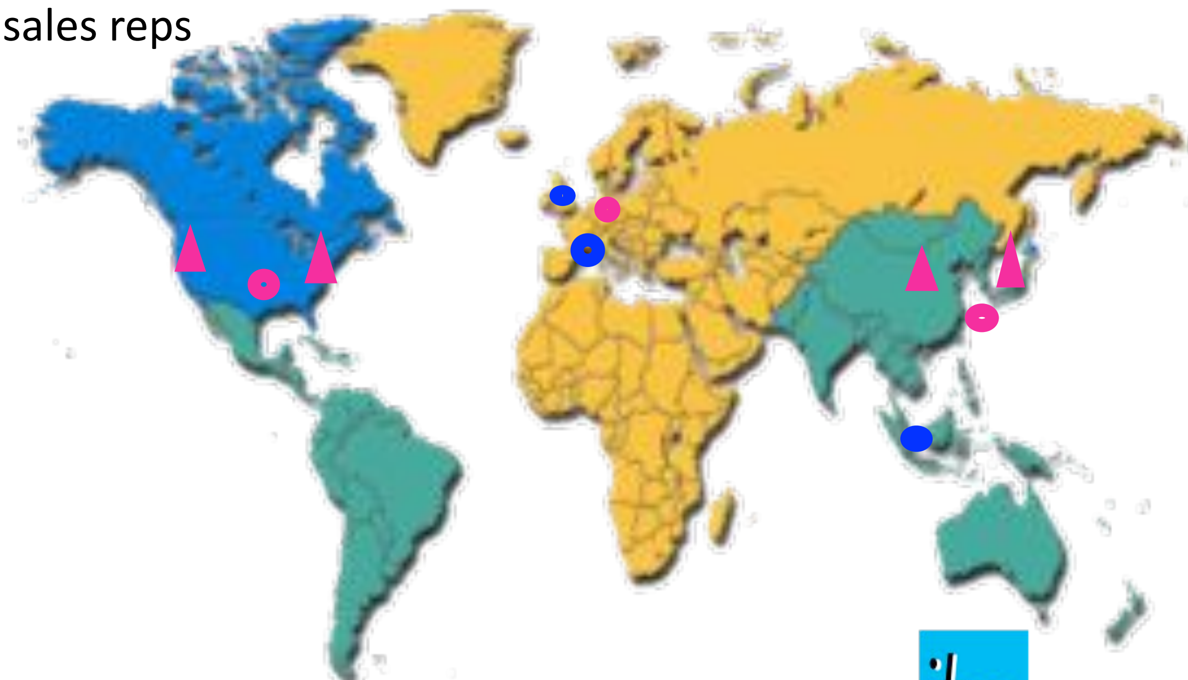
P1-16 **Simulation of BF_3 Plasma Immersion Ion Implantation into Silicon**
A. Burenkov[1], A. Hahn[1], Y. Spiegel[2], H. Etienne[2], and F. Torregrosa[2]
[1]Fraunhofer Institute for Integrated Systems and Device Technology, Germany, [2]Ion Beam Services, France

P2-30 **Application of Plasma Immersion Ion Implantation for next generation devices: FinFet and III-V channel CMOS**
F. Torregrosa[1], Wei-Yip Loh[2], Y. Spiegel[1], Chris Hobbs[2], H. Etienne[1], Richard Hill[2], Wei-e Wang[2], and Paul Kirsch[2]
[1]IBS, France, [2]SEMATECH, U.S.A.

IBS, Ion Beam Services

25 years of Ion Implant Expertise

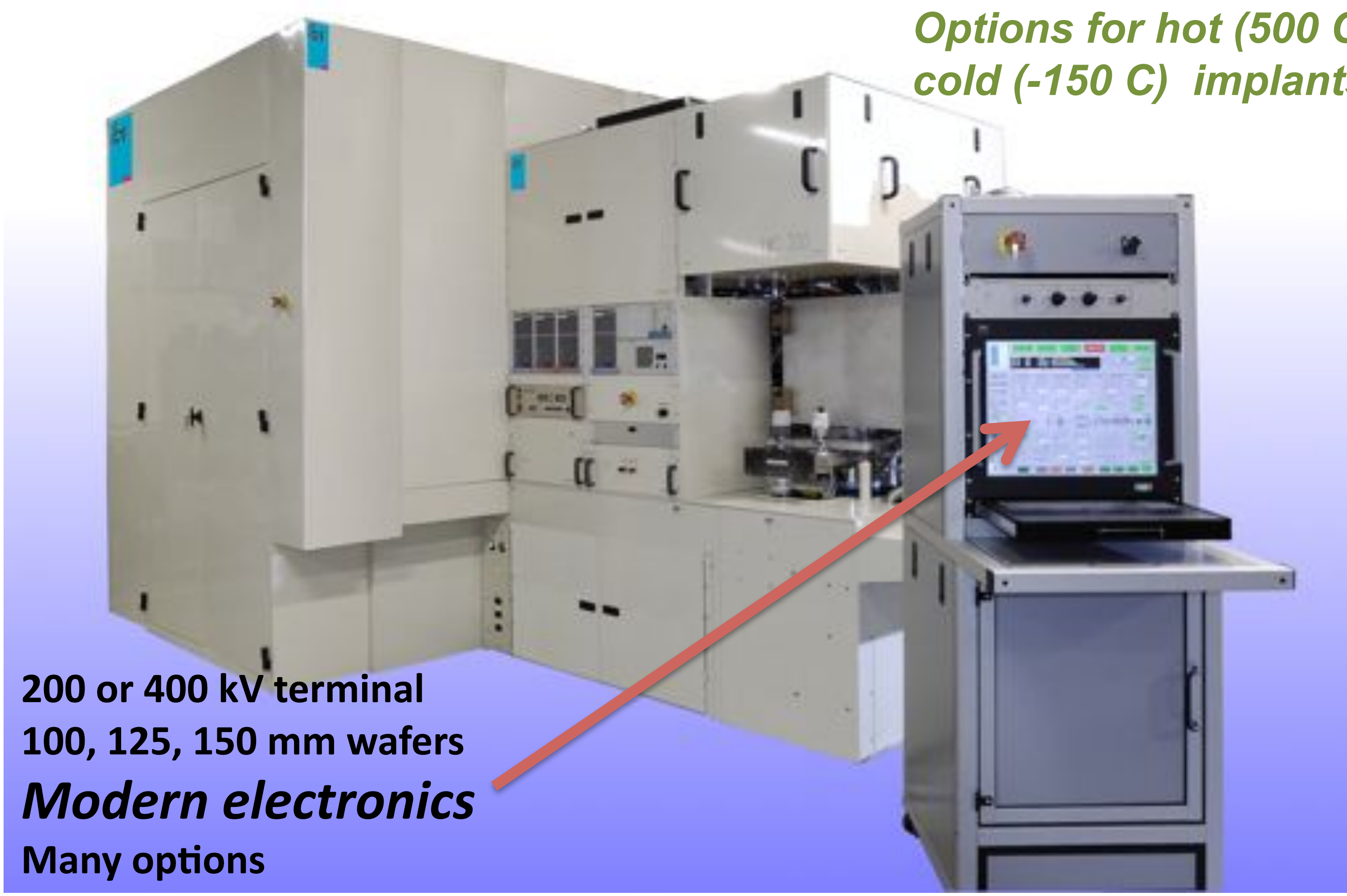
- **Created in 1987, HQ in France**
  - Subsidiaries in UK, SG
  - Worldwide Offices and sales reps



- **3 Business Units**
  - Doping & Components
  - Equipment & Services
  - PULSION

IMC-200/400 Ion Implanter

Options for hot (500 C) and cold (-150 C) implants



200 or 400 kV terminal

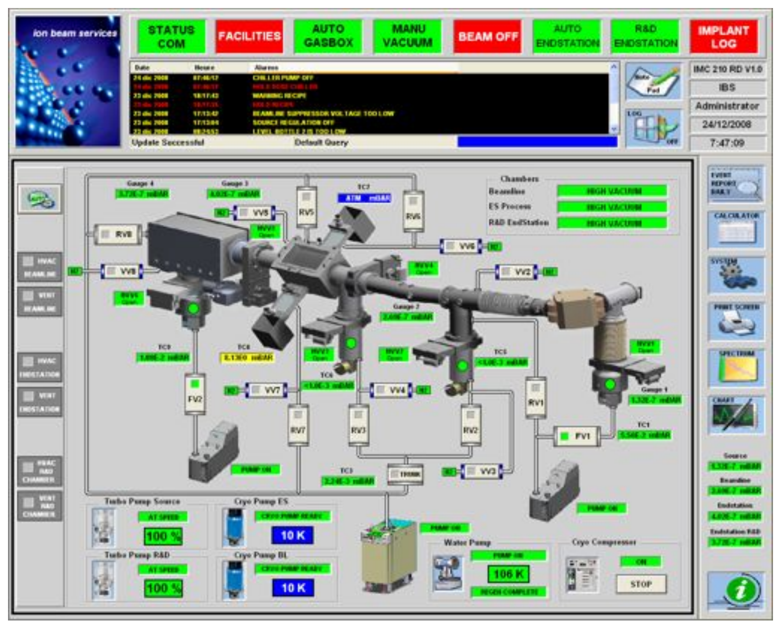
100, 125, 150 mm wafers

Modern electronics

Many options

IMC-200/400 : Easy to Use

- **Intuitive and easy to use interface**
  - Touchscreen, mouse or keyboard
  - Live error reports
  - Maintenance routines
  - Datalogging, mass spectrum, interlocks, …



IMC-200/400 : Easy to Maintain

- **Simple design, easy troubleshooting**
  - Minimum cabling (networked communication)
  - Self-diagnosis electronics
  - Manufacturing documentation provided

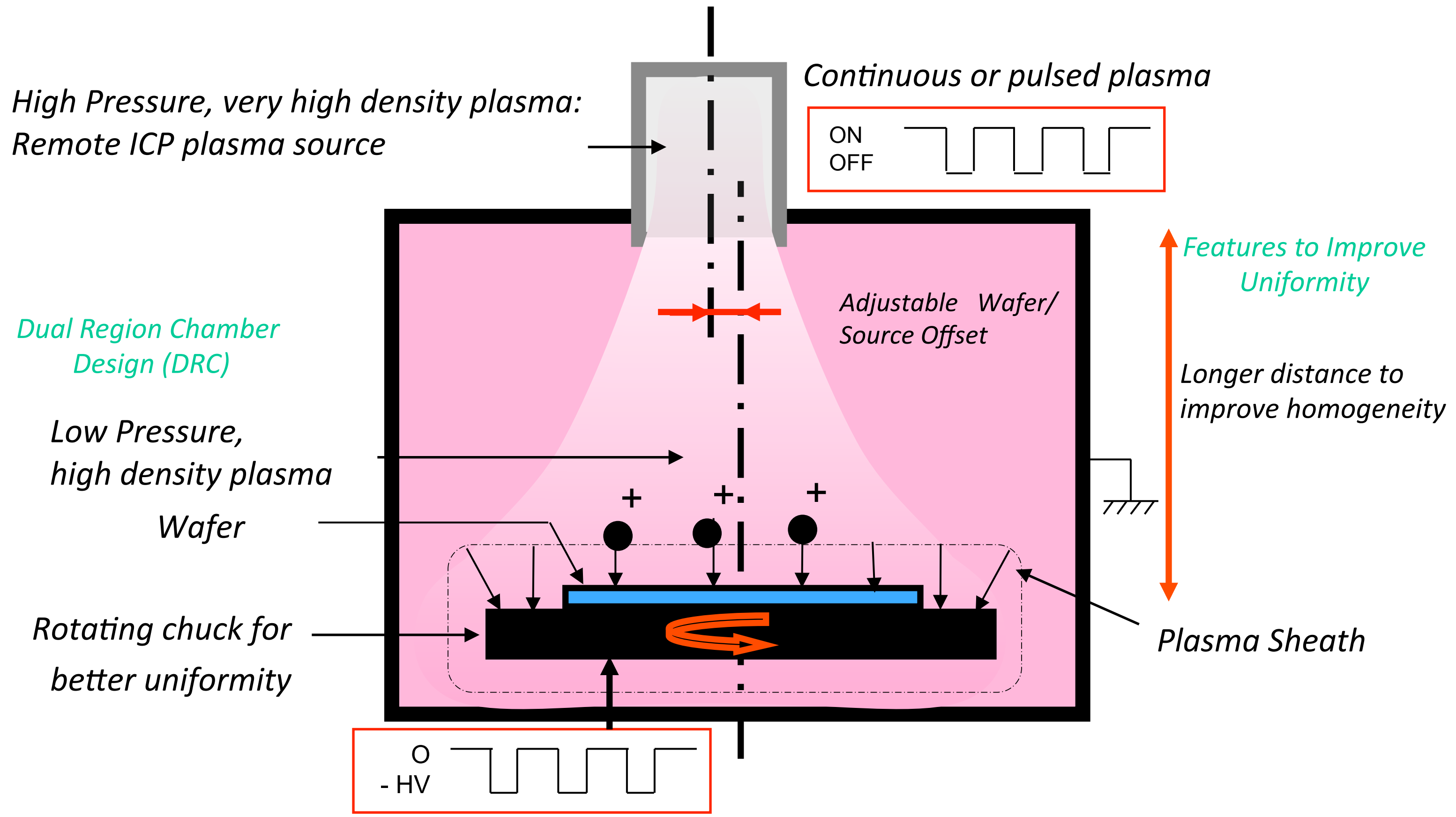
- ***Very little dependence on IBS for spare parts !!***
  - Electronics/Electrical parts available at any electronics dealer
  - Parts available for 15+ years, with ascending compatibility
  - Widely used PLC & electronics package

- **Direct modem support for fast assessments**
  - Remote troubleshooting
  - Uploads/Downloads/Updates

PULSION® configurations

PULSION nano	PULSION Auto-loading	PULSION HP Auto-loading
 		
Manual loading 1 chamber	Auto loading 1-2 chambers	Auto loading 1-4 chambers
Labs	Device qualification	Production

PULSION® : Plasma Immersion Ion Implantation



PULSION® Versatile low-flow configuration, 0-30 kV standard (40kV option)

Pulsion PIII: High Throughputs

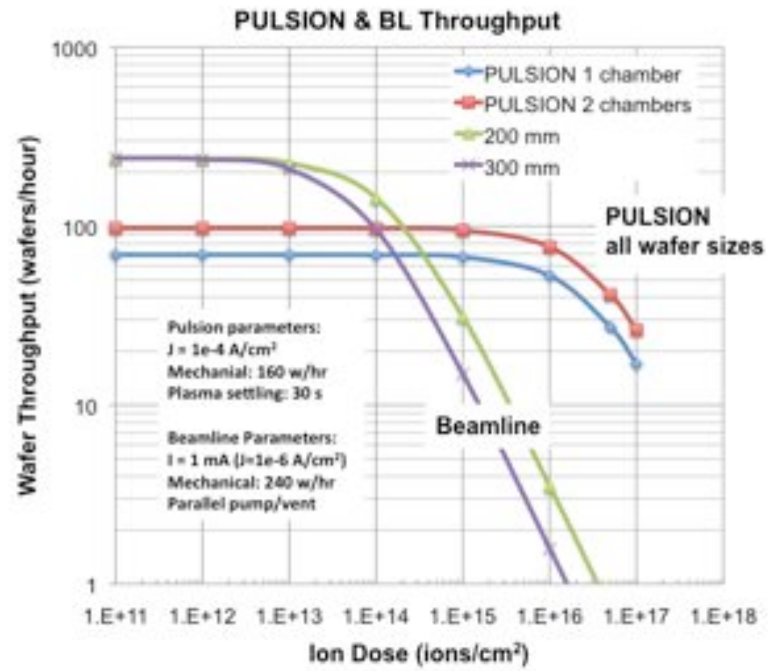
Low-cost, low-footprint tool for high-dose (>5e14) and low-energy (<30 kV) process.

Dopants: (B, As, P, etc.)

- Enhanced silicide contact Rc.
- Raised SD epi doping
- Shallow junctions
- PV cell doping
- Trench and fin doping

Non-dopants: (Ge, Si, N, F, S, Al, etc.)

- Amorphization for laser anneals, stain, etc.
- High-k dielectric Vth tuning
- Silicide phase stabilization
- Stress memorization
- PR “freezing” for dual-litho
- Si-nano crystals for EEPROM cells



Plasma Immersion Ion Implantation For Sub 22nm Node Devices: FD-SOI and Trigate Nano-Wire

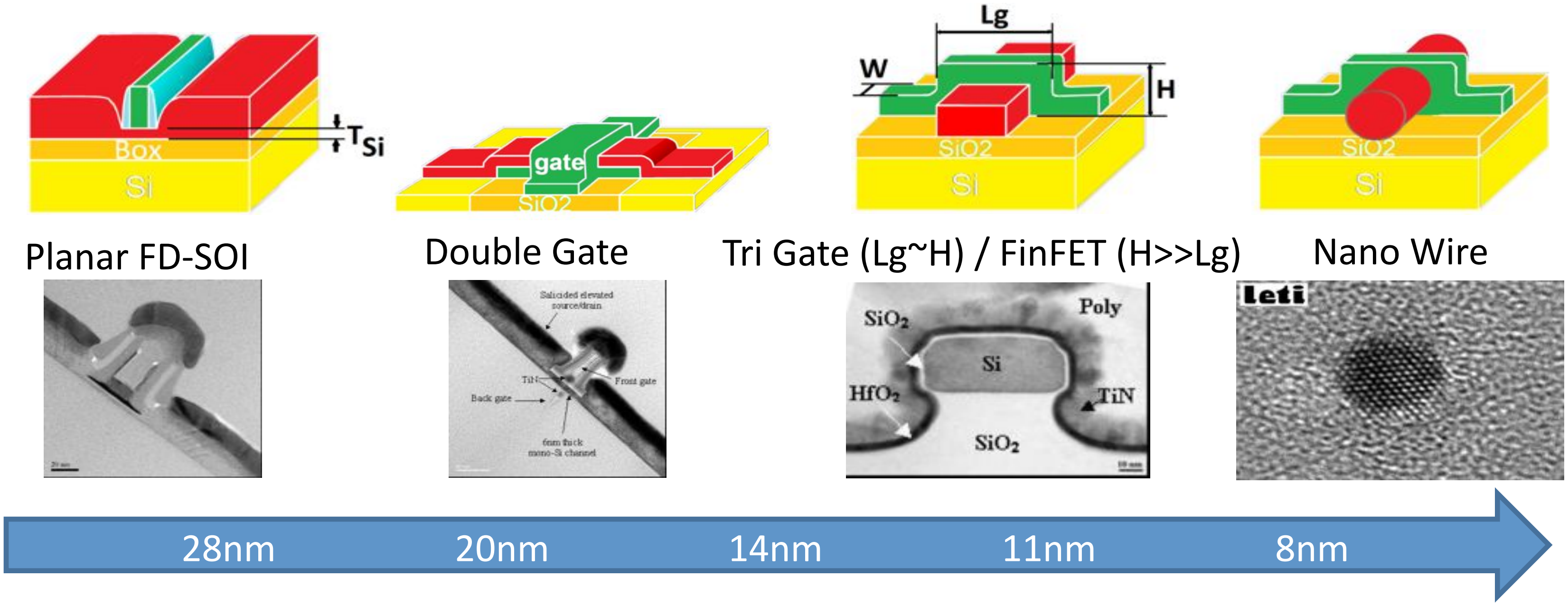
J.Duchaine[*], F. Milési[+], R. Coquant[-], S.Barraud[+], F. Gonzatti[+], S. Reboh[+], F. Mazen[+], F.Torregrosa[*]

[+] *CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France*

[*] *IBS, ZI Peynier- Rousset, Avenue Gaston Imbert prolongée, 13 790 Peynier, France*

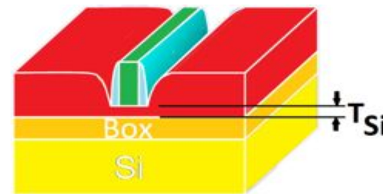
[-] *STMicroelectronics, 850, rue J. Monnet, 38926 Crolles, France*

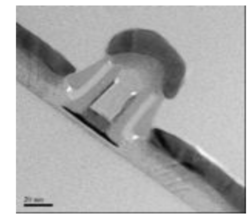
Fully-Depleted Channels

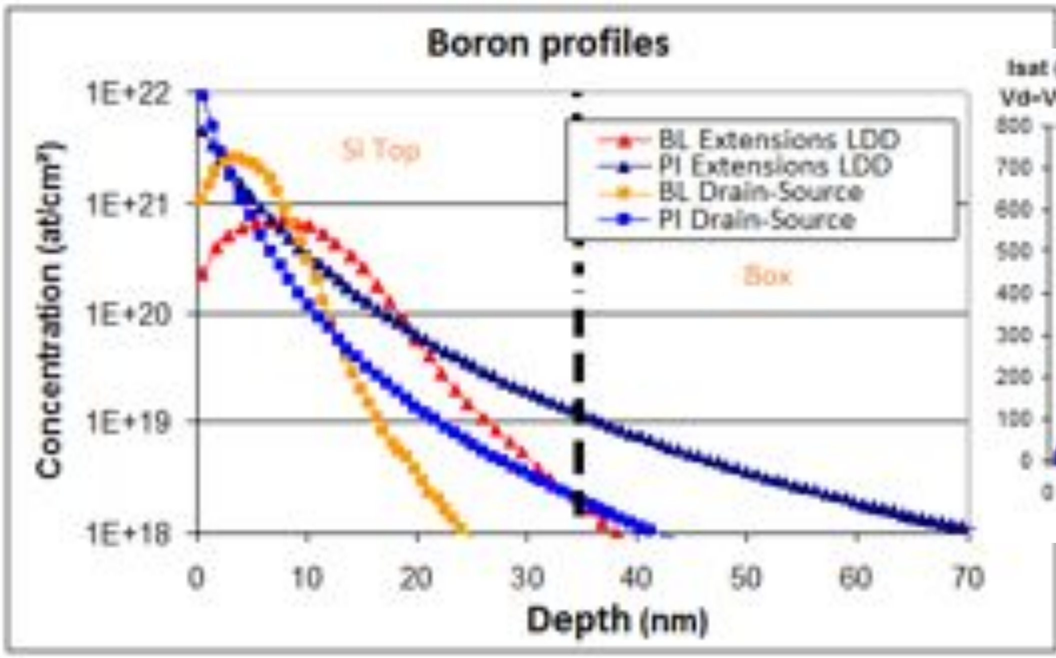


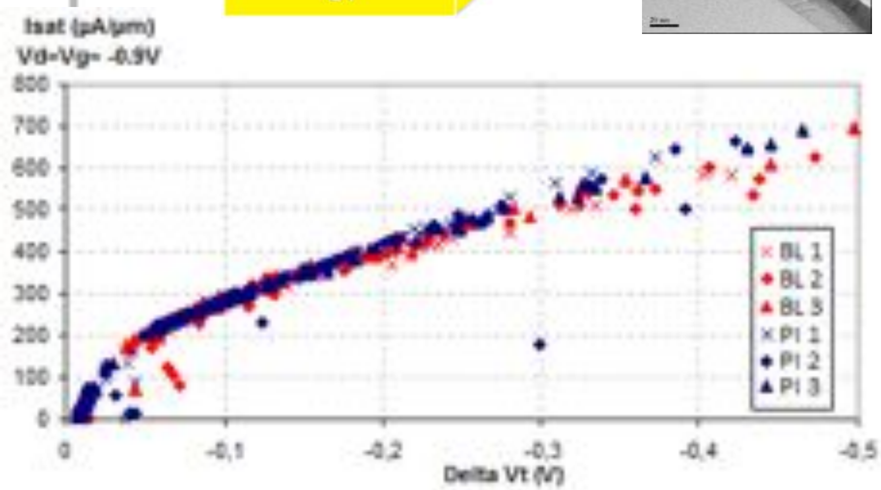
Planar FD-SOI: Direct transfer to PIII

Direct, non-optomized, transfer of SD implant for SDC and SDE matches beamline.



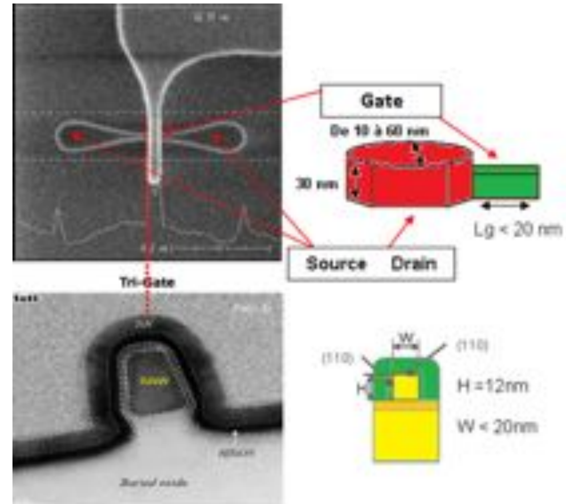






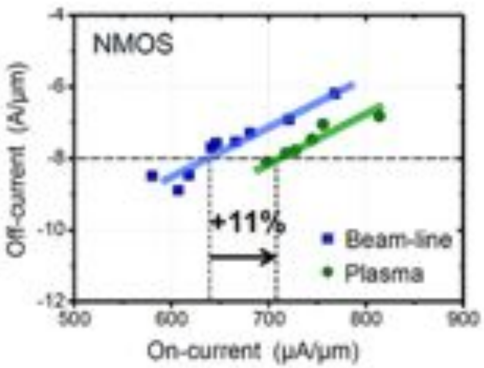
Isat as function of ΔVt for differents Lg & W=10µm

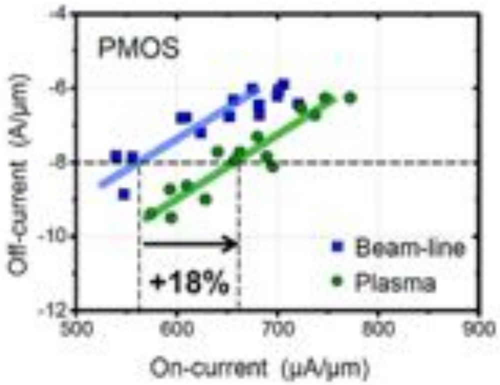
Tri-Gate finFET

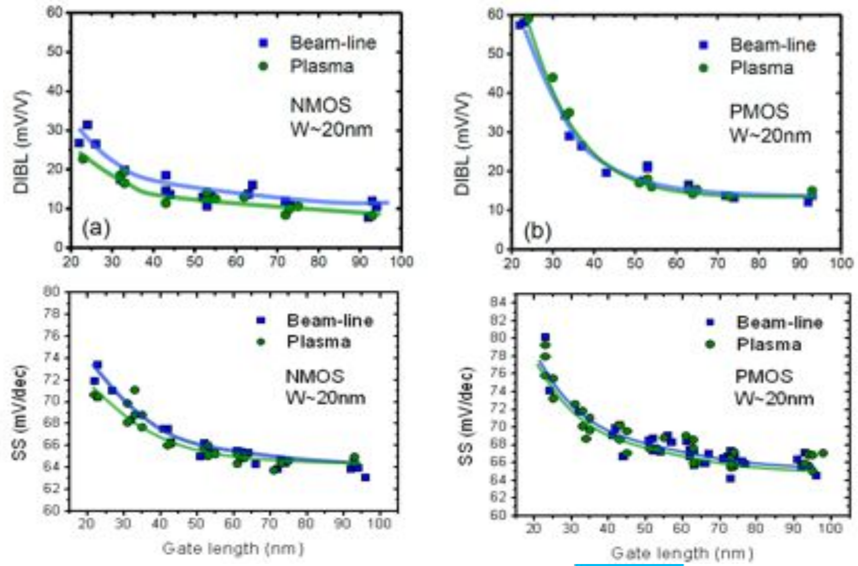


Excellent CMOS transistor characteristics.

PIII give improves Ion; +11% for nMOS, +18% for pMOS
Low contact resistance, conformal fin doping.





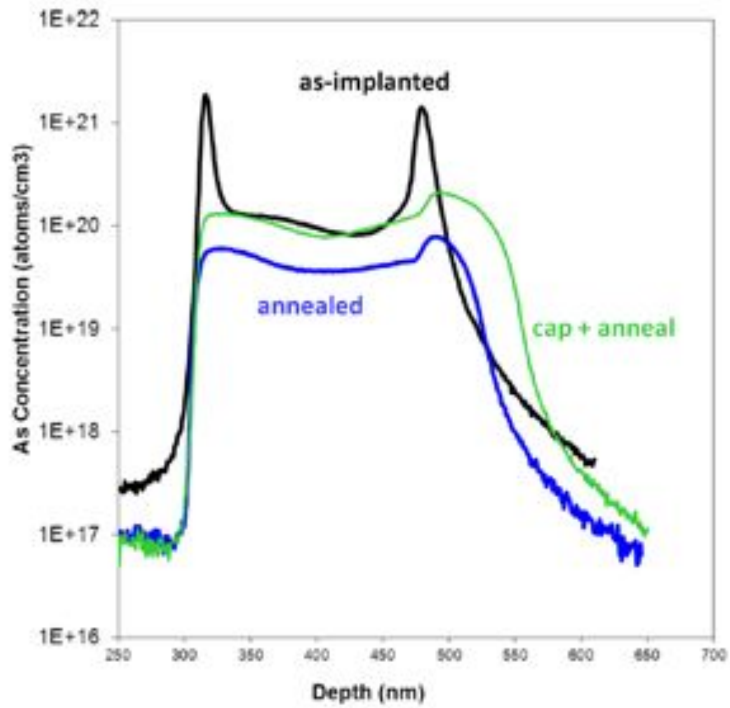


PIII AsH_3 Doping of FinFETs

Pulsion PIII provides good sidewall doping.

Cap during anneal inhibits As outdiffusion.

Post anneal doping nearly uniform (conformal) in depth by poly-SIMS.



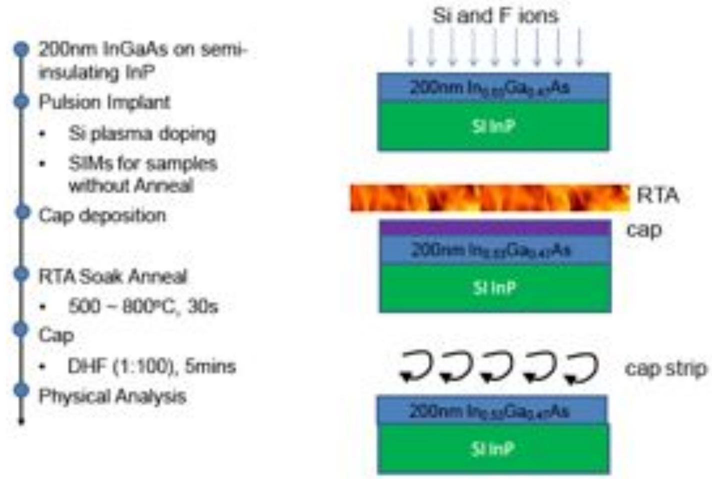
APPLICATION OF PLASMA IMMERSION ION IMPLANTATION FOR NEXT GENERATION DEVICES
FINFET AND III-V CHANNEL CMOS

F. Torregrosa (1), Wei-Yip Loh (2), Y. Spiegel (1), Chris Hobbs (2) H. Etienne (1), Richard Hill (2), Wei-e Wang (2), Paul Kirsch (2)
(1) IBS, Rue G Imbert Prolongée, ZI Peynier-Rousset, 13790 Peynier, France
(2) SEMATECH, 257 Fuller Road # 1 Albany, NY 12203, USA

PIII for $In_{53}Ga_{47}As$ Doping

Pulsion PIII process provides high-activation, shallow junction Si doping of InGaAs.

Process Steps for III-V Samples



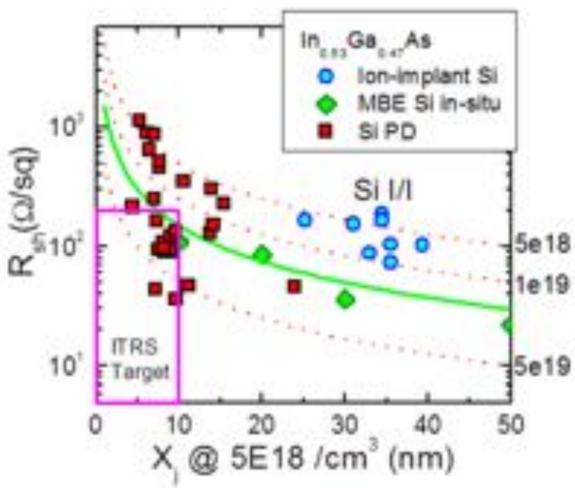
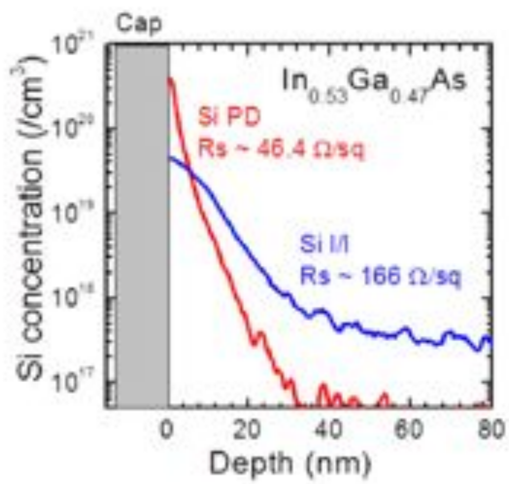


Figure of merit for junction doping in $In_{0.53}Ga_{0.47}As$. Si plasma doping results in significantly shallower junction depth and higher dopant incorporation compared to ion-implantation and in-situ doping technique. Green lines shows the focus of in-situ doping of Si during InGaAs epi deposition.



SIMS profile of Si in InGaAs introduced via Si plasma doping and conventional ion-implantation. Si plasma doping results in very steep abrupt profile with low background doping compared to ion-implantation.

Formation of Si nano-crystals for FLASH

Fabrication Of Si Nanocrystals In Thin SiO_2 Layers By Plasma Immersion Ion Implantation Followed By Thermal Annealing

Y. Spiegel[1], C. Bonafos[2], A. Slaoui[3], F. Torregrosa[1], J. Groenen[2], S. Bhabani[3], G. BenAssayag[2], and P. Normand[4]

[1]*IBS, France,*

[2]*CEMES-CNRS, France,*

[3]*InESS, France,*

[4]*IMEL/NCSRD, Greece*

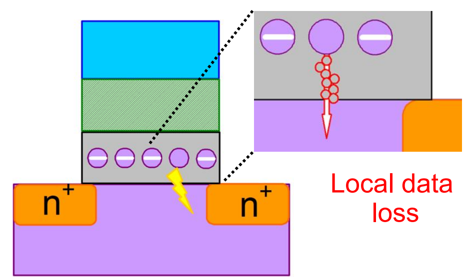
Nano-Si Floating Gates

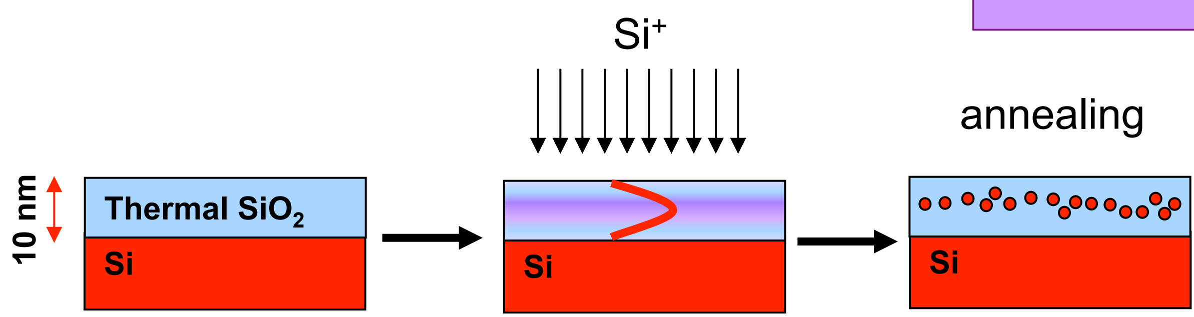
Replace solid poly-Si floating EEPROM gate with *distributed* layer of Si nano-crystals.

Process needs (1) High Si^+ dose (2) low energy.

Ideal for Pulsion use.

Loss nearby the storage node

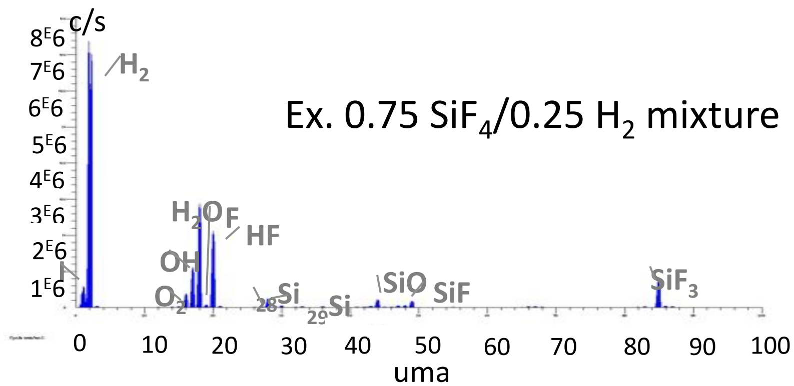




- **Thin layers**: 5-10 nm
- **Ultra Low Energy**: 0.5-5 keV
- **Dose** : $5x10^{15}$-$2x10^{16}$ ions/cm² → About 10 at.%
- **High temperature annealing** (conventionnal N_2 or RTA) → phase separation

Process Optimization

- Si implantation with SiF_4 / SiH_4 / H_2 mixtures
- In Situ Mass spectrometry analysis

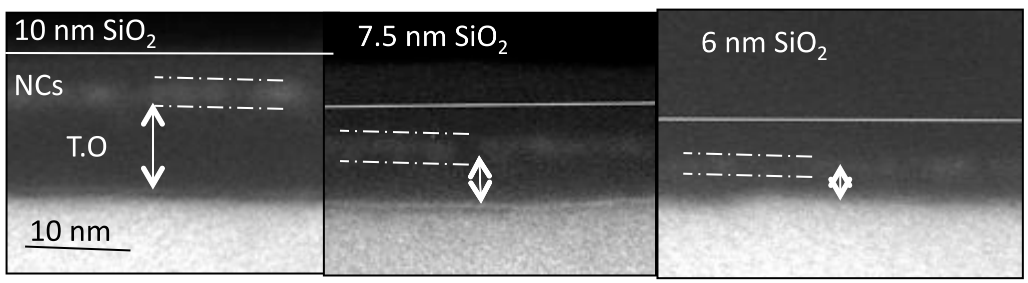


Targets

- **Maximization of Si/F ratio**
- **Minimization of H_2 and HF**

Implantation conditions	
Gas	SiF_4 / SiH_4 / H_2 mixtures
Pressure	5^E-4 to 1^E-2 mBar
Gas flow	2 to 10 sccm
Aceleration voltage	0.5 to 5 kV
Dose	1E16 to 7E16 at/cm²

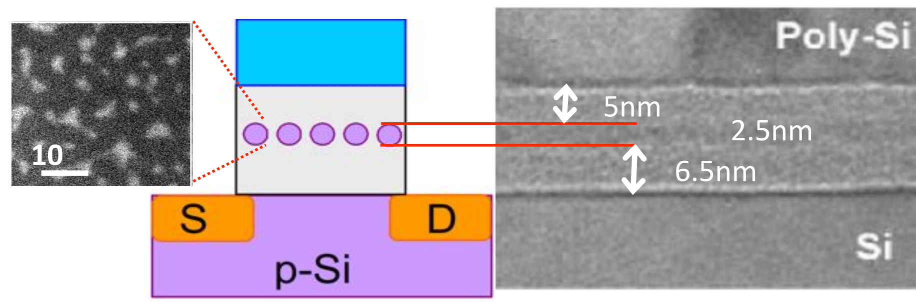
Tuning oxide thickness to locate Si NCs near channel



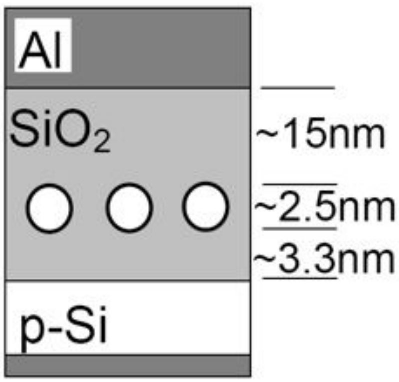
T.O=8.3 nm **T.O=4 nm** **T.O=2.4 nm**

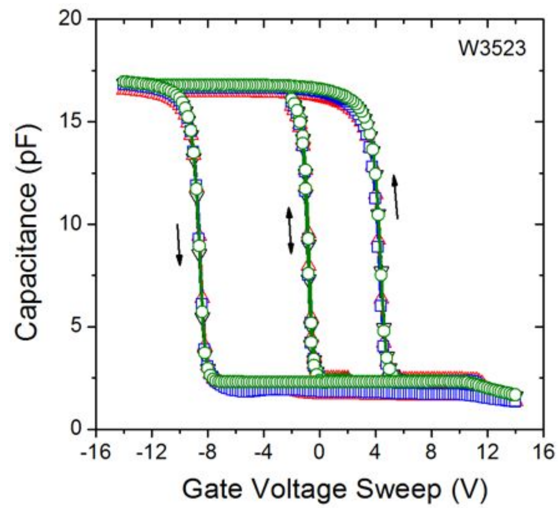
Single memory cells for EEPROM-like applications

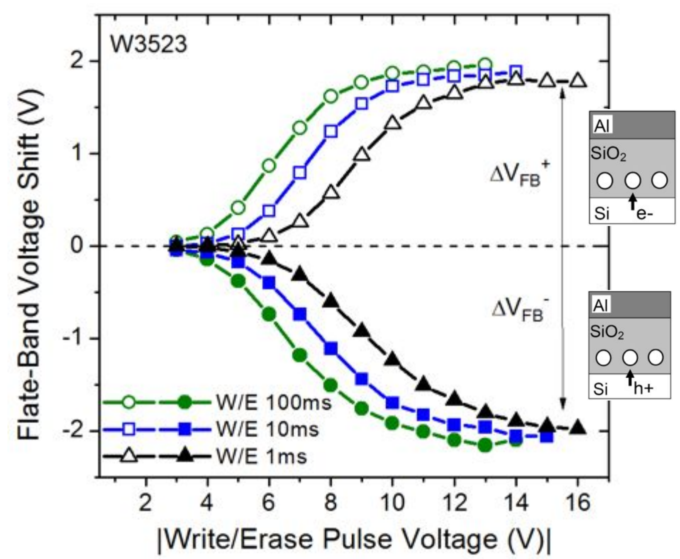
ULE-IBS + oxidizing annealing



Excellent read/write and data retention characteristics.







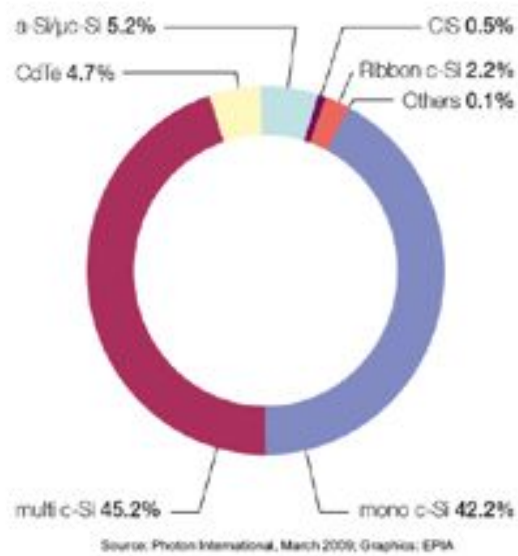
- **Long time extrapolation: 10 years retention at 85°C, 0.42V (RT, 0.6V)**

Low cost purification of multicrystalline silicon by Plasma Immersion Ion Implantation (PIII)

E. A. Kouadri Boudjelthia, *E. Ntsoenzok, G. Regula, R. Benoit, H. Etienne, M. Thomas, M. F. Barthe.*

Monocrystalline silicon
- Good quality
- Efficiency: 15-25%
- Expensive

Multicrystalline silicon
-Less expensive
-Intermediate quality
-Efficiency: 12-20%



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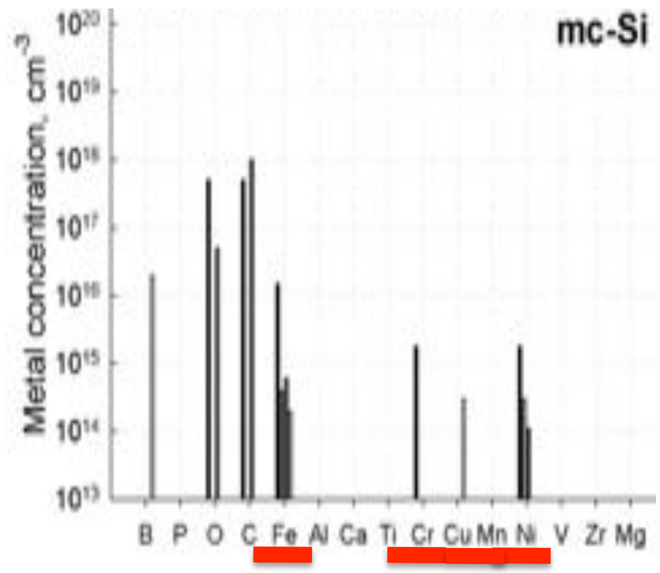
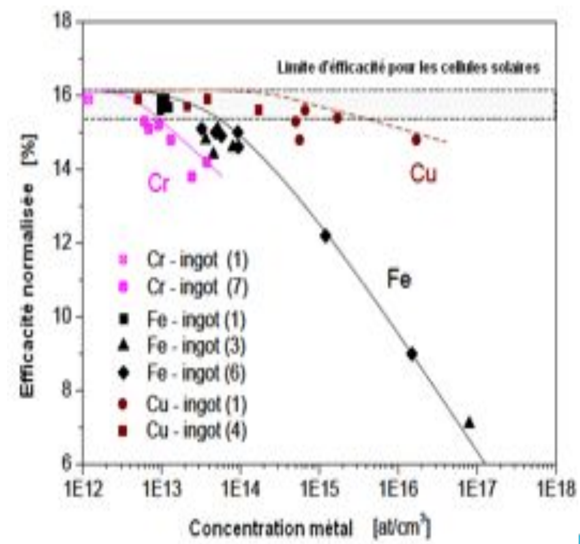
PV Poly-Si is full of Metals



Multi-crystalline Si PV cells have high metal content.

High metal content kills carrier lifetime and limits PV efficiency.

How to reduce metal levels (raise mc-Si efficiency) at modest cost ?



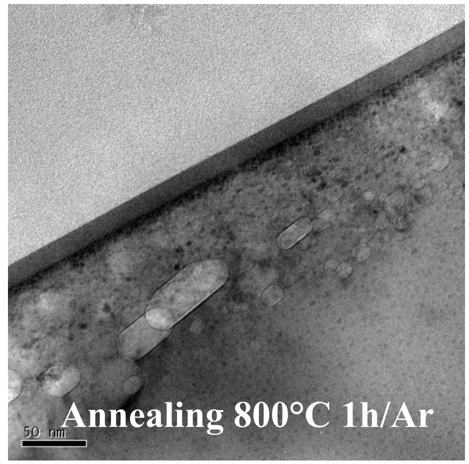
A.A. Istratov et al./ Materials Science and Engineering B 134 (2006) 282-286

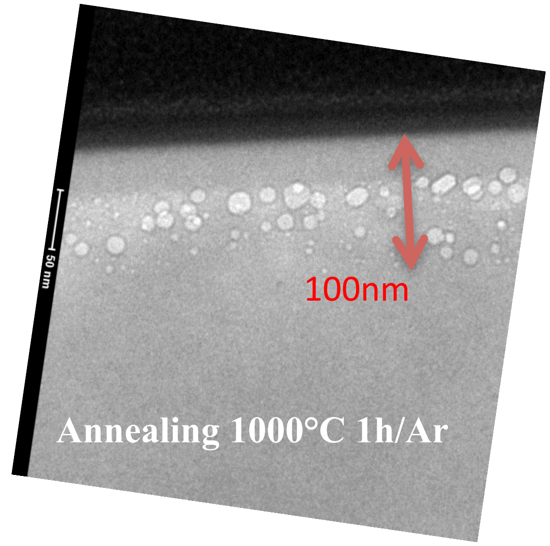
Hydrogen Implants for Voids

TEM

Implantation: PIII
20kV, 5 10^{16} H/cm^2

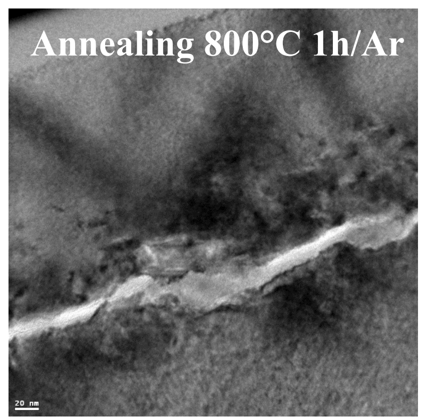
Distributed voids

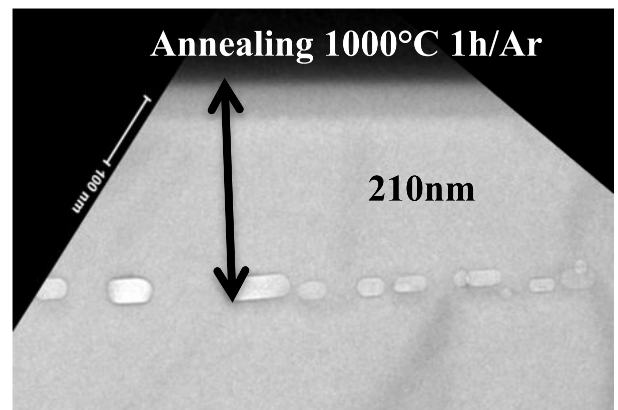




Implantation: Beamline
20keV, 5 10^{16} H/cm^2

Delamination of Si





Metals are Gettered to Voids

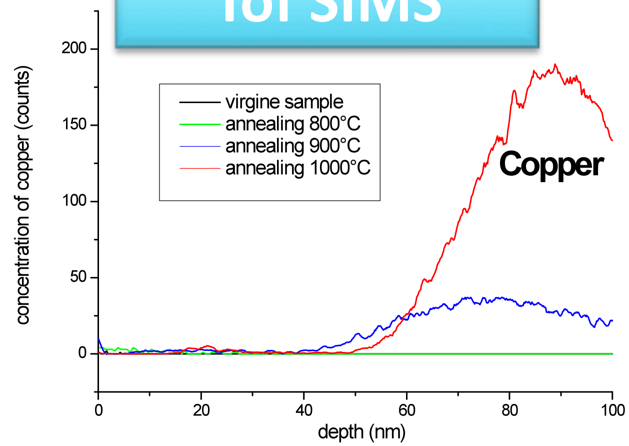
Annealing at 1000 C getters Cu and Ni to the H-created voids.

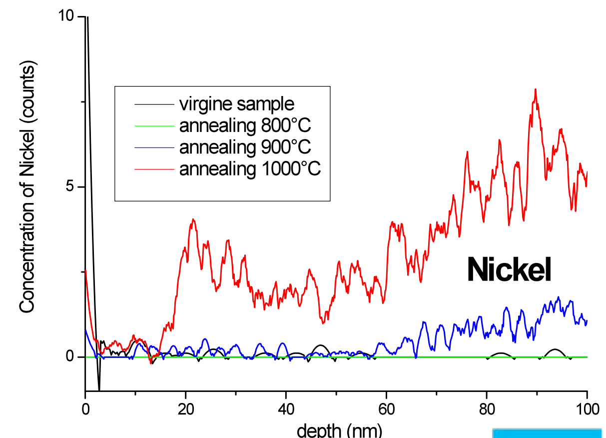
Process concept:

- **Implant high-dose H with PIII.**
- **Anneal at 800 C to form voids.**
- **Anneal at 1000 C to getter metals.**
- **Etch off top 100 nm surface layer.**
- **Process higher efficiency MC-PV.**

Process less effective for Fe and Cr (??).

Tof SIMS





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A Review of IBS-related Papers at IIT12

Michael Current: Current Scientific
(Frank Torregrossa: IBS)

1. *PIII process for finFets, FDSOI, nano-wires*
2. *PIII for USJ in InGaAs*
3. *Formation of Si nano-crystals for EEPROM*
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