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Alloy Composition of 6061 Aluminum

- Silicon minimum 0.4%, maximum 0.8% by weight
- Iron no minimum, maximum 0.7%
- Copper minimum 0.15%, maximum 0.40%
- Manganese no minimum, maximum 0.15%
- Magnesium minimum 0.8%, maximum 1.2%
- Chromium minimum 0.04%, maximum 0.35%
- Zinc no minimum, maximum 0.25%
- Titanium no minimum, maximum 0.15%
- Other elements no more than 0.05% each, 0.15% total
- Remainder Aluminium (95.85%–98.56%)

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PVD Silicon Coating for Implanter Parts

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- The Ion Implant community has used high purity Silicon PVD coatings for implant disk shields, beamline and target chamber parts for over 10 years.
- The basic requirements for our Silicon coatings include:
  - High purity level for Al, Fe, Cr, Cu, Mg, etc.
  - Good Adhesion
  - Smooth surface finish to eliminate particles.
  - Low wear (surface erosion) during customer operation
- In 2009, Factory Integrated Solutions (FIS) began Silicon coating services, located within CORE Systems’s main facility in Sunnyvale, CA
- This capability has resulted in:
  - Improved predictability of coating cycle times
  - Minimized rework and improved deliveries
  - Provided the means for continuous improvement

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FIS PVD vs PECVD

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- FIS and CORE Systems conducted a careful study of the various attributes of both PECVD and PVD and concluded that PVD was the preferred choice for Silicon coating of implanter parts
- This choice was based on the following:
  - Equivalent or better elemental purity with no surface voids
  - Lower cost by eliminating expensive facility systems to handle hazardous materials
  - Equivalent or better wear, adhesion and particle performance
  - Better operational flexibility
- The comprehensive disk coating paper **(1)** done by Eaton (Axcelis) shows data from PECVD, PVD, SiC, and Plasma-Spray Coating. This paper provides an excellent reference.

(1) "Performance of a New Silicon-coated Disk Material: Disk Manufacturing Control and Production Device Experience". Stone, L. et al. Proceedings of the 12th International Conference on Ion Implantation Technology Proceedings Kyoto, Japan. IEEE 1998

Problems with Plasma-Sprayed Silicon

(1) "Performance of a New Silicon-coated Disk Material: Disk Manufacturing Control and Production Device Experience". Stone, L. et al. Proceedings of the 12th International Conference on Ion Implantation Technology Proceedings Kyoto, Japan. IEEE 1998

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A. Plasma-Sprayed Silicon **(1)**

Most commonly used in the industry is a form of "plasma-sprayed" silicon (see Fig. 1). This coating is deposited by a process in which silicon powder is melted into droplets and sprayed under [illegible] metal surface. The resultant coating has a porous layered structure, with variations in grain size and in levels of various potential contaminants. The contamination sources can be attributed to the impurities in the raw material, process environment (in air) and plasma spray gun (material wear under high temperatures). The g[illegible] and the surface finish can vary from 3.2 to 12.5+ microns R_a. This surface finish requires additional, undesirable post-spray finishing that produces high particle counts. For these reasons, improvements are required in the finish as well as possible improvement in the overall quality of the coating as far as contaminant and particle control is concerned.

Porous Layered Structure

Poor Uniformity, Particle and Contamination Control

High Temperature Process

Surface Roughness Requires Post Spray Finishing

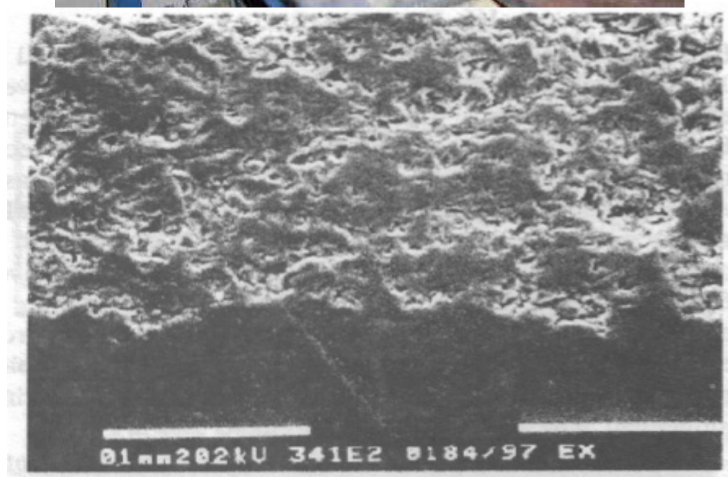

Fig. 1. Plasma-sprayed Si on Al substrate (cross-section).

PVD Sample (1) vs FIS HDP Layered Film

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(1) “Performance of a New Silicon-coated Disk Material: Disk Manufacturing Control and Production Device Experience”. Stone, L. et al. Proceedings of the 12th International Conference on Ion Implantation Technology Proceedings Kyoto, Japan. IEEE 1998

B. Sputter-deposited Silicon **(1)**

…The 20 micron columnar Si film revealed high levels of metallic contaminants…See Fig. 2. **“The primary reason for not pursuing this process was its low growth rate and associated high cost.”**

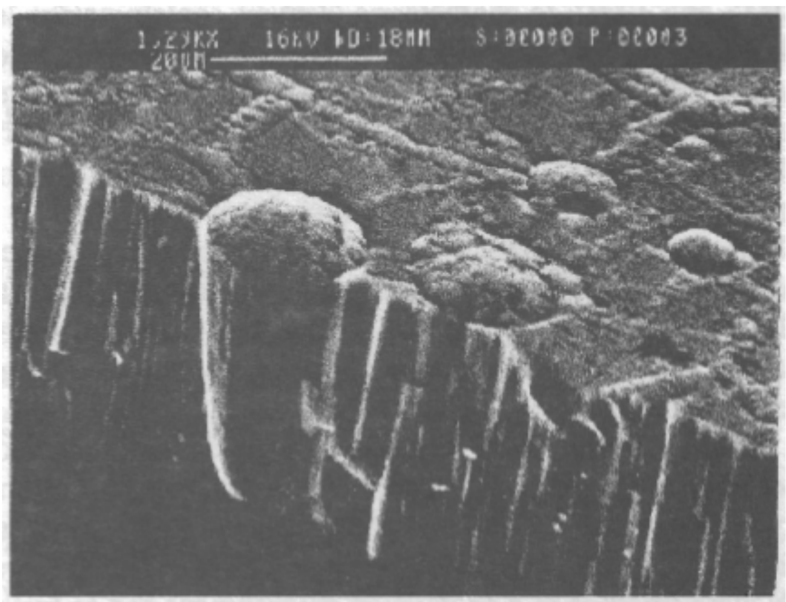
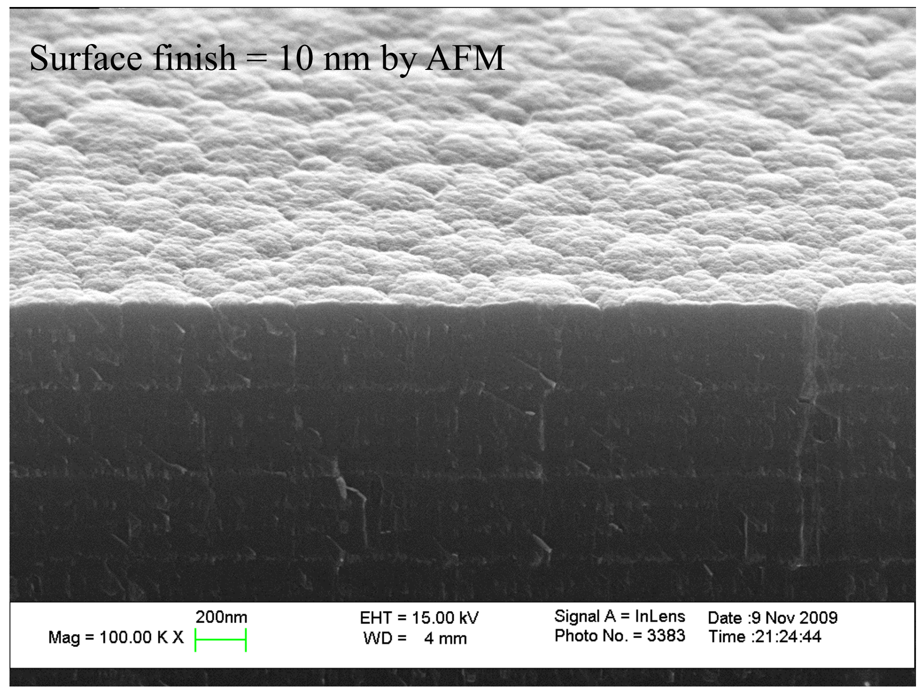


Fig. 2. Sputtered Si on Al substrate (cross-section)

SEM Image @ 70 Degrees for the top 3.2 microns of the FIS PVD-sputtered coating demonstrating the elimination of the columnar structure by high density plasma layered interface.



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PECVD vs FIS PVD

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16 Micron PECVD Film from Axcelis Paper

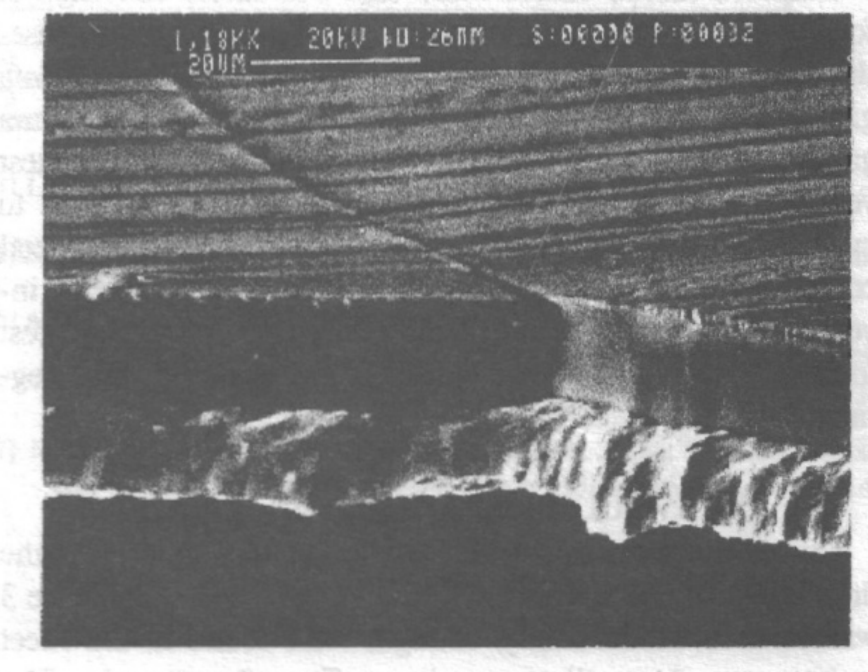
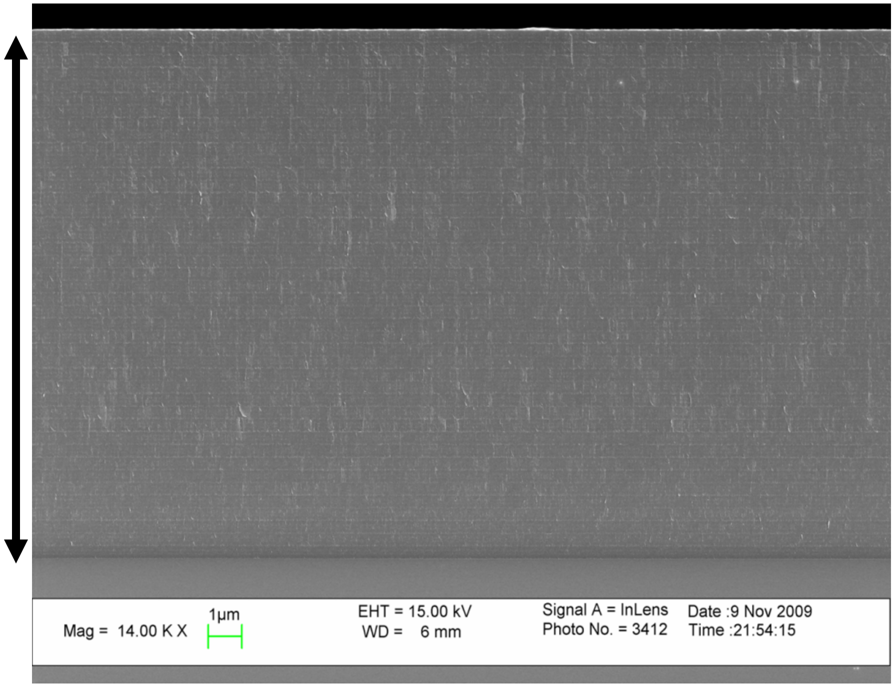


Fig. 3. PE CVD Si on Al foil (cross-section).

16 Microns SEM Image of FIS HDP PVD Film @ 90 Degrees



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Wear Data – PECVD vs PVD

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TABLE 2
Ion Beam Test Stand Sputter/Wear Evaluation

Sample	Energy	Angle	reduced loss	loss/ 6 mo's	yield
	kV	*degrees*	*mm/(Cb/cm2)*	*ave., um*	*atoms/ion*
PE CVD Si	30	0	1.50	3.37	1.20
"	30	80	1.50	3.37	1.20
"	50	80	3.17	7.12	2.54
"	70	80	2.50	5.62	2.00
Plasma spr. Si	50	0	9.82	22.09	9.46
Sputtered Si	40	80	1.25	2.81	1.20

Wear data from Eaton (Axcelis) paper **(1)** is shown here **- PVD is 2X better than PECVD**

(1) "Performance of a New Silicon-coated Disk Material: Disk Manufacturing Control and Production Device Experience". Stone, L. et al. Proceedings of the 12th International Conference on Ion Implantation Technology Proceedings Kyoto, Japan. IEEE 1998 fi SILICON

FIS Silicon Film Characteristics

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- Thickness, Uniformity and Appearance
  - Uniform dark Silicon color with no visible defects
  - Thickness uniformity better than plus-minus 3%
  - Step coverage > 40% one inch below top of vertical wall
- RBS Data
  - The films are extremely clean and only contain Si and about 0.1 atomic % Ar
  - There are no metallic impurities - no detection of C or O either
  - The RBS spectra looks just like bulk Silicon
- AFM Data
  - Surface roughness measured at less than 10 nm, - grain size 250 – 500 nm
- SIMS analysis on Sample Aluminum Coupon after 16 micron Silicon coating
  - Less than 0.5 PPM each for Fe, Ni, Cu, Cr, Mo, Zn, Mg and Al
- Density by cross section SEM
  - Columnar structure eliminated by high density plasma layered interface
  - Visually 100% as shown by micro cross-section
- Adhesion
  - Cleared standard Scotch tape and Kapton tape pull test

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Dimensions and Capabilities

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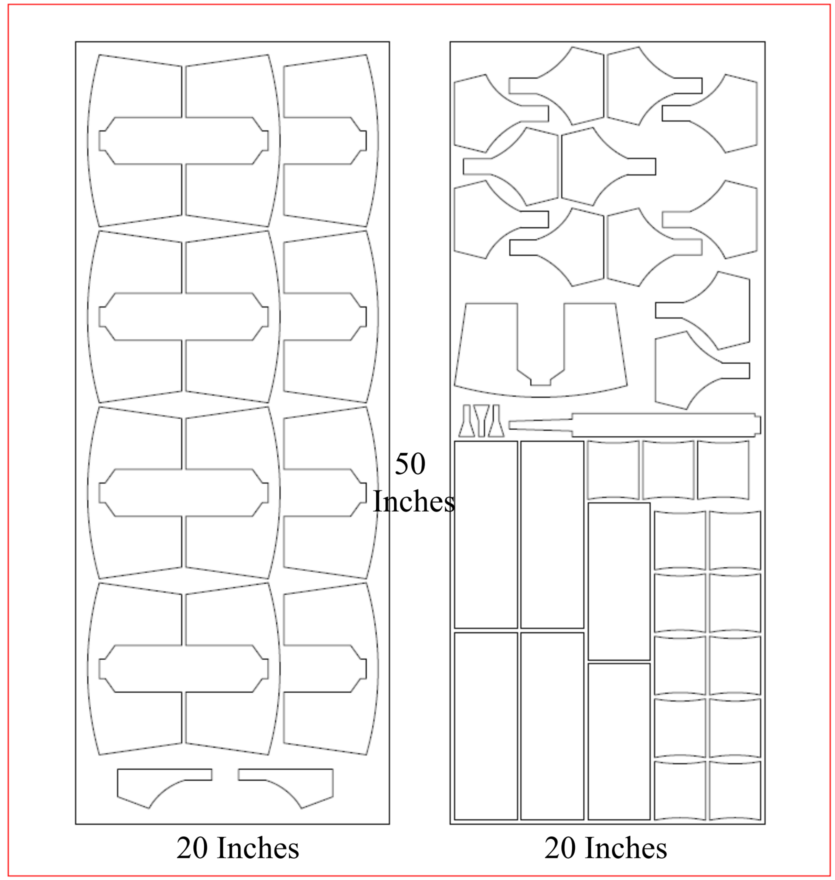
The pallet is 20 inches by 50 inches with 2.0 inch clearance below obstructions in the deposition path…(20” x 50” x 2.0”)

FIS can deposit Silicon films as thick as 45u on any size or shape product that fits within this envelope

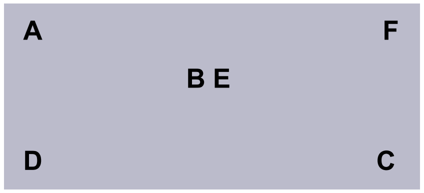
Temperature sensitive tooling other than II disk shields can also be coated including graphite beam shields, etch tooling etc.

FIS can provide one week or better cycle time for 200mm GSD shields

GSD Shield Set



Uniformity Data with Pallet Position



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Wafers sent to out for Profilometer measurements:						Alpha Step 200		
			Thickness			Thickness per Cycle		
Test Date	Position	# of cycles	Top (um)	Center (um)	Flat (um)	Top (um)	Center (um)	Flat (um)
10/22/13	A	3	2.57	2.57	2.49	0.86	0.86	0.83
10/22/13	B	3	2.42	2.42	2.45	0.81	0.81	0.82
10/22/13	C	3	2.39	2.49	2.51	0.80	0.83	0.84
10/24/13	A	20	15.6	16.9	17.3	0.78	0.85	0.87
10/24/13	B	20	15.8	16.2	16	0.79	0.81	0.80
10/24/13	C	20	16.25	16.13	15.91	0.81	0.81	0.80
10/29/13	D	3	2.5	2.63	2.61	0.83	0.88	0.87
10/29/13	E	3	2.59	2.57	2.54	0.86	0.86	0.85
10/29/13	F	3	2.48	2.51	2.41	0.83	0.84	0.80
11/21/13	A	20	16.6	16.4	16.6	0.83	0.82	0.83
11/21/13	B	20	16.2	16.2	16.4	0.81	0.81	0.82
11/21/13	C	20	16.5	16	16.4	0.83	0.80	0.82
12/8/13	A	22	18.4	18.3	18.2	0.84	0.83	0.83
12/8/13	C	22	18.1	17.9	17.8	0.82	0.81	0.81

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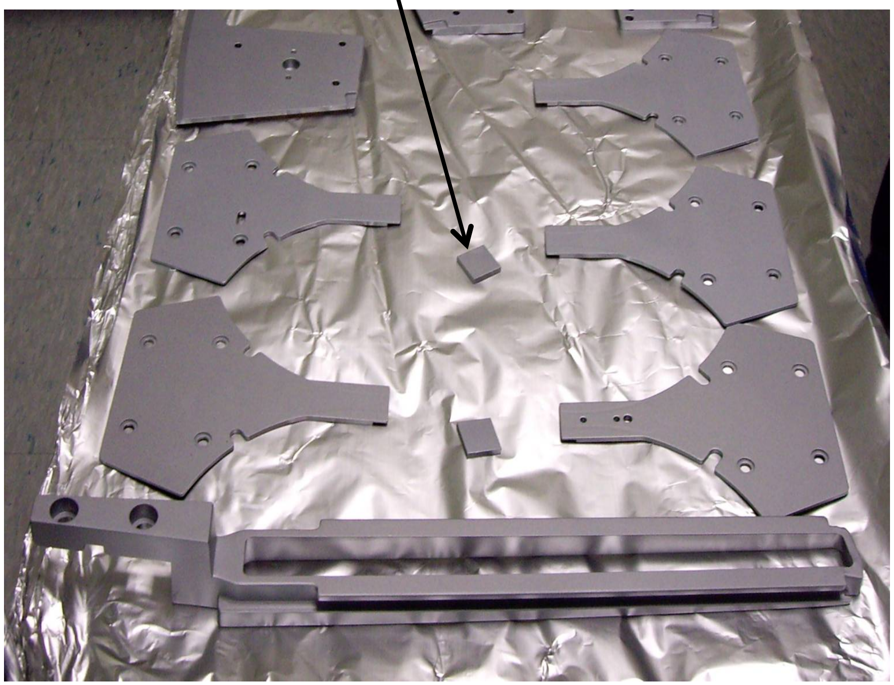
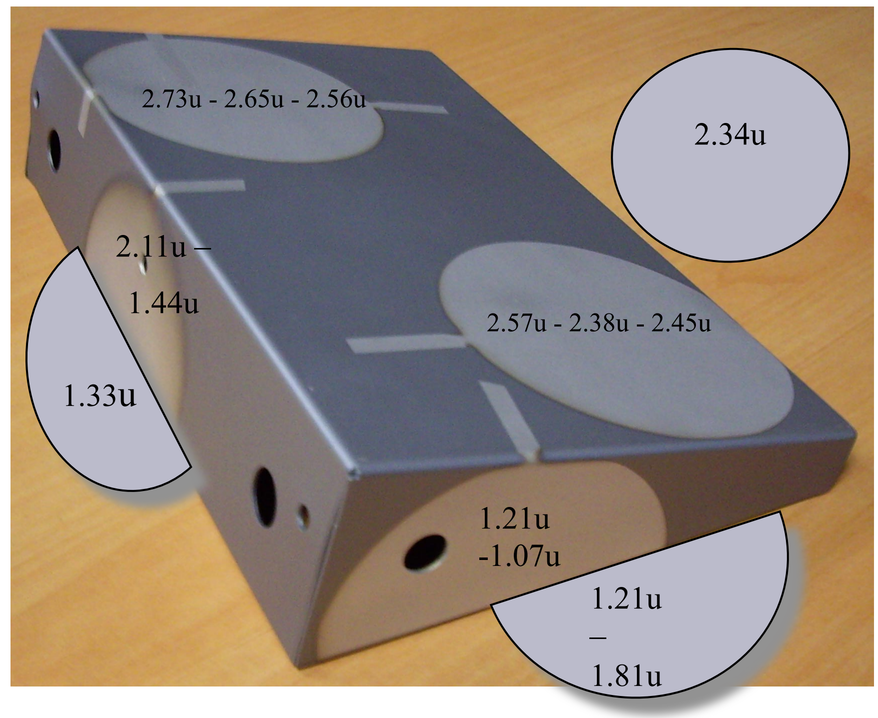
GSD Shields & Beam Window
Note: Test Coupon



Step Coverage



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SIMS data for 16 micron coating

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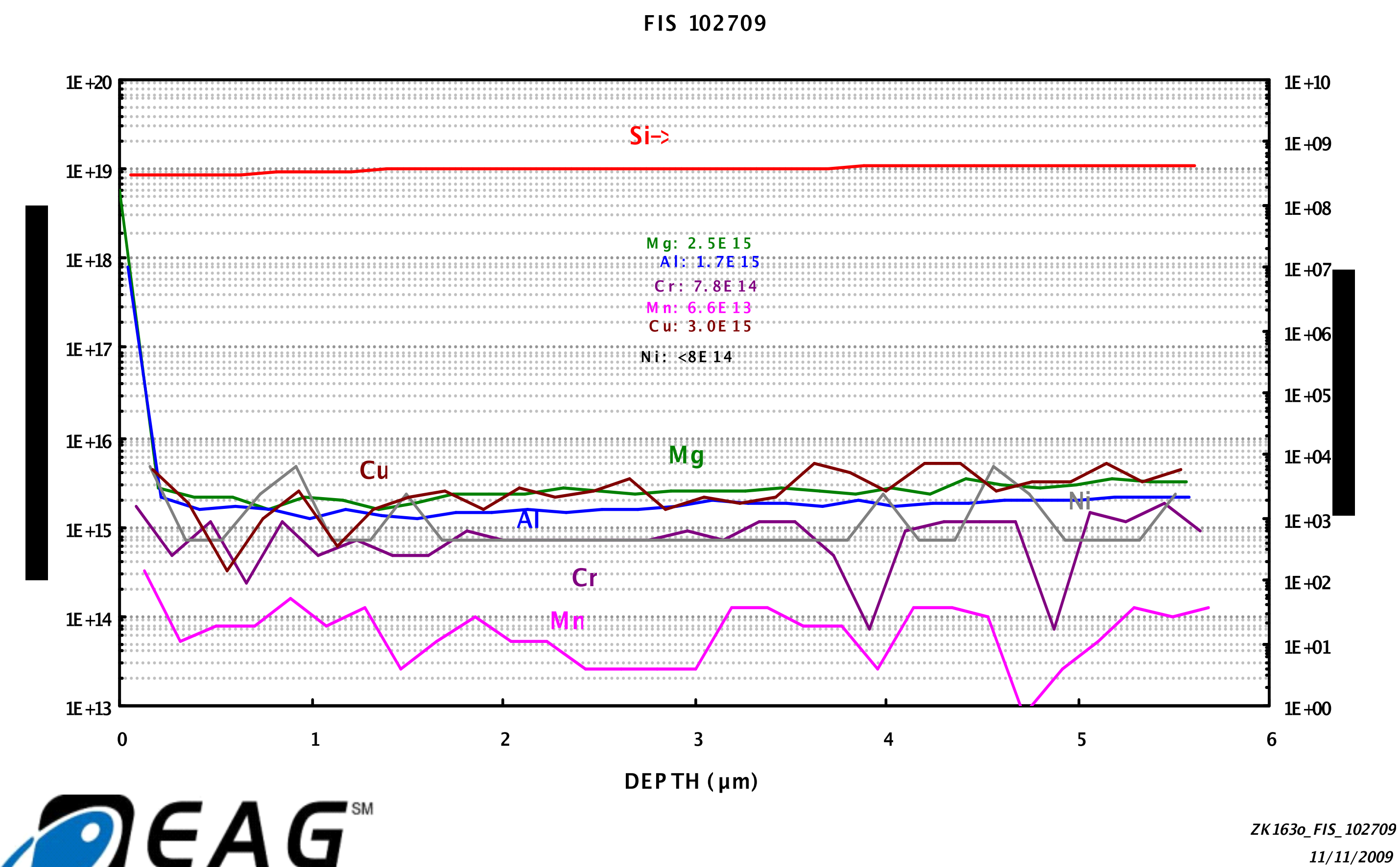

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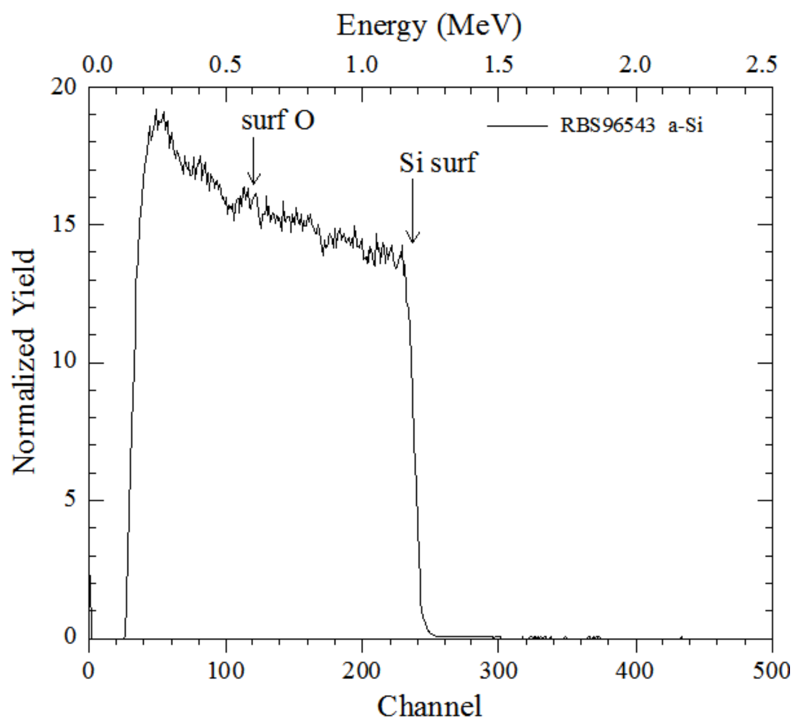
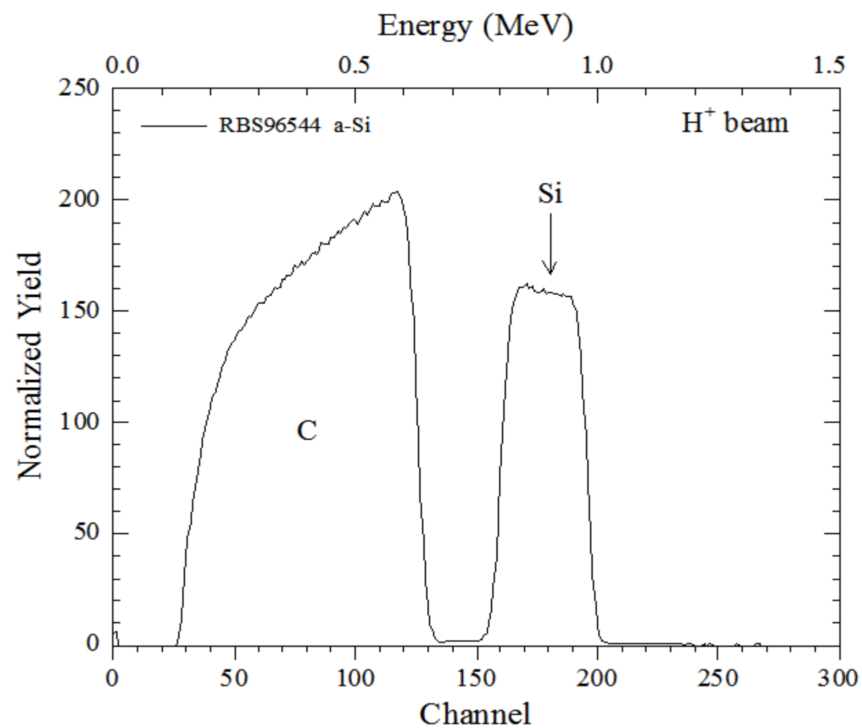
RBS Spectra on Graphite Coupon





The standard He RBS spectrum, which doesn't have sufficient energy to penetrate the entire film, but shows a small O surface peak, as well as the same height as you would expect from a bulk Si substrate

The He gives +9% bulk density and the H gives -7% bulk density. The average is bulk density.
So, I'd say these films are pretty damn close to bulk density.

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SEM Image @ 70 deg

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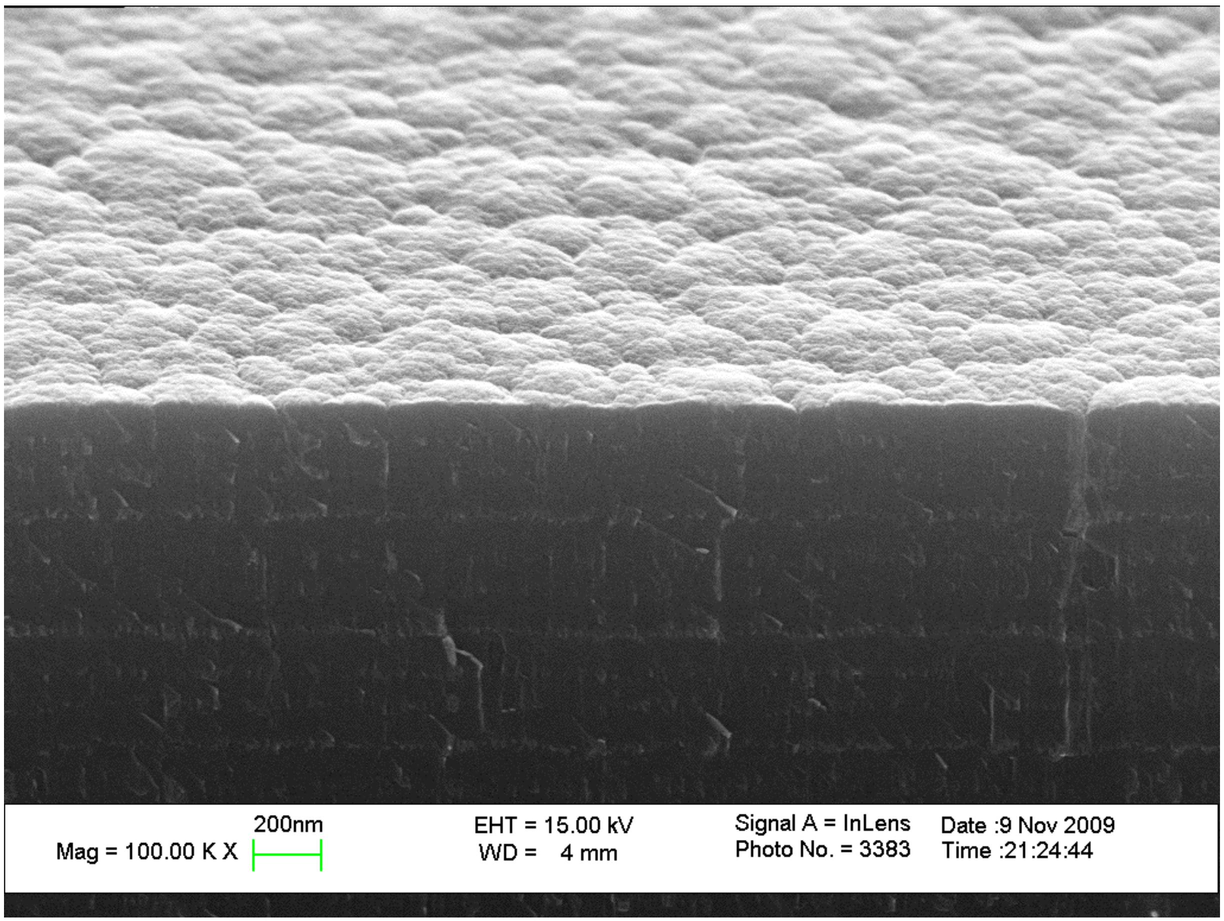

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SEM Image @ 90 deg

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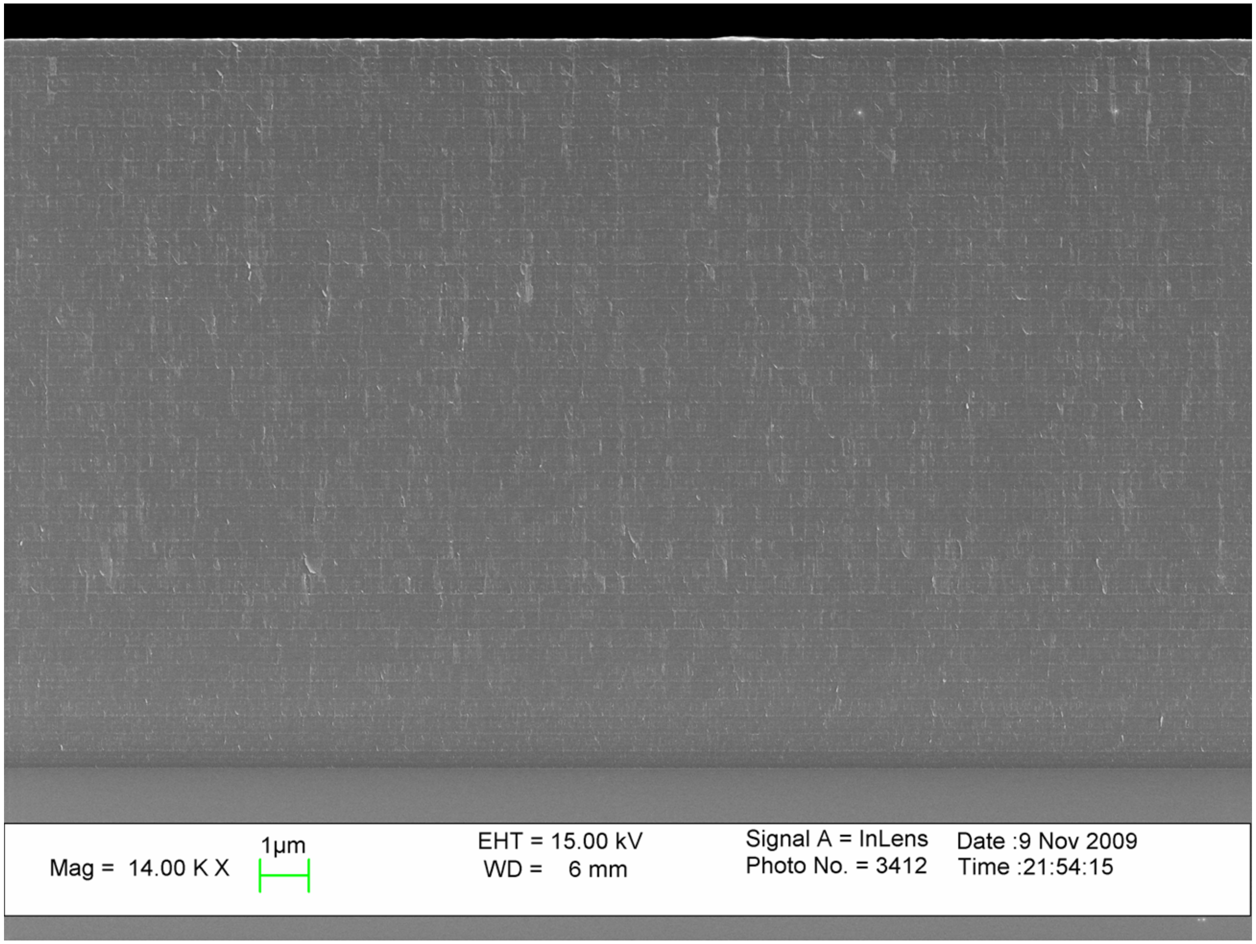

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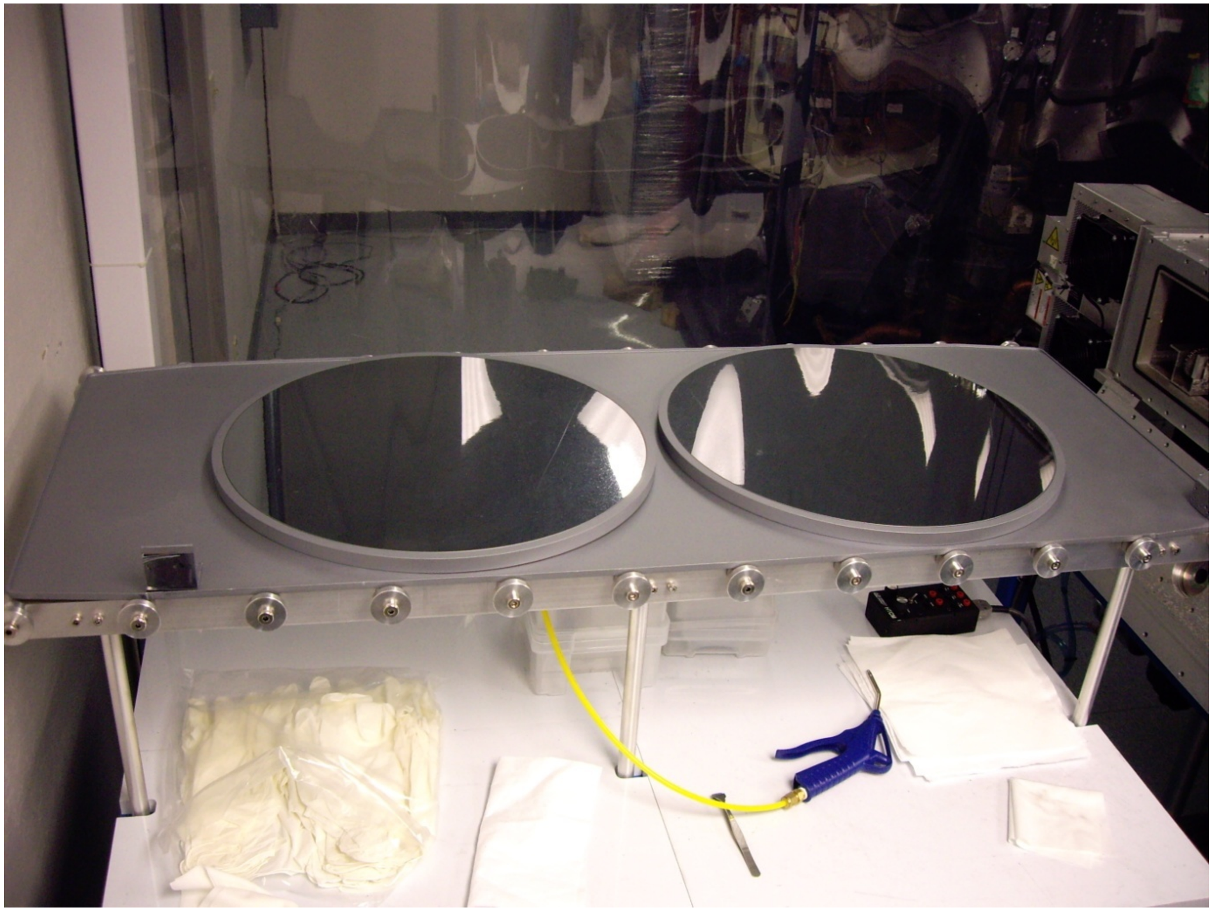
PSG450 Mechanical Wafers



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"Accelerating the transition to 450 mm wafers"

PSG450

(PVD-Si-Glass450): Mark0

"Mechanical" 450 mm Si Encapsulated Glass Wafers"

Function:

Low-cost approximation of Si 450 mm wafers for mechanical testing of wafer handling, load ports, storage and robotic apparatus.

Physical description:

Doubled side PVD Si coatings on 450 mm glass wafer blanks.

Cost Target:

Approximately $700/wafer. Less in quantity

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Comparison of Properties

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Property	Si wafer	Mark0	Mark1	Notes
	SEMI M74-1108	May, 2012	TBD	
Diameter	450+/- 0.2 mm	450+/- 0.2 mm		
Thickness	925+/- 25 um	1100 um	thinner	Si coating ≈4 um +/-3%, Glass blank = 1100+/-100 um
Weight	not specified (340 g)	400 g	lighter	
Bevel angle	45° or 22°	45°	shallower	Bevel depth = 250 um SEMI std depth= 120 or 508 um
Notch depth	1 mm	1 mm		
Notch angle	90°	90°		
Surface	polished	RMS ≈ 10 nm, reflective, few visible defects		Grain size = 250-500 nm, columnar RBS tested: Si film at bulk density
Doping level	not specified	P-type 0.1 ohm-cm		
Metals	not specified	<0.5 PPM tested for Fe, Ni, Cu, Cr, Mo, Zn, Mg, Al		
Other elements	not specified	≈0.1% Ar in Si		
Adhesion	not applicable	Scotch and Kapton tape test passed		

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Summary

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- Exposed Aluminum in a high energy process chamber can be coated with high purity Silicon to prevent cross contamination
  - High purity level for Al, Fe, Cr, Cu, Mg, etc.
  - Smooth surface finish to eliminate particles.
  - Low wear (surface erosion) during customer operation
  - Improved predictability of coating cycle times
  - Minimized rework and improved deliveries
- The quality of the deposited film has allowed us to create inexpensive 450mm Silicon coated glass wafers for mechanical testing of wafer handling, load ports, storage and robotic apparatus.