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Alloy Composition of 6061 Aluminum

- **Silicon** minimum 0.4%, maximum 0.8% by weight
- **Iron** no minimum, maximum 0.7%
- **Copper** minimum 0.15%, maximum 0.40%
- **Manganese** no minimum, maximum 0.15%
- **Magnesium** minimum 0.8%, maximum 1.2%
- **Chromium** minimum 0.04%, maximum 0.35%
- **Zinc** no minimum, maximum 0.25%
- **Titanium** no minimum, maximum 0.15%
- Other elements no more than 0.05% each, 0.15% total
- Remainder **Aluminium** (95.85%–98.56%)
FIS LLC

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PVD Silicon Coating for Implanter Parts

- The Ion Implant community has used high purity Silicon PVD coatings for implant disk shields, beamline and target chamber parts for over 10 years.

- The basic requirements for our Silicon coatings include:
  - High purity level for Al, Fe, Cr, Cu, Mg, etc.
  - Good Adhesion
  - Smooth surface finish to eliminate particles.
  - Low wear (surface erosion) during customer operation

- In 2009, Factory Integrated Solutions (FIS) began Silicon coating services, located within CORE Systems’s main facility in Sunnyvale, CA

- This capability has resulted in:
  - Improved predictability of coating cycle times
  - Minimized rework and improved deliveries
  - Provided the means for continuous improvement
FIS and CORE Systems conducted a careful study of the various attributes of both PECVD and PVD and concluded that PVD was the preferred choice for Silicon coating of implanter parts.

This choice was based on the following:

- Equivalent or better elemental purity with no surface voids
- Lower cost by eliminating expensive facility systems to handle hazardous materials
- Equivalent or better wear, adhesion and particle performance
- Better operational flexibility

The comprehensive disk coating paper (1) done by Eaton (Axcelis) shows data from PECVD, PVD, SiC, and Plasma-Spray Coating. This paper provides an excellent reference.

Problems with Plasma-Sprayed Silicon


A. Plasma-Sprayed Silicon

Most commonly used in the industry is a form of “plasma-sprayed” silicon (see Fig. 1). This coating is deposited by a process in which silicon powder is melted into droplets and sprayed under high velocity gas flow onto the substrate surface. The resultant coating has a porous layered structure, with variations in grain size, number of particles, and other potential contaminants. The contamination source can be attributed to the impurities in the raw material, process environment (in air) and plasma spray gun (material wear under high temperatures). The porosity and the surface finish can vary from 3.2 to 12.5+ microns Ra. This surface finish requires additional finishing steps such as etching or grit blasting that produces high contrast images. For these reasons, improvements are required to minimize as well as possible improvement in the overall quality of the coating as far as contaminant and particle control is concerned.

- Porous Layered Structure
- Poor Uniformity, Particle and Contamination Control
- High Temperature Process
- Surface Roughness Requires Post Spray Finishing

Fig. 1. Plasma-sprayed Si on Al substrate (cross-section).
PVD Sample (1) vs FIS HDP Layered Film


B. Sputter-deposited Silicon (1)

…The 20 micron columnar Si film revealed high levels of metallic contaminants…See Fig. 2. “The primary reason for not pursuing this process was its low growth rate and associated high cost.”

SEM Image @ 70 Degrees for the top 3.2 microns of the FIS PVD-sputtered coating demonstrating the elimination of the columnar structure by high density plasma layered interface.

Surface finish = 10 nm by AFM

Fig. 2. Sputtered Si on Al substrate (cross-section)
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PECVD vs FIS PVD

16 Micron PECVD Film from Axcelis Paper

16 Microns SEM Image of FIS HDP PVD Film @ 90 Degrees

http://www.factinsol.com
Wear Data – PECVD vs PVD

TABLE 2
Ion Beam Test Stand Sputter/Wear Evaluation

<table>
<thead>
<tr>
<th>Sample</th>
<th>Energy</th>
<th>Angle</th>
<th>reduced lost</th>
<th>lost 6 mo’s</th>
<th>yield</th>
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<tbody>
<tr>
<td></td>
<td>kV</td>
<td>degrees</td>
<td>mm/(Cb/cm²)</td>
<td>ave., um</td>
<td>atoms/ion</td>
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<tr>
<td>PECVD Si</td>
<td>30</td>
<td>0</td>
<td>1.50</td>
<td>3.37</td>
<td>1.20</td>
</tr>
<tr>
<td>&quot;</td>
<td>30</td>
<td>80</td>
<td>1.50</td>
<td>3.37</td>
<td>1.20</td>
</tr>
<tr>
<td>&quot;</td>
<td>50</td>
<td>80</td>
<td>3.17</td>
<td>7.12</td>
<td>2.54</td>
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<tr>
<td>&quot;</td>
<td>70</td>
<td>80</td>
<td>2.50</td>
<td>5.62</td>
<td>2.00</td>
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<tr>
<td>Plasma spr. Si</td>
<td>50</td>
<td>0</td>
<td>9.82</td>
<td>22.09</td>
<td>9.46</td>
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<tr>
<td>Sputtered Si</td>
<td>40</td>
<td>80</td>
<td>1.25</td>
<td>2.81</td>
<td>1.20</td>
</tr>
</tbody>
</table>

Wear data from Eaton (Axcelis) paper (1) is shown here - PVD is 2X better than PECVD

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FIS Silicon Film Characteristics

- Thickness, Uniformity and Appearance
  - Uniform dark Silicon color with no visible defects
  - Thickness uniformity better than plus-minus 3%
  - Step coverage > 40% one inch below top of vertical wall

- RBS Data
  - The films are extremely clean and only contain Si and about 0.1 atomic % Ar
  - There are no metallic impurities - no detection of C or O either
  - The RBS spectra looks just like bulk Silicon

- AFM Data
  - Surface roughness measured at less than 10 nm, - grain size 250 – 500 nm

- SIMS analysis on Sample Aluminum Coupon after 16 micron Silicon coating
  - Less than 0.5 PPM each for Fe, Ni, Cu, Cr, Mo, Zn, Mg and Al

- Density by cross section SEM
  - Columnar structure eliminated by high density plasma layered interface
  - Visually 100% as shown by micro cross-section

- Adhesion
  - Cleared standard Scotch tape and Kapton tape pull test
Dimensions and Capabilities

The pallet is 20 inches by 50 inches with 2.0 inch clearance below obstructions in the deposition path…(20” x 50” x 2.0”)

FIS can deposit Silicon films as thick as 45u on any size or shape product that fits within this envelope

Temperature sensitive tooling other than II disk shields can also be coated including graphite beam shields, etch tooling etc.

FIS can provide one week or better cycle time for 200mm GSD shields
# Uniformity Data with Pallet Position

<table>
<thead>
<tr>
<th>Test Date</th>
<th>Position</th>
<th># of cycles</th>
<th>Top (um)</th>
<th>Center (um)</th>
<th>Flat (um)</th>
<th>Alpha Step 200</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Thickness per Cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Top (um)</td>
</tr>
<tr>
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<td>A</td>
<td>3</td>
<td>2.57</td>
<td>2.57</td>
<td>2.49</td>
<td>0.86</td>
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<tr>
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<td>20</td>
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<td>16.25</td>
<td>16.13</td>
<td>15.91</td>
<td>0.81</td>
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<tr>
<td>10/29/13</td>
<td>D</td>
<td>3</td>
<td>2.5</td>
<td>2.63</td>
<td>2.61</td>
<td>0.83</td>
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<tr>
<td>10/29/13</td>
<td>E</td>
<td>3</td>
<td>2.59</td>
<td>2.57</td>
<td>2.54</td>
<td>0.86</td>
</tr>
<tr>
<td>10/29/13</td>
<td>F</td>
<td>3</td>
<td>2.48</td>
<td>2.51</td>
<td>2.41</td>
<td>0.83</td>
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<tr>
<td>11/21/13</td>
<td>A</td>
<td>20</td>
<td>16.6</td>
<td>16.4</td>
<td>16.6</td>
<td>0.83</td>
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<tr>
<td>11/21/13</td>
<td>B</td>
<td>20</td>
<td>16.2</td>
<td>16.2</td>
<td>16.4</td>
<td>0.81</td>
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<tr>
<td>11/21/13</td>
<td>C</td>
<td>20</td>
<td>16.5</td>
<td>16</td>
<td>16.4</td>
<td>0.83</td>
</tr>
<tr>
<td>12/8/13</td>
<td>A</td>
<td>22</td>
<td>18.4</td>
<td>18.3</td>
<td>18.2</td>
<td>0.84</td>
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<tr>
<td>12/8/13</td>
<td>C</td>
<td>22</td>
<td>18.1</td>
<td>17.9</td>
<td>17.8</td>
<td>0.82</td>
</tr>
</tbody>
</table>
GSD Shields & Beam Window
Note: Test Coupon

Step Coverage

- 2.73u - 2.65u - 2.56u
- 2.11u - 1.44u
- 1.33u
- 2.57u - 2.38u - 2.45u
- 1.21u - 1.07u
- 1.21u - 1.81u
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SIMS data for 16 micron coating
The standard He RBS spectrum, which doesn't have sufficient energy to penetrate the entire film, but shows a small O surface peak, as well as the same height as you would expect from a bulk Si substrate.

The He gives +9% bulk density and the H gives -7% bulk density. The average is bulk density. So, I’d say these films are pretty damn close to bulk density.
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SEM Image @ 70 deg
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SEM Image @ 90 deg

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PSG450 Mechanical Wafers
FI Silicon

“Accelerating the transition to 450 mm wafers”

PSG450
(PVD-Si-Glass450): Mark0

“Mechanical” 450 mm Si Encapsulated Glass Wafers”

**Function:**
Low-cost approximation of Si 450 mm wafers for mechanical testing of wafer handling, load ports, storage and robotic apparatus.

**Physical description:**
Doubled side PVD Si coatings on 450 mm glass wafer blanks.

**Cost Target:**
Approximately $700/wafer. Less in quantity
# FI Silicon

## Comparison of Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Si wafer</th>
<th>Mark0</th>
<th>Mark1</th>
<th>Notes</th>
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<td></td>
<td>SEMI M74-1108</td>
<td>May, 2012</td>
<td>TBD</td>
<td></td>
</tr>
<tr>
<td>Diameter</td>
<td>450+/- 0.2 mm</td>
<td>450+/- 0.2 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thickness</td>
<td>925+/- 25 um</td>
<td>1100 um</td>
<td>thinner</td>
<td>Si coating ≈4 um +/-3%, Glass blank = 1100+/-100 um</td>
</tr>
<tr>
<td>Weight</td>
<td>not specified (340 g)</td>
<td>400 g</td>
<td>lighter</td>
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<tr>
<td>Bevel angle</td>
<td>45° or 22°</td>
<td>45°</td>
<td>shallower</td>
<td>Bevel depth = 250 um SEMI std depth= 120 or 508 um</td>
</tr>
<tr>
<td>Notch depth</td>
<td>1 mm</td>
<td>1 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Notch angle</td>
<td>90°</td>
<td>90°</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Surface</td>
<td>polished</td>
<td>RMS ≈ 10 nm, reflective, few visible defects</td>
<td>Grain size = 250-500 nm, columnar RBS tested: Si film at bulk density</td>
<td></td>
</tr>
<tr>
<td>Doping level</td>
<td>not specified</td>
<td>P-type 0.1 ohm-cm</td>
<td></td>
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<tr>
<td>Metals</td>
<td>not specified</td>
<td>&lt;0.5 PPM tested for Fe, Ni, Cu, Cr, Mo, Zn, Mg, Al</td>
<td></td>
<td></td>
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<tr>
<td>Other elements</td>
<td>not specified</td>
<td>≈0.1% Ar in Si</td>
<td></td>
<td></td>
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<tr>
<td>Adhesion</td>
<td>not applicable</td>
<td>Scotch and Kapton tape test passed</td>
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</tr>
</tbody>
</table>
Exposed Aluminum in a high energy process chamber can be coated with high purity Silicon to prevent cross contamination

- High purity level for Al, Fe, Cr, Cu, Mg, etc.
- Smooth surface finish to eliminate particles.
- Low wear (surface erosion) during customer operation
- Improved predictability of coating cycle times
- Minimized rework and improved deliveries

The quality of the deposited film has allowed us to create inexpensive 450mm Silicon coated glass wafers for mechanical testing of wafer handling, load ports, storage and robotic apparatus.