Ultratech
TECHNOLOGY ACCEPTED

Laser Spike Annealing for 20nm and Beyond

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Outline

- Introduction
- Dual Beam LSA for Long Dwell Applications
  - Defect annealing
  - De-activation/Re-activation
  - Stress reduction
  - 3D structures
- Dual beam LSA for Low Temperature Applications

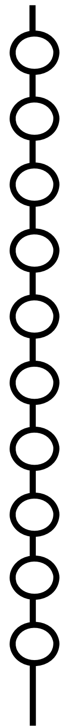
Requirements for Advanced Annealing for 20nm and Below

- Ability to form highly activated, defect free ultra shallow junctions
  - Possible elimination of spike RTA
- Compatibility with HKMG process flow
- Compatibility with 3D structures
- Low Stress / Compatibility with advanced strain engineering
- Low temperature capability
- Layout independent process control

Millisecond Annealing Logic Applications

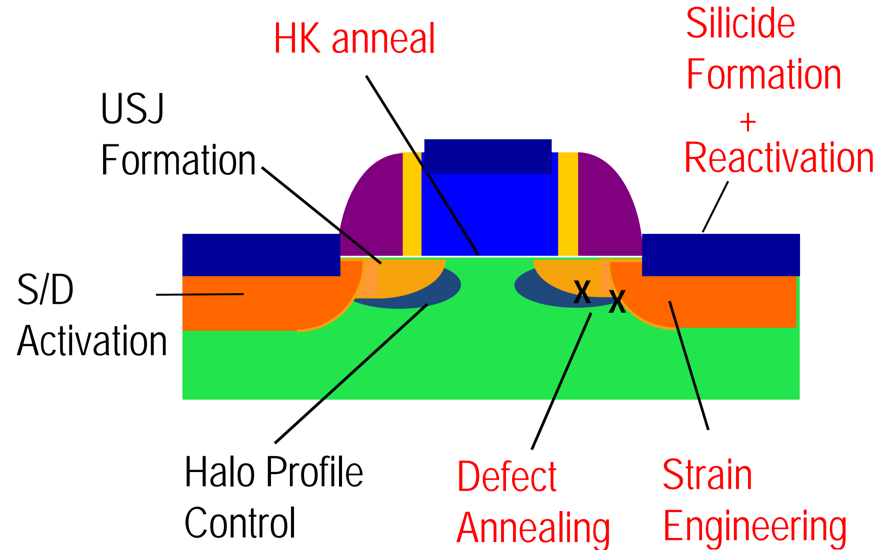
Device Flow

LSA Insertion Points:



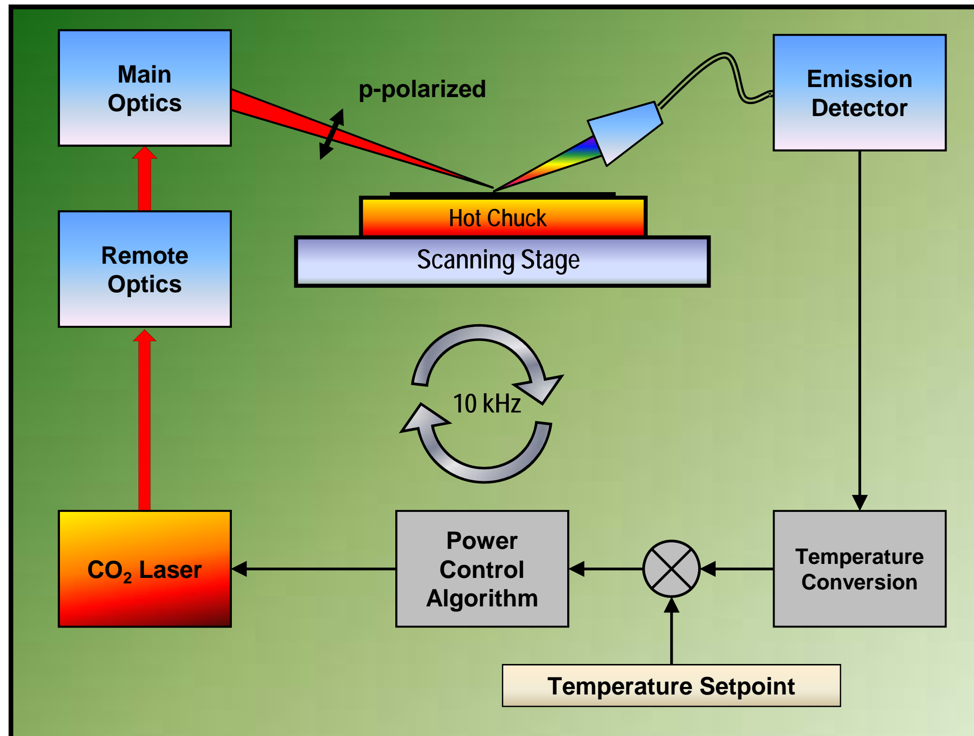
LSA Insertion	Step
	Isolation
	Gate Dielectric
	Gate Formation
	S/D Extension & Halo
① →	SW Spacer Formation
② →	SMT Process
③ →	Deep S/D Implantation
④ →	S/D spike RTA
⑤ →	Ni Silicidation
	BEOL Process

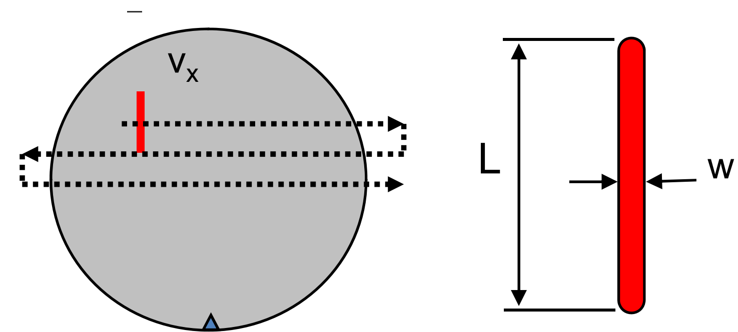
Device Applications



- **Expanded applications lead to multiple LSA insertion steps**

LSA101 Basic Platform (Single Beam)

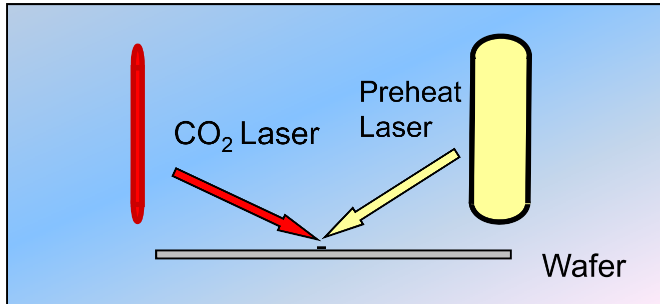


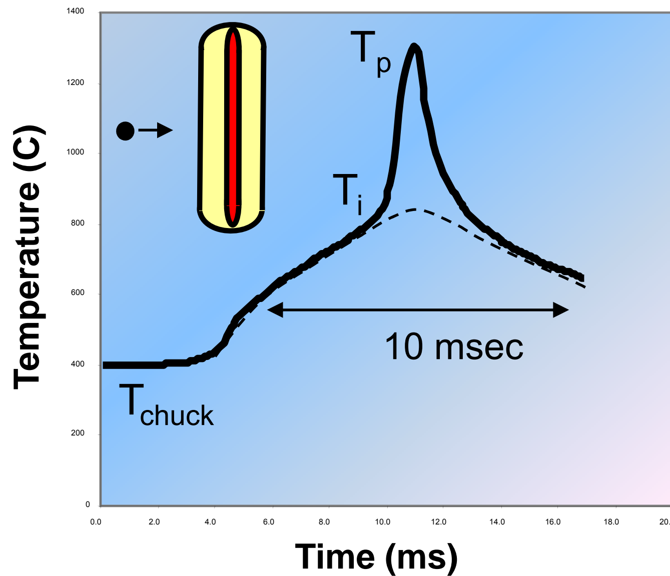


$$\text{Dwell time} = \frac{w}{v_x}$$

- Long wavelength, Brewster angle, p-polarized → Within-die Uniformity
- Temperature feedback control → Die-to-die Repeatability
- Localized stress field, flexible dwell time → Low stress
- Low CoO (Max throughput = 60wph)

Dual Beam LSA for Long Dwell Applications

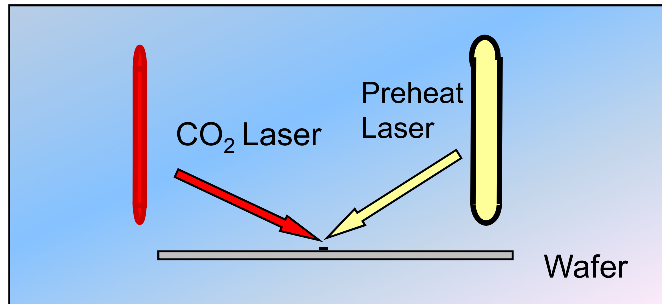


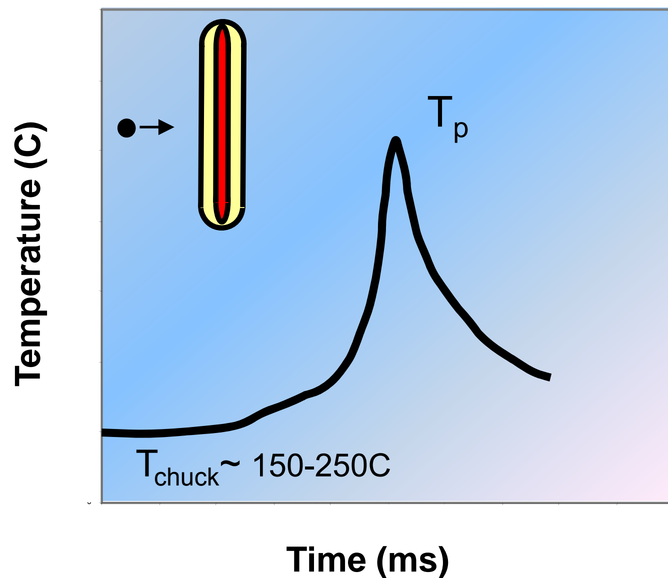


Key highlights

- A second laser beam is added to the system to expand process capabilities
- Allows access to the time regime ~ 10 msec
- Used for front end processes, e.g.,
  - Defect anneal
  - Solid phase regrowth
  - Stress reduction

Dual Beam LSA for Low Temperature Applications





Key highlights

- Preheat laser beam is added to the system to locally heat silicon to ~ 400C so that CO2 laser can be absorbed at low chuck temperatures
- Temperature measurement and control system designed for lower temperature range 500-1000C
- Used for low middle of line processes such as:
  - Nickel silicide formation
  - Post silicide dopant re-activation

Laser Spike Annealing Process Space

Temperature (°C): 200, 400, 600, 800, 1000, 1200, 1400

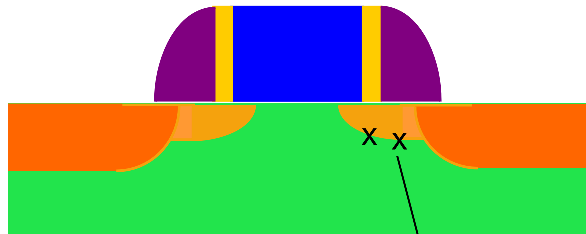
Time: 100us, 1ms, 10ms, 100ms, 1s, 10s

LSA101 (single beam) — High T
LSA101D (dual beam) — Long Dwell
LSA101L (dual beam) — Low T
RTA
Low T RTA

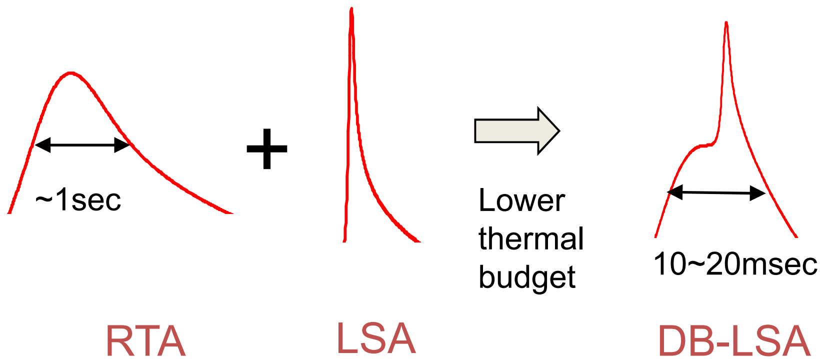
- **Field upgradable dual-beam LSA enables a wide range of applications on the LSA101 platform**

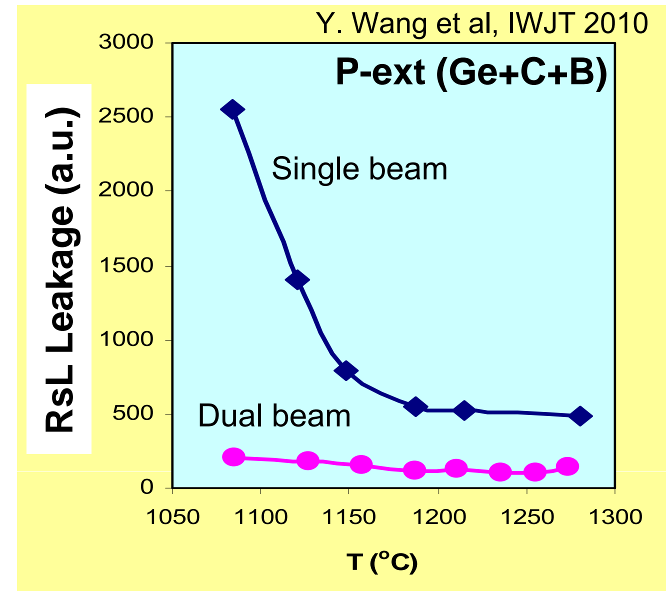
Long Dwell Applications

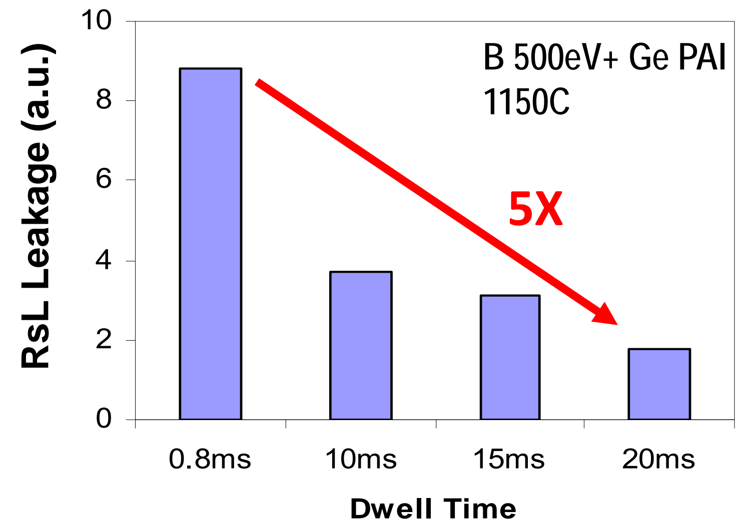
DB-LSA For LSA-only Integration



Defect anneal







DB-LSA provides a path to further reduce the thermal budget for sub-28nm generations

Long Dwell for N-type SD-Extension (As 2keV 1e15cm-2)

SIMS

Dwell: 10ms

1200°C
1100°C
1000°C
as-implanted

Concentration (cm^{-3})
1.E+22
1.E+21
1.E+20
1.E+19
1.E+18
1.E+17

0 10 20 30
Depth (nm)

Rs

1000°C
1100°C
1200°C

(b) As 2keV, 1e15cm^{-2}

Rs (ohm/sq)
900
700
500
300

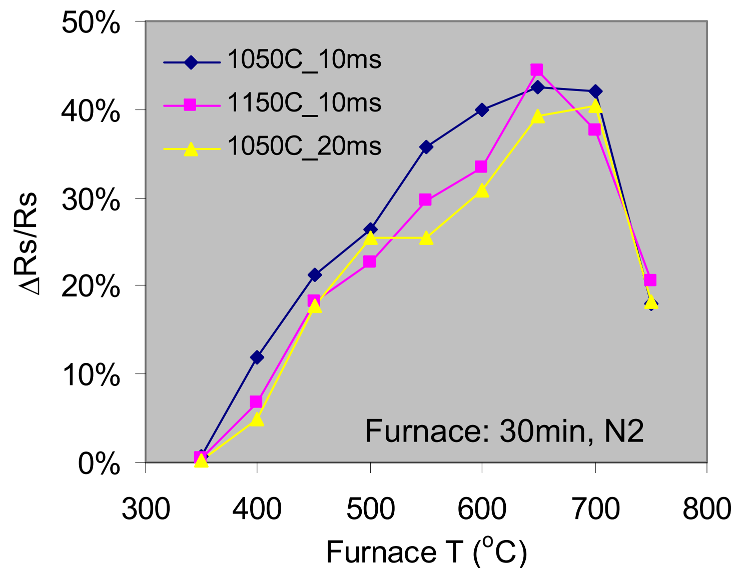
5 10 15 20 25
Dwell Time (ms)

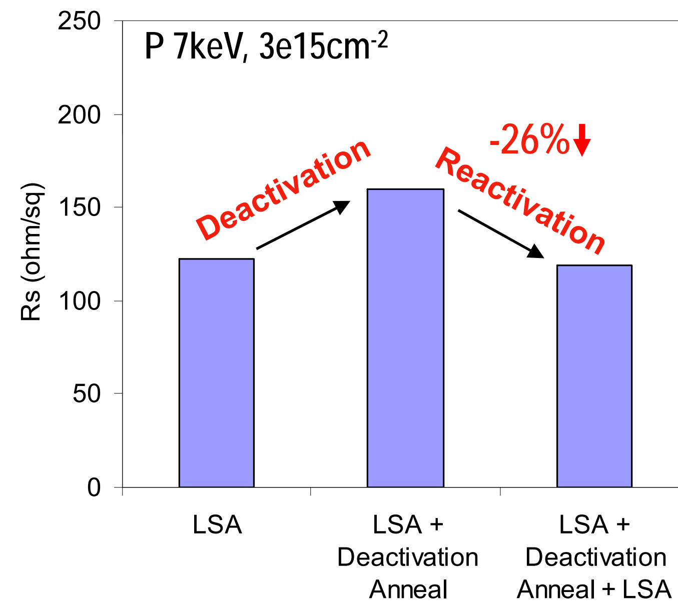
TEM Cross-section (1200C)

10nm

Y. Wang et al, IWJT 2011

Phosphorus Deactivation



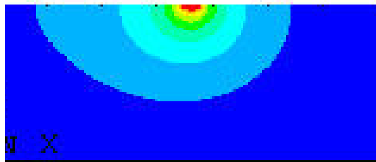


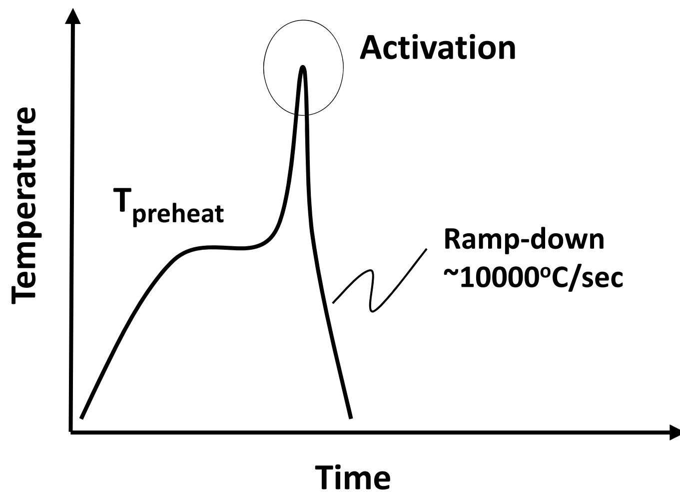
Y. Wang et al, IWJT 2011

- For P, dopant deactivation occurs at very low T; reverse annealing starts ~650°C.
- Original activation is fully recovered after second LSA

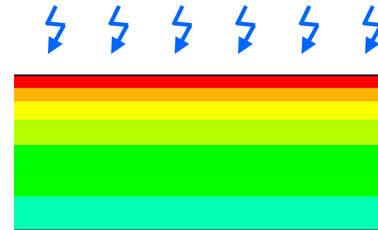
Temperature Profiles: LSA vs. FLA

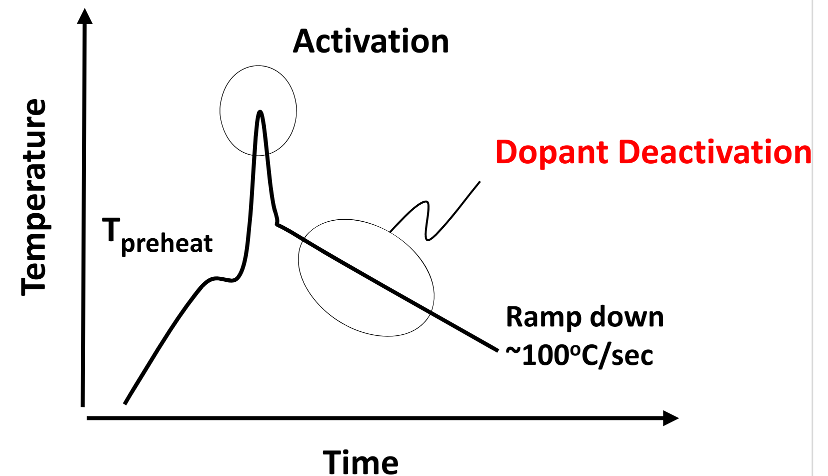
Dual Beam LSA





FLA w/ Backside Preheating

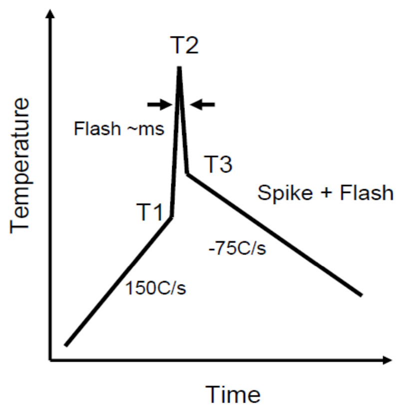




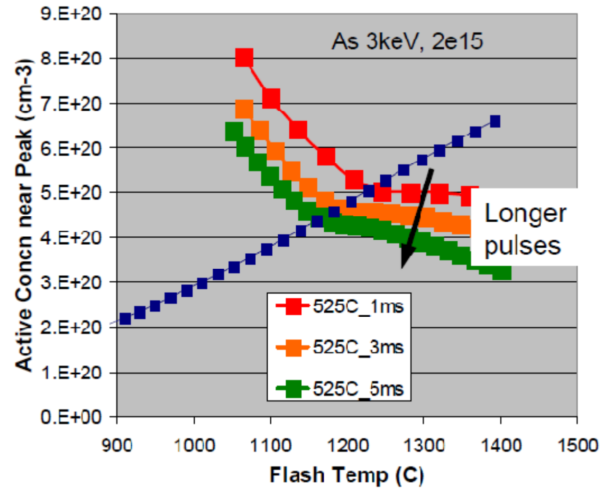
- **Anneal time and preheating temperature limited in lamp-based annealing system due to dopant deactivation from slow heat dissipation**

Example: Deactivation in Flash Anneal

Kennel (Intel, RTP'10)

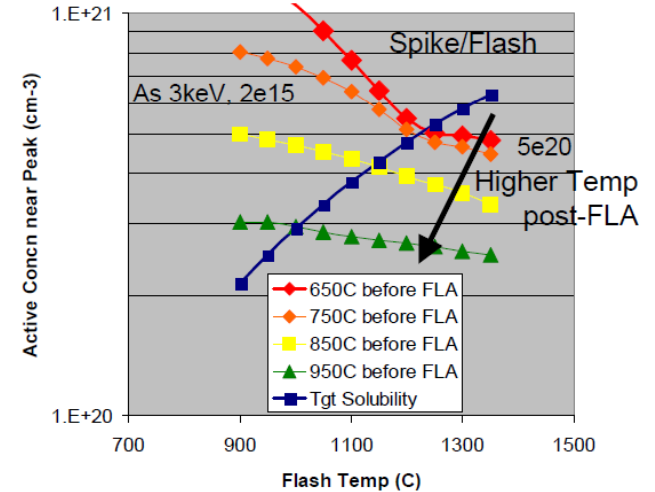


(a) Impact of anneal time



Longer anneal time
→ Slower ramp down

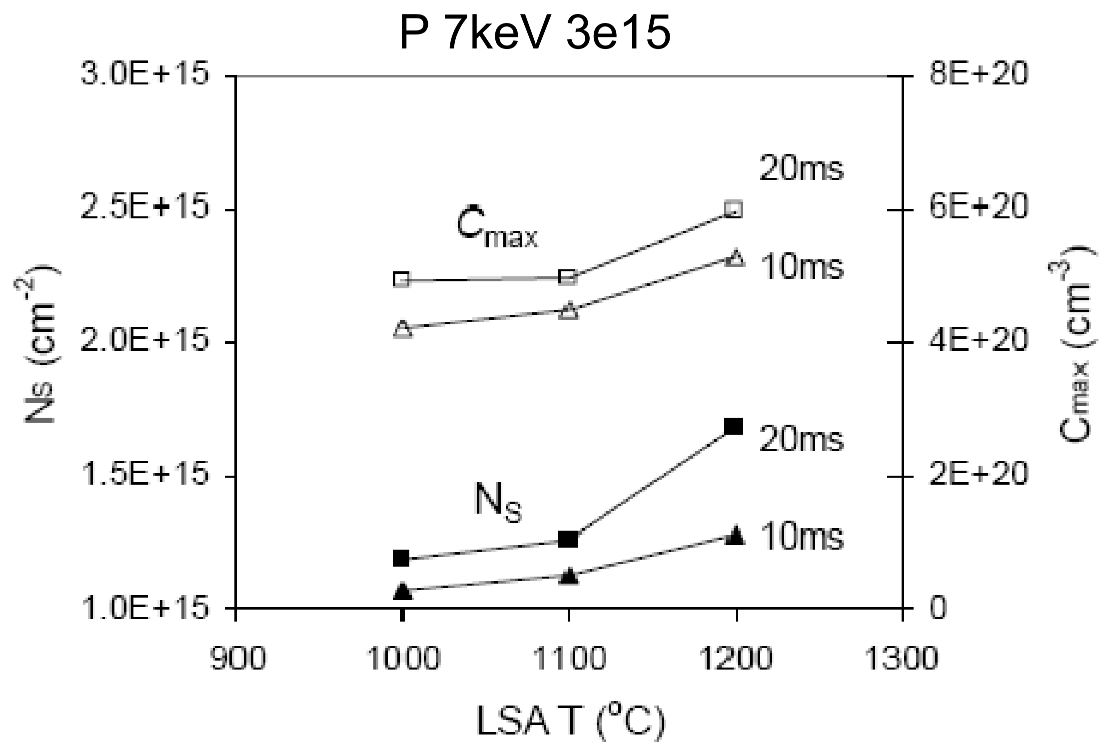
(b) Impact of intermediate T1



Higher T1 → Higher T3

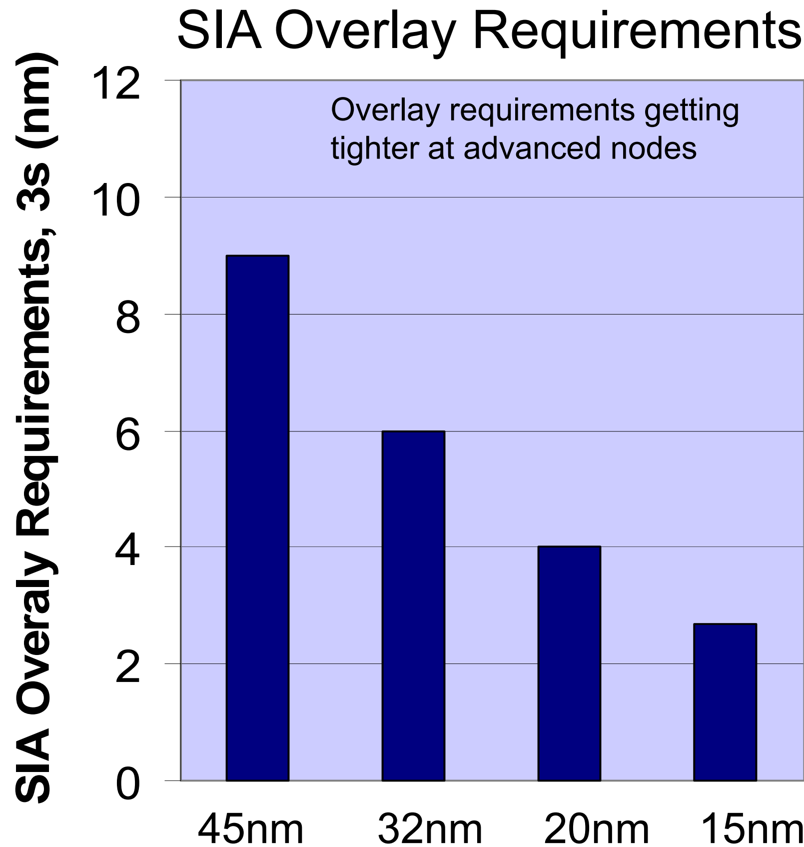
- In lamp based annealing, longer dwell or higher intermediate T results in lower active concentration due to deactivation.

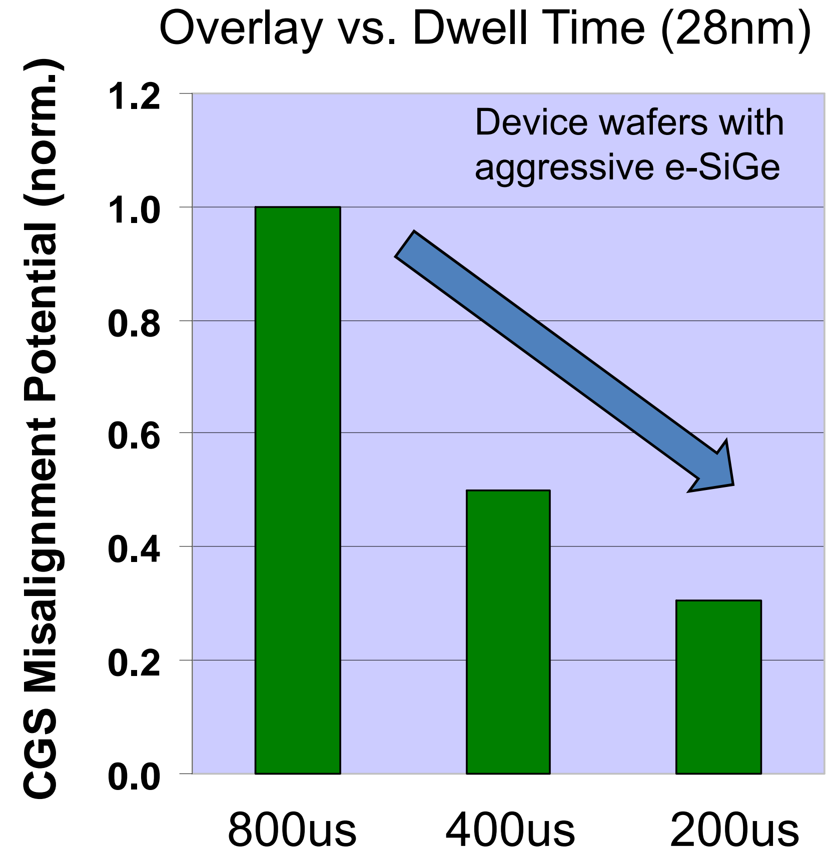
Example: Activation in LSA for Long Dwell



- **Fast cool down →Active carrier concentration increases with increasing dwell time**

Stress Management: Low Dwell Time for Overlay Improvement



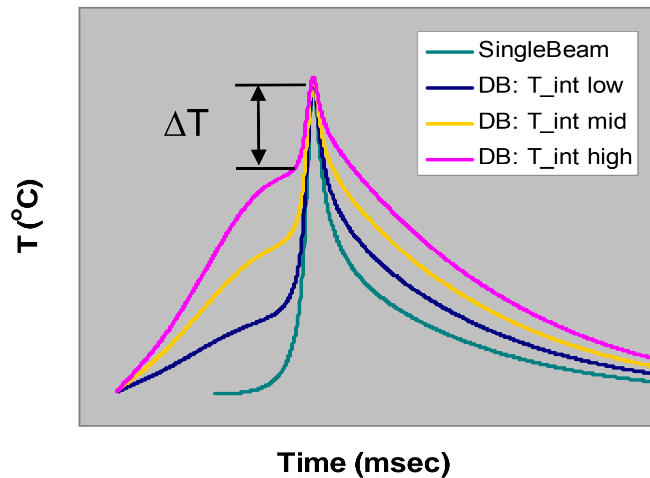


- Near peak temperature, short dwell times can reduce wafer warpage and overlay errors (typical visco-elastic behavior)

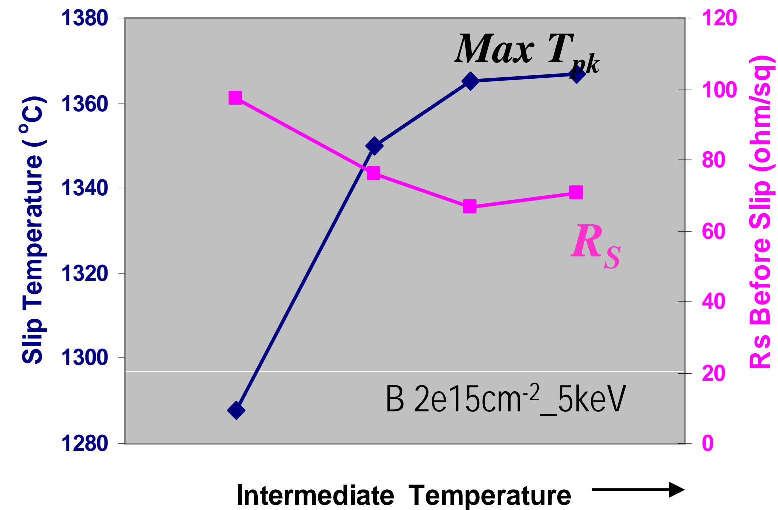
Stress Reduction By DB-LSA

Y. Wang et al. (IWJT 2010)

(a) T profile : single vs DB-LSA



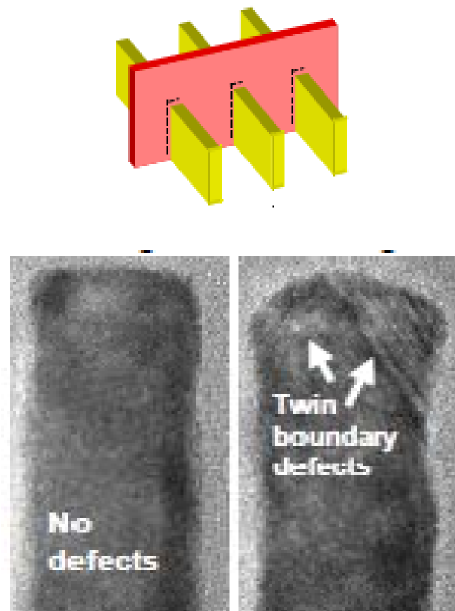
(b) Impact of intermediate T



- Stress can be reduced by reducing thermal gradients during the ramp up
- Maximum annealing temperature can be improved by dual beam LSA. As a result, lower Rs can be achieved without slip.

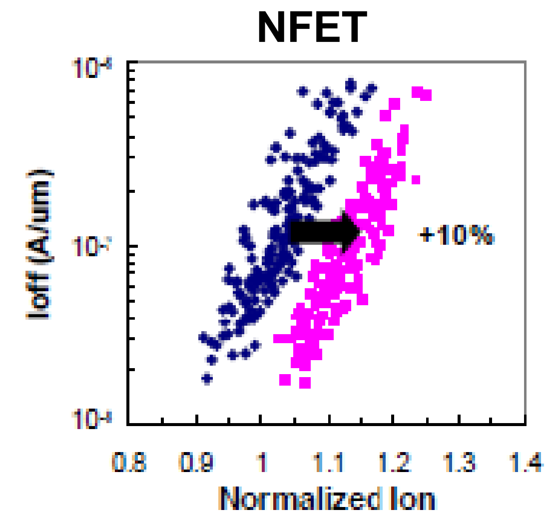
Application to 3D Structures

(a) Defect annealing



(b) Junction Activation for FinFET (Single beam)

- Ext. anneal
- Epi pre-clean
- Epi PFET/NFET
- Spacer2
- Multistep S/D I.I.
- S/D anneal (LSA)
- Ni silicidation
- BEOL process



Source: Yamashita et al, VLSI 2011

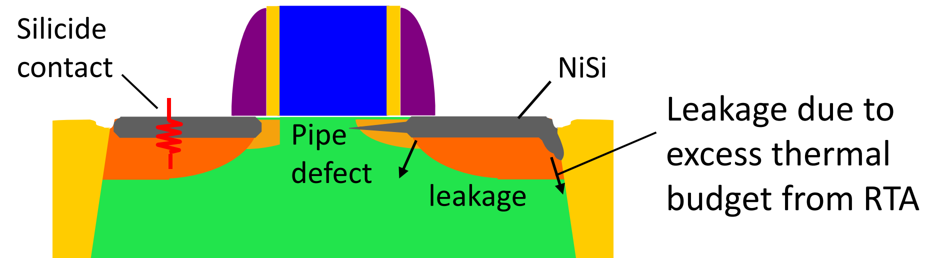
LSA is extendible to 3D transistor structures

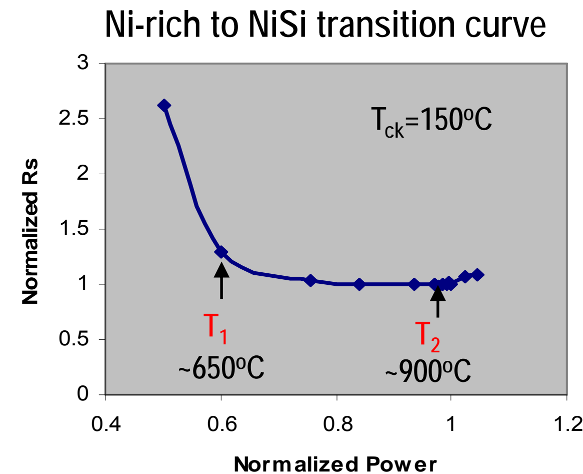
Low Temperature Applications

DB-LSA For Ni Silicide Leakage Reduction

- USJ Formation
- Ni Dep
- RTP1 (Ni-rich silicide)
- Selective Etch
- RTP2 (NiSi formation)

Replace by DB-LSA



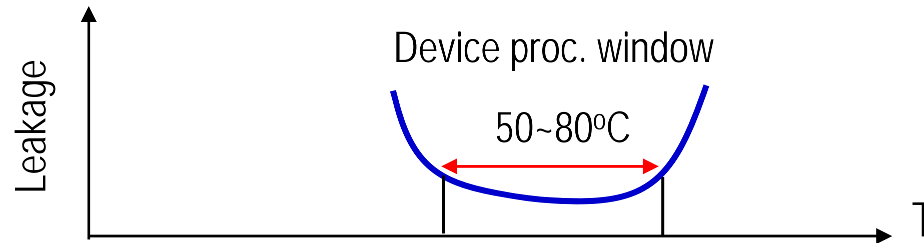


Y. Wang et al. (IWJT 2010)

- **Low thermal budget nature of LSA minimizes silicide diffusion & junction leakage**

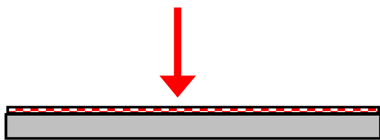
Within-die Temperature Uniformity for Nickel Silcide Formation (after Selective Etch)

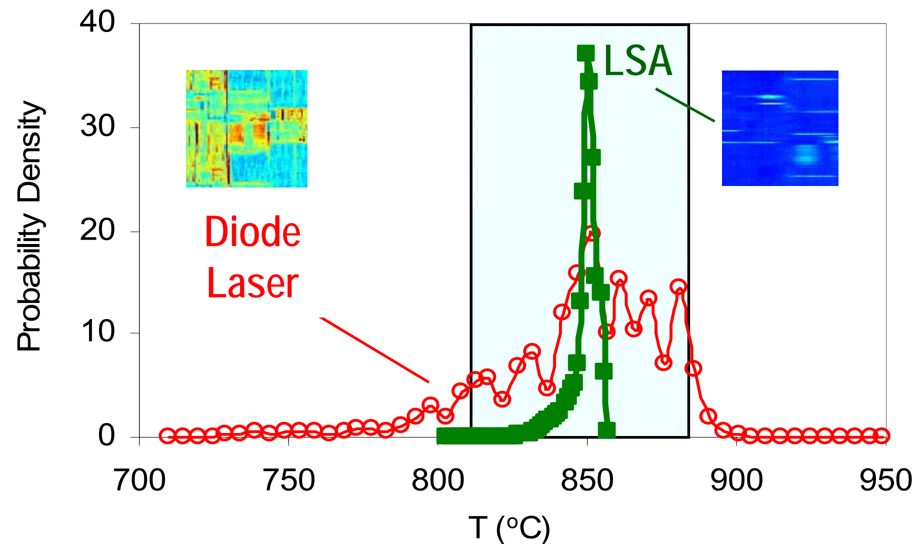
Temperature uniformity calculated from measured reflectance maps



Diode Laser

Short λ (850nm)
Near normal





LSA

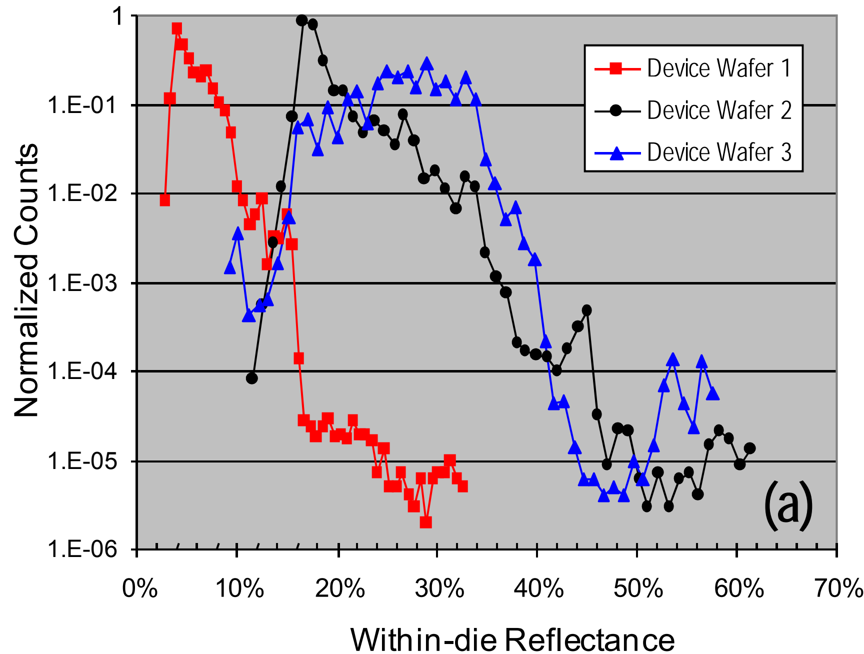
CO2 laser
Brewster angle

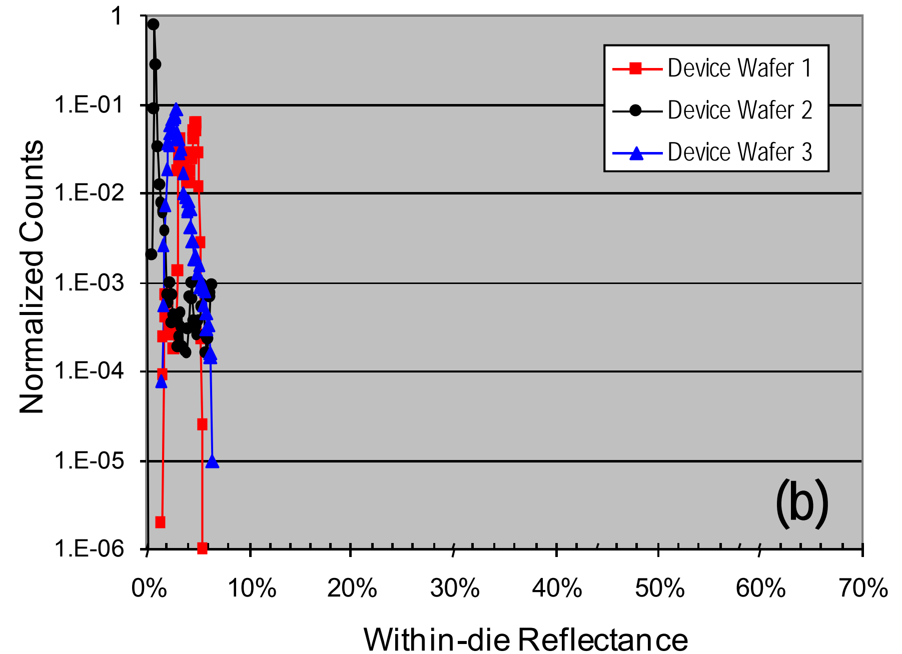
J. Hebb et al., ASMC 2011

- **Advantage of minimal pattern effect retained for NiSi using LSA**
- **Pattern effects can cause layout dependent yield loss**

Silicide Pattern Effect Comparison (Different Device Layouts)

Histograms of Measured Die Reflectance Maps





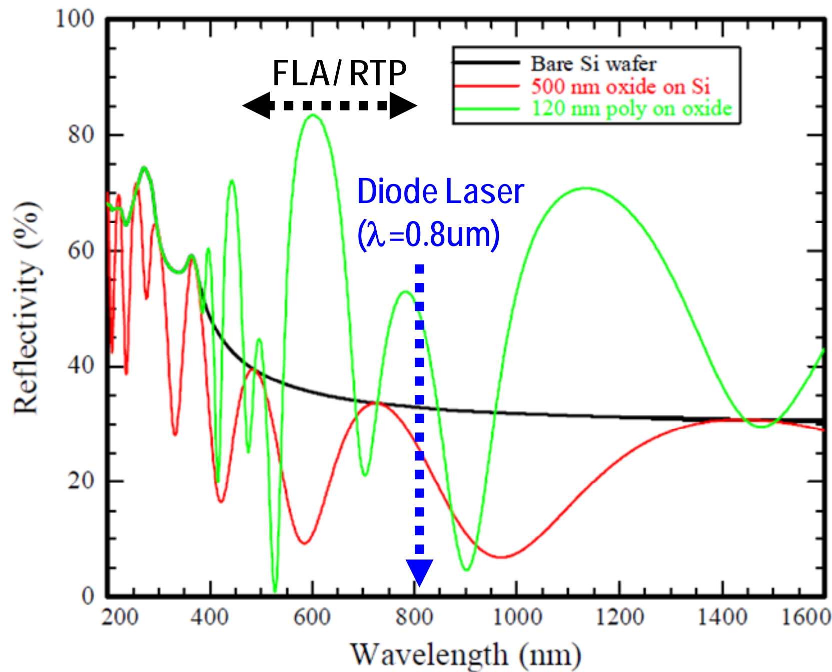
J. Hebb et al., ASMC 2011

LSA shows much tighter distribution within-die and product-to-product.

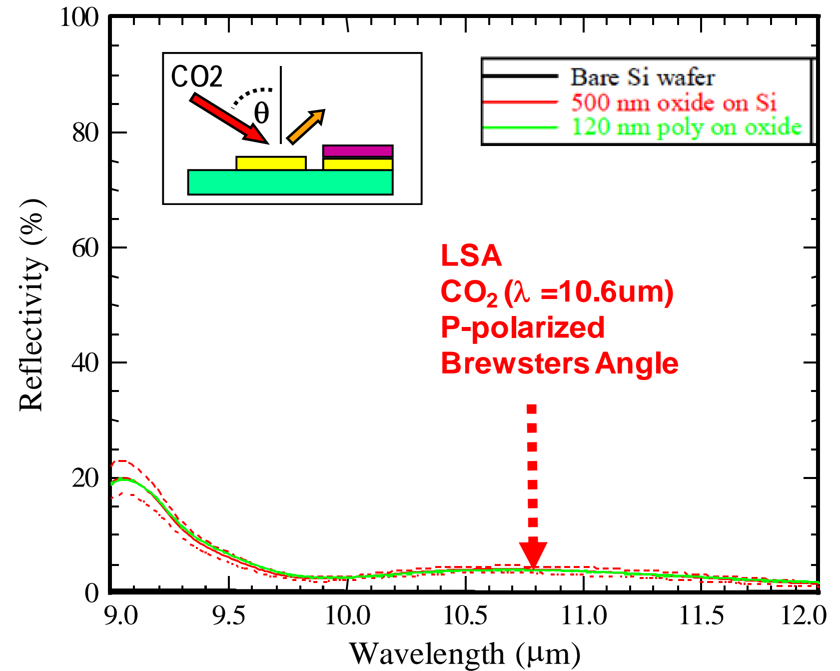
Pattern Effects:

Interference Effects for Competing Technologies

Short λ, normal incidence



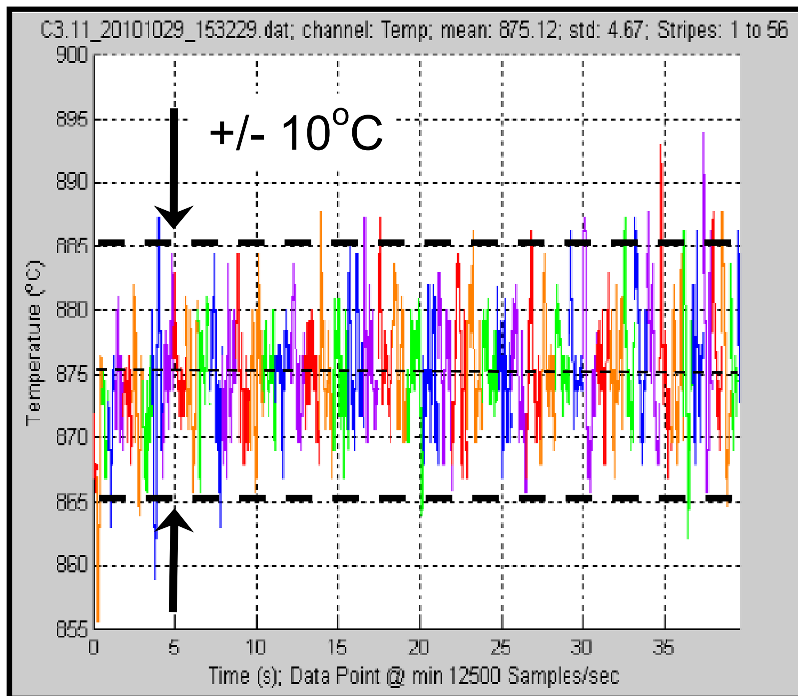
Long λ + Brewster θ + p-polarization



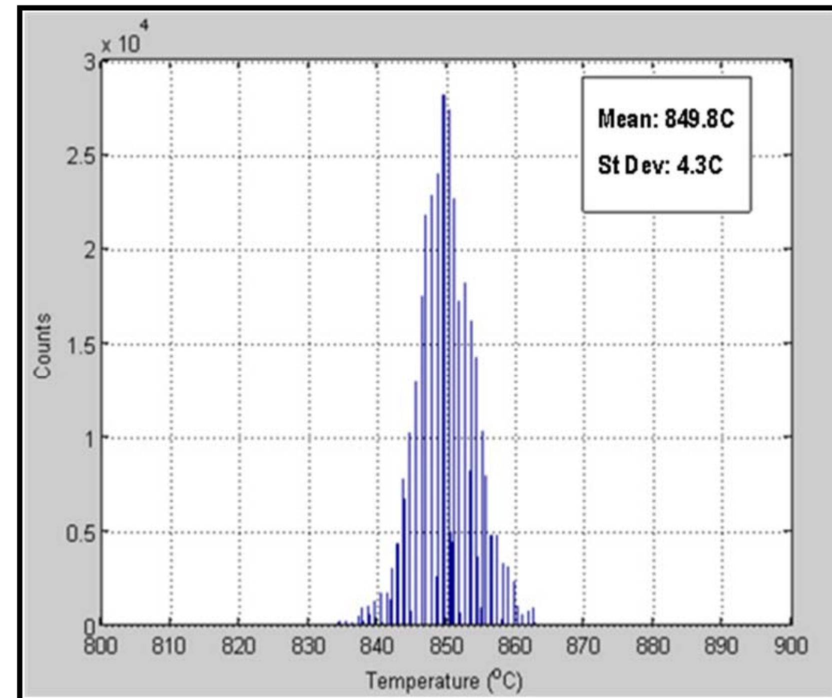
- **Pattern effect caused by thin film interference variations**
- **LSA configuration almost eliminates sensitivity to device film variations**

LSA Closed-loop Temperature Control on Nickel Silicide Device Wafers

Example: T-t trace



Example: T Histogram



J. Hebb et al., ASMC 2011

Closed-loop temperature control is stable and controls to ~ +/- 10C

Summary

- LSA will continue to be a key enabling technology in providing advanced annealing & precision doping engineering solutions for performance boost and leakage reduction for 20nm and beyond
- Dual beam has greatly extended LSA capabilities which will open up new applications
  - Long dwell capabilities enable such applications as defect annealing, dopant (re)activation, and stress reduction. Fast ramp down is a key advantage for maximum dopant activation.
  - Low temperature capabilities enable applications such as nickel silicide formation and post silicide anneal. Minimal pattern effects and real time temperature control are key capabilities required for extendibility
- LSA is extendible to 3D structures for defect annealing and junction activation