The case for thin film silicon solar

Technical Challenges and Opportunities

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EFFICIENCY - SCALE - COST

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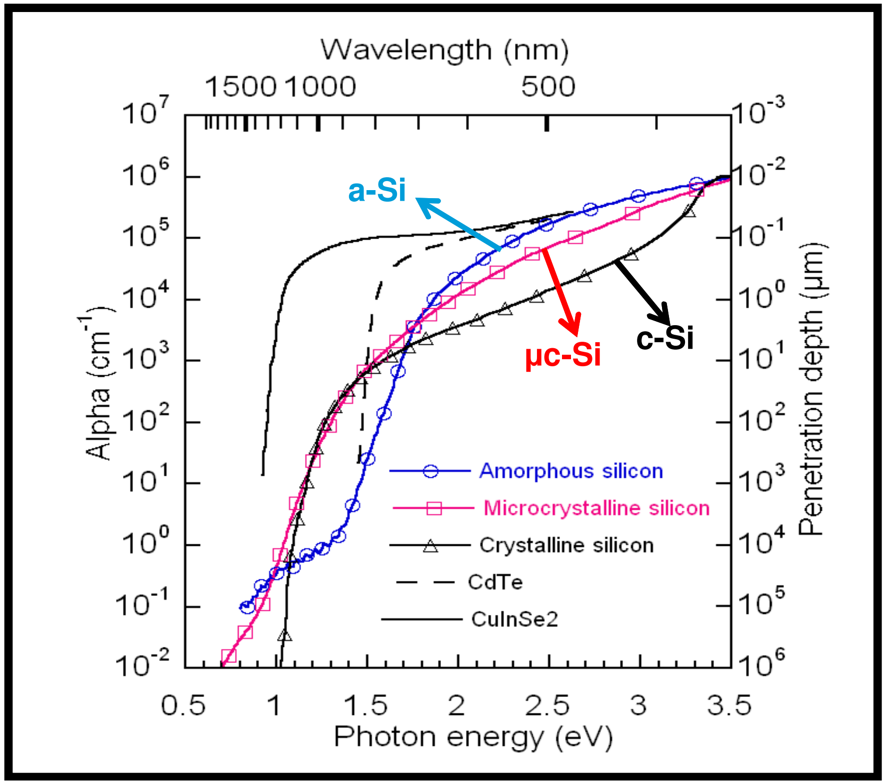
Contents

- Introduction to thin film silicon
- Amorphous and microcrystalline silicon solar cells
- Micromorph tandem concept
- ThinSilicon technology
- Path to 12% module efficiency
- Light Trapping in Solar Cells
- Closing Remarks

Why thin film silicon?

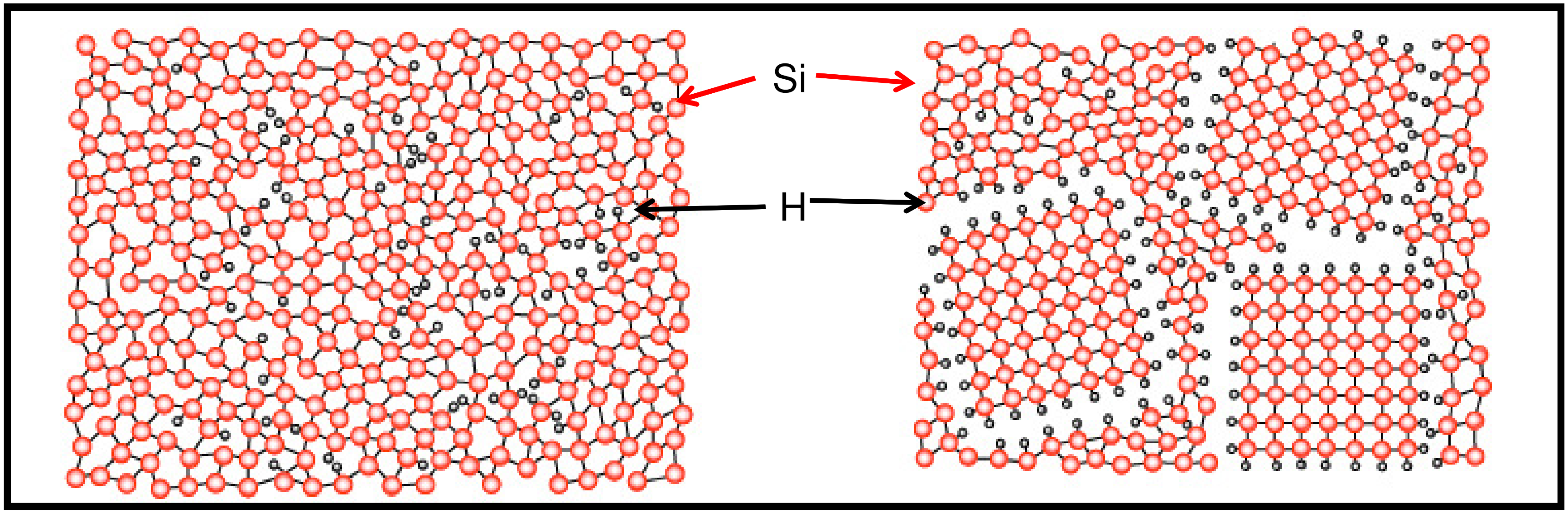
Some advantages

- Higher absorption in a-Si and µc-Si over c-Si; need films only a few microns
- Easy to deposit at large scale; PECVD well matured technology due to LCD industry (1.1 m X 1.4 m)
- Monolithic integration and automation
- Lower temperature co-efficient; higher panel output (kwh output /kW installed)
- No use of exotic or expensive materials i.e. In, Te, Ag
- Energy payback sooner than c-Si



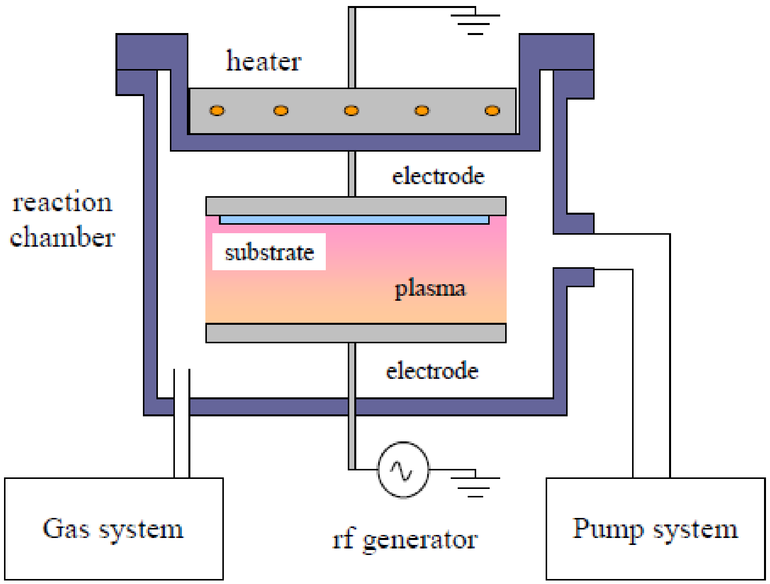
Absorption co-efficient vs energy band gap for various semiconductor materials

Two types of TF-Si: a-Si and μc-Si



Amorphous silicon (a-Si)	Microcrystalline Silicon (μc-Si)
Highly disordered; dangling bonds passivated by hydrogen	Small grains or nanocrystals surrounded by amorphous matrix
Low **μτ** product	**μτ** product a-Si < μc-Si < c-Si
Staebler-Wronski effect leads to light induced degradation	No evidence of Staebler-Wronski effect
Eg ~1.75ev; absorbs visible spectrum	Eg ~1.1ev; absorbs visible + IR
Thickness ~ 0.3μm; low deposition time	Thickness ~ 1-3μm; higher deposition time

Deposition technology



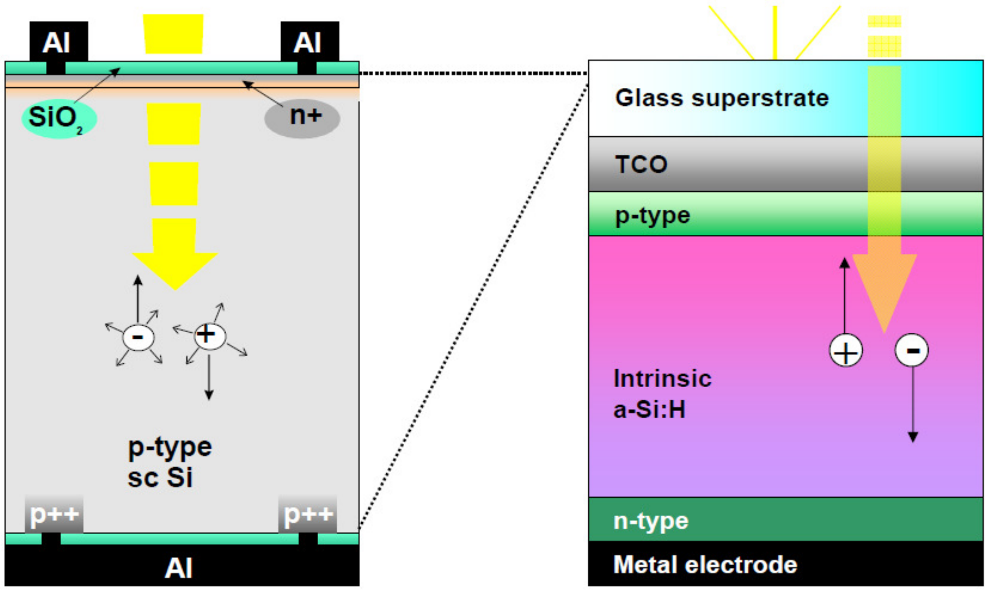
Plasma Enhanced CVD

- Low deposition temperature
- Large area deposition
- Easy doping and alloying
- SiH_4, H_2, PH_3, B_2H_6

	Amorphous silicon (a-Si)	Microcrystalline Silicon (µc-Si)
H_2/SiH_4 ratio	4 to 1 to 25/1	100/1 to 200/1
Power density (mW/cm2)	~ 100mW/cm2	~ 500mW/cm2
Pressure (Torr)	1 to 3 torr	5 to 9 torr
Deposition Rate	3 ~ 5A/s	5 ~ 7 A/s

Key device difference in TF-Si vs c-Si

C-Si devices are p-n junction; TF-Si are p-i-n, Why?

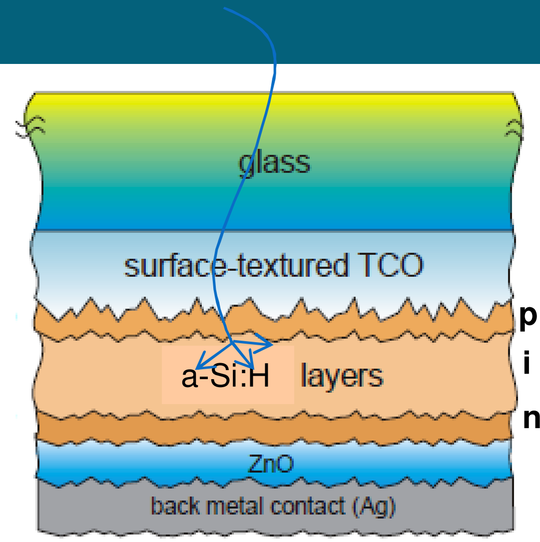


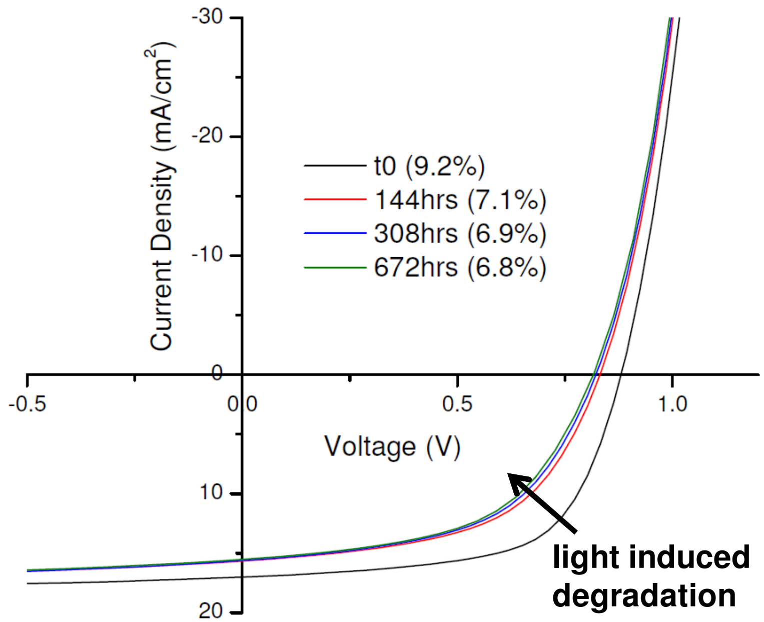
c-Si (200-300 μm)   a-Si:H (0.3-0.5 μm)

- Minority carrier diffusion in c-Si is good; poor in a-Si
- $L_{diff} = \sqrt{D\tau} \approx \sqrt{\frac{k_b T}{q}\mu\tau}$, but $\mu\tau$ is extremely low in a-Si
- Hence, the need for drift driven device, $L_{drift} = \mu\tau E \approx \mu\tau \frac{V_{bi}}{L_i}$
- i-layer in p-i-n provides the internal electric field E

Single junction cells

- Single junction a-Si modules are no longer competitive @ 6% efficiency
- Low efficiency due to lower Jsc (no IR absorption) and low FF (due to light induced degradation)
- The electric field is reduced in degraded state due to charged dangling bonds
- Excess impurities in the film (O, C) will also reduce electric field





Challenges to increase efficiency

Suppress light induced degradation

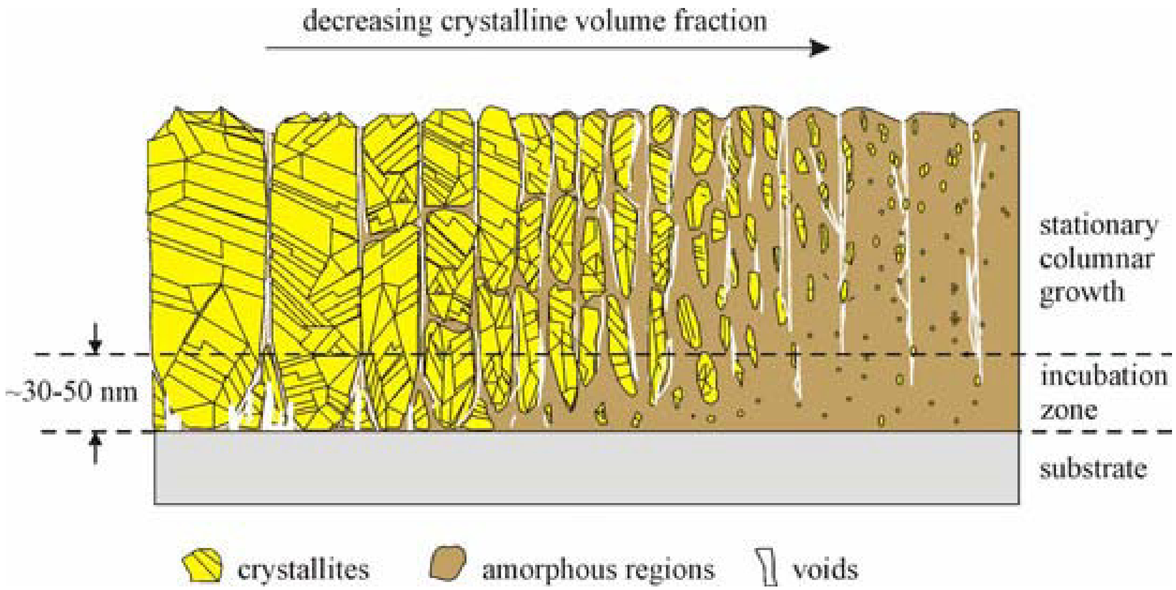
- Stable material like polymorphous Si or μc-Si:H
- Multi-junction cells – a-Si cell receives less light; low LID

Increase efficiency

- Capture light from IR part of the spectrum – use low band-gap materials
- Improve light trapping – multiple light passes
- Multi-junction cells – split the solar spectrum

Microcrystalline Silicon

- Mixed phase material – small crystallites passivated by amorphous matrix
- Highly dilute SiH_4 with H_2 – excess hydrogen etches weaker silicon bonds to create small crystallites
- Hydrogen passivation crucial for device performance

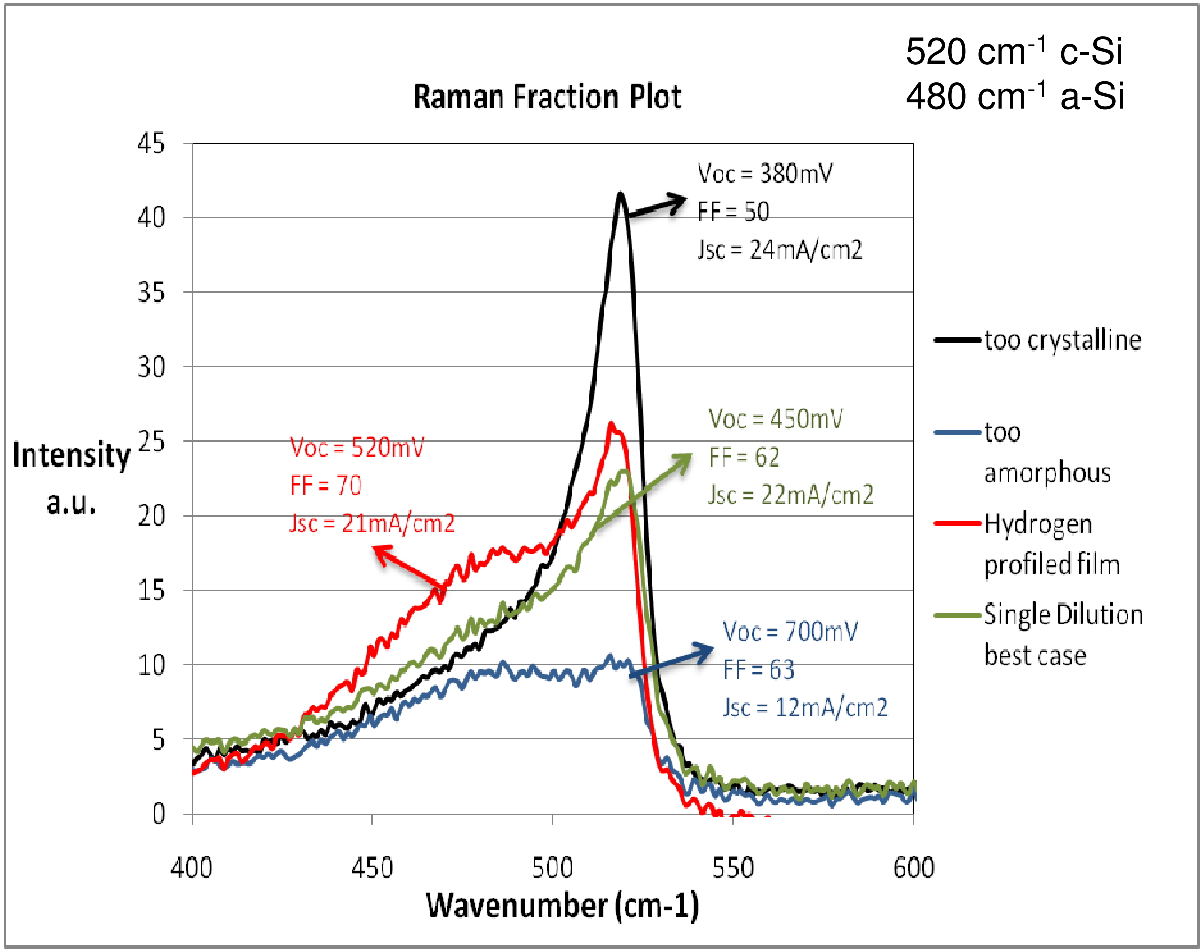


- Incubation amorphous layer should be avoided
- Uniform crystallinity throughout the film is preferred for high Voc
- Avoid ion bombardment to preserve crystal structure

Picture courtesy C. Sholten, IMT Neuchatel

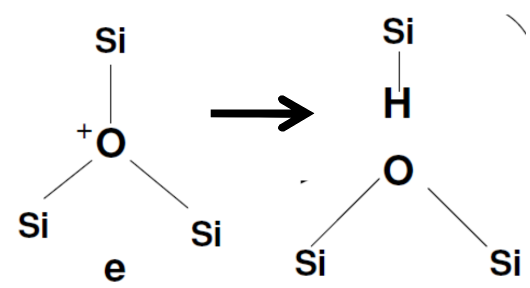
Microcrystalline Silicon

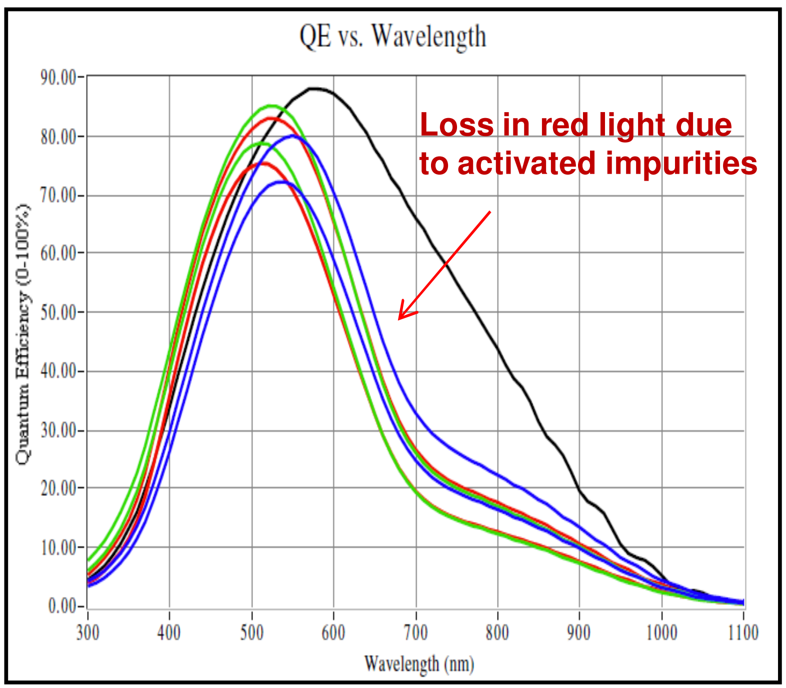
- Raman shift – indication of crystalline fraction (c.f.) in the film
- Strong Voc correlation with crystal fraction ~ 50 to 60% volume c.f. optimum

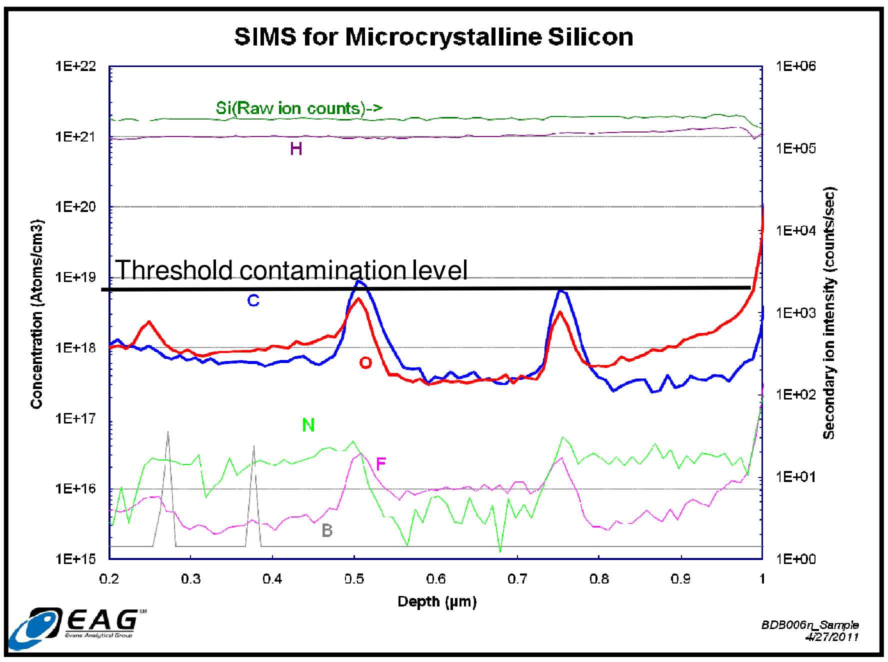


Microcrystalline Silicon

- Device performance highly sensitive to impurity concentration in film
- Reactors have to be maintained contaminant free
- Oxygen acts as a charged defect that reduces the red light response considerably

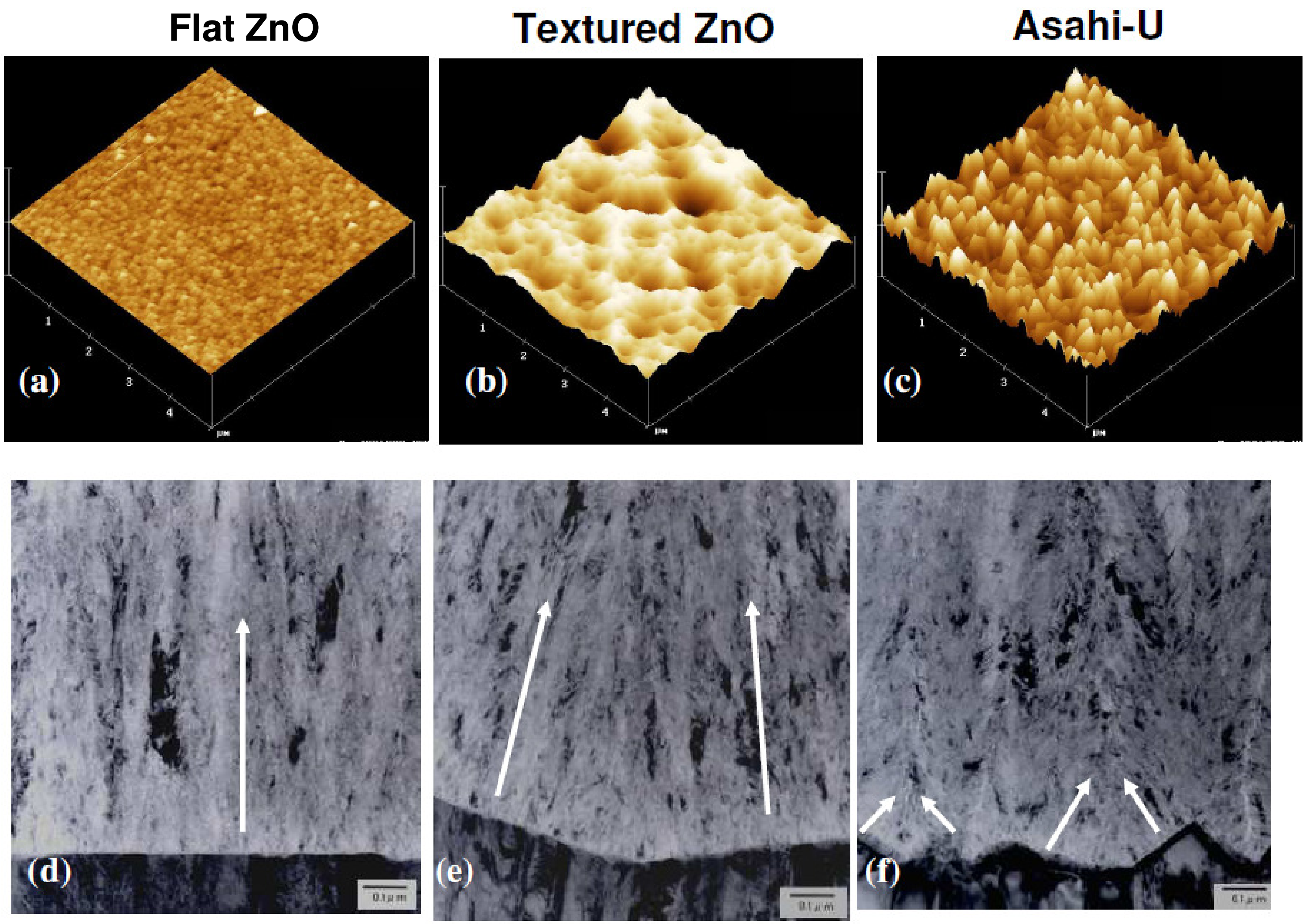






Microcrystalline Silicon

Growth of microcrystalline silicon depends on underlying texture



Picture courtesy of Michio Kondo, AIST

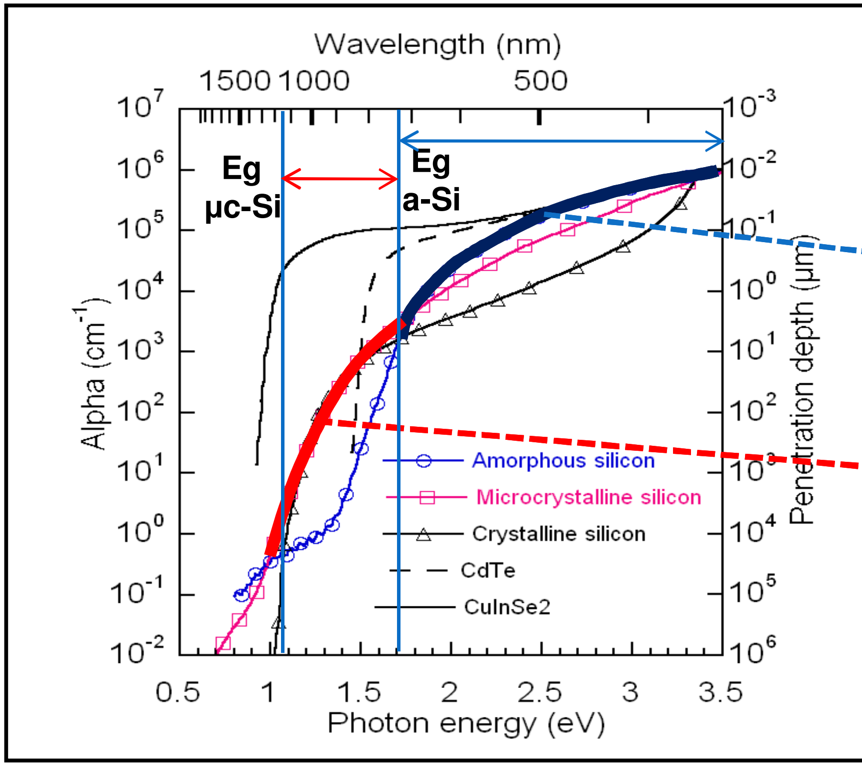
Microcrystalline Silicon

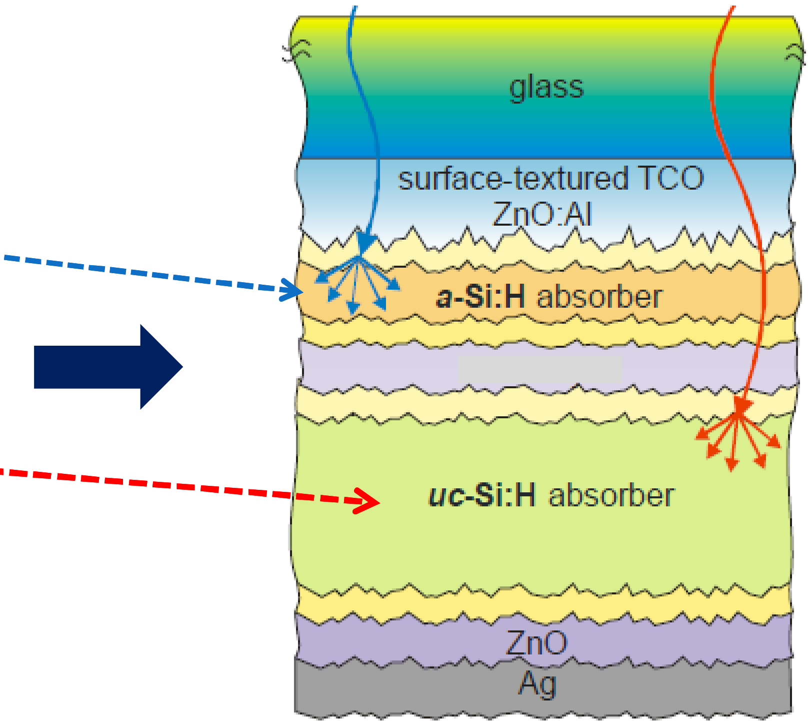
- Single junction microcrystalline silicon cell efficiency ~ 8.0-9%
- V_{oc} = 0.53V , J_{sc} = 22 mA/cm2, FF =0.7 (1.1 μm film)
- J_{sc} being high, single junction mc-Si modules not made (losses in TCO)

How do we increase efficiency of thin film silicon?

- Multi-junction cells – split the solar spectrum (a-Si + μc-Si)
- Capture light from IR part of the spectrum – use low band-gap materials
- Improve light trapping – multiple light passes

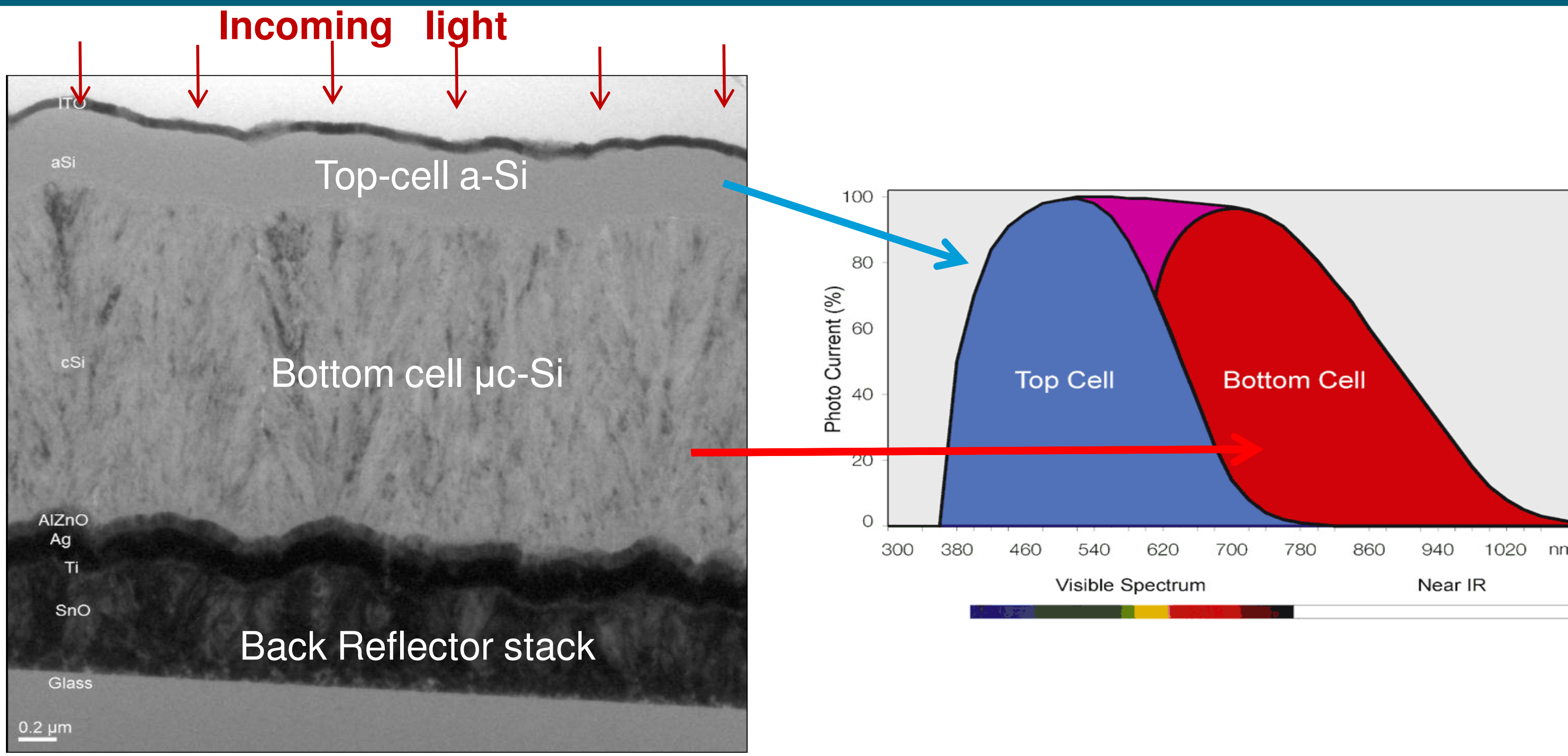
Micromorph or tandem cell





- Split the solar spectrum → a-Si captures visible light and µc-Si IR
- $Voc = Voc_{top} + Voc_{bot}$ and $Jsc = Jsc_{top} = Jsc_{bot}$
- Lower current device means less resistive losses in TCO layers

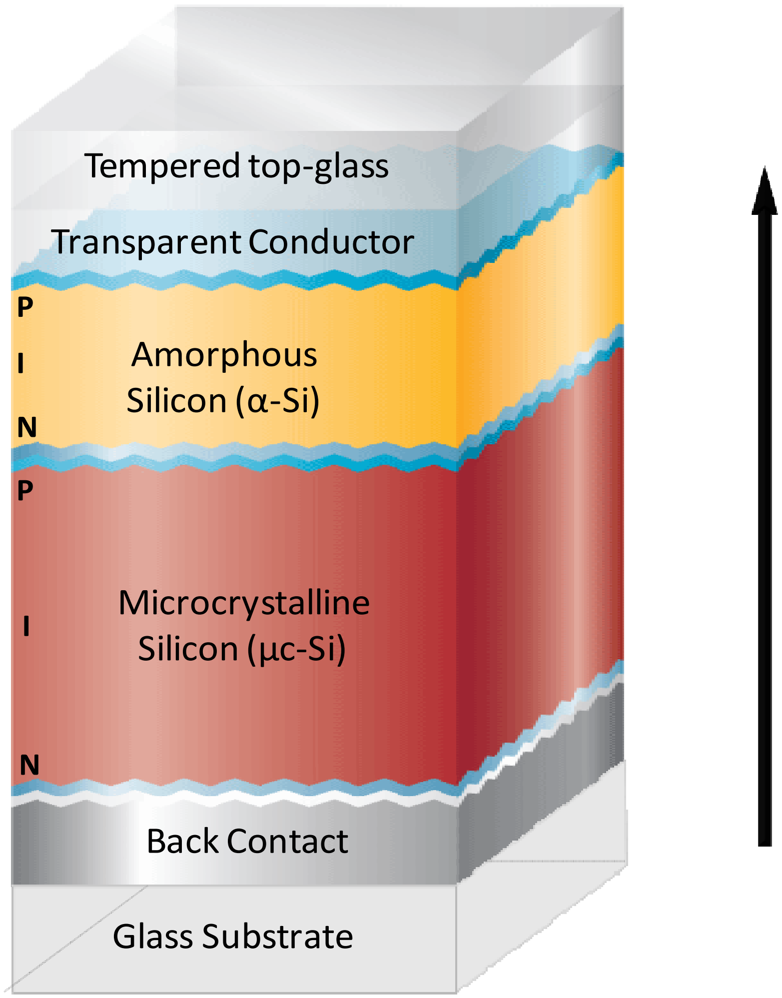
Micromorph or tandem cell



- Energy gaps of 1.1eV(μc-Si) and 1.8eV(a-Si) are optimal combination
- Top cell receives less light leading to reduced overall LID
- A-Si thickness ~ 0.3μm and μc-Si thickness ~ 1-3μm.
- Standard lab stable cell efficiencies 11-12%. Production module efficiencies between 8-10% (Sharp, Oerlikon, MHI)

The ThinSilicon Way

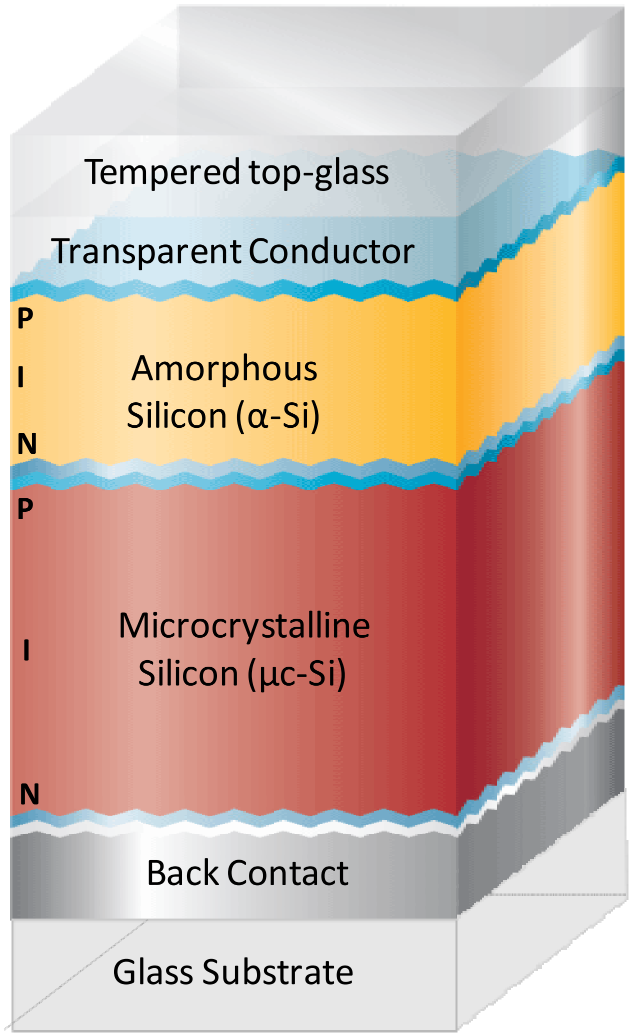
- All glass based TF-Si companies do superstrate or p-i-n configuration
- ThinSilicon pursues substrate or n-i-p configuration. Why?



- Tempered top glass
- Increased Voc
- Reduced degradation
- Increased photocurrent
- Increased deposition rate
- Improved light trapping

Benefits of Substrate configuration

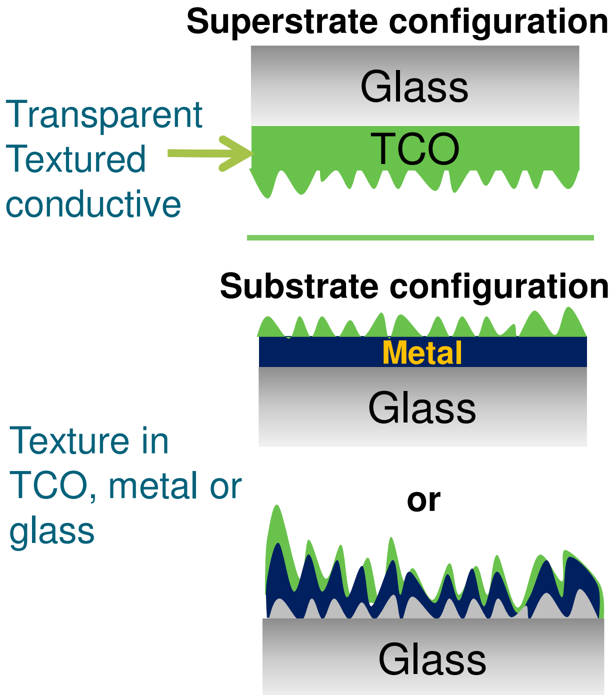
1. High temperature a-Si deposition



- In superstrate or p-i-n, temperature of a-Si i-layer <200C due to boron diffusion
- For substrate or n-i-p, temperature of a-Si can be >200C – no boron diffusion
- Increased a-Si temperature reduces band gap – leads to higher Jsc in the red
- High temperature films more stable leading to lower LID. (Si-H >> Si-H2)
- Higher temperature a-Si can be deposited at higher rates

Benefits of substrate configuration

2. Improved light trapping



- In superstrate or p-i-n, front TCO needs to be transparent, textured & conductive
- For substrate or n-i-p, the back reflector provides texture & conductivity – need not be transparent
- This greater degree of freedom opens up several avenues of providing texture

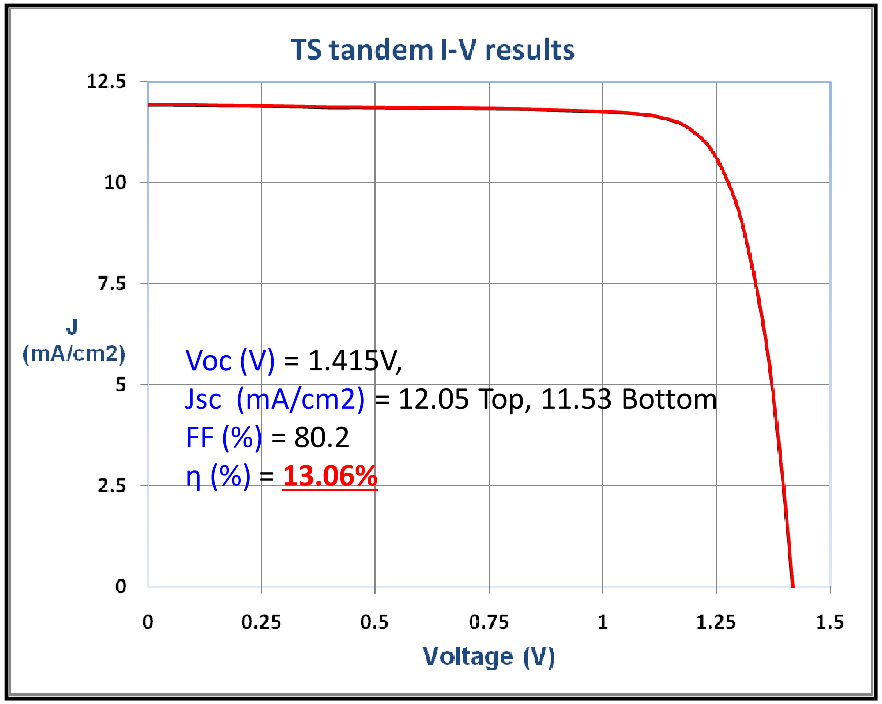
3. Higher Voc in a-Si cell

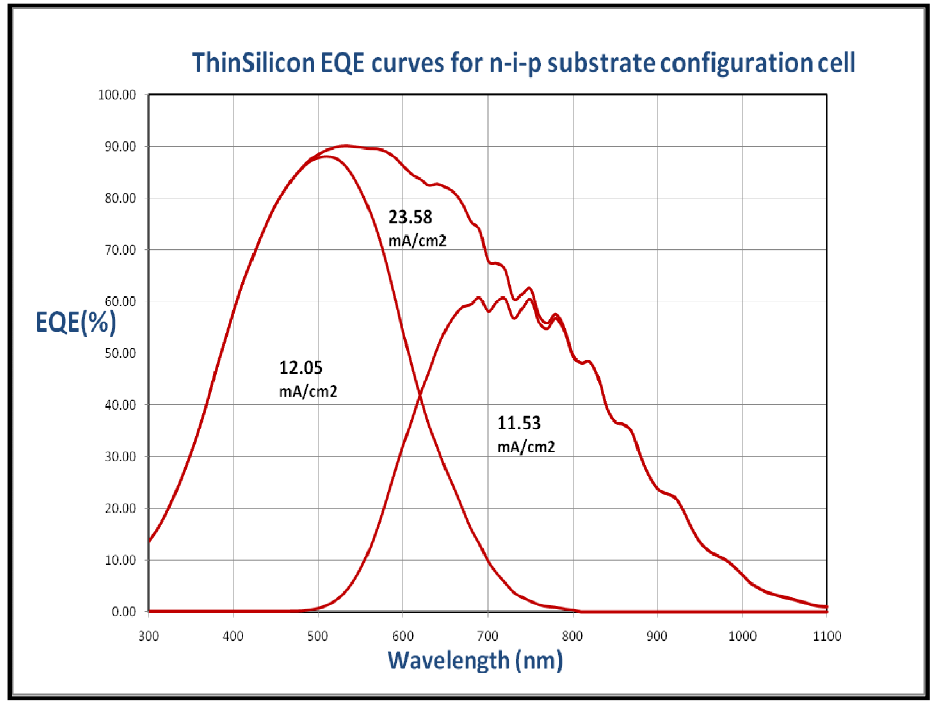
Protocrystalline p-layers possible in substrate or n-i-p configuration; results in higher Voc due to high bandgap

Module Fabrication

- Laser scribing used to make monolithic integration of module
- Green and IR lasers used to remove each layer
- Superstrate configuration uses glass side scribing
- Substrate configuration uses film side scribing
- Production laser scribing speeds of 1m/s are routine

ThinSilicon Efficiencies





- State of the art cell efficiencies 13%+.
- Considering LID and other losses, module efficiencies > 10%+ modules
- No special interlayers or AR coatings used
- Technology transfer to GEN5 size PECVD reactor underway
- Production level depositon rates used

Path to 12% modules

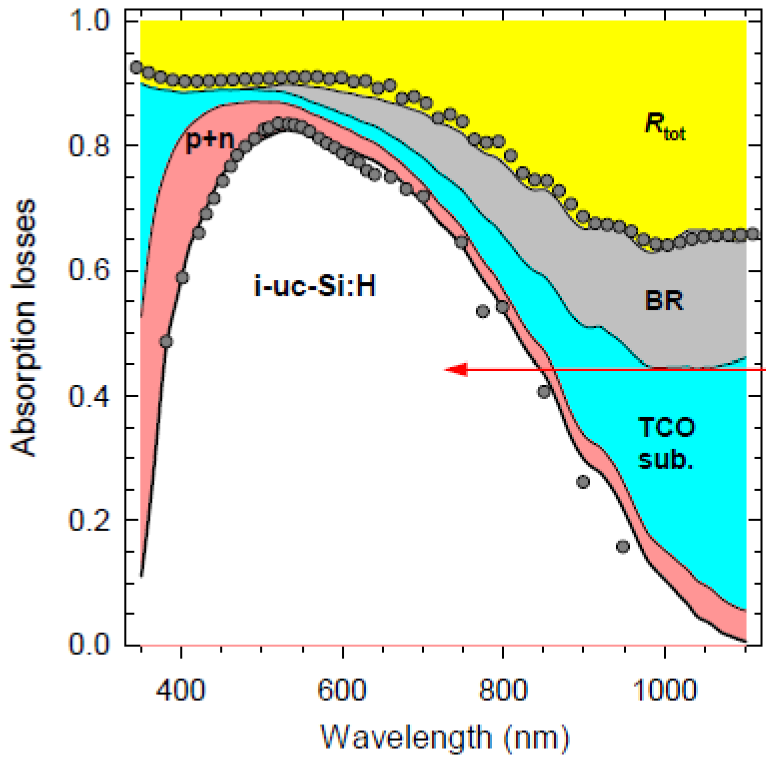
- 10% modules not good enough to compete with competition
- But 12% modules @ 0.5$/watt very attractive
- Stable cells of 13.8% needed

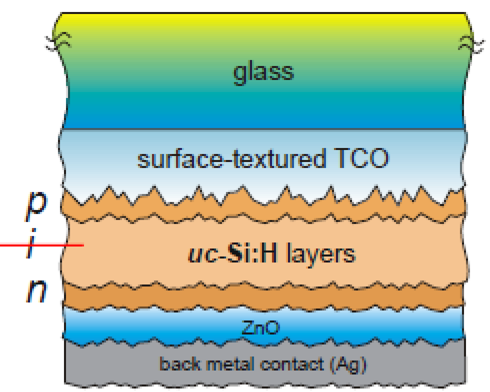
How do we get there?

- Multi-junction cells – split the solar spectrum (a-Si + μc-Si)
- Capture light from IR part of the spectrum – use low band-gap materials
- Improve light trapping – multiple passes to increase absorption
- Some modeling results would be helpful

Optical and Electrical Modeling

- Janez Krc modeled several losses taking place as light enters the cell
- What if we were able to absorb most if not all of the light?





Janez Krc.

Source Janez Krc 2007 MRS Sym Proc

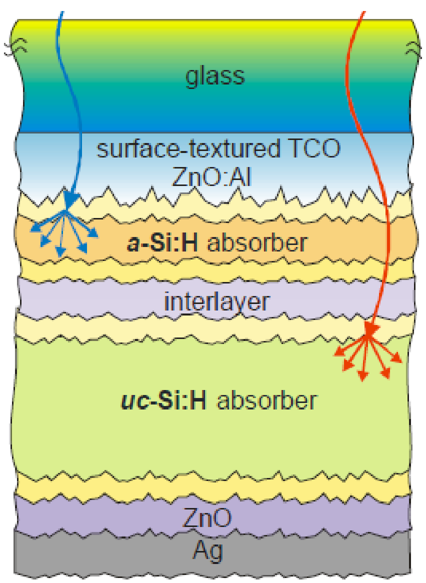
Optical and Electrical Modeling

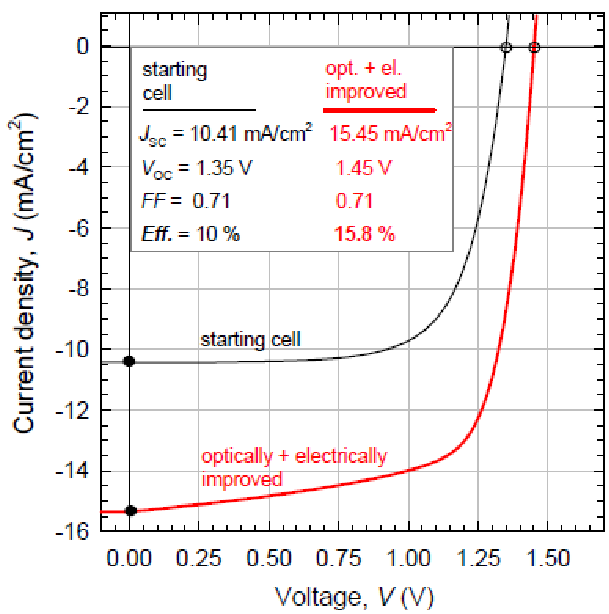
Janez Krc et al. performed optical & electrical modeling using simulator SUNSHINE

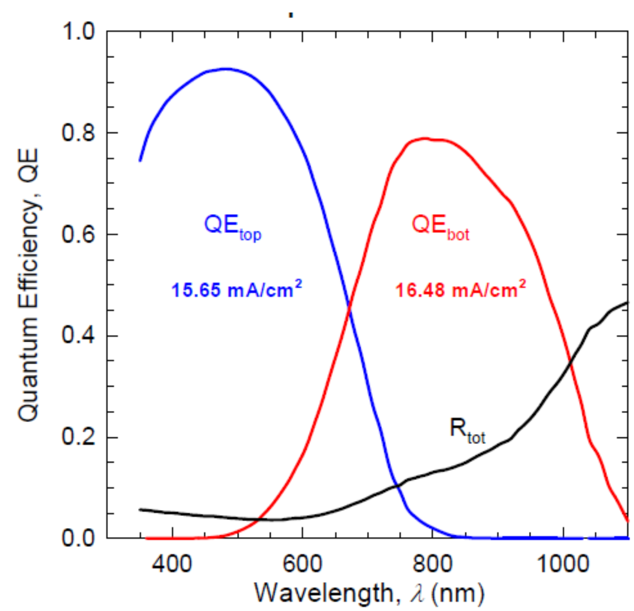
Several assumptions made to construct an ideal tandem cell

- Ideal TCO haze parameters H = 1
- Broad (lambertian) angular distribution function (ADF) of scattered light
- Reduced absorption in optically non-active layers (TCO & doped layers)
- Improve back reflector with enhanced reflectance of 98% (presently @ 80%)
- Improve light in-coupling by ARC, intermediate reflector

Ideal tandem stable solar cell efficiency = 15.8% → 13.5% module efficiency







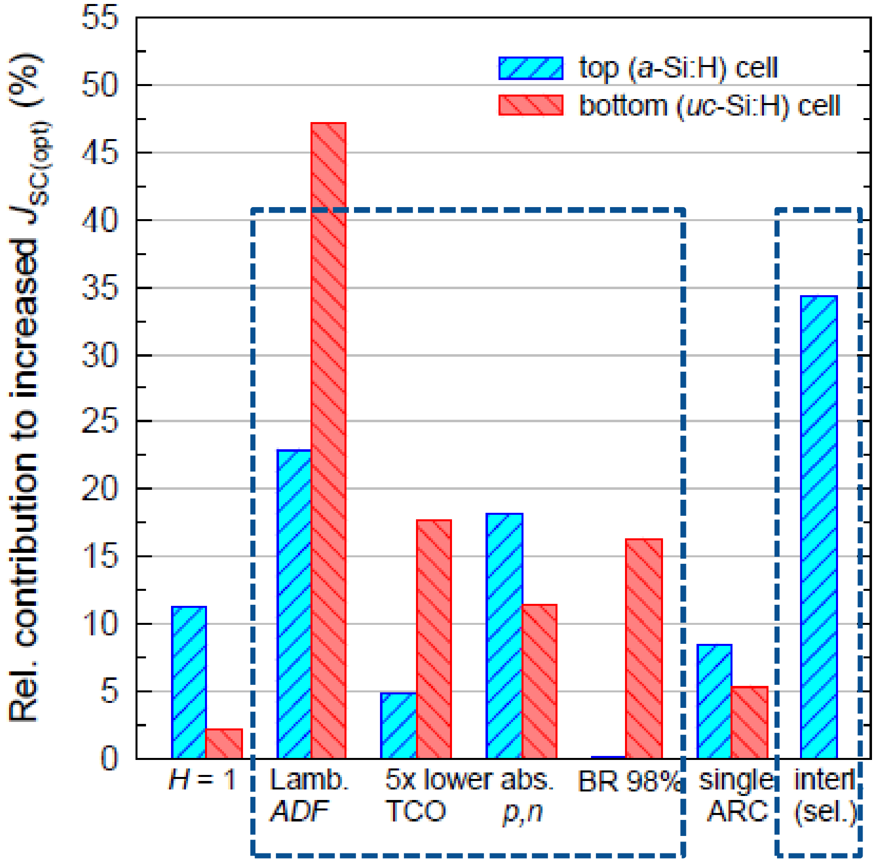
Source Janez Krc 2007 MRS Sym Proc

Optical and Electrical Modeling

- Almost all of the η increase comes from Jsc
- Several assumptions contribute differently to Jsc of top and bottom cell

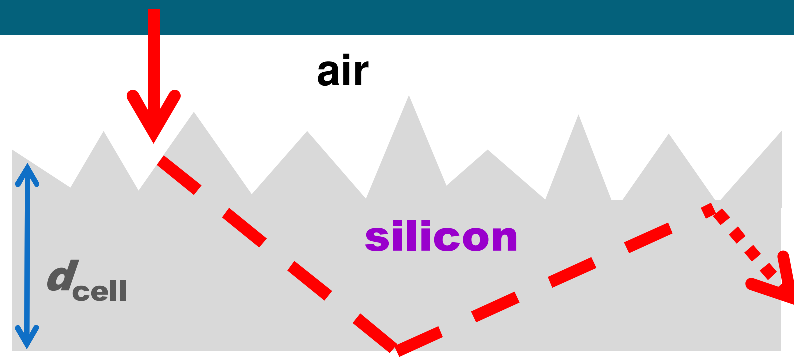
Areas of focus for ThinSilicon

- Make back reflector texture as close to lambertian as possible
- Reduce optical absorption in doped layers
- Reduce plasmon absorption at back TCO/metal interface



Source Janez Krc 2008

Light trapping



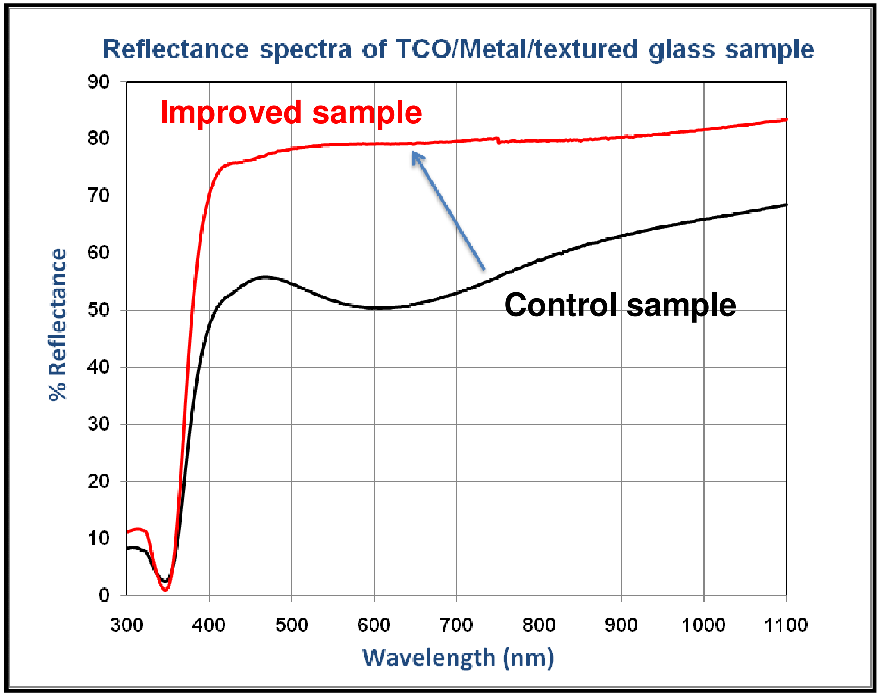
- Increase optical path length in silicon
- Optical path is **m** times longer than cell thickness
- Yablonovitch et al. calculated **m = 4n²**.For air-semiconductor system m ~ 50
- But for TCO-semiconductor system, **m ~ 16**
- Present calculated value of m in a standard uc-Si cell is 5. (5 passes only)
- There is room for improvement! How?

Possibly 2 ways

- Reduce plasmonic absorption at metal-TCO interfaces
- Improve texture of back contact to induce internal reflection

Absorption losses in TCO/metal systems

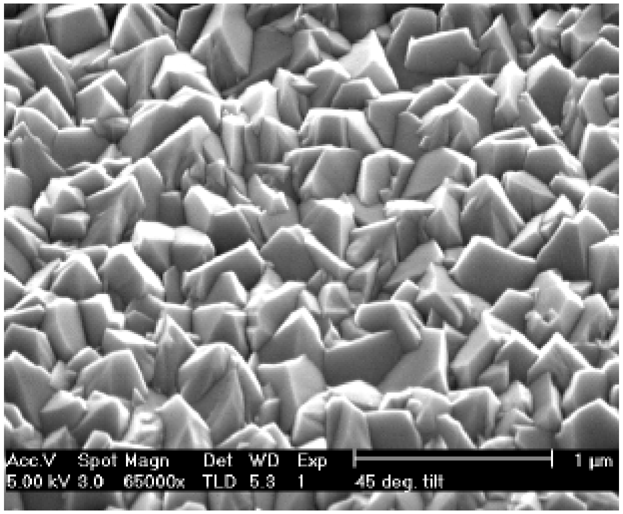
Reflectance Spectra



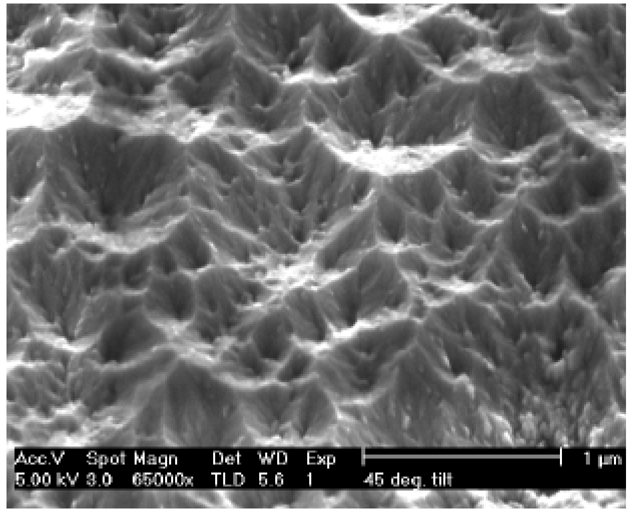
- Significant increase in reflectance of TCO/metal systems
- Overall efficiency increase by 10% relative
- Significant, but still lots of room to improve

Different types of back contact texture

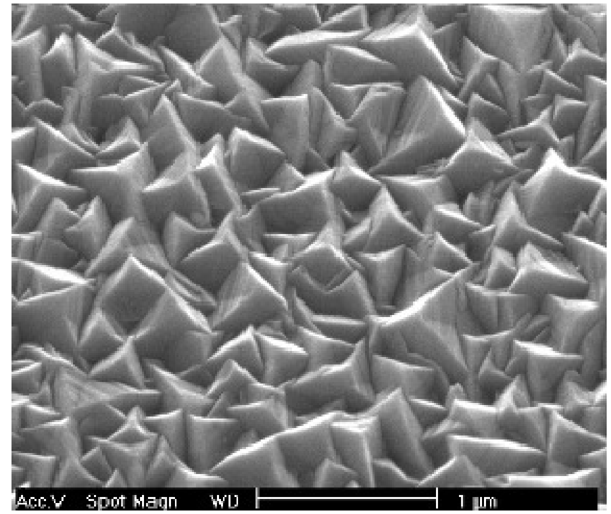
None of the commercially available textured TCO films provide ideal light trapping



SnO2:F



Wet etched ZnO:Al



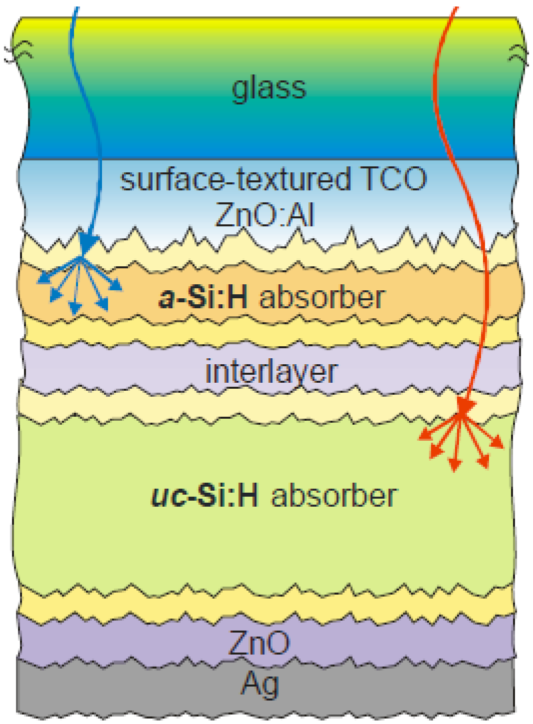
LPCVD ZnO:B

Some novel ideas include

- Texturing glass off the float line – Dow Corning, Intersolar 2011
- Substrate with nanocones – Professor Yi Cui, Stanford University
- Plasmonic nanostructures – Professor Harry Atwater, Caltech
- Diffraction gratings 1-D, 2-D – Professor Miro Zeman, Delft University

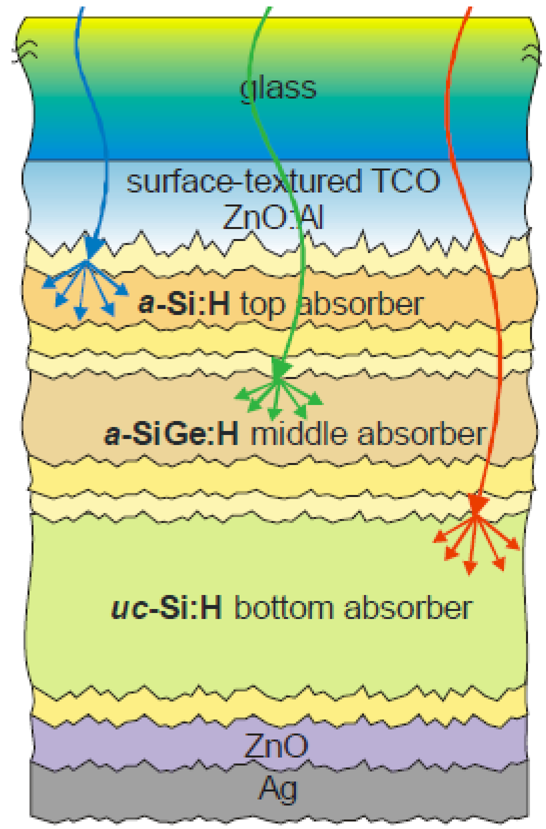
Other advanced cell concepts

Tandem cell with Intermediate Reflector



- Interlayer reflects light back into the top cell
- Need for interlayer to be transparent and conductive

Triple junction cell

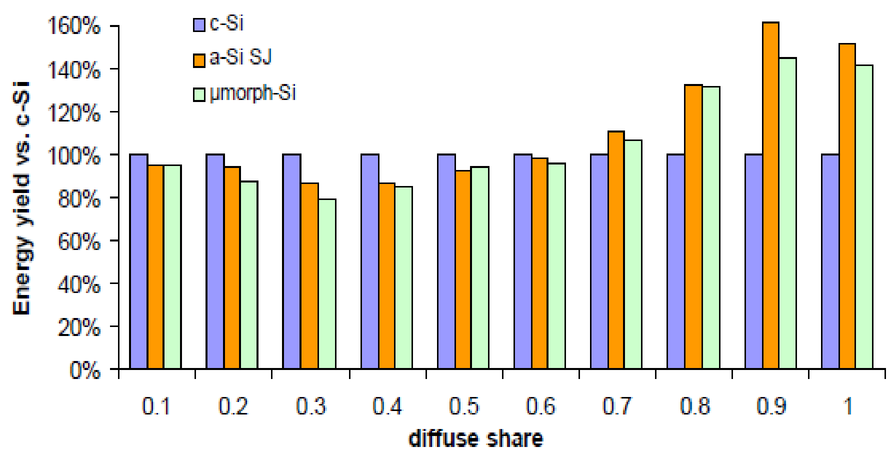


- Without Ge, difficult to reduce band gap of middle cell
- Increases manufacturing complexity

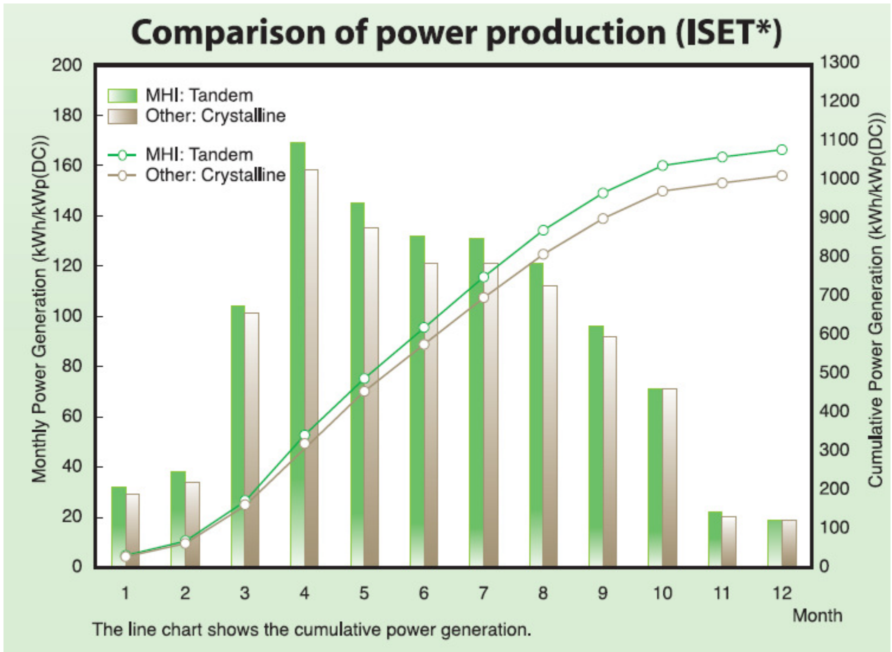
Energy Yield Output of thin film silicon

Energy Yield = Energy output (kwh) / Rated Watt (W)

- Thin film silicon has higher energy yield than c-Si in hot climates and diffuse light conditions
- Amorphous silicon has lower power loss temperature coefficient (-0.2%/K for a-Si vs -0.4%/K for c-Si)
- Thin film Silicon performs better under highly diffuse light conditions – due to blue rich spectrum



Grunow et al, 24th PVSEC Conference



Mitsubishi tandem module data sheet

Summary

- Present status of thin film silicon ~ 8-10% module efficiency
- ThinSilicon's substrate configuration allows possibility of >10% module efficiency
- To reach 12% module efficiency, significant improvement in light trapping is needed

Questions?

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