Key Junction Technology Points From: IWJT-2011 & VLSI Symposium 2011 for Tri-Gate and UTBB-SOI & 37th IEEE-PVSC 2011

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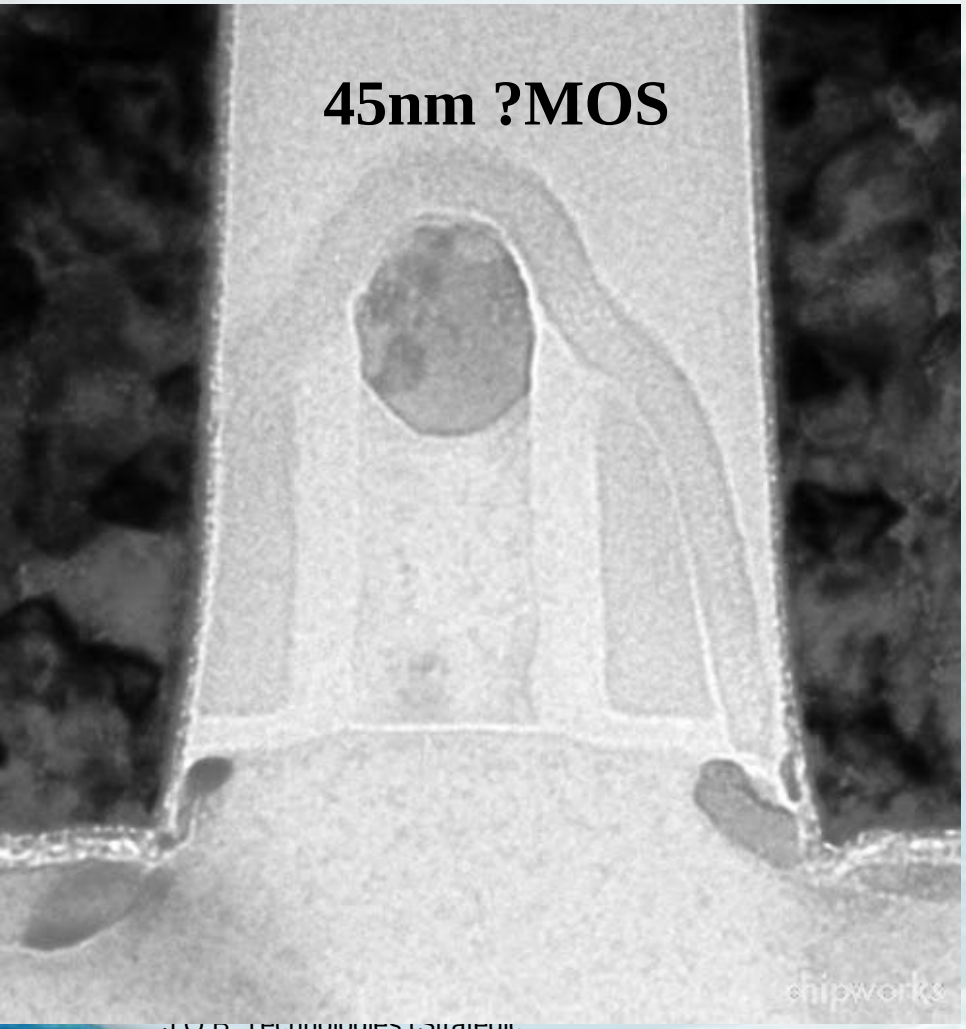
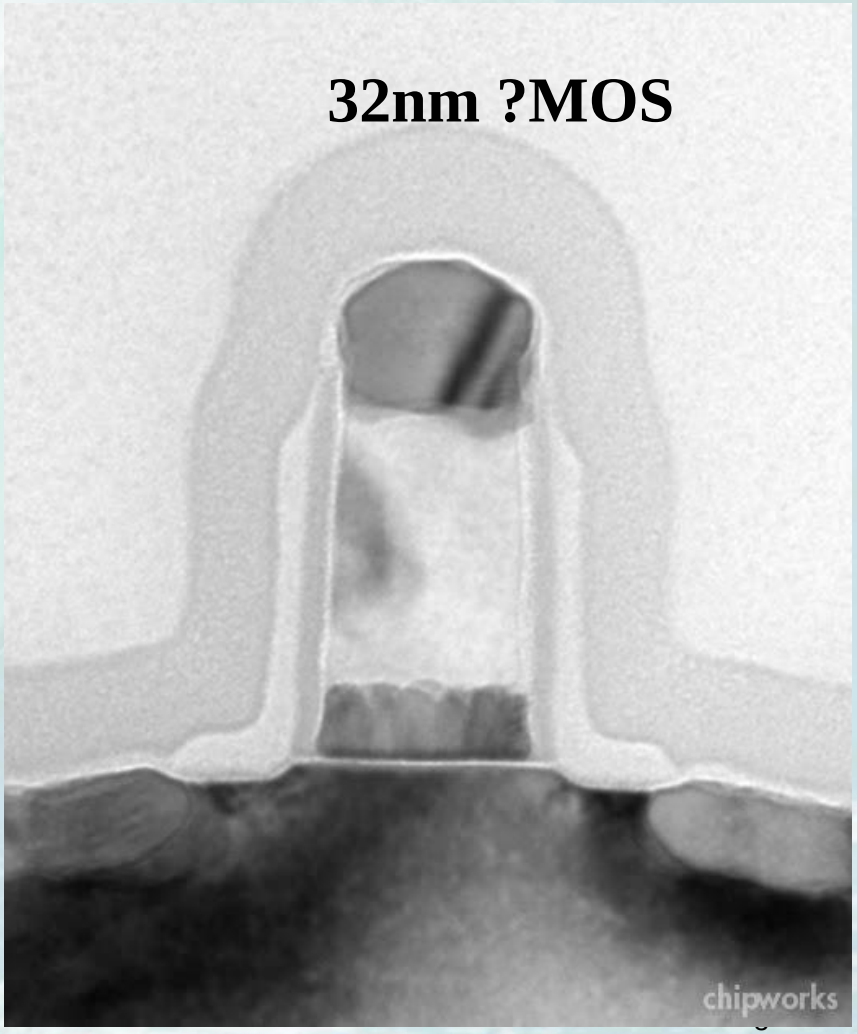
Outline

- Introduction: 32/28nm, & 22/20nm nodes
- Tri-Gate Doping reports from VLSI Sym & International Workshop on Junction Technology June 2011 Kyoto, Japan
  - Evening panel rump session on “Can Fin/FET/FD-SOI Compensate for the Stagnation in Scaling?”
  - IMEC & JOB on beam-line and IBS on plasma FinFET doping
  - IBM/Alliance & Toshiba/Japan papers on Tri-gate
- FD-SOI Doping reports from VLSI Sym & International Workshop on Junction Technology June 2011 Kyoto, Japan
  - IBM/Alliance 2 papers on UTBB-SOI
  - MIRAI/Selete papers on NFET Vt variation dominated by B-HALO TED!
- 37th IEEE-PhotoVoltaic Specialist Conference June 20-24, 2011 Seattle, WA
  - Selective Emitter Formation by: 1) Laser Diffusion Doping, 2) Dopant Paste or 3) Patterned Implantation
- Summary

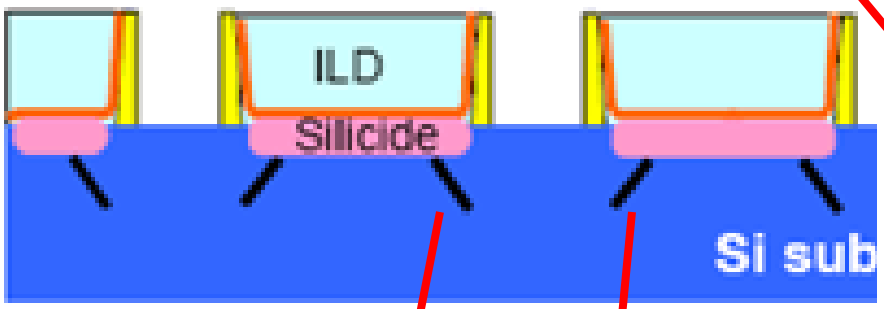
Panasonic/Matsushita 32nm Node HK/MG First Only Dual Stress Liner, No eSiGe & No Stacking Fault Stressor

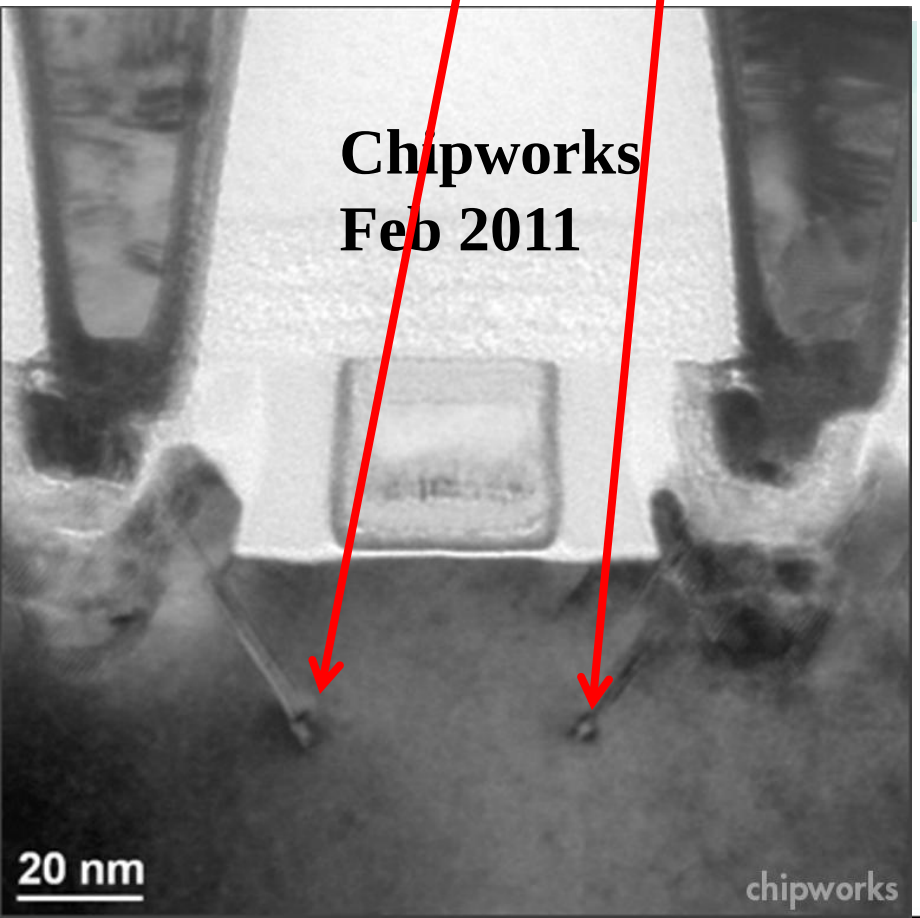




Chipworks Feb 2011

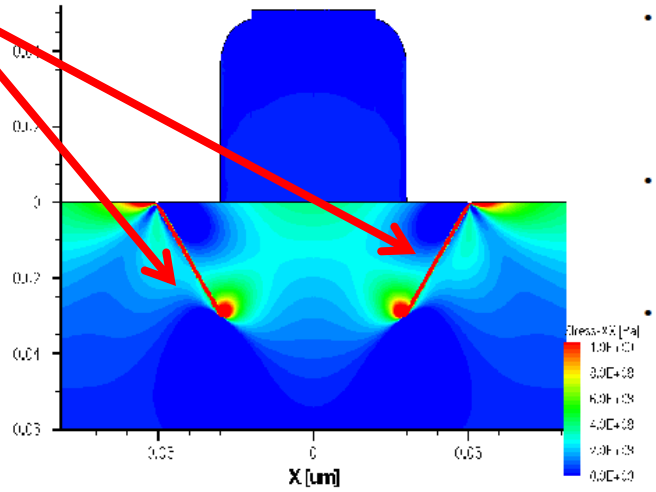
Intel's 32nm Node With Stacking Fault Stressor!





Chipworks Feb 2011

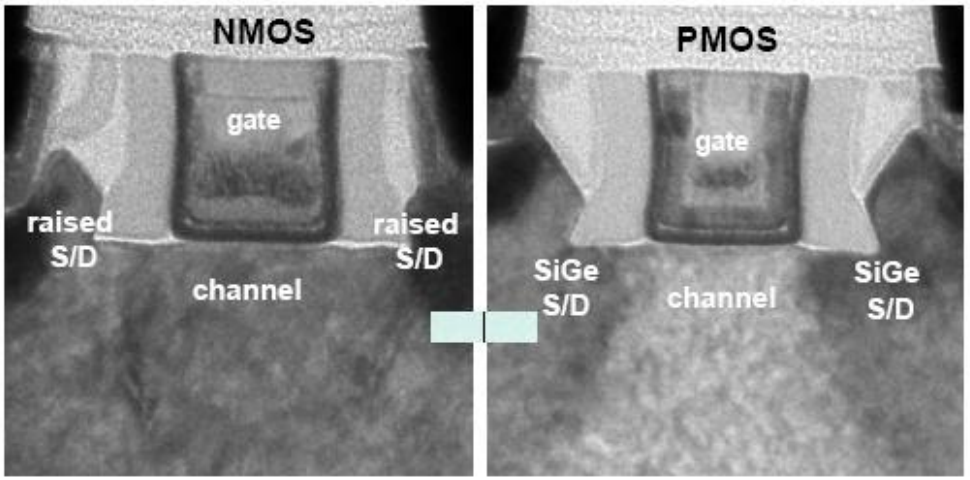
Stress Induced by {111} Stacking Fault



- Missing (i.e. vacancy) {111} plane due to SMT for a 30nm deep amorphized Si
- ~350 MPa tensile longitudinal stress is present in the channel
- There is compressive stress in dark blue areas, but it is not shown here to better see details of tensile stress distribution

Synopsys Dec 2010

SYNOPSYS® Predictable Success



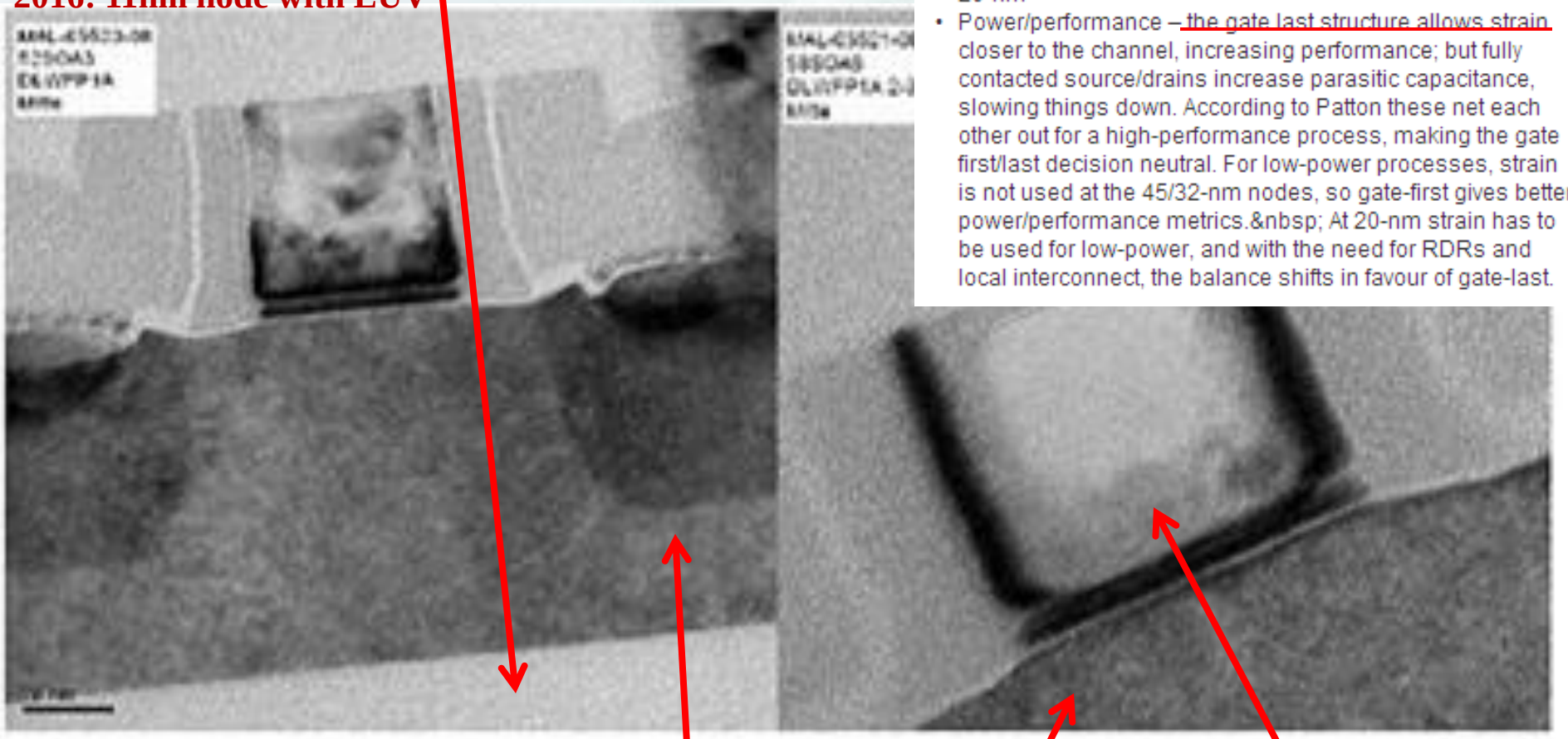
Intel IEDM 2009

Fig. 5 - Cross section of NMOS and PMOS devices showing raised S/D regions for reduced parasitic resistance.

Jan 18, 2011
IBM/GF/Samsung CPT
22/20nm PD-SOI

2014: 14nm node with double exposure and a change to EUV
2016: 11nm node with EUV

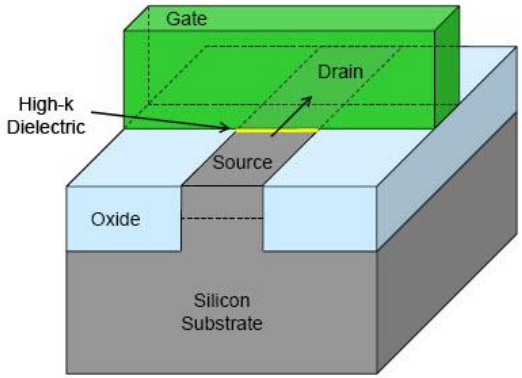
- Density – gate-first has higher density, since gate-last requires restricted design rules (RDRs). That prevents orthogonal layout, requiring local interconnect; but at 20-nm RDRs are needed for lithography, so that advantage disappears.
- Scaling – it's easier to scale without having to cope with RDRs; at 20-nm there's no choice.
- Process simplicity – it's obviously easier to shrink if you can keep the same process architecture, whether it be to 32- or 20-nm
- Power/performance – the gate last structure allows strain closer to the channel, increasing performance; but fully contacted source/drains increase parasitic capacitance, slowing things down. According to Patton these net each other out for a high-performance process, making the gate first/last decision neutral. For low-power processes, strain is not used at the 45/32-nm nodes, so gate-first gives better power/performance metrics. At 20-nm strain has to be used for low-power, and with the need for RDRs and local interconnect, the balance shifts in favour of gate-last.



GLOBALFOUNDRIES PMOS and NMOS (right) Gate-Last Transistors [2]

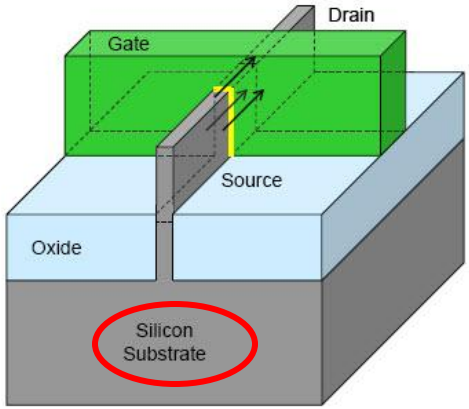
Intel Press Release May 4, 2011: 3-D Tri-Gate For 22nm Node

Traditional Planar Transistor



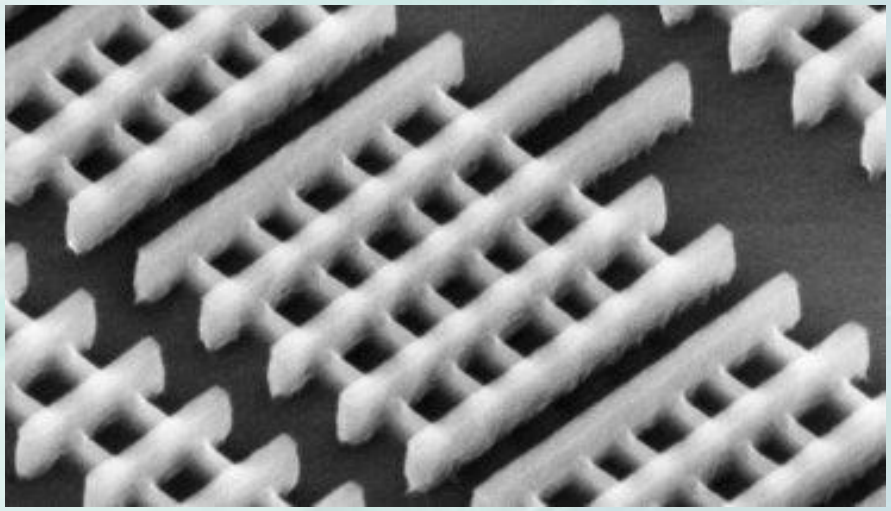
Traditional 2-D planar transistors form a conducting channel in the silicon region under the gate electrode when in the "on" state

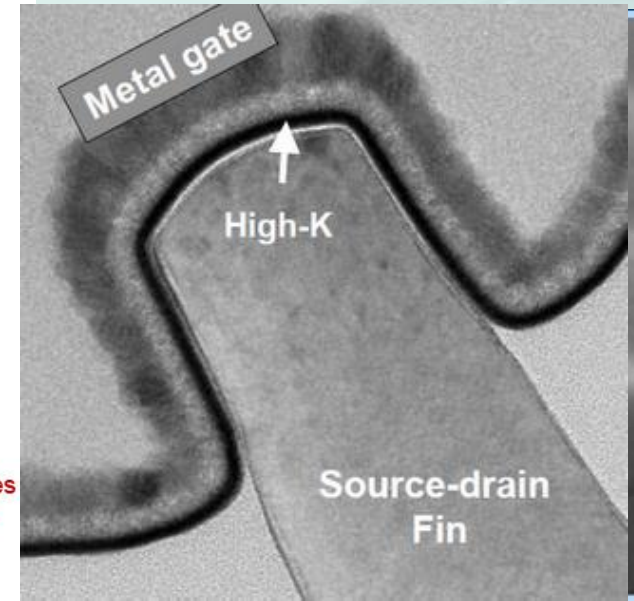
22 nm Tri-Gate Transistor

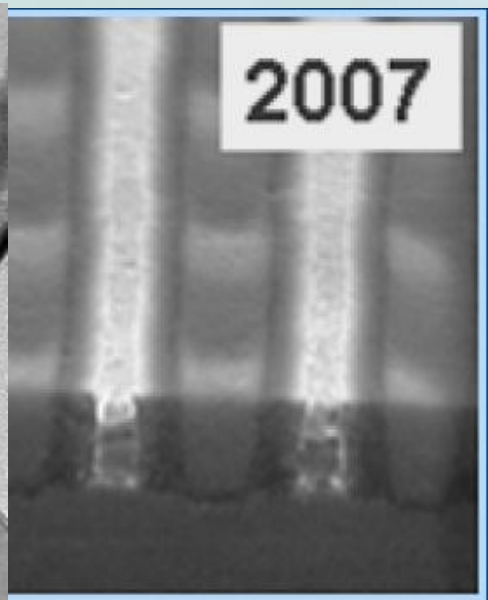


3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

Transistors have now entered the third dimension!







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  - IMEC, JOB and IBS on FinFET doping
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R-1: Can FinFET/FDSOI Compensate for the Stagnation in Scaling?

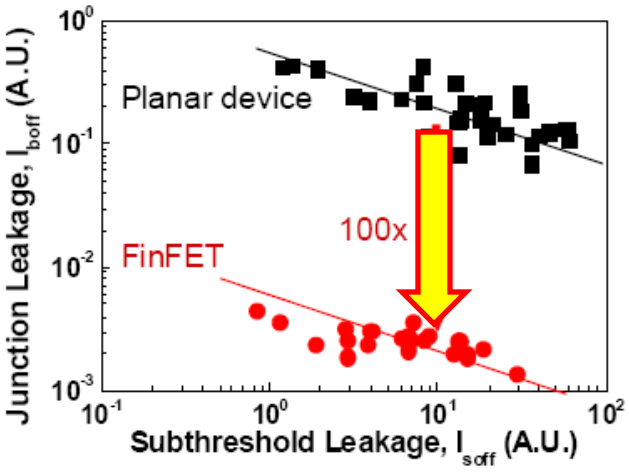
Moderators: M. Hane, *Renesas Electronics Corp.*
C. Mazure, *Soitec Group*

Panelists: A. Strojwas, *PDF Solution*
C. Hu, *Univ. of California, Berkeley*
K. Okada, *Tokyo Institute of Technology*
M. Bohr, *Intel Corp.*
M. Haond, *STMicroelectronics*
S. Venkatesan, *GLOBALFOUNDRIES*

CMOS Bulk technology is facing serious issues with respect to further device down scaling in spite of the fact that many new technologies have successfully been developed, such as strain techniques, high-K dielectric and metal-gate-electrode. Despite that, performance scaling trend seems to stagnate when moving towards further advanced CMOS nodes. Fully-depleted (FD)-devices (planar SOI or Fin-type) are known as promising device structures for revitalizing CMOS scaling by means of the short-channel-effect mitigation, lower leakage, smaller variability, and so on. Such the new device structures will strongly impact not only on LSI core device/process technology but also on chip modules architecture and circuit design paradigm. This panel discussion will be aimed at addressing key challenges for the introduction of planar-FDSOI or Fin-FET in conjunction with future technology scaling prospects, and several key questions:

- How Fin-FET/FDSOI can be integrated within an LSI chip?
- On such a chip, should Fin-FET/FDSOI be applied for the whole area, including analog circuit, or for a partial area, such as SRAM blocks?
- Which generation would be practically viable for Fin-FET/FDSOI introduction and what are the specific reasons for this?

22/20nm FinFET CMOS



CC Wu, TSMC, IEDM-2010, paper 27.1

Figure 15. N-FinFETs junction leakage decreases by 100 times at the same I_{soff} leakage compared to the planar NFETs using similar process conditions.

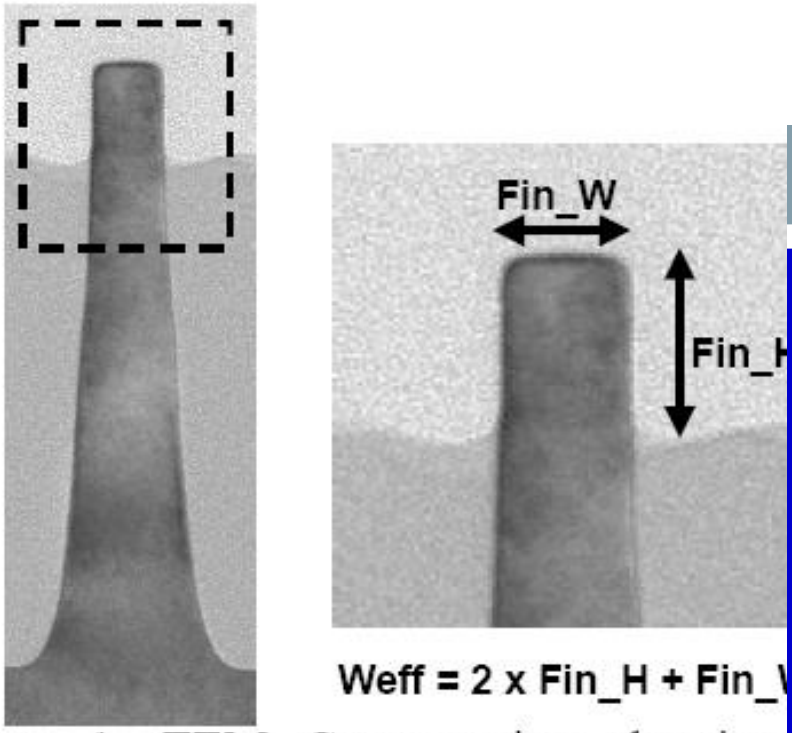
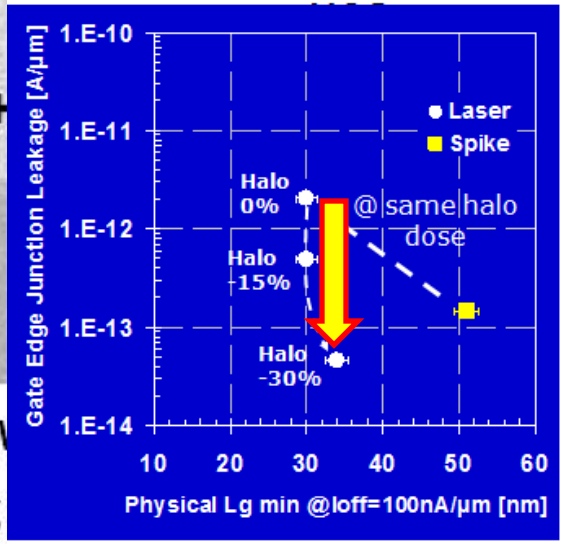


Figure 1. TEM Cross-section showing vertical fin sidewall in the area of interest.

Junction leakage 'pragmatic' containment

Halo dose reduction



- Spike → Laser : 10x penalty in junction leakage
- Diffusion-less → **halo strength can be dramatically reduced** without SCE control loss
- Huge reduction in Band-To-Band tunneling leakage

Halo dose: 0% → As 3.5e13 cm-2

Lower Tri-Gate Channel/HALO Doping

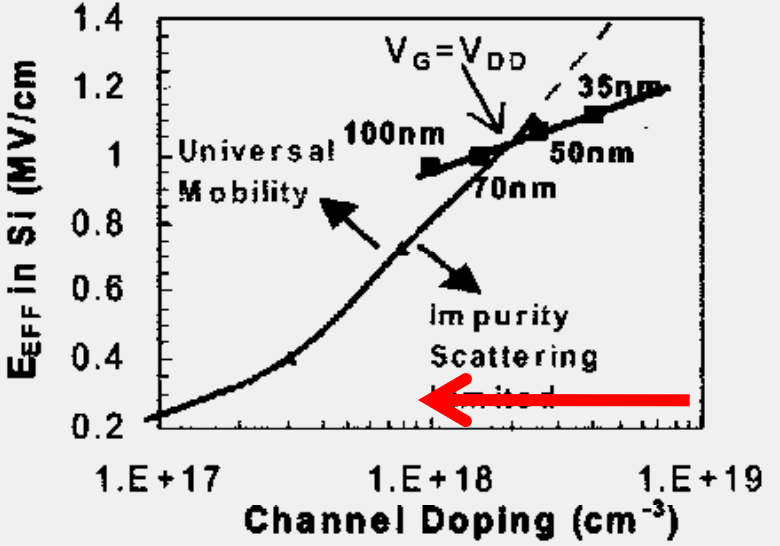
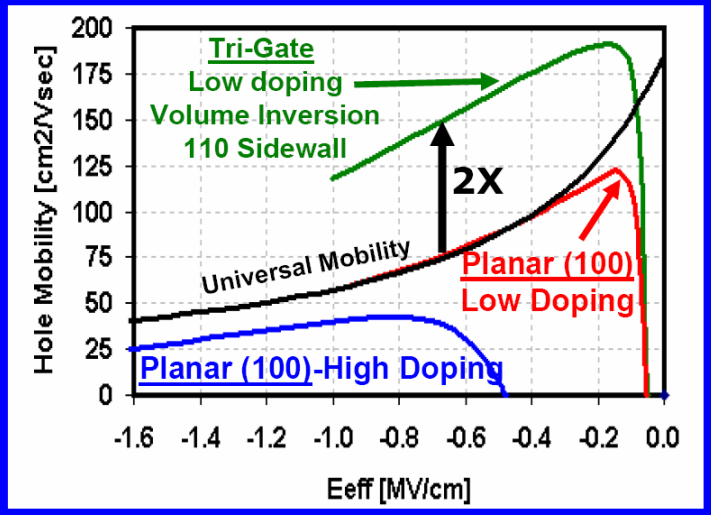


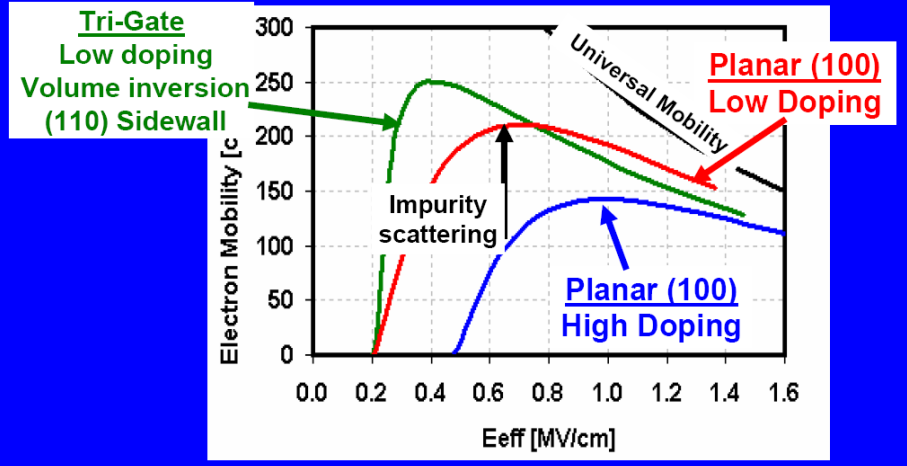
Fig. 5 Universal mobility vs. channel impurity scattering dominated regimes. Device falls off the universal mobility controlled regime for 35nm L_{GATE}.

PMOS Tri-Gate Mobility (Long Channel)



Low doping and the <110> sidewall surface leads to over 2x increase in hole mobility

NMOS Tri-Gate Mobility (Long Channel)



- 40% long channel mobility improvement comes from low body doping in Tri-Gate at low to moderate vertical fields
- Minimal mobility degradation due to <110> sidewall and surface roughness scattering

S2-1 paper by Sue Felch of IBS on plasma doping of Fin structures. Sue showed that the plasma process can be varied from deposition mode to implantation to etching and that conformal doping of 3-D Fin structures can be produced by selecting process conditions where deposition and implant are more dominant than etching. What surprised me was when she showed the As doping SIMS profiles after anneal compared to boron in Fig.4. A huge lose in As dopant level was detected from 2E21/cm3 before anneal to <5E19/cm3 after anneal for a loss of >30x (97%) as shown in SIMS of Fig.7. This might explain why Applied reported having to use an in-situ oxide capping layer for their Conforma plasma doping system. Without an oxide cap Applied reported an arsenic surface dopant loss of >65% after anneal!

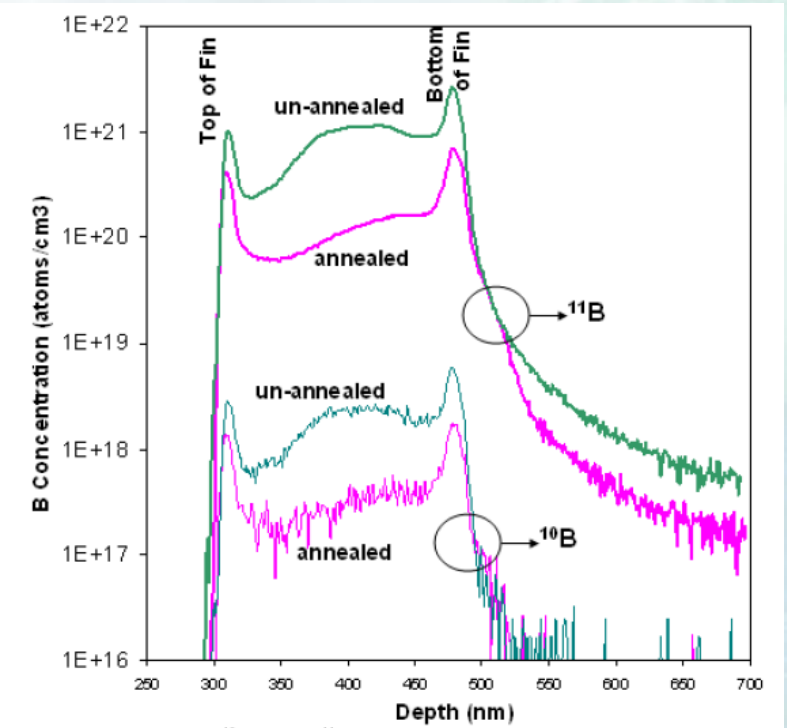


Figure 4: SIMS ^{10}B and ^{11}B isotope depth profiles through the un-annealed and annealed BF_3 plasma doped fins. The spikes at the top and bottom correspond to the top of the fin and the trench bottom.

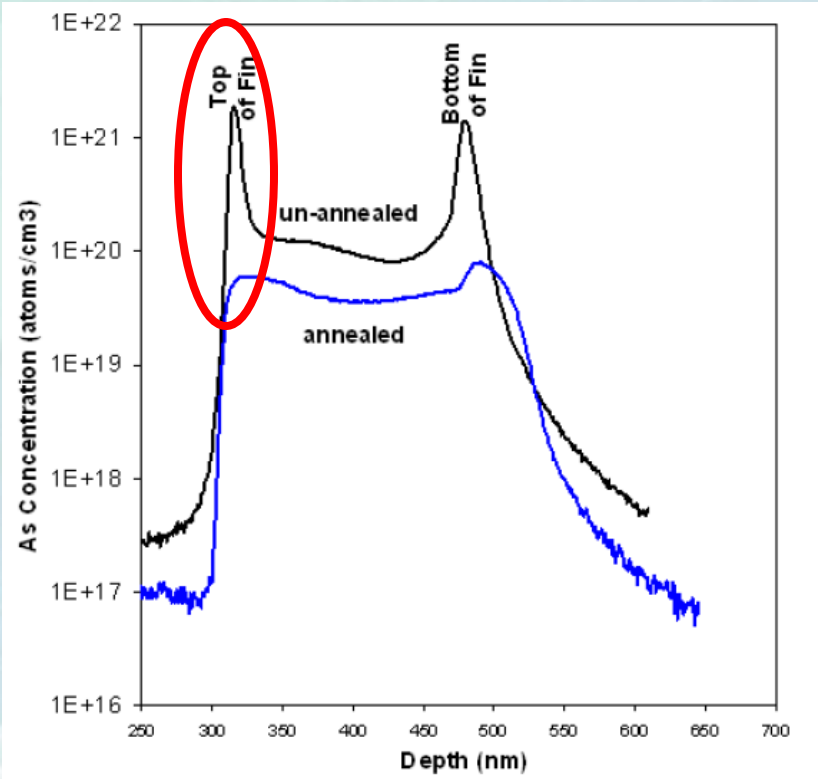


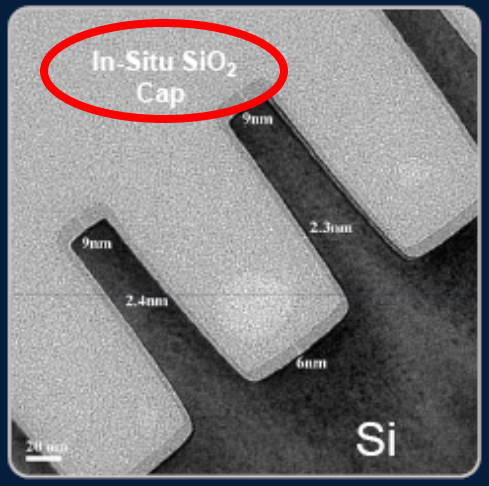
Figure 7: SIMS As depth profiles through the un-annealed and annealed AsH_3 plasma doped fins. The spikes at the top and bottom correspond to the top of the fin and the trench bottom.

Improving Retained Dose

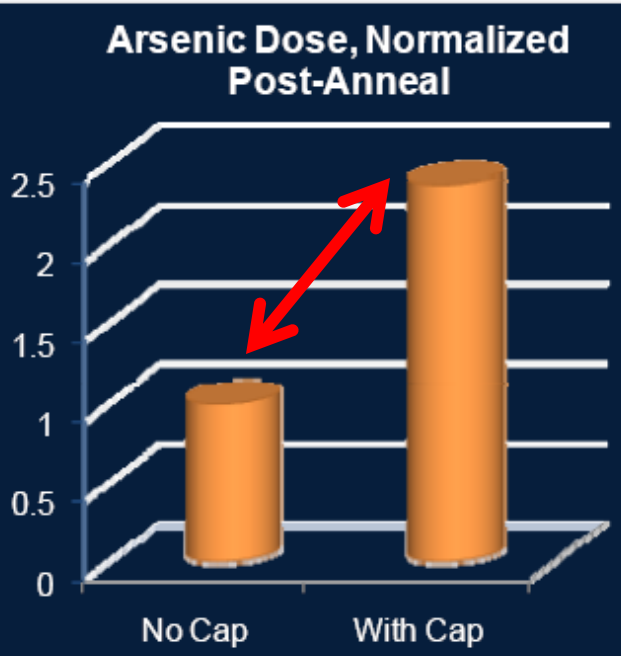
Implant → In-Situ Cap → Anneal

Sequence

Results



Oxide cap on Si fin test structure



Use of the Conforma system's in-situ SiO_2 cap can more than double the retained dose after anneal

Note: Assumes use of cap oxide is compatible with integration scheme.

S5-1 paper by IBS on their PULSION plasma doping system for FD-SOI with LETI. They mentioned they use wafer rotation in improve the plasma doping within wafer uniformity but they did not show any wafer uniformity data. They did show a direct comparison of B-SIMS profile for BF3 4.5kV plasma and BF2 4.5keV beam-line in Fig.8 with an Xj at 1E19/cm3 of 19-20nm. Trying to grow an SEG epilayer on the BF3 plasma doped silicon surface resulted in highly defective epi as shown in Fig.7. The effects of BF3 plasma doping on the epi growth rate reduction as a function of dose is shown in Fig.6 while that for n-type plasma is in Fig.5.

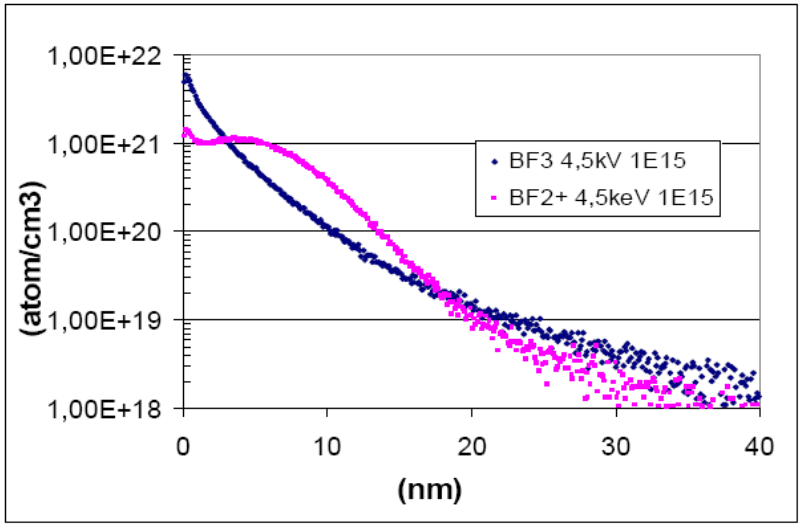


Fig.8: Comparison of the SIMS profiles of boron obtained after Beam Line implantation with BF_2^+ at 4,5kV and $1x10^{15}$ at/cm²and PULSION® with BF_3 at the same energy and dose.

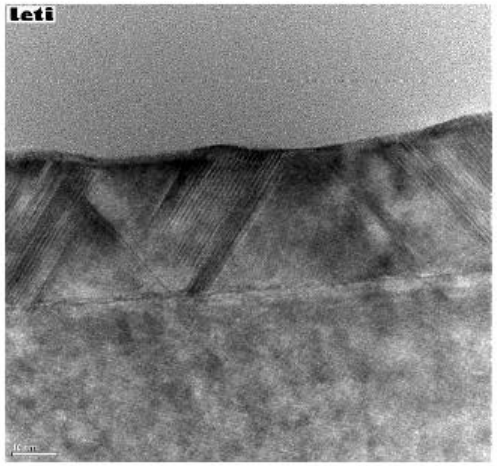


Fig. 7: Example of defective grown layer after a BF_3 implantation and the SEG process. Stacking faults and twins are observed.

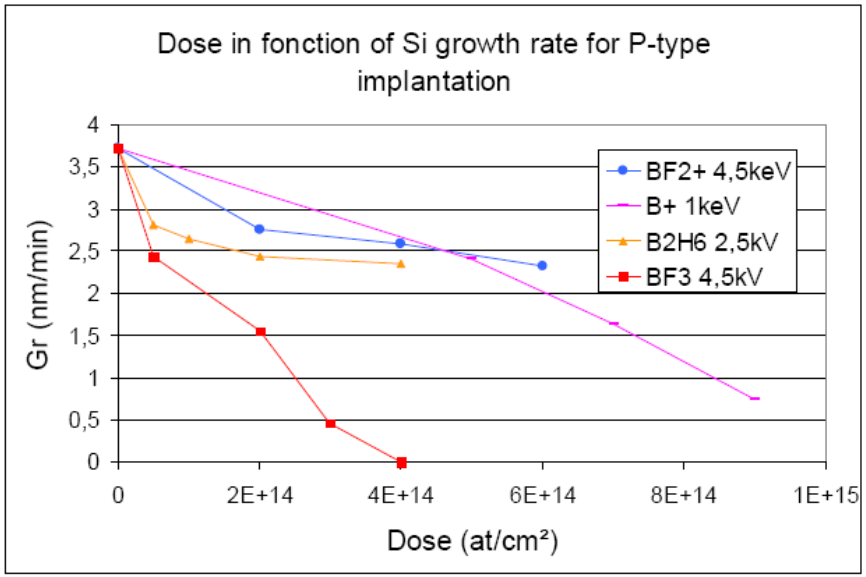


Fig. 6: Growth rate as a function of implantation dose for PD (BF_3 and B_2H_6) and BL (BF_2^+ and B^+) implantation (P-Type).

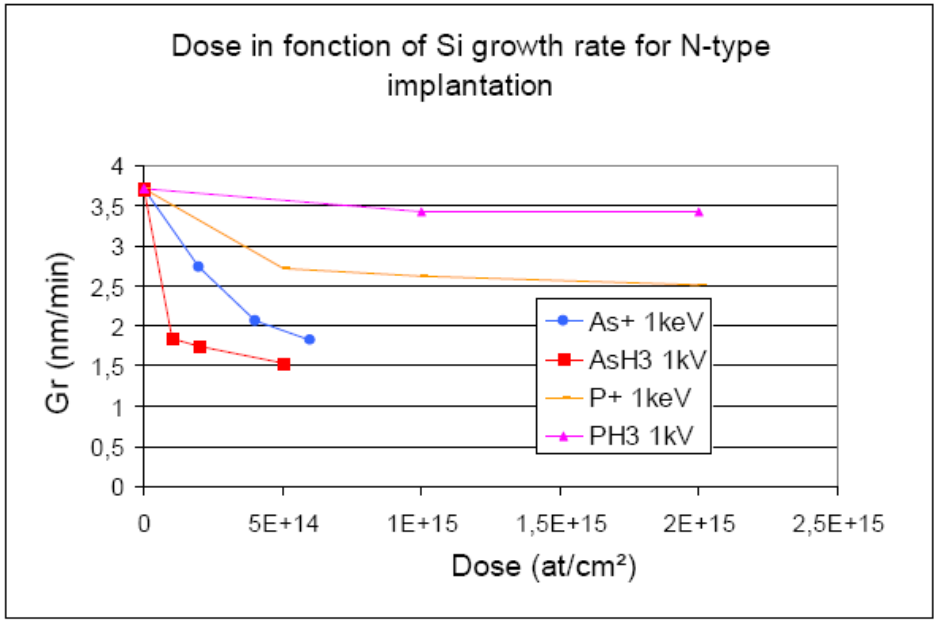


Fig. 5: Growth rate as a function of dose for PD (PH_3 and AsH_3) and BL (As^+ and P^+) implantation (N-Type)

4A-5 paper by IBM on Tri-Gate SRAM. The process flow for their SOI Tri-gate is shown in Fig.3 using extension implantation and Fig.6 shows the X-TEM images. They said they used implantation for S/D but after silicide the junction leakage was degraded by as much as 4 orders of magnitude due to NiSi encroachment of the NFET with a 970C RTA as shown in Fig.7 for process A & B while process E gave best results. He said you cannot implant the Fin and concluded that innovation in junction technology is required but gave no details!

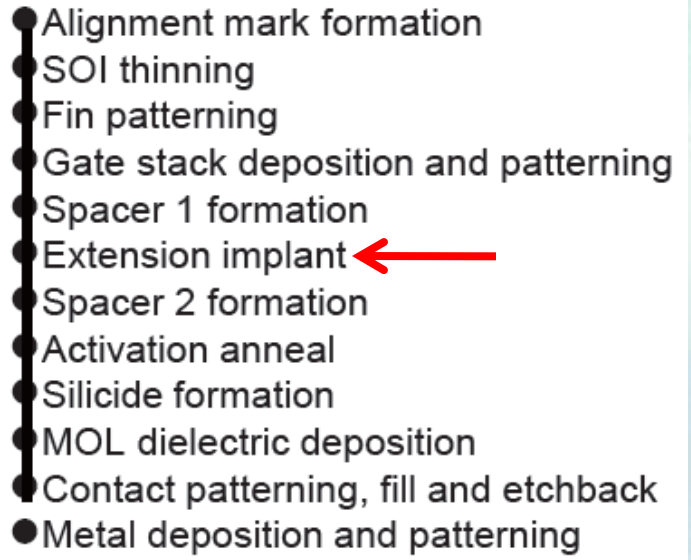


Fig 3: Process flow. Mixed electron beam and optical lithography (MXL) was used for all patterning with commercially available EUV compatible lithography materials.

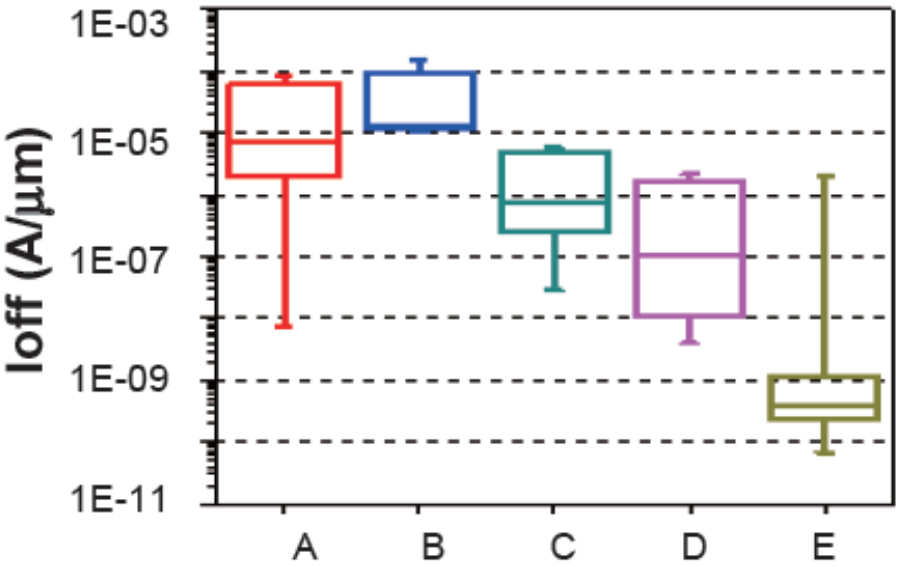


Fig 7: NFET junction leakage as a function of silicide and implant process. Process (E) employed a thin silcide offset spacer and a NiPt silicide formed using a novel sputtering technique.

<u>2A-2</u> paper by IBM Alliance Albany on sub-25nm FinFET. Stated they have successfully implemented Fin extension doping via conformal doping and showed it was 20% better in doping the Fin than beam-line implant in Fig.7 for NFET improving device performance by 10% in Fig.8. This result is surprising based on the huge n-type dopant loss reported by Applied (>65%) and IBS (97%) for plasma doping and also the defective epi growth on these plasma doped junctions reported at IWJT. For PFET they reported Ron was reduced by 50% in Fig.9 improving devices by 25% in Fig.10 but no details were given on the conformal doping process A or B.

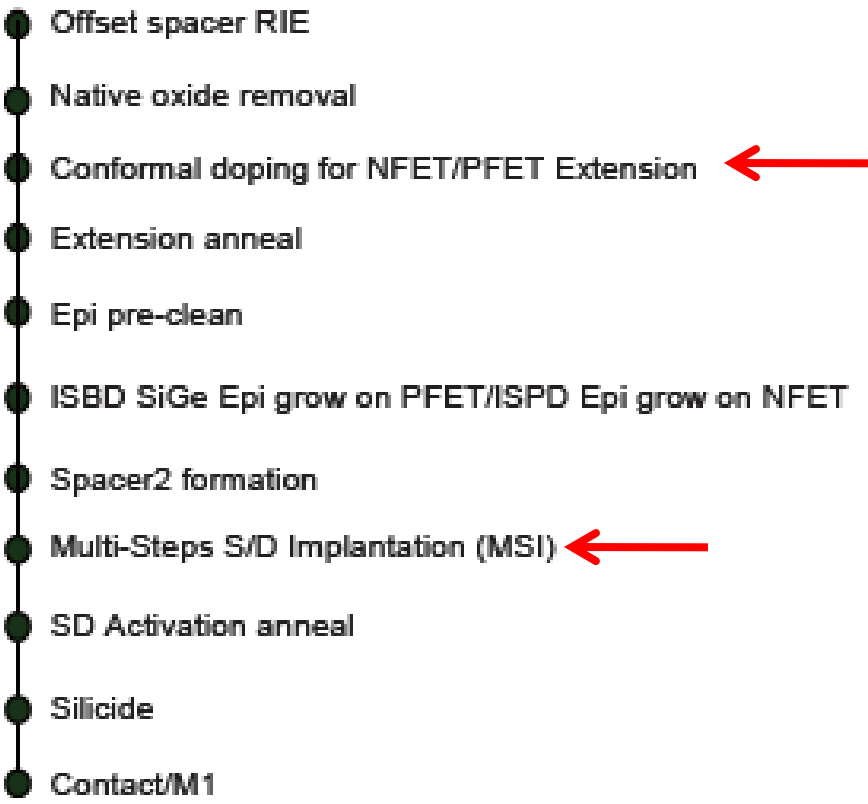


Fig. 4 Process flow of NFET /PFET with conformal doping and epitaxial growth.

7-3 paper by Toshiba on Tri-gate nanowire. They used As implant >1E15 for NFET S/D doping before epi raised S/D and reported poor results due to residual poly/amorphous regions so they switched to As implant after epi raised S/D and results improved as shown in Figs. 6, 7 & 8. Therefore implantation can still be used even for Tri-gate with undoped or in-situ doped Epi depending on the process integration scheme you select.

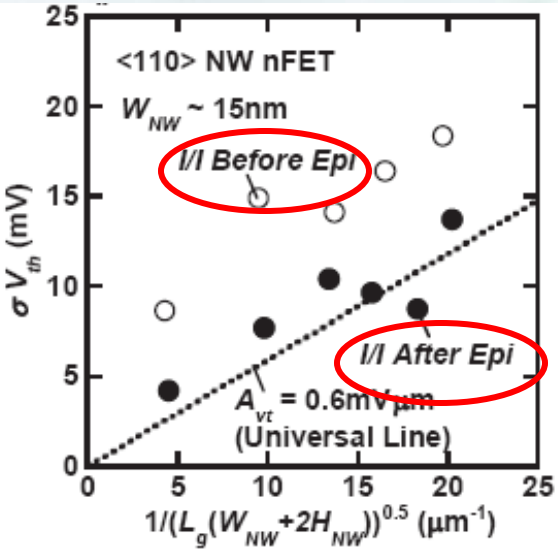
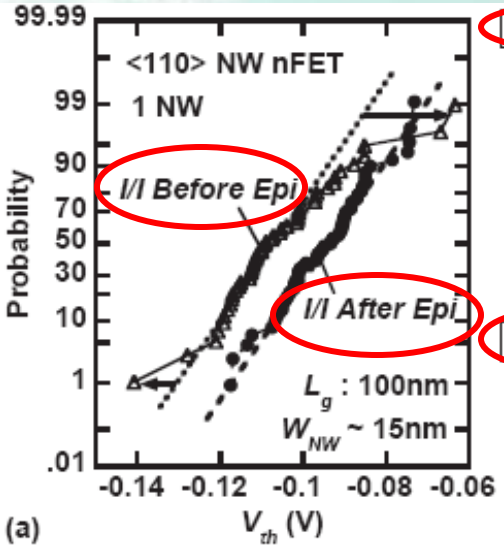


Fig.6. Pelgrom plot of NW nFETs with I/I before/after epi. By I/I after epi, σV_{th} approaches the univ. line.



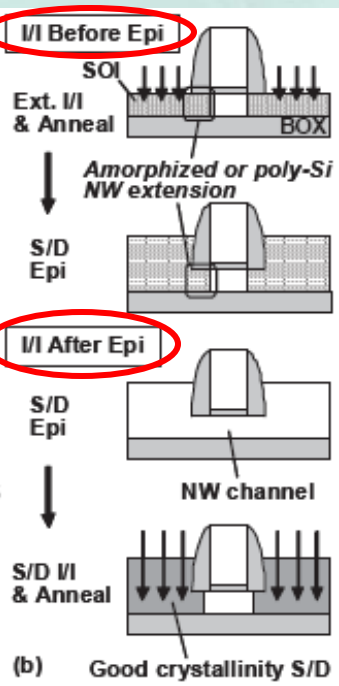


Fig.7. (a) V_{th} distribution and (b) fabrication process of NW nFETs with I/I before/after epi.

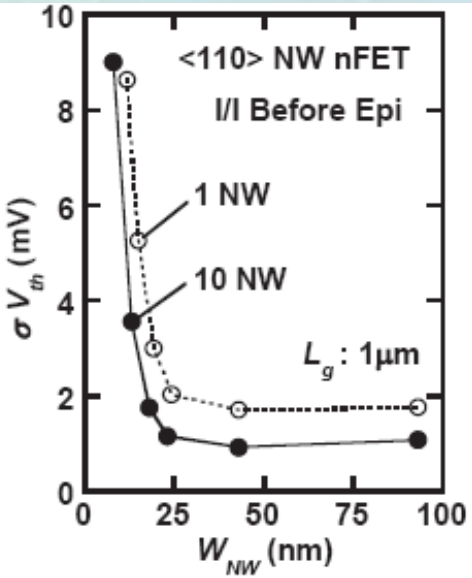


Fig.8. σV_{th}-W_{NW} of NW nFETs with 1 or 10 NW. σV_{th} reduces by NW increase.

IMEC IWJT-2011 Invited Paper #S8-2: Dopant & Carrier Profiling For 3-D Device Architectures

- For 22nm node and beyond, FinFET have now emerged as the device of choice due to performance improvement (increased Id) and power reduction (low leakage).
- Comparing SIMS chemical profiles to SSRM electrical levels IMEC concludes: A large inactive fraction is present so that the conformality of electrical carriers is higher than chemical dopant implying that characterization of electrical conformality will be completely different than chemical conformality. One should not extrapolate the electrical conformality based on the chemical conformality!
- 45 degree tilt chemical conformality =36% by SIMS while electrical conformality=78% by SSRM and resistor data showed **65 degree tilt =100% electrical conformality!**

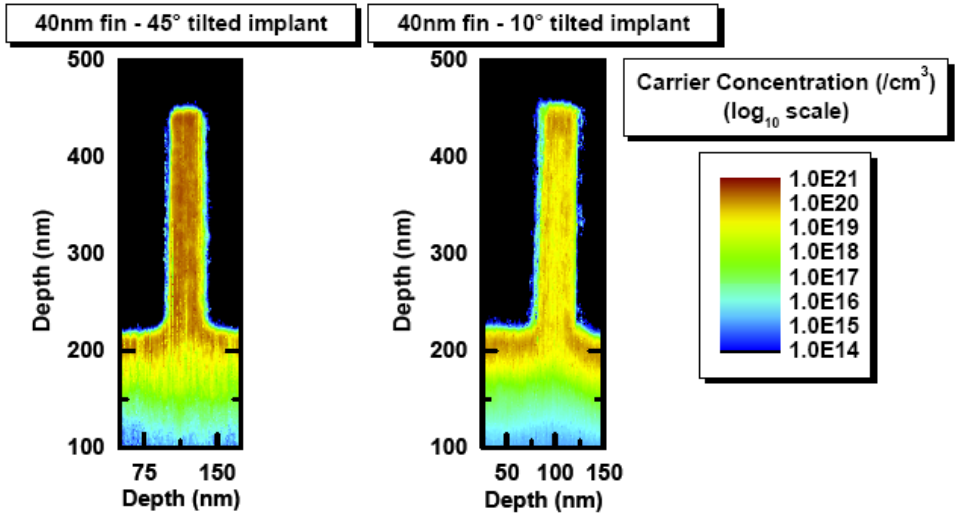


Figure 9: 2D-SSRM map of active carrier concentration of BF_2 implanted at 45° and 10°

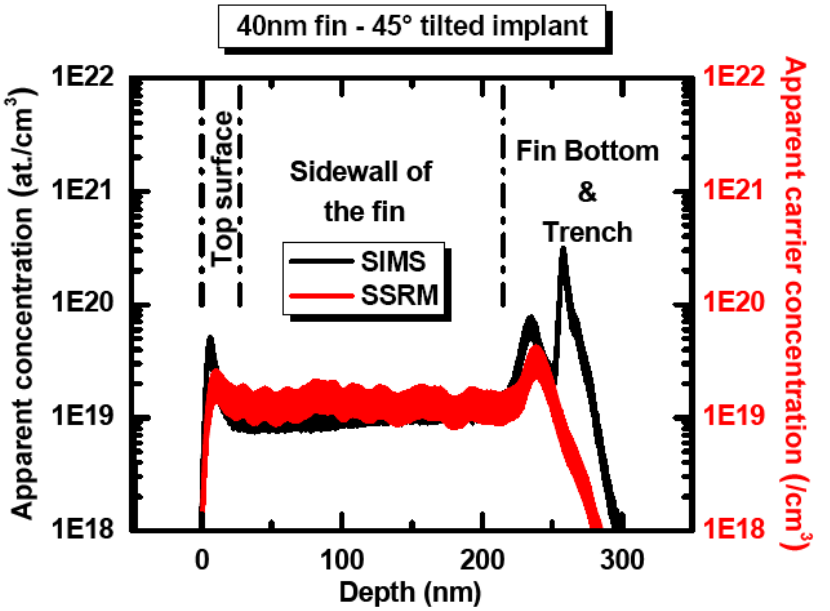


Figure 10: SSRM vs. SIMS (45° implant). SSRM profile is calculated from figure 10. ([8] for the procedure)

Table 1: Comparison of conformalities obtained for dose retention using APT, SIMS and theoretical values. Also conformality values for active percentage of retained dose are mentioned as measured with SSRM.

	Conformality (Sidewall/top) (%)	Conformality (Sidewall/top) (%)
Retained dopants	45° tilted implant	10° tilted implant
Theoretical Model [7]	**46**	**7.5**
SIMS	**36**	**9.0**
Atom Probe	**39**	**12.5**
Active percentage of dopants		
SSRM	**78**	**29**

High Tilt p+ & n+ Molecular Implantation For 3-D Structures: Retained chemical Dose Versus Electrical Activation Limited Conformal Doping

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&

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INSIGHTS 2009

April 28, 2009

P-Type Dopant Implant Matrix

Nissin Claris 0 to 60 Degree Tilt Angle (BF2 & B18H22)

IMEC Quantum-X 0 to 45 Degree Tilt Angle (monomer B)

P-Type	Substrate No.	Ion	Energy [keV]	Dose [/cm2]	Tilt [deg]	Twist [deg]	RS		TW		as I/I SIMS	after anneal
							(Ω/sq)	%STD	TW units	%STD	(Xj) A	SIMS (Xj) A
B18-Tilt Depend	slot1	B18	8.0	5.50E+13	0	0	1007.00	2.759	205.23	2.170	110	100
	slot2		8.0		15		1027.40	2.652	203.97	2.210		
	slot3		9.0		30		1014.40	2.739	224.16	2.420		125
	slot4		11.0		45		1026.40	2.816	255.79	2.310		
	slot5		16.0		60		1038.00	2.873	355.94	2.050		
BF2-Tilt Depend	slot6	BF2	2.00	1.00E+15	0	0	2233.50	1.820	537.41	0.900		
	slot7		2.00		15		2439.20	1.831	532.75	0.970		
	slot8		2.00		30		2535.40	1.719	530.15	1.020		
	slot9		3.00		45		1928.10	1.635	568.92	0.680		
	slot10		4.00		60		1766.80	1.460	581.78	0.480		
(B-Tilt Depend)	slot11	B	0.50	1.00E+15	0	0	2035.00	2.515	597.82	1.200		
	slot12		0.52		15		1983.00	3.104	594.29	1.110		
	slot13		0.58		30		2027.00	2.580	617.06	0.720		
	slot14		0.71		45		2007.00	2.468	629.77	0.420		
	slot15		1.00		60							
B18 Energy Depend	slot16	B18	8.0	5.50E+13	60	0	1688.80	2.693	183.59	1.910		
	slot17		16.0				1045.00	2.917	353.95	2.050		
	slot18		32.0				658.33	4.105	582.90	0.390		
BF2 Energy Depend	slot19	BF2	2.0	1.00E+15	60	0	3995.00	1.409	436.46	2.230		
	slot20		4.0				1668.90	1.671	579.73	0.490		
	slot21		8.0				750.80	0.948	582.16	0.410		

Duffy *et al.*, Appl. Phys. Lett. **90**, 241912 (2007)

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Borland et al., Insights-2009

Summary

- Monomer B had the highest retained chemical dopant level >1E15/cm2 but lowest dopant activation level Bss=2.8E19/cm3 with Flash annealing.
- B18H22 had a retained chemical dopant level of 5.5E14/cm2 but the highest dopant activation level Bss=1.1E20/cm3 with Flash annealing.
- As4 retained chemical dopant level was 7.5% higher than AS and the dopant activation Rs value was also 7.5% higher.
- FinFET
  - Run device study with customer
  - Try Xe-PAI & In-PAI high tilt with B and B18H22 from above
  - Try Sb-vs-P for n+ FinFET

S7-3 paper by myself. My message was that for Tri-Gate with a 1 to 1 aspect ratio a dual mode **63.5 degree tilt** implant for the Fin will give you equal 100% chemical conformality on the top and side wall of the Tri-gate Fin especially when you use hydrogen surface passivation compared to oxide surface passivation at high tilt angles and/or low energies.

Influence of Surface Passivation on B, $B_{18}H_{22}$ and $B_{36}H_{44}$ Retained Dose for USJ

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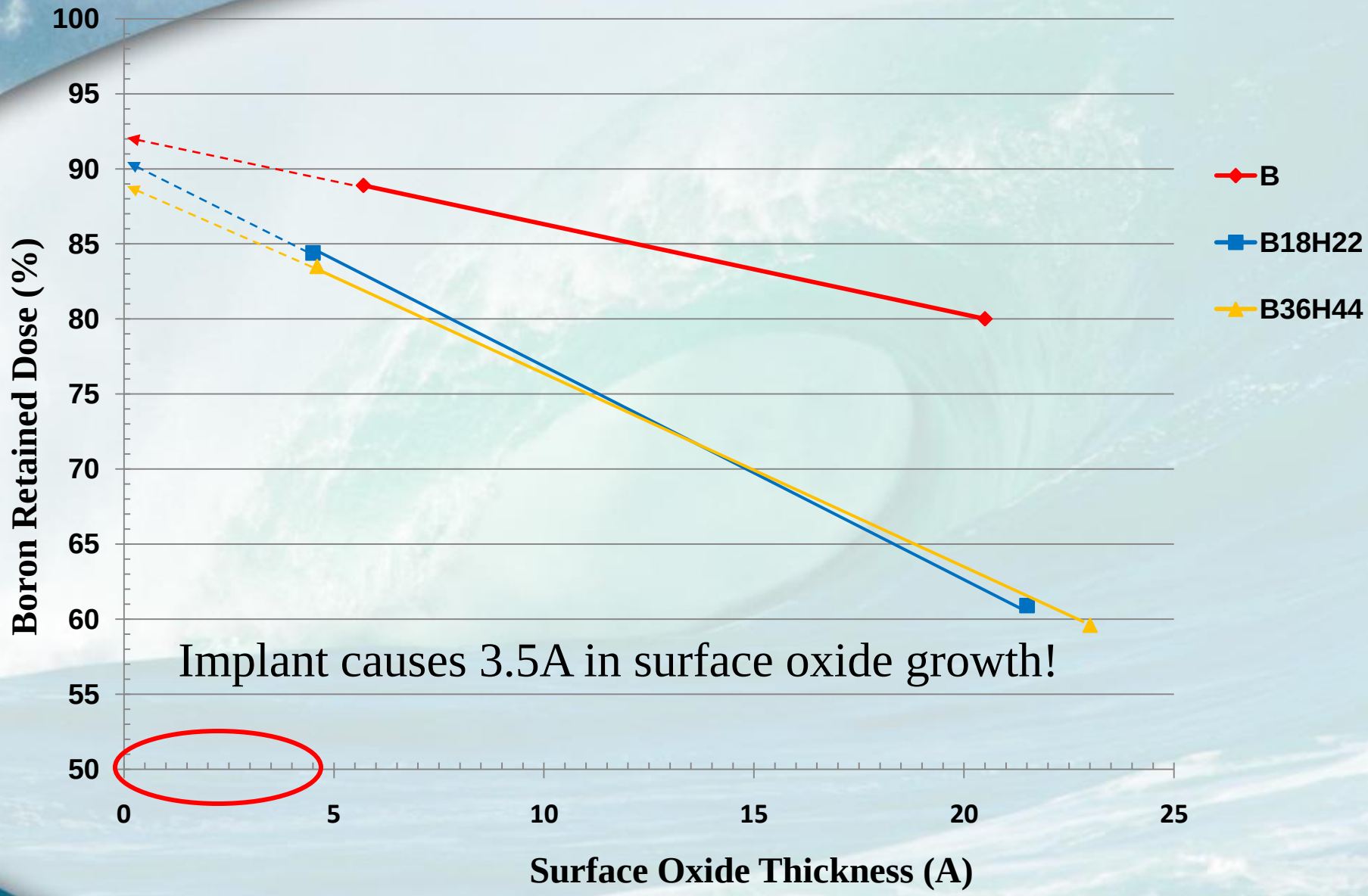
Temel Buyuklimanli
EAG
East Windsor, New Jersey


100
95
90
85
80
75
70
65
60
55
50
Boron Retained Dose (%)
0
5
10
15
20
25
Surface Oxide Thickness (A)
B
B18H22
B36H44
Implant causes 3.5A in surface oxide growth!

Renesas Used Ellipsometry To Determine Amorphous Layer Depth

B18 a-layer is 2x deeper than CBH and B36 is 2.5x

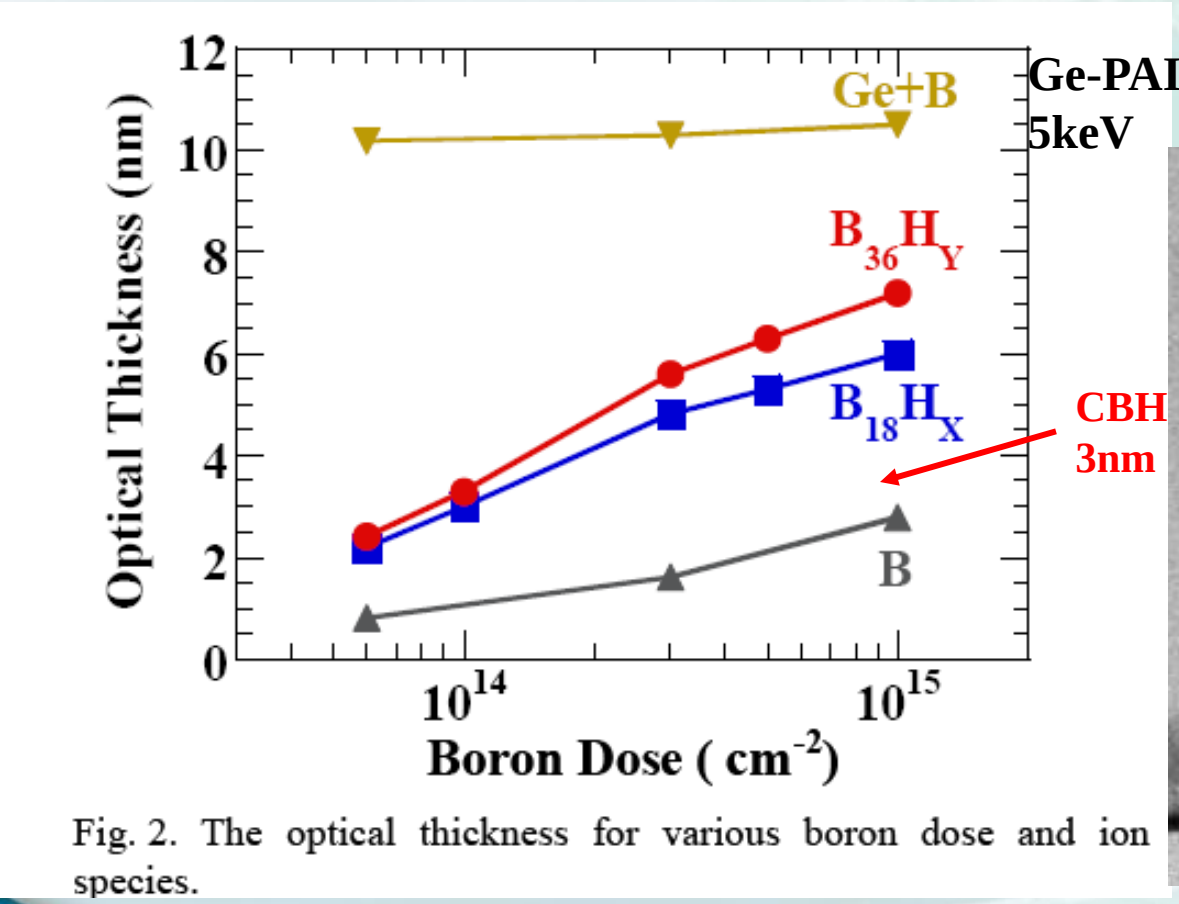
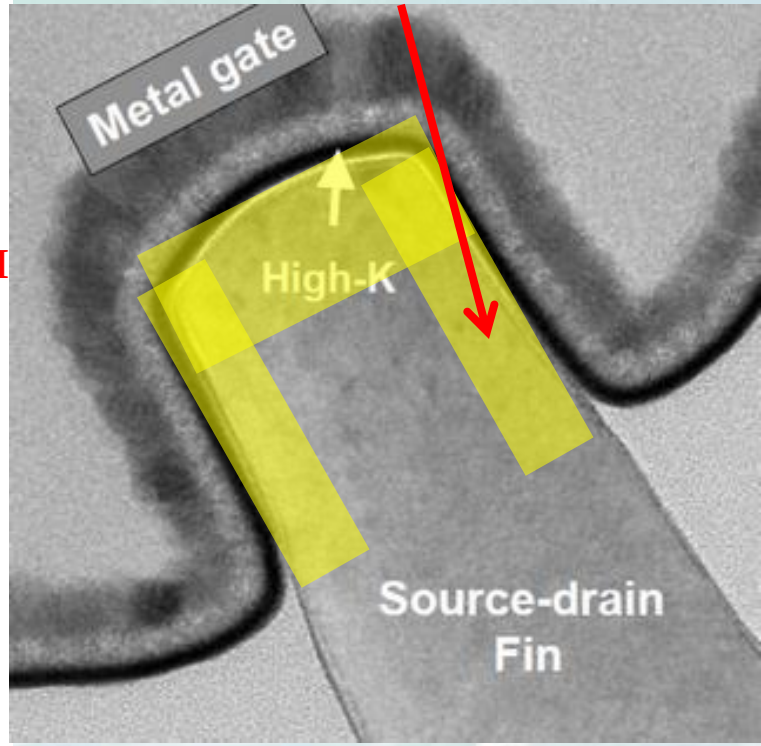


Fig. 2. The optical thickness for various boron dose and ion species.

Key is Damage Free Fin so Avoid Complete Amorphization of FIN! Use B18H22!



Kawasaki et al., Renesas, IWJT-2009, paper S2-1

Outline

- Introduction: 32/28nm, 22/20nm & 16/14nm nodes
- Tri-Gate Doping reports from VLSI Sym & International Workshop on Junction Technology June 2011 Kyoto, Japan
  - Evening panel rump session on “Can Fin/FET/FD-SOI Compensate for the Stagnation in Scaling?”→ FinFET or UTBB-SOI at 20nm & beyond?
  - IMEC, JOB, IBS and SEN on FinFET doping
  - IBM/Alliance & Toshiba/Japan papers on Tri-gate
- FD-SOI Doping reports from VLSI Sym & International Workshop on Junction Technology June 2011 Kyoto, Japan
  - IBM/Alliance papers on UTBB-SOI
  - MIRAI/Selete paper on NFET B-HALO TED dominated Vt variation
- 37th IEEE-PhotoVoltaic Specialist Conference June 20-24, 2011 Seattle, WA
  - Selective Emitter Formation by: 1) Laser Diffusion Doping, 2) Dopant Paste or 3) Patterned Implantation
- Summary

<u>7-1 paper</u> by IBM Alliance on ET-SOI for 22nm Lg improving on the implant free process using all in-situ doped epi raised S/D with faceting in Fig.1 below. The multiple Vt devices are control with different gate stack workfunction tuning layers in conjunction with back gate bias so no implant doping at all since the channel is undoped as shown in Figs. 3 & 4 for NFET & PFET

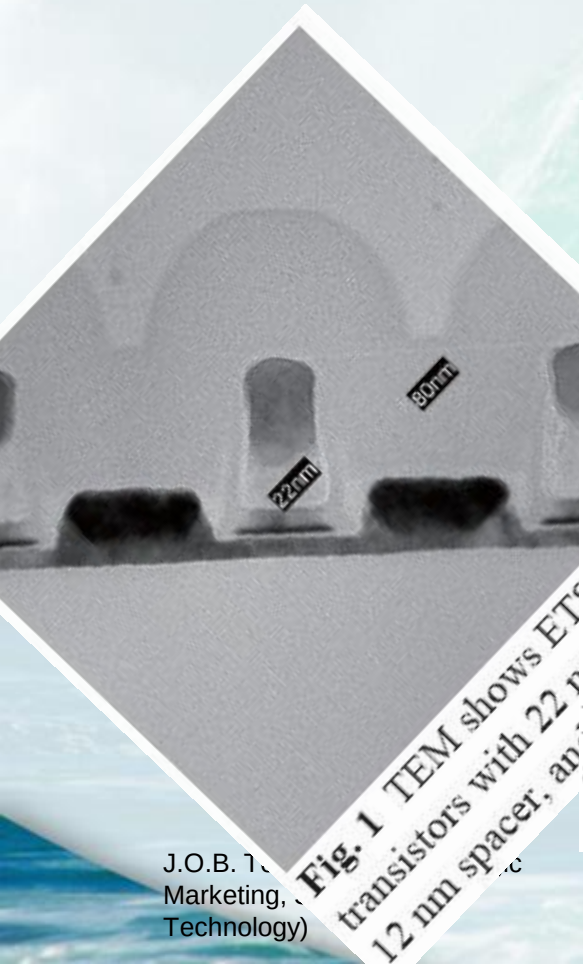


Fig. 1 TEM shows ET
transistors with 22
12 nm spacer, an

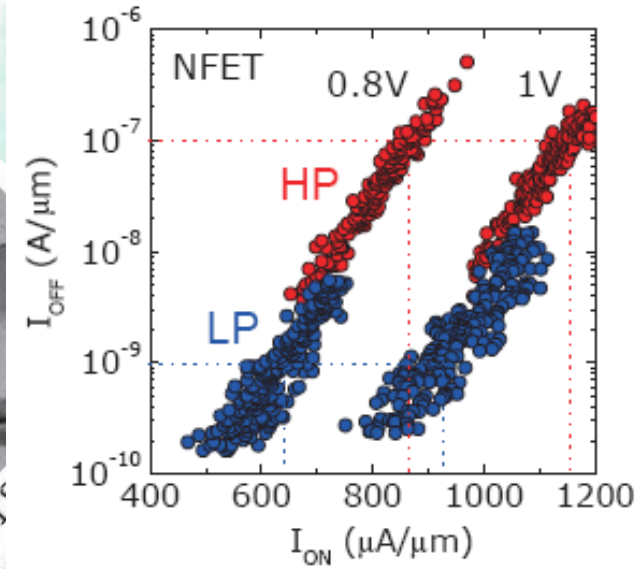


Fig. 3 I_{on}-I_{off} characteristics of HP and LP NFET transistors at V_{DD} = 1 V and 0.8 V

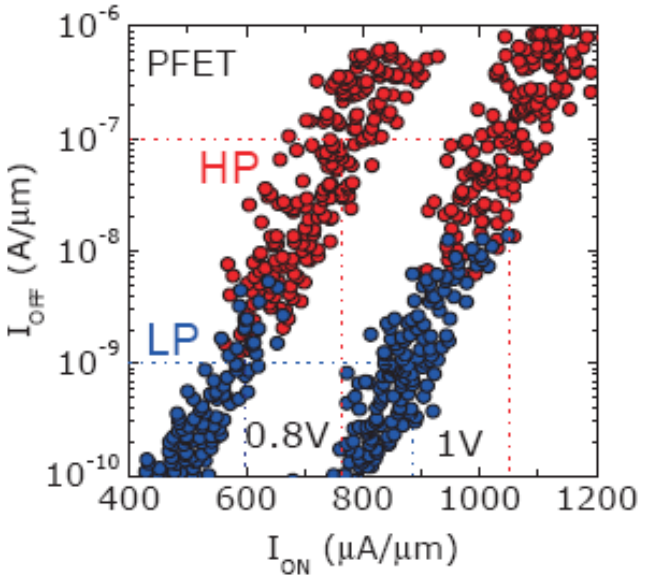


Fig. 4 I_{on}-I_{off} characteristics of HP and LP PFET transistors at V_{DD} = 1 V and 0.8V

<u>9A-2 paper</u> by IBM/Albany Alliance. They demonstrated the back bias on the ET-SOI (UTBB-SOI) using multi-step implant into the raised S/D Epi with tilted implantation in Fig.1.

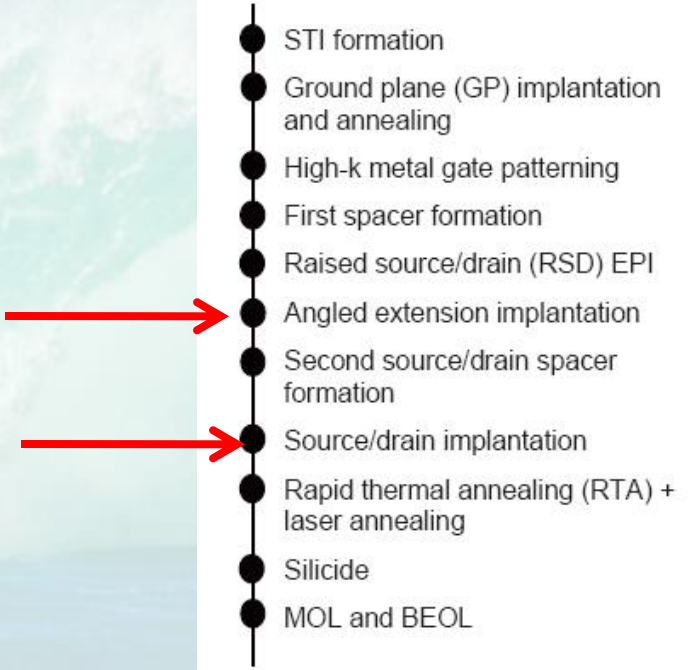


Fig. 1 A simplified UTBB integration flow, featuring conventional gate first high-k metal gate and raised source/drain EPI process. The preservation of thin SOI layer during gate RIE and first spacer formation is key for integration integrity.

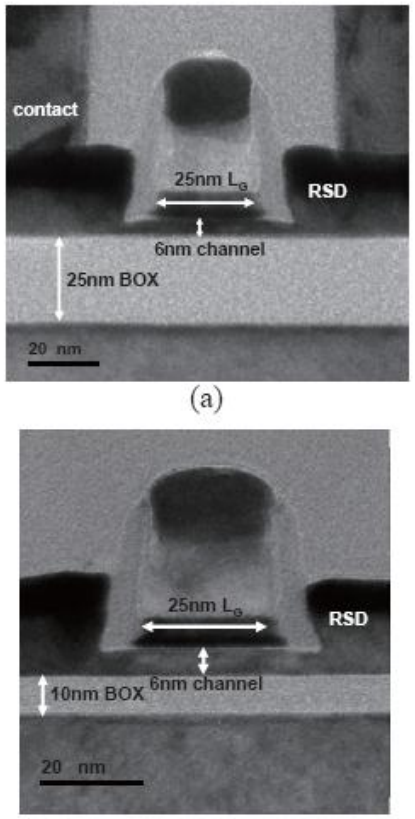


Fig. 2 TEM cross-section of (a) 25nm BOX and (b) 10nm BOX UTBB devices with gate length of 25nm and channel thickness of 6nm.

See Mogami IWJT-2011 Paper #S1-1:

Variability Issues and Advanced Process Technology for Variation Mitigation

- Vt variation of pMOS is smaller than that for nMOS
- pMOS Vt variation dominated by Random Dopant Fluctuation
- nMOS Vt variation is larger than RDF!
- Compared channel/HALO dopants of boron, phosphorus, arsenic and antimony and only B-channel doping from HALO showed reverse SCE therefore As n+SDE defects caused B-TED and B pile-up at the channel surface. Use C co-implant to reduce B-HALO TED and reduce nMOS Vt variation!

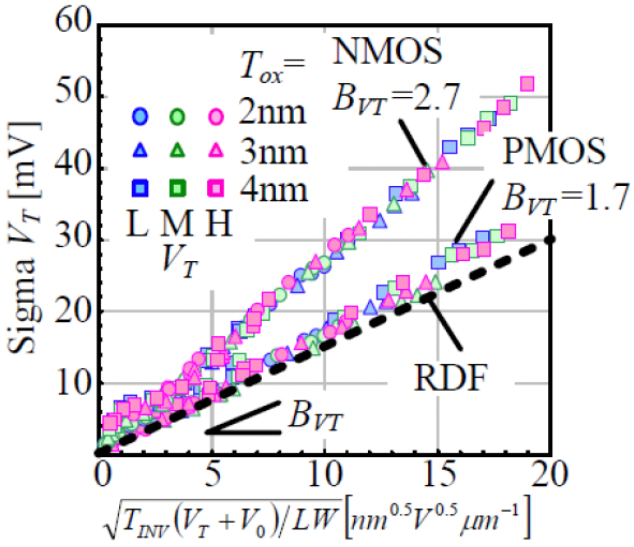


Figure 7 Relation between Vth variation and Vth and Tox for N/P-MOSFETs.

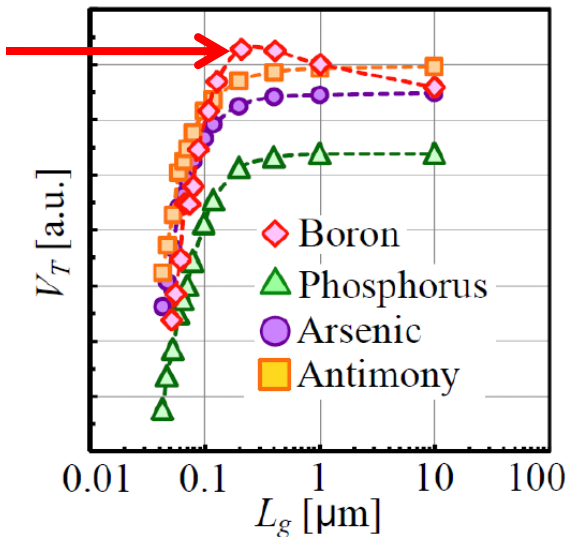


Figure 8 Relation between channel dopant and short channel effect

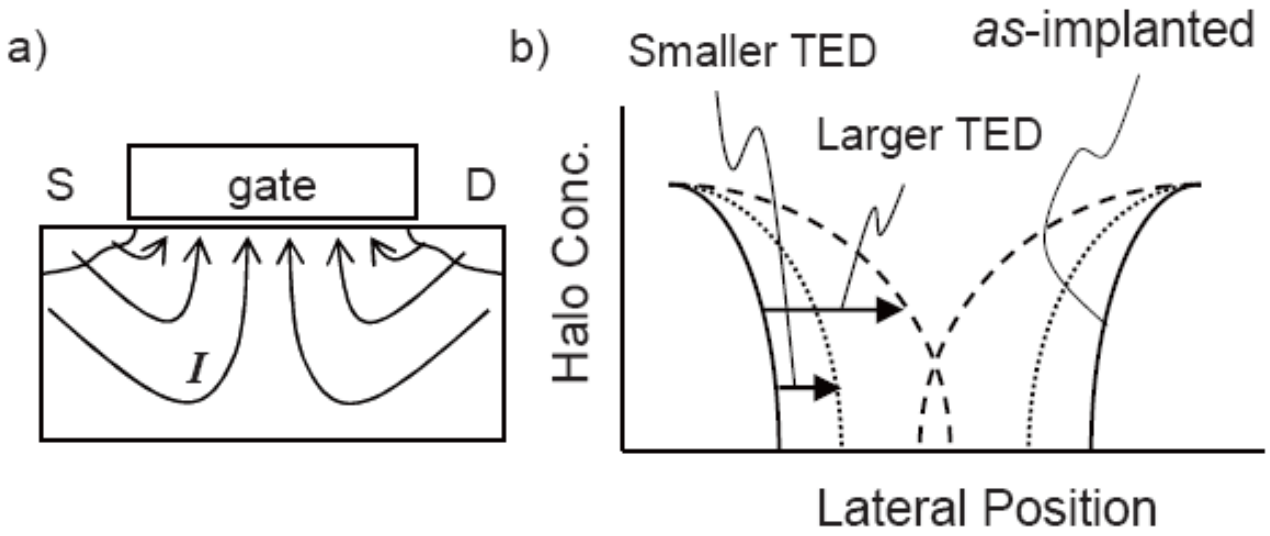


Fig.2 Boron diffusion modulation model for explaining reported experimental behavior of NFET random V_{VT} fluctuation (RDF).

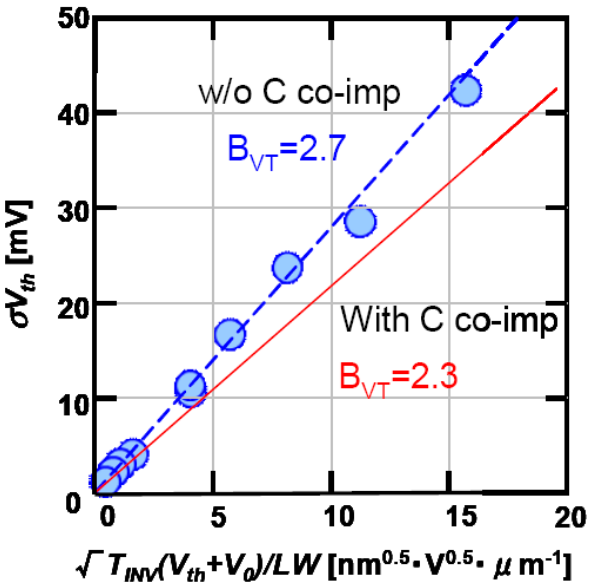
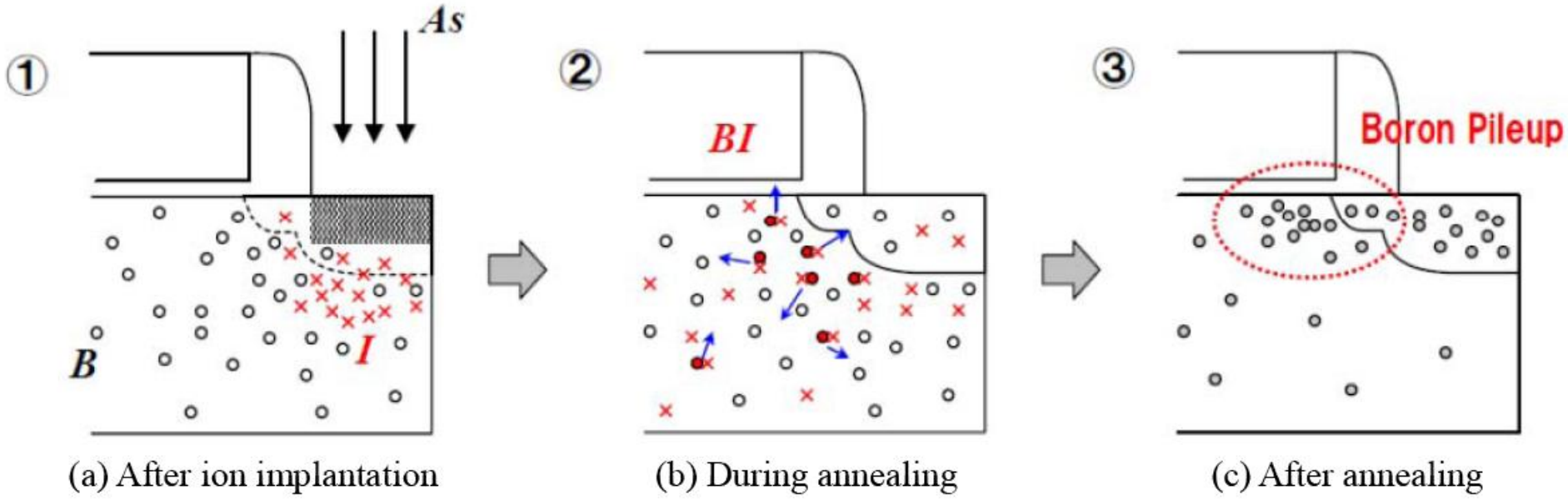


Figure 11 Carbon co-implantation effect for Vth variation mitigation of NMOSFET



(a) After ion implantation (b) During annealing (c) After annealing

Figure 9 Boron transient enhanced diffusion

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Paper 23: Joint paper between UNSW & Centrotherm on "Record Large Area P-type Cz Production Cell Efficiency of 19.3% Based on LDSE Technology".

Paper 617: Poster H-43 by Centrotherm on "Selective Emitter by Laser Diffusion on c-Si Solar Cells in Industrial High Efficiency Mass Production".

Paper 25: Joint Innovalight & Hanwha Solar talk on "Efficiency Gain of Silicon Ink Selective Emitters at Module Level". Using the Innovalight Cougar process for SE they inserted the silicon ink screen print step before diffusion to increase cell efficiency to >19%. On the module level they reported Homo-Emitter (HE) modules power=215.8W and efficiency=15.98% while Selective Emitter (SE) modules power=228.6W and efficiency=16.92%.

Paper 560: Joint Varian & Suniva on "High Efficiency Selective Emitter Enabled Through Patterned Ion Implantation".

Top 50 Solar PV Module Efficiency (Mono-Crystalline)

SOLARPLAZA
EMPOWERING YOUR SOLAR BUSINESS

#	Company	Module Efficiency	Module Type	Cell Efficiency
1	Sunpower	19.60%	E19 / 320 SOLAR PANEL	22.40%
2	AUO Solar	19.50%	PM318B00	
3	Sanyo Electric	19.00%	HIT-N240SE10	21.60%
4	Jiawei	18.30%	JW-S100	21.01%
5	Crown Renewable Energy	18.30%	Summit 100LM	
6	JA Solar	16.84%	JAM5(L)-72-215/SI	19.10%
7	Trina Solar	16.40%	TSM-210DC80	18.10%
8	CNPV Solar	16.20%	CNPV-105M	18.80%
9	Yingli Solar	16.20%	Panda 265 Series	18.50%
10	Jetion	16.20%	JT315SAc	18.30%
11	LG Solar	16.20%	LG260S1C	
12	China Sunergy	16.06%	CSUN205-72M	19.00%
13	ET Solar	16.06%	ET-M572205 205W	18.94%
14	Hareon Solar	16.06%	HR-205W	18.80%
15	Suniva	16.00%	Optimus 260	19.20%
16	Siliken	16.00%	SLK60M6L 260Wp	
17	Topray	15.80%	SLSM-180D 305W	
18	FVG	15.75%	FVG 84-125 230W	17.90%
19	Group Dmegc Magnetics	15.73%	DM255-M156-6	18.00%
20	Sunrise Solartech	15.70%	SR-M572200-1	18.50%
21	Suntech	15.70%	PLUTO200-Ade	19.00%
22	Jinko Solar	15.67%	JKM-200M (K16S)	18.25%
23	Risen	15.66%	SYP200S-M	
24	Frankfurt CS Solar	15.66%	FS 200W MON	
25	Chaori	15.66%	CRM200S 125M-7	
26	Eoplly New Energy	15.66%	125M/72-200	
27	Era Solar	15.66%	ESPSA 200	
28	CETC	15.60%	ZKX-200D-24	18.00%
29	Silfab	15.60%	SLA255M	
30	Topsola	15.53%	TSM60-156M	17.82%
31	Bisol	15.40%	BMO/25	17.20%
32	Hanwha SolarOne	15.30%	SF160	16.50%
33	Astronergy	15.30%	CHSM5612M 195	
34	DelSolar	15.30%	D6M_B3A-WT series 250	
35	Perlight	15.27%	PLM-250/24	18.00%
36	JMS Solar	15.27%	JMS-CS 180M 195	
37	Mage Solar	15.25%	Mage Powertec Plus 255/5 MR	17.80%
38	Solon	15.24%	SOLON Black 230/07	
39	PV Power Technologies	15.12%	SM-240MH0	
40	Renesola	15.06%	JC245S-24/Bb	
41	Schüco	14.90%	SPV 210 SMAU-1	
42	Aleo Solar	14.90%	S19.245	
43	Eging	14.90%	EGM 190	
44	Astom	14.88%	ASH190m-72	
45	Sun Earth Solar Power	14.88%	Sun Earth M 190W	
46	Hyundai	14.80%	HiS-S215 SF	
47	Win Win Precision	14.73%	WSP-245M6	
48	Kioto Photovoltaics	14.72%	KPV 220 M	
49	Sharp Solar	14.70%	NU-U240F2	
50	Solar-Fabrik	14.70%	Premium L-Mono 245	

-3.4%

-3.9%

-2.8%

-2.3%

-3.3%

ElectroIQ, July 7, 2011

Summary

- **Bulk Tri-Gate** starting production at 22nm node by Intel, others considering it at 20nm node and beyond.
  - Intel reports multi-implants to control Vt and lower channel doping level with SiGe and HK/MG last strain technology. Fin S/D doping by recess then in-situ doped epi raised S/D.
  - Fin extension doping options by beam-line (JOB, IMEC & Toshiba) or plasma (IBS, IBM)
- **UTBB-SOI** proposed at 20nm node by ST, others considering it at 14nm node
  - In-situ doped epi raised S/D proposed by IBM
  - Tilted beam-line implantation into epi raised S/D by IBM
- MIRAI/Selete reports **nMOS Vt variation** dominates due to B-HALO TED and C co-implant reduces TED effects
- **Solar Selective Emitter** doping options laser diffusion by Centrotherm, dopant paste by Innovalight and mask implantation by Varian.