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IEDM 2010 Short Course
15nm CMOS

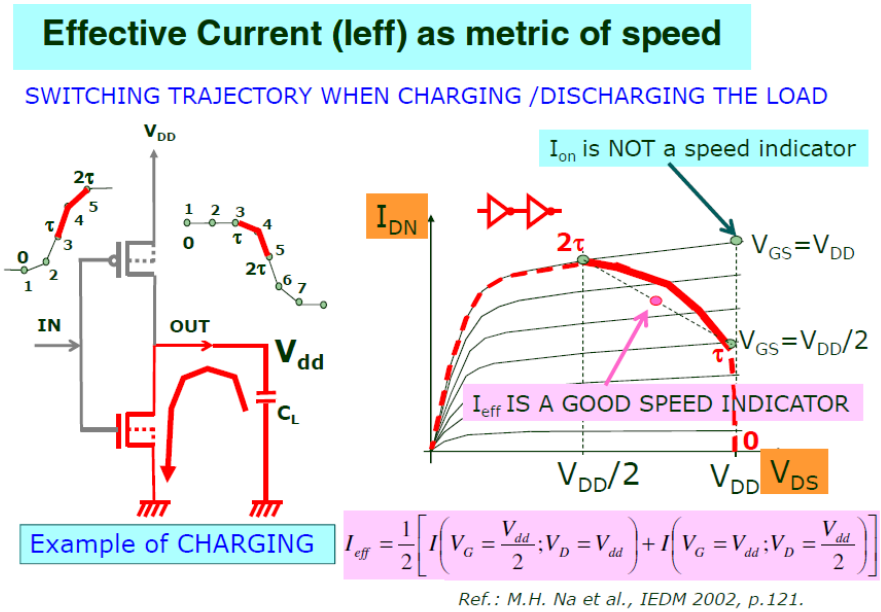
P. J. Timans

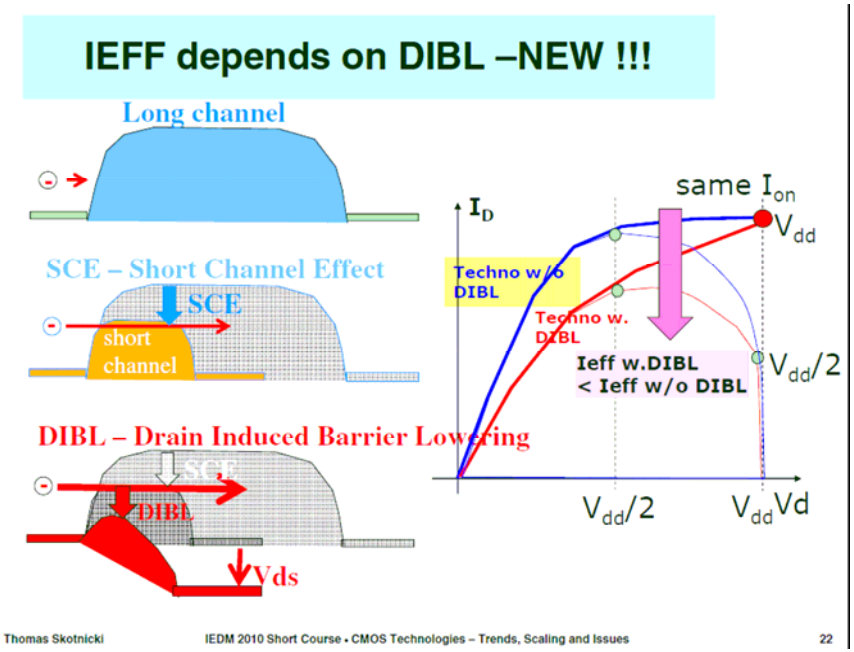
JTG Meeting, 2 February 2011

Short Course Contents

- Course Organized by Kelin Kuhn, Intel
- Presenters
  - CMOS Technologies – Trends, Scaling and Issues (Thomas Skotnicki, ST)
  - 15nm Device Challenges and Solutions (Mukesh Khare, IBM)
  - Lithography for the 15nm Technology Node (Sam Sivakumar, Intel)
  - BEOL Technology toward the 15nm Technology Node (Yoshihiro Hayashi, Renesas)
  - Device/Circuit Interactions at the 15nm Technology Node (Clive Bittlestone, TI)
- Here we'll focus on the 1st two tutorials

Metrics for Success in Scaling





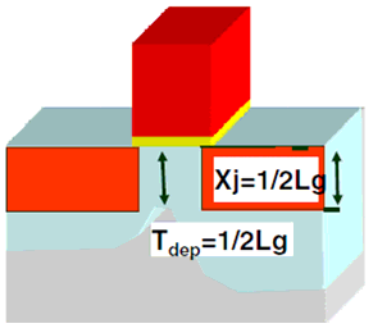
- Switching performance dominated by dynamic characteristics: I_{eff} metric, which depends on DIBL
- DIBL metric is especially relevant to low power applications

Bulk Scaling Limit

WHY DOES THE PLANAR MOSFET FAIL ?

(Ref.: *T. Skotnicki, et al., Electron Device Letters, Vol 9, N° 3, 1998)*

$$DIBL = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{X_j^2}{L_{el}^2}\right)\frac{T_{ox}}{L_{el}}\frac{T_{dep}}{L_{el}}V_{DS}$$



Suppose : Lel=2/3Lg

$$2.4\left(1+\frac{3^2}{4^2}\right)\frac{1}{20}\frac{3}{4}V = 140mV$$

REF.: T. Skotnicki, invited paper ESSDERC 2000, pp. 19-33, edit. Frontier Group

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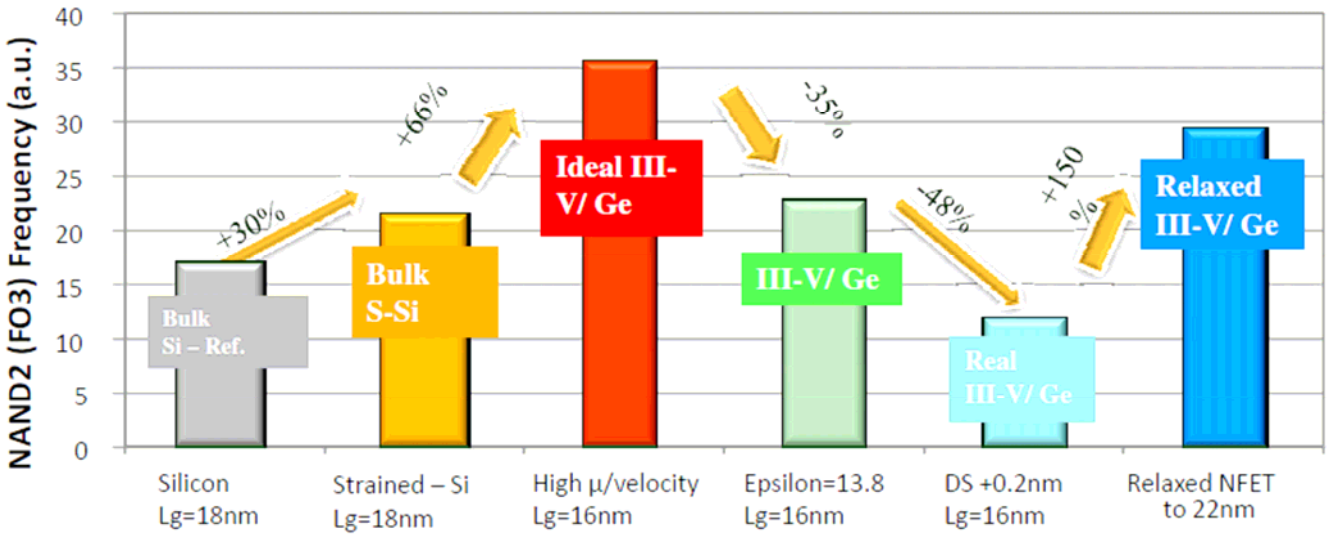
- Limited scope for scaling planar device
- Improvement possible through μ boost
  - BUT - much of the feasible boost has already been used up

III-V Channel: Hard to Scale & Keep Performance

Step-by-Step High-μ Material Analysis for 16nm node at Ioff = 0.5nA/μm

Material	Epsilon	Kvs	Kμ	DS (nm)	remark
S-Si (n)	12	1.7	1.8	+0.3	Full Strain-Si
S-Si (p)	12	1.5	7	+0.5	Full Strain-Si
UTB	12	1.1	1.2	+0.3	Slightly Strained
Virtual III-V	13.8	>3	10	+0.5	High μ for electron
Ge	16	1.5	3	+0.5	High μ for holes



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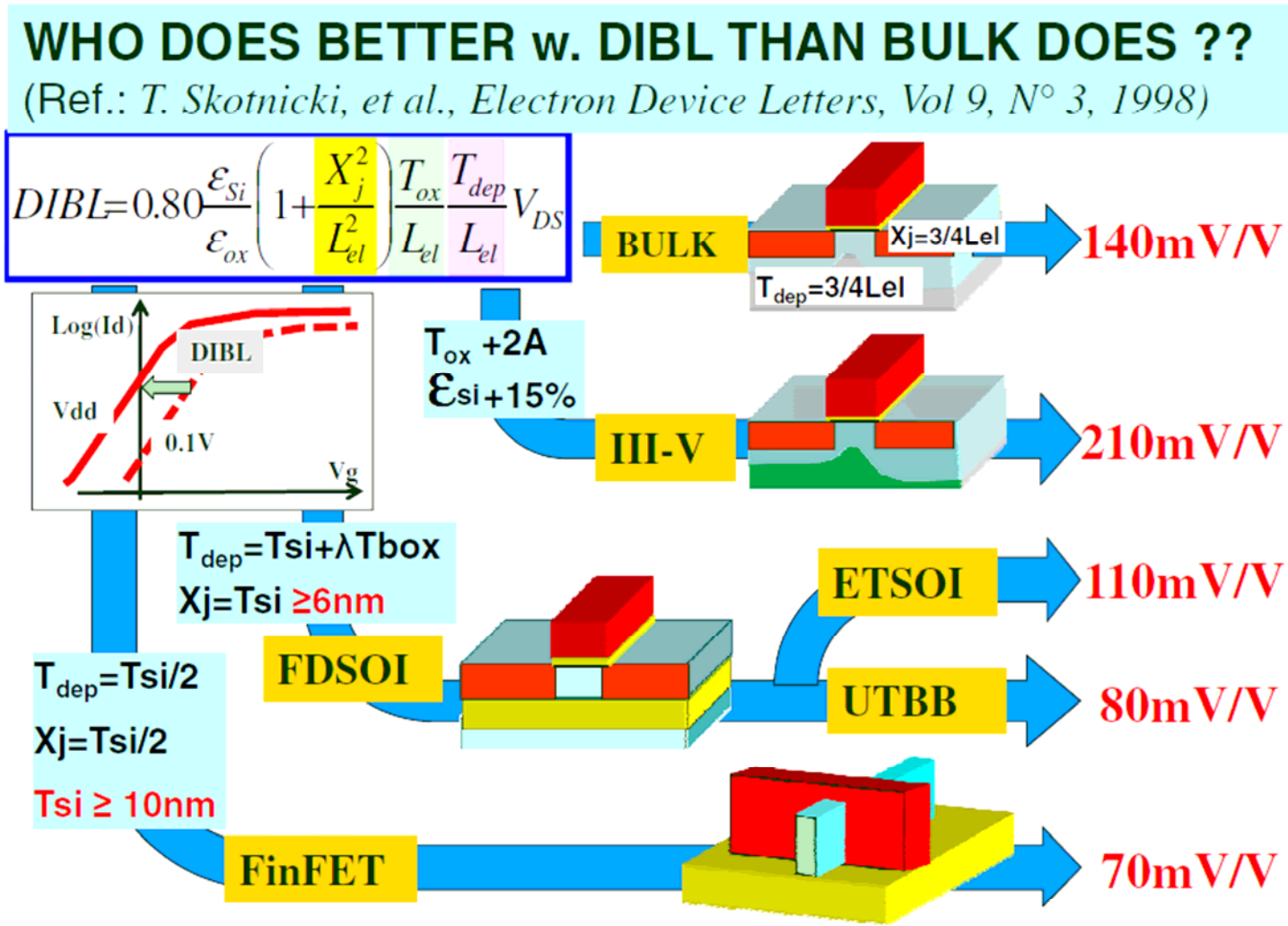
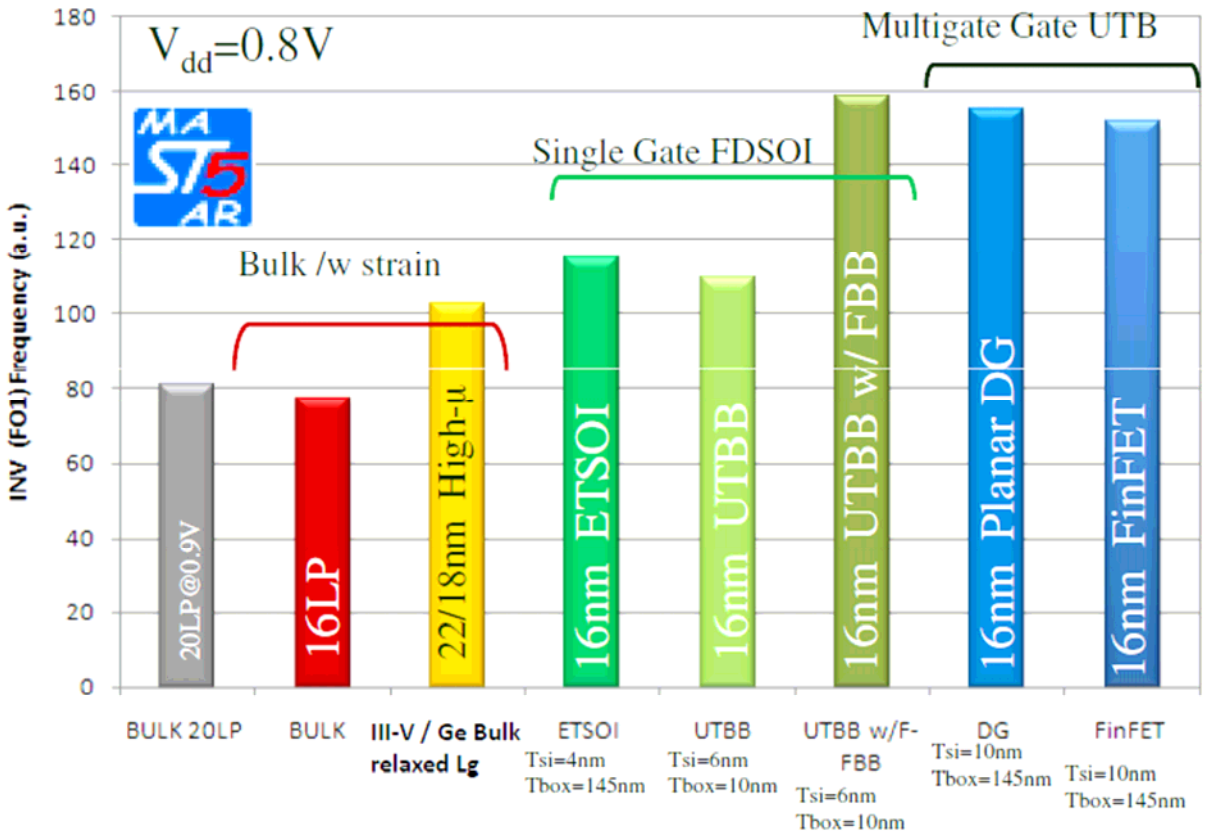
Fully-Depleted Devices Improve DIBL



Performance Comparisons

Reduced DIBL along w. FBB (Forward-Body Bias) provide the winning solution with FDSOI @ 16nm



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T. Skotnicki: Advocating Planar FDSOI

PERSPECTIVE

- All rational reasonings indicate that 15nm CMOS (at least the 14nm LP) should switch from Bulk to UTBB (Ultra Thin Body and BOX) SOI
- Once this accomplished, UTBB will remain the principal platform for 2-3 generations, since its scalability (thanks to thin BOX) is very good, similar to that of FinFET
- For further nodes, scaling may stop and thus render performance increase with high-μ materials (e.g. III-V) more efficient, as these materials manifest their advantage only with relaxed geometry (n-1 with respect to n)

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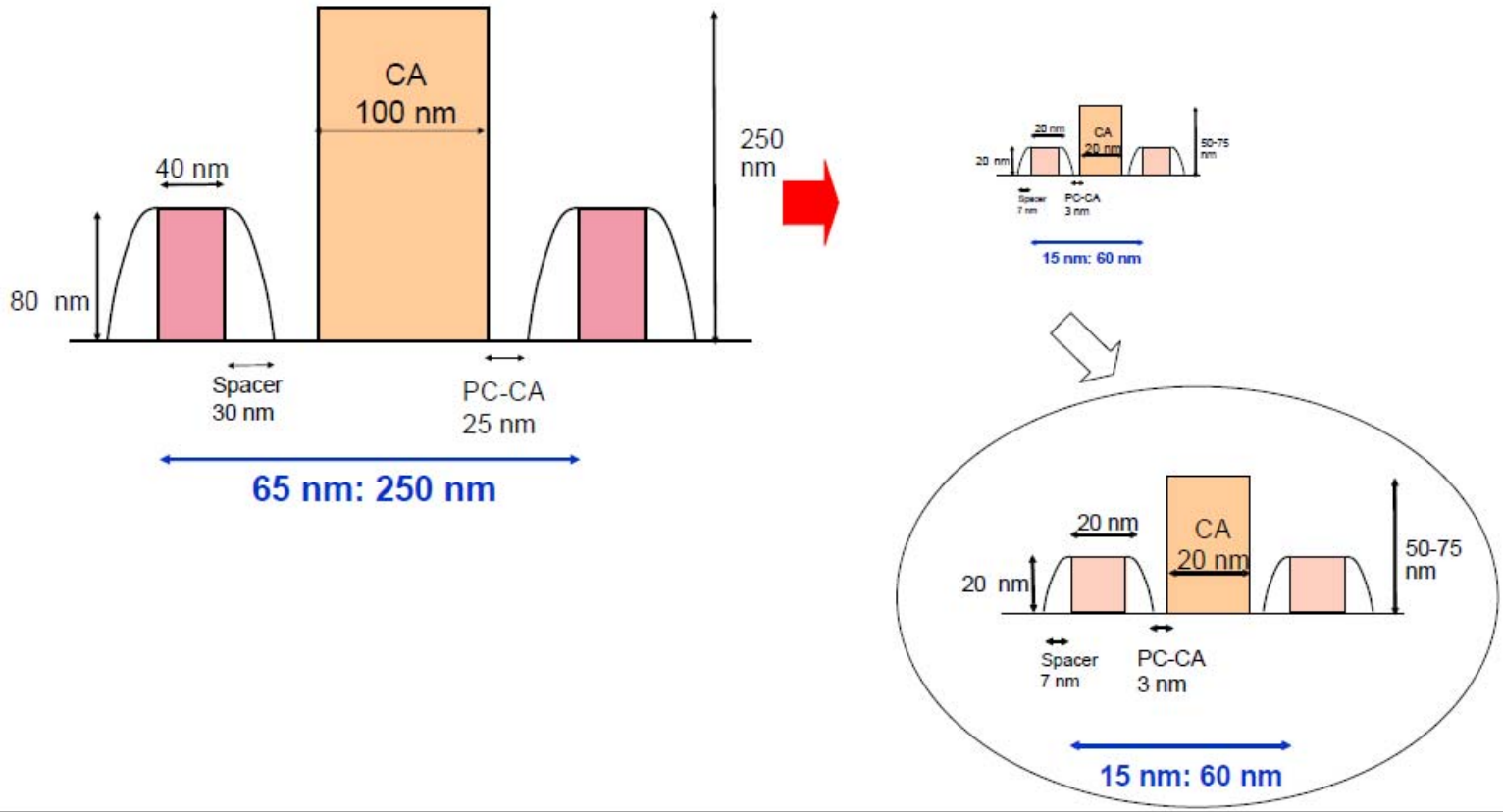
M. Khare: Illustration of 15nm CMOS



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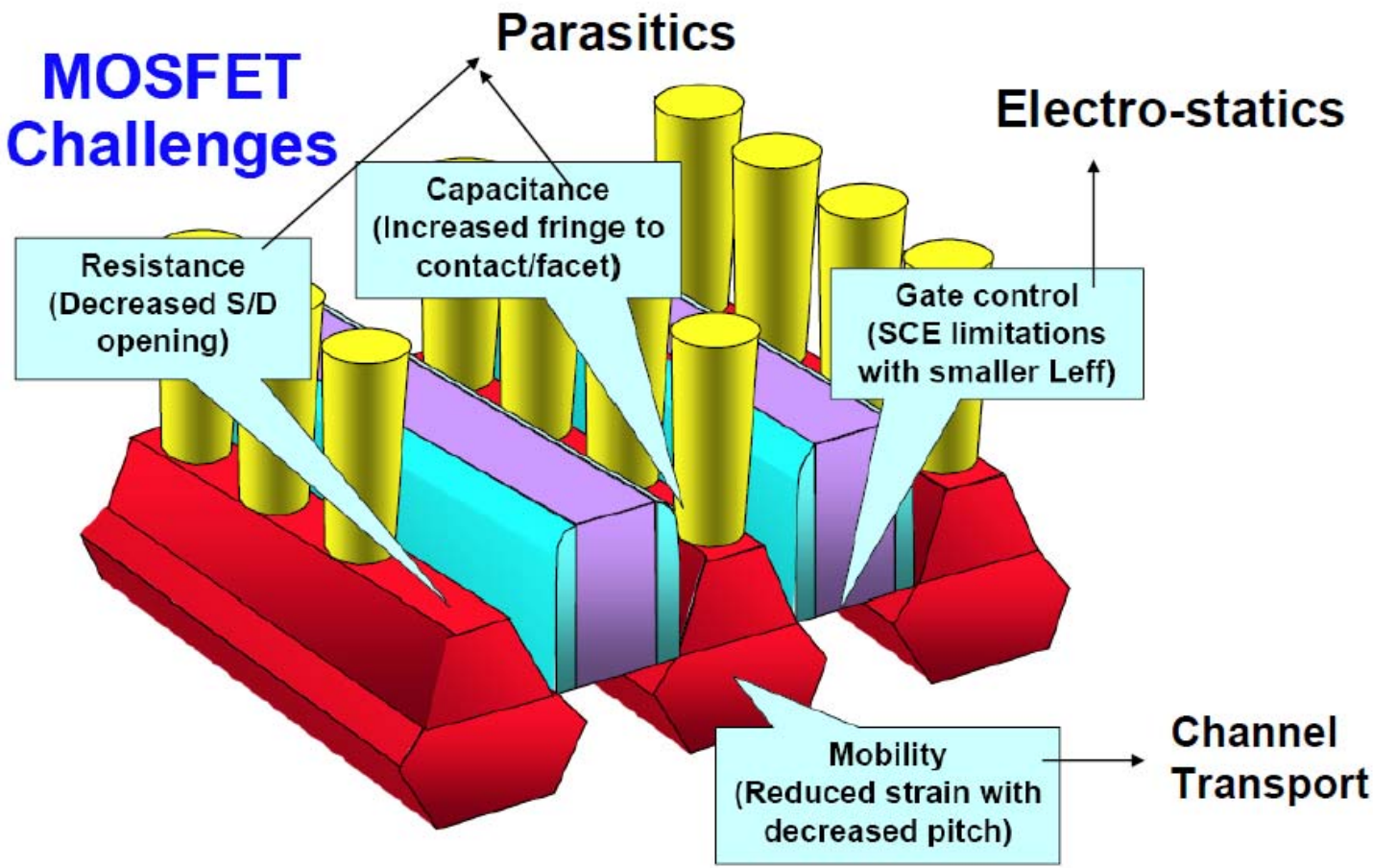
Scaling Challenges



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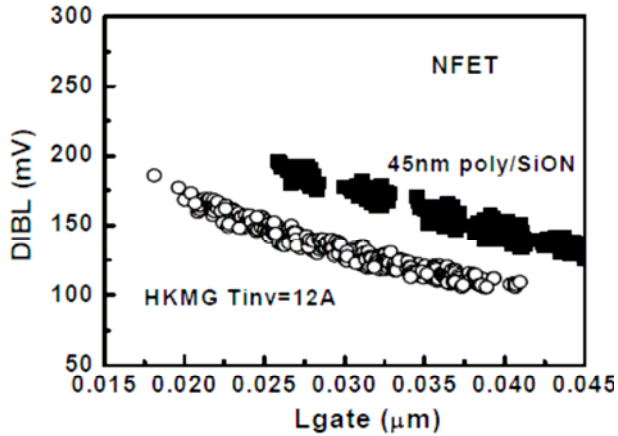
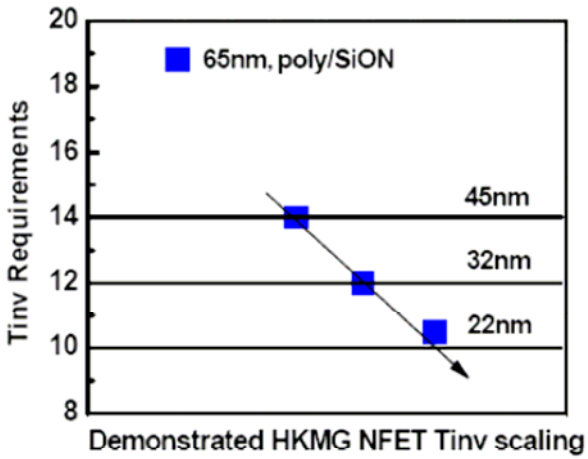
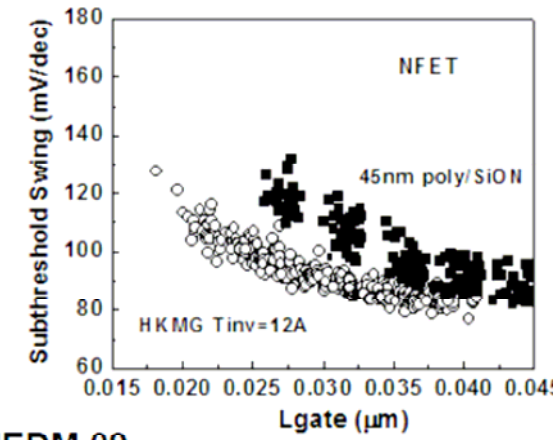
Gate Dielectric Scaling Has to Continue

- Experimental data:
  - DIBL reduction
  - SS reduction
- T_{INV} scaling (hardware) for the future nodes







K. Henson, IEDM 09

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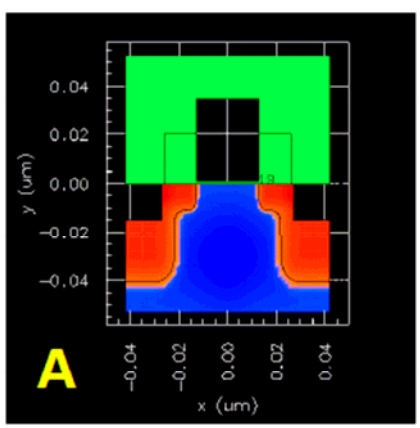
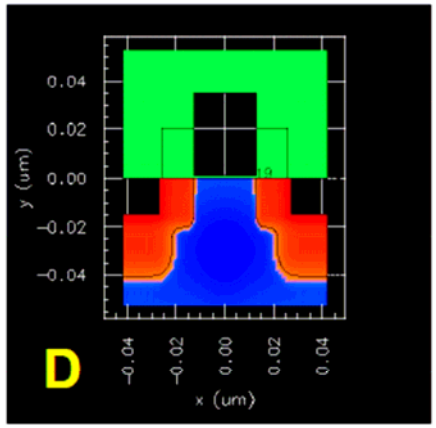
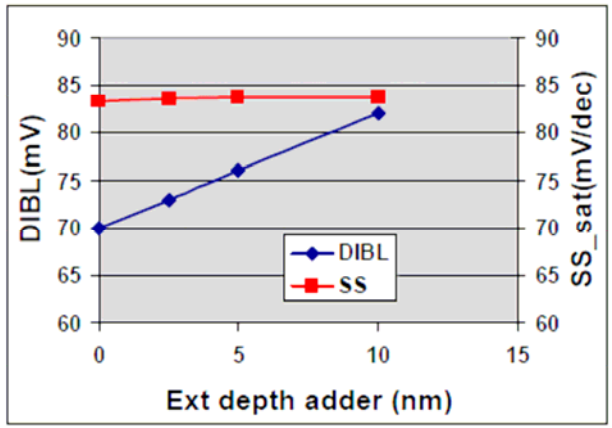
Junction Depths Have to Scale Too

- 15nm Device Design Study for four different extension depth
  - A) Base, B) Base + 2.5nm, C) Base+5nm, D) Base + 10n

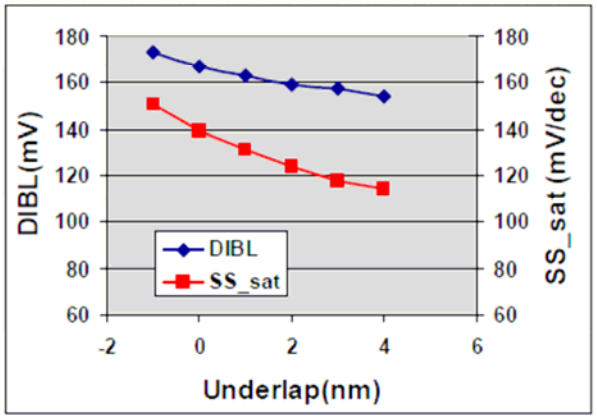


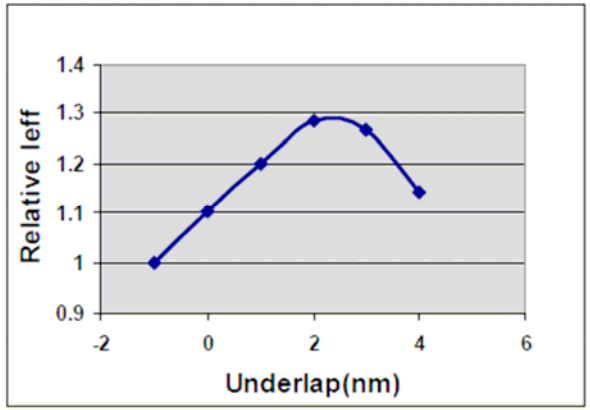




- DIBL increases with junction depth
  - -Field lines from drain reach source away from region of gate control
- SS is rather insensitive to junction depth

Underlap Optimization

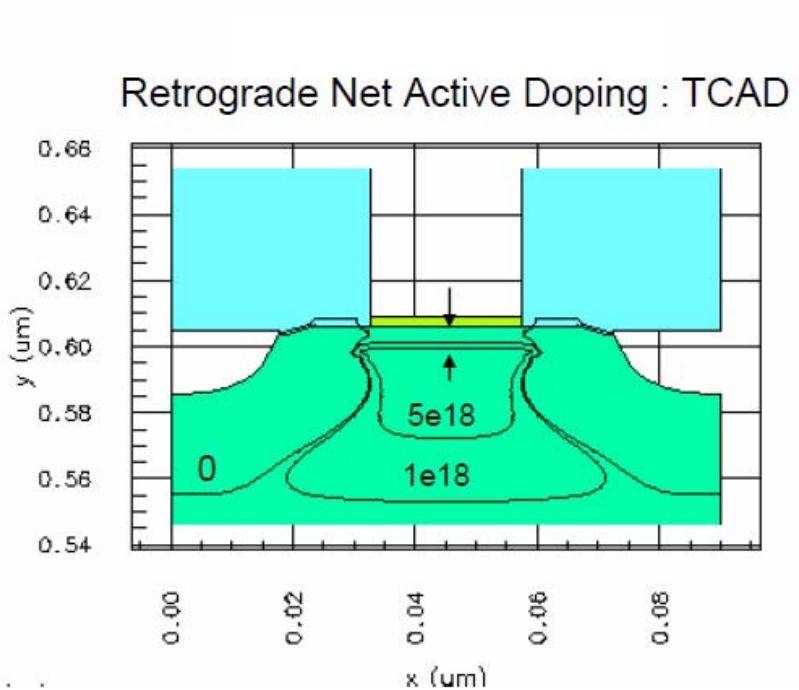




- Effect of under-lap junction on 15nm device electrostatics
  - SS shows improvement with under-lap condition
  - DIBL shows less impact as doping decreases as L increases
- Ieff vs under-lap plot shows Electrostatics vs External Resistance Trade-off
- Under-lap can help electrostatics if initial SCE is poor

Vt Variability can be Improved

TCAD study comparing halo and retrograde well for same Ioff (Dennard and Jin Cai)



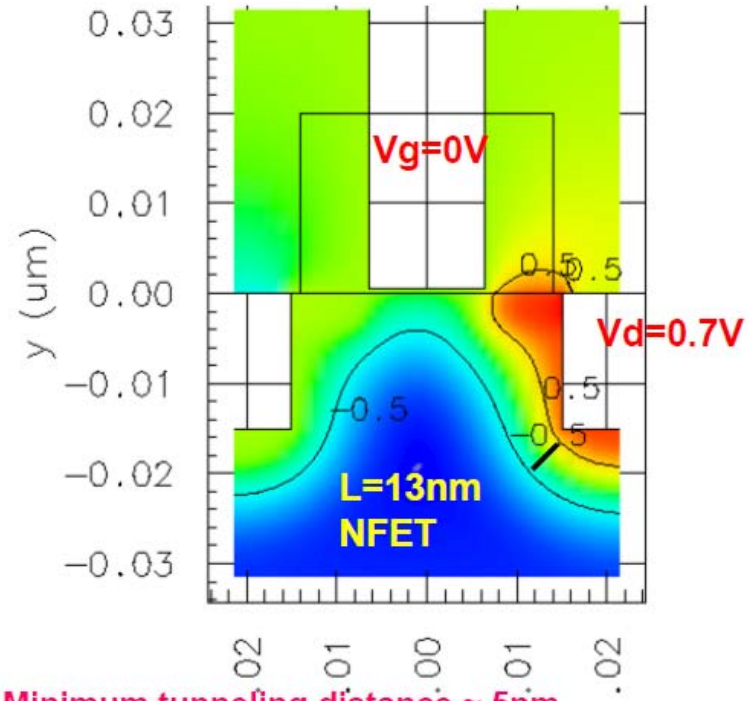
W/L = 40nm/25nm
SRAM Pass gate example

σVt Halo 56mV
σVt Retrograde 28mV

Process innovations and reduced thermal budgets needed to attain steep retrograde profiles (Doping changes > 1 order of magnitude per 10nm)

Retrograde well can reduce σVt by 50% compared to Halo

Band-to-Band Tunnelling Issue for Low Power



Minimum tunneling distance ~ 5nm

BTBT near drain junction botttom ~ 10nA/μm

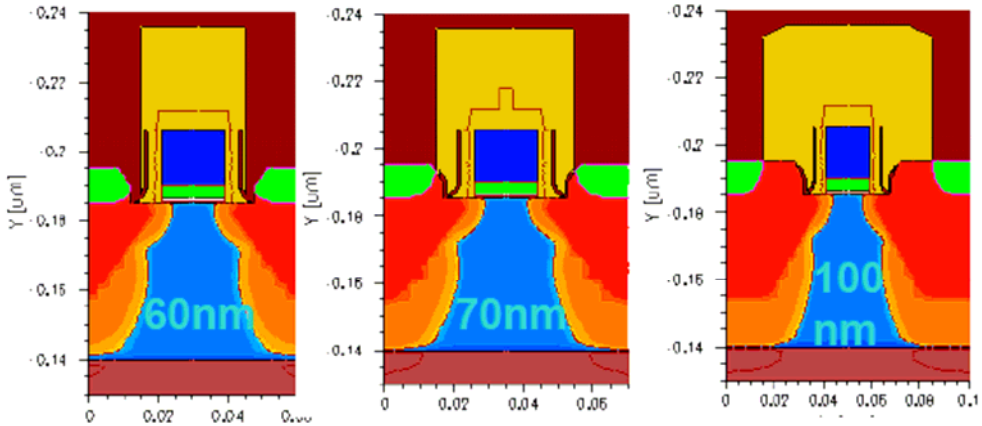
Need BTBT < 30pA/μm

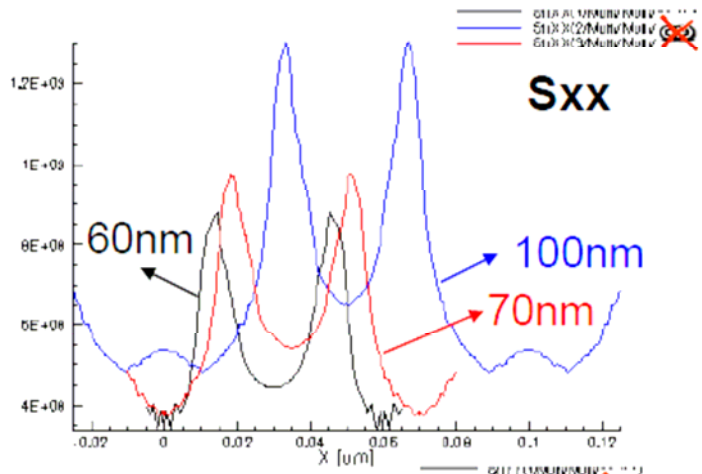
Device under-lap helps with GIDL (BTBT near gate edge on drain side) in addition to helping with SS leakage

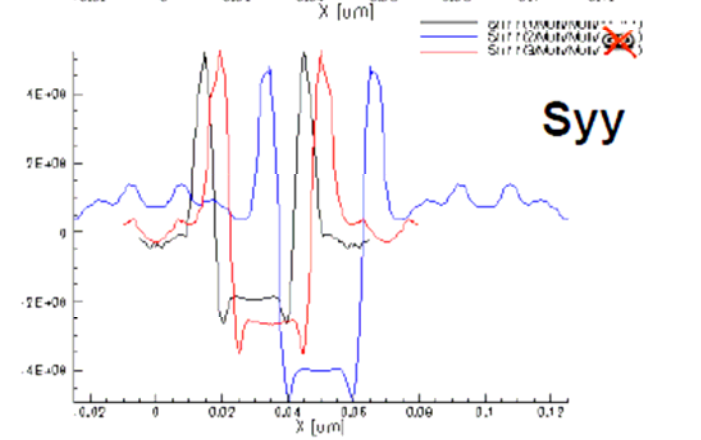
Need intelligent well/SD doping strategies to minimize deep junction BTBT

Pitch-Scaling: Loss of Strain

- Below shows TCAD prediction of stress decay from pitch scaling for 18nm Lgate device





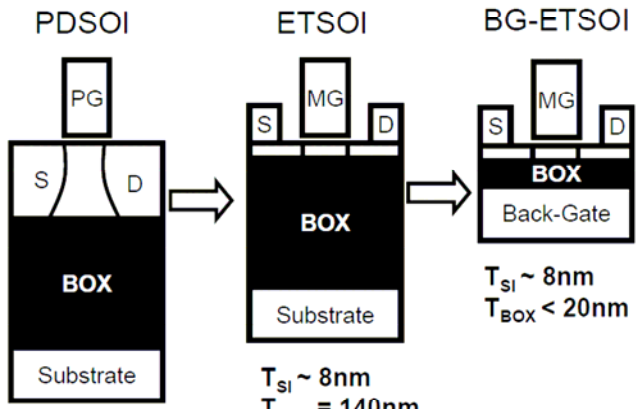


Shrinking pitch for fixed L=18nm shows decreasing Sxx and Syy for NFETs with same stressor proximity

Challenging to compensate mobility decrease from doping and tinv

SOI Progressing to Fully-Depleted Mode

Scaling Path for SOI

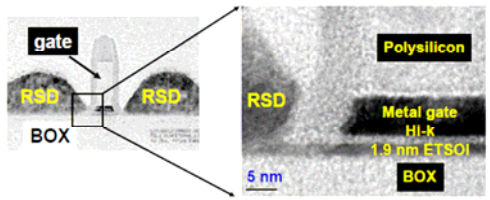


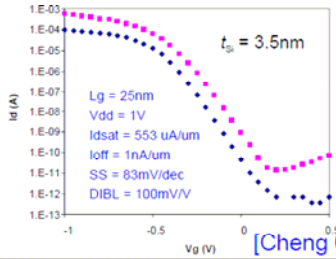
[Cai 08]

ETSOI scaling

- SOI thickness (t_{SI}) scaling is required along with gate length (L_g) as technology is scaled.
  - L_g/t_{SI} ratio is critical for scaling ETSOI while maintaining good electrostatics.

	22nm	15nm	11nm
Lg (nm)	**25**	**20**	**16**
t_{SI} (nm) (L_g/t_{SI} = 4)	**6.3**	**5**	**4**





[Cheng 09-1]

Finfets / Trigates: Parasitics Challenges

- Trigate has less Ctb penalty than FinFET
  - Top channel also conducts current

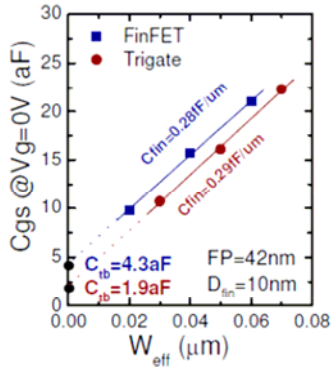


Fig. 4 C_{gs} vs W_{eff}. The extracted C_{tb} of FinFET is 4.3aF per fin, while Trigate has less C_{tb} of 1.9aF per fin.

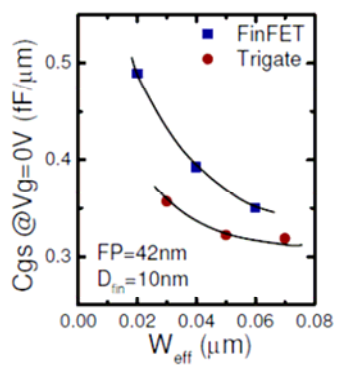
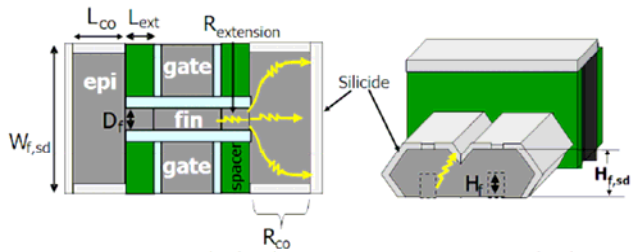


Fig. 5 Normalized C_{gs} vs. W_{eff}. FinFET has ~15% more C_{gs} penalty compared to Trigate at same W_{eff}.

C.-H. Lin, et al., 2010 SOI Conference

- FinFET $R_{parasitic}$ which includes
  - the resistance of the portion of the thin body fin which is ungated (Rextension)
  - current spreading from the thin body region of the source/drain to the epitaxially fattened region
  - current extraction through a three-dimensional silicide profile



- S/D extension engineering and silicide contact resistivity are the keys to lower the parasitic resistance

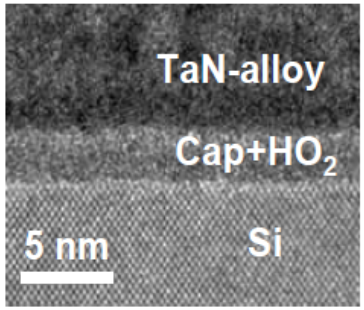
M. Khare: IEDM 10 Short Course – 15nm CMOS Device

Effort Continues to Reduce EOT

SiOx IL modification/Direct Scavenging in Gate First HKMG
K. Choi et al., VLSI 2009

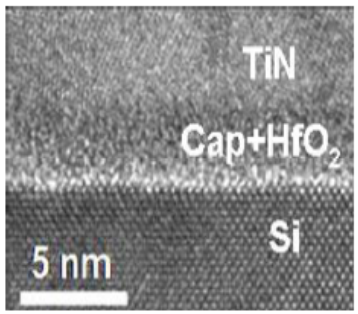
- Silicon interface preparation
- HfO_2 deposition
- Cap layer deposition
- TaN-alloy + Poly-Si deposition
- Gate etch
- Self aligned process flow
- S/D RTA 1000 °C, 5 sec
- Poly-Si silicidation + FGA
- Silicide to M1 process flow

pFET



- Silicon interface preparation
- HfO_2 deposition
- Cap layer deposition
- TiN + Poly-Si deposition
- Gate etch
- Self aligned process flow
- S/D RTA 1000 °C, 5 sec
- Poly-Si silicidation + FGA
- Silicide to M1 process flow

nFET



- **nFET: K boosting cap layer is used=>enables a higher k IL**
- **pFET: SiOx layer is scavenged by TaMN alloy where Gibbs free energy of oxide formation per O atom: |M| > |Si| (> |Ta|): Si reduction / M oxidation thermodynamically favorable**

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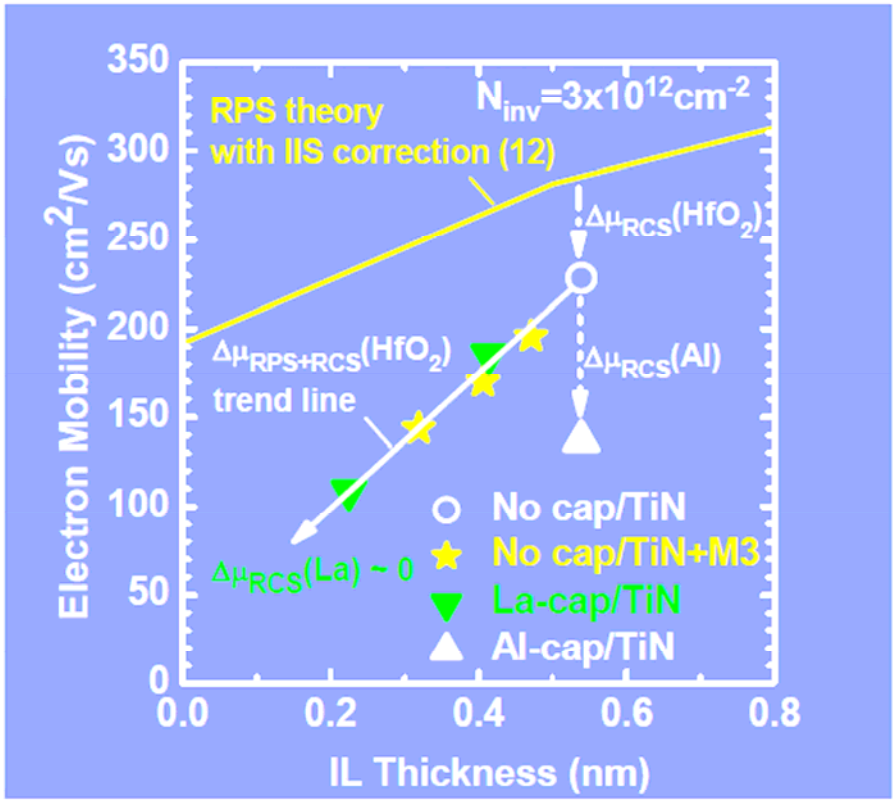
Interface Layer Scaling

T. Ando et al., IEDM 2009



Mobility ∝ $T^{-0.81}$

→Soft optical phonon of HfO_2

$T_{IL} = EOT_{meas} - EOT_{HfO2}$

where

$EOT_{HfO2} = (\varepsilon_{sio2} / \varepsilon_{HfO2}) * T_{physHfO2}$

$\varepsilon_{HfO2} = 20$

(12) M. V. Fischetti et al.,
J. Appl. Phys. **90**, 4587 (2001)

- **Remote IL scavenging → Intrinsic RPS+RCS from HfO_2**
- **La-cap → No additional RCS = Intrinsic IL scaling**
- **Al-cap → additional RCS**

M. Khare (IBM) - Conclusions

Summary – 15nm CMOS Device

- **Conventional device scaling**
  - Aggressive gate stack and junction engineering can enable a stable design point
  - Performance expectations from such device will be limited due to increased parasitic
  - Innovations in mobility and resistance reduction is mandatory to sustain this structure
  - Leakage and variability will be of fundamental concern for such device adoption
- **Fully Depleted devices are viable alternative**
  - A promising alternative is emerging and may find its way into 15nm
  - Electrostatics, intrinsic variability and leakage characteristics are superior
  - Un-doped body offers better mobility
  - Several parasitic effects need to be understood and addressed
  - Manufacturability challenges of alternate devices will dominate its introduction
- **High-K Metal Gate**
  - Need constant innovations for aggressive EOT scaling (<0.6nm)
  - Scaling by the use of IL scavenging is one promising path

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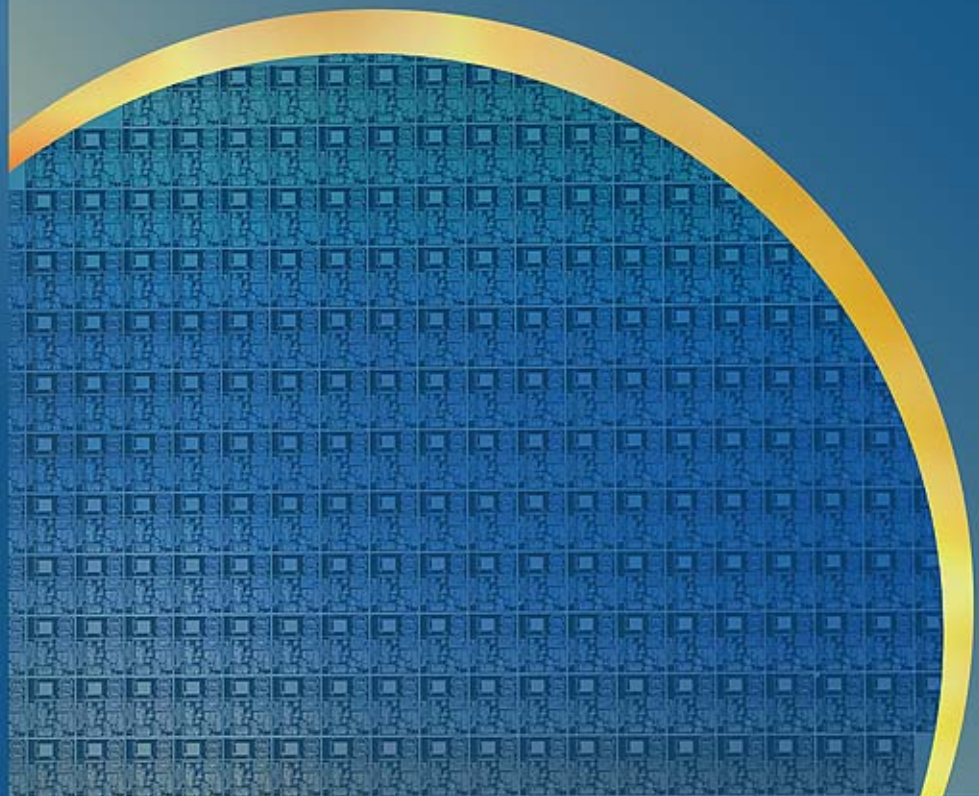

Innovation
Speed
Solutions