High Performance Germanium N-MOSFET with Antimony Dopant Activation Beyond $1x10^{20}$ cm^{-3}

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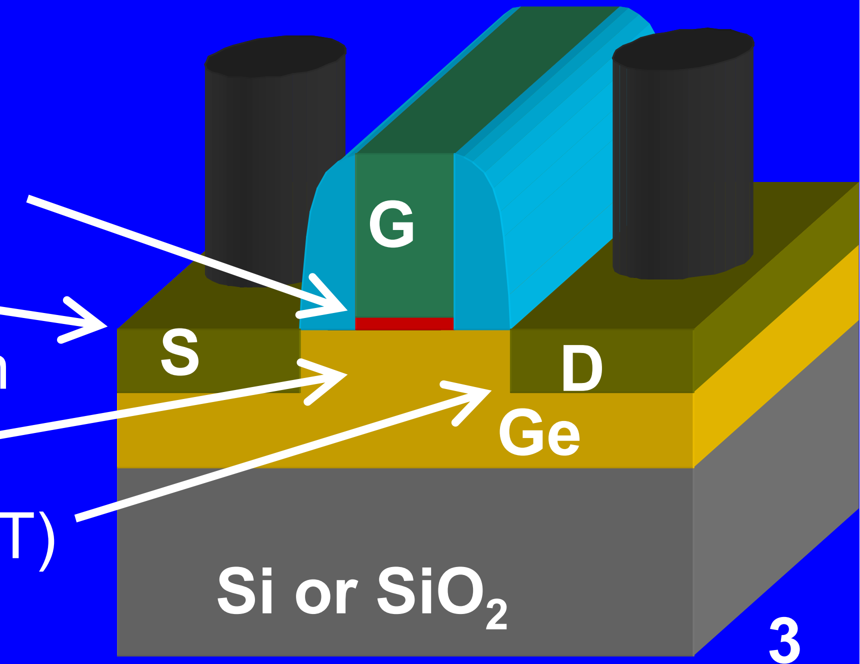
Outline

- Germanium MOS : problems and solutions
- Dopant activation in Ge
- Laser Thermal Processing (LTP)
  - Theoretical calculations
  - Sheet resistance & TEM
  - Raman analysis
  - SIMS
  - Spreading Resistance Profile (SRP) & benchmarks
  - N+/P junction diode
  - MOSFET
- Contributions
- Future Work

High Mobility Channel Ge

	Si	Ge
Bulk μ_e(cm²/Vs)	1600	3900
Bulk μ_H(cm²/Vs)	430	1900
Band gap (eV, 300K)	1.12	0.66
Dielectric constant	11.9	16

- Advantages
  - High carrier mobility
  - Compatible to Si LSI
  - Lower T process
  - V_{dd} scaling
- Problems
  - Surface Passivation issues
  - Deep S/D junctions
  - Poor N-type dopant activation
  - Small electron mobility gain
  - Band-to-band tunneling (BTBT) leakage



Ge MOS and Solutions

- **Surface Passivation Issues**
  - **Thermal[1] GeO_2[2], Ge_3N_4 Interfacial Layers (IL) with High-k**
  - **Ultra-thin[3] GeO_2 IL using SPA radical oxidation**
- **Ultra Shallow Junctions[3]**
  - **Plasma Immersion Ion Implantation (P-III)**
- **High Dopant Activation**
  - **Laser Thermal Processing (LTP)[4]**
  - **Rapid Thermal Annealing (RTA) [5]**
- **Mobility Booster- Uniaxial Stress Engineering[6]**
- **BTBT Reduction - Si-Ge-Si Hetero-structure design[7]**

[1] T. Nishimura et al. , VLSI Symp. 2010, [2] D. Kuzum et al. , IEDM 2009
[3] G.Thareja et al, Dev. Res. Conf., 2010 [4]] This work
[5] G. Thareja et al., Elec. Dev. Lett. (unpublished), 2010.
[6] M. Kobayashi et al, VLSI Symp. 2009, [7] T. Krishnamohan et al, VLSI Symp. 2006

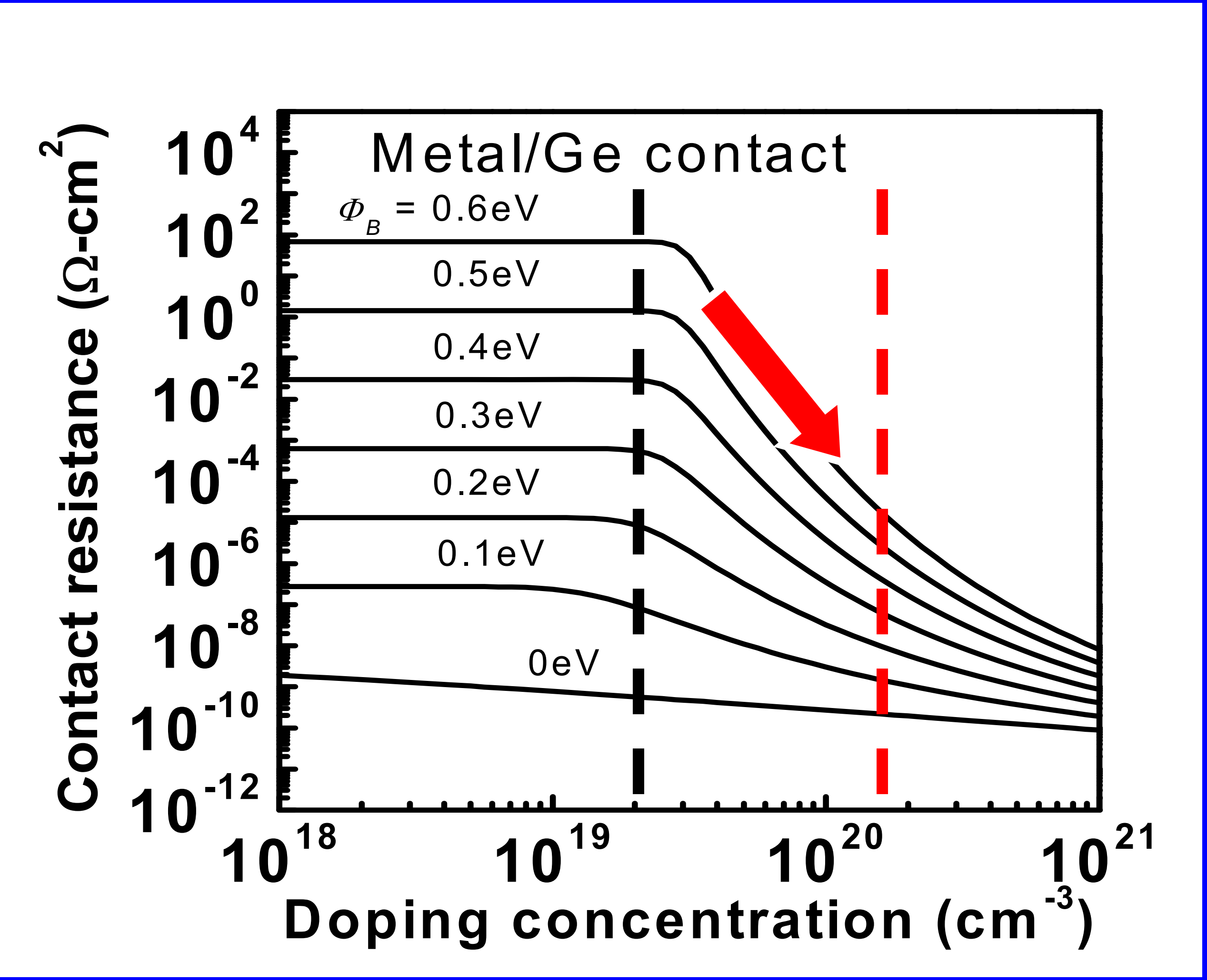
Poor Dopant Activation: Parasitic Resistance

- **Impact of series resistance**
  - Decrease gate overdrive
  - g_m reduction
- **Resistance scaling**
  - Channel resistance scalable
  - Contact resistance not scalable

$$\rho_c \propto \exp\left(\frac{\Phi_B^{eff}}{N_{sd}^{1/2}}\right), area^{-1}$$

$$R_{sh} \propto \frac{1}{N_{sd} x_j}$$

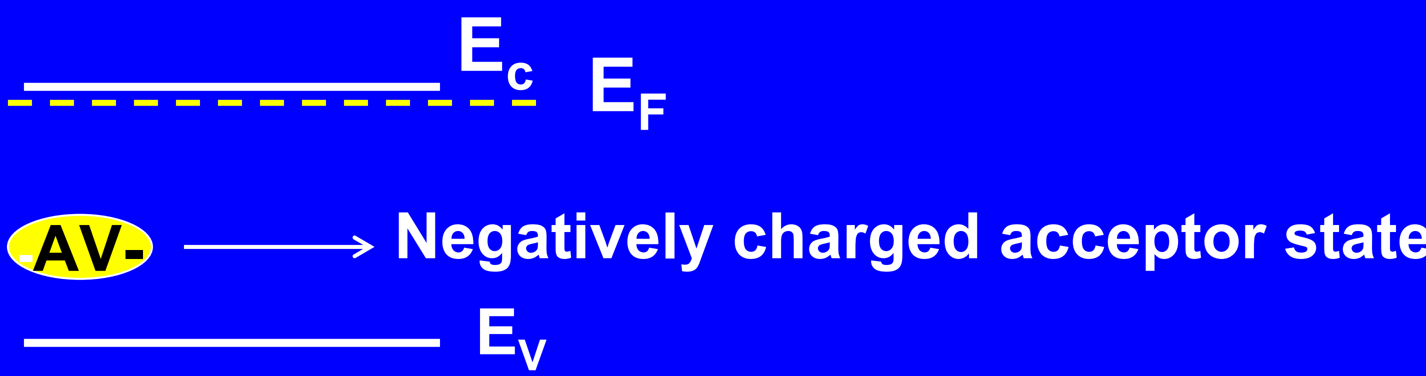
Contact Resistance



Doping ↑, ρ_c ↓

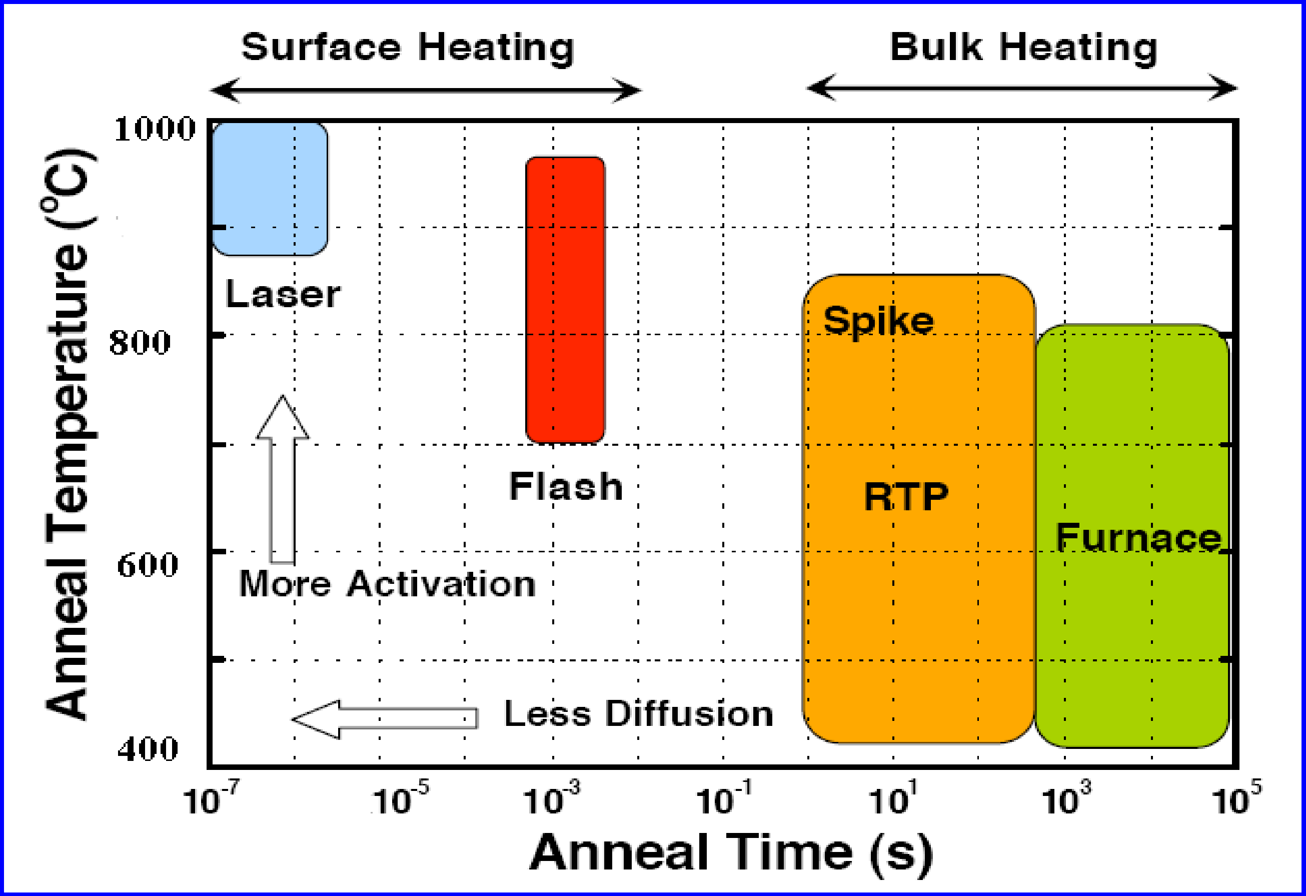
N-type Dopant Activation in Ge

- Ion implantation generates damage in Ge.
- Damage centers form acceptor level defects[1,2]
  - Compensates the donor electrical activation



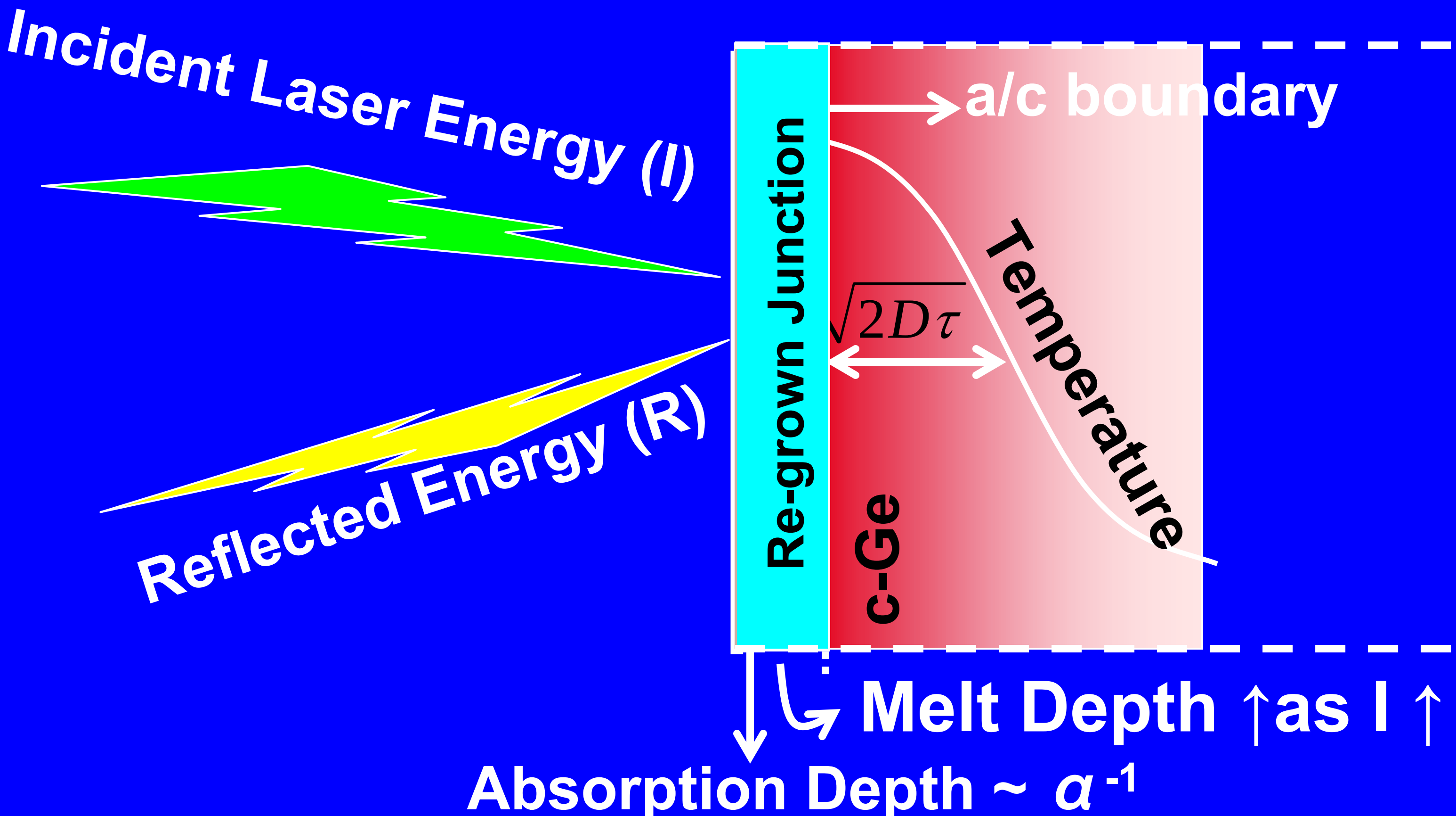
[1] A. Chroneos et al., J. Appl. Phys., 113724, 2008
[2] V.P. Markevich et al., Phys. Rev. B, 235213, 2004

Dopant Activation for USJ in Ge



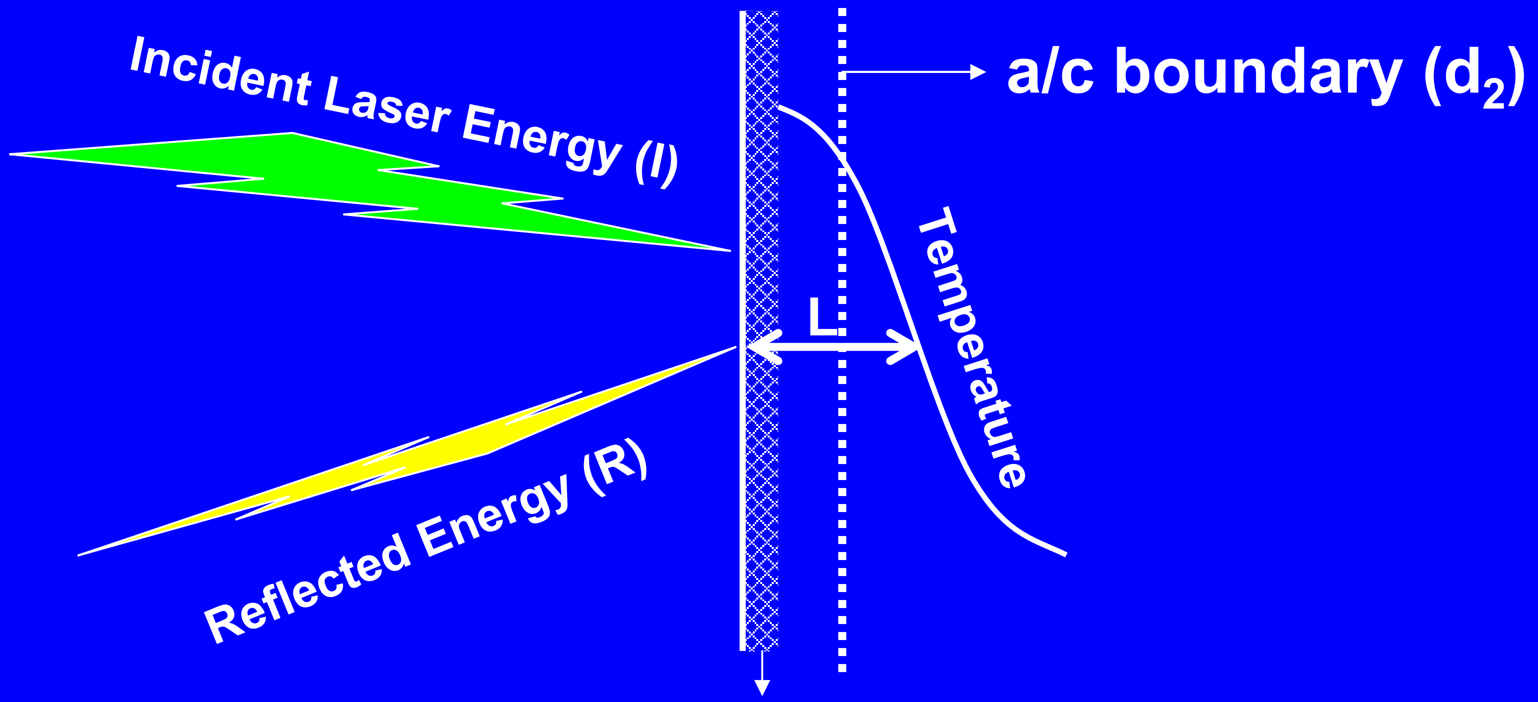
- Laser Thermal Processing (LTP)
  - High dopant activation
  - Reduced diffusion
  - Implantation damage annihilation (Melt – Regrowth)

LTP Scenario



Melt → **Regrowth**

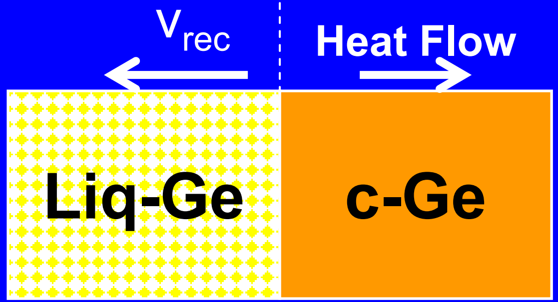
Theoretical Estimation of Laser Anneal Parameters



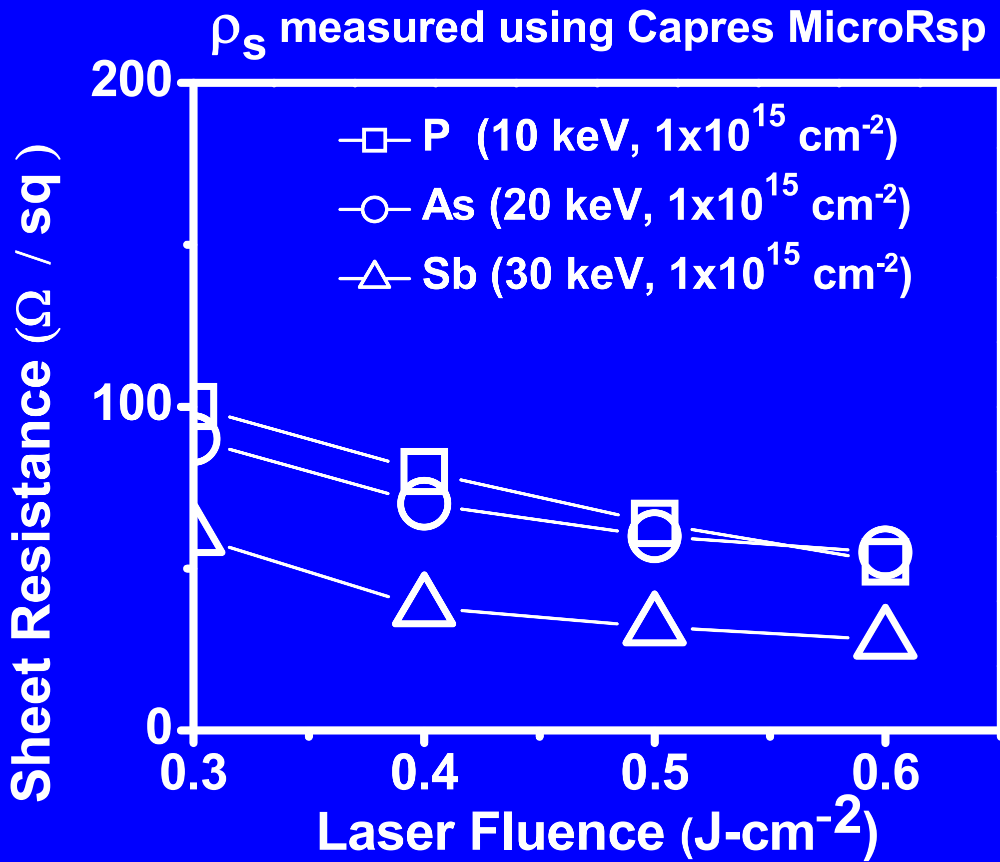
Absorption Depth (d_1) ~ α^{-1}

- D = Heat Diffusivity (cm^2/sec)
- τ = Pulse width
- α = Absorption Coefficient (cm^{-1})
- L = Characteristic Heat Diffusion length = $\sqrt{2D\tau}$
- d_1 = Laser Absorption Depth = α^{-1}
- d_2 = amorphous/crystalline (a/c) boundary depth

- Heat diffusivity = D = $\kappa / \rho C_p \sim 0.2\ cm^2/s$
- Characteristic heat diffusion length = L = $\sqrt{2D\tau}$
- Absorption depth = $d_1 = \alpha^{-1}$ = 20nm
- $d_1 << L$
- a/c boundary depth = $d_2 \sim$ 20nm (order of x_j)
- $d_2 << L$ (One pulse is sufficient to melt the a region)
- Annealing threshold
  - Heat required to melt the amorphous region
    - $C_p * \rho * d_2 * \Delta T = (1 - R) * I * \tau$
    - $I \sim 0.3\ J/cm^2$ (Shallower junctions have low annealing threshold)
- Re-crystallization velocity (v_{rec})
  - Latent heat liberated at the a/c interface = $\Delta H_m * \rho * v_{rec}$
  - Heat flow into the substrate ~ $\kappa * (T_m / L)$
  - Heat balance ⟶ $v_{rec} \sim$ 7 cm/sec

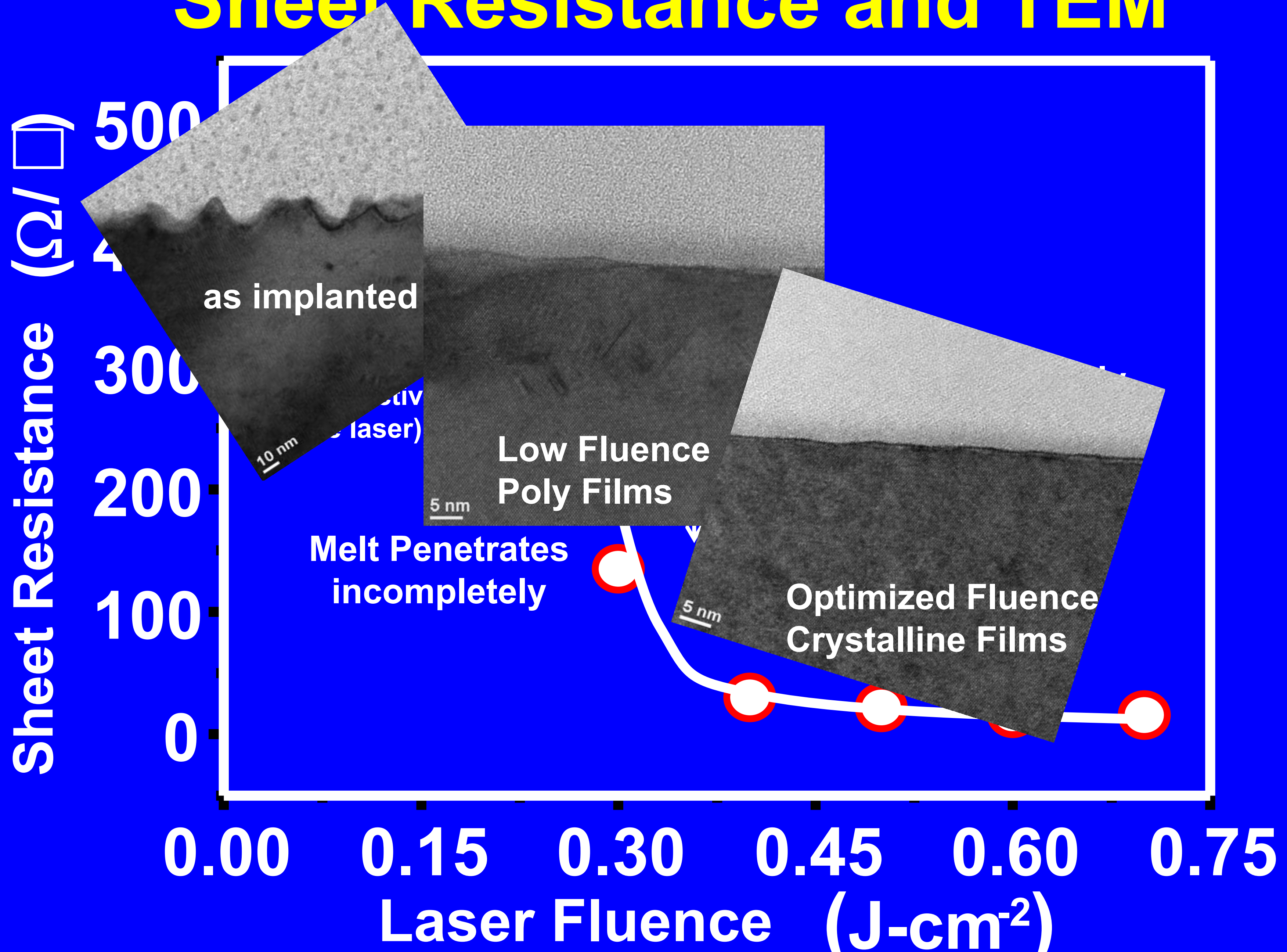


Sheet Resistance

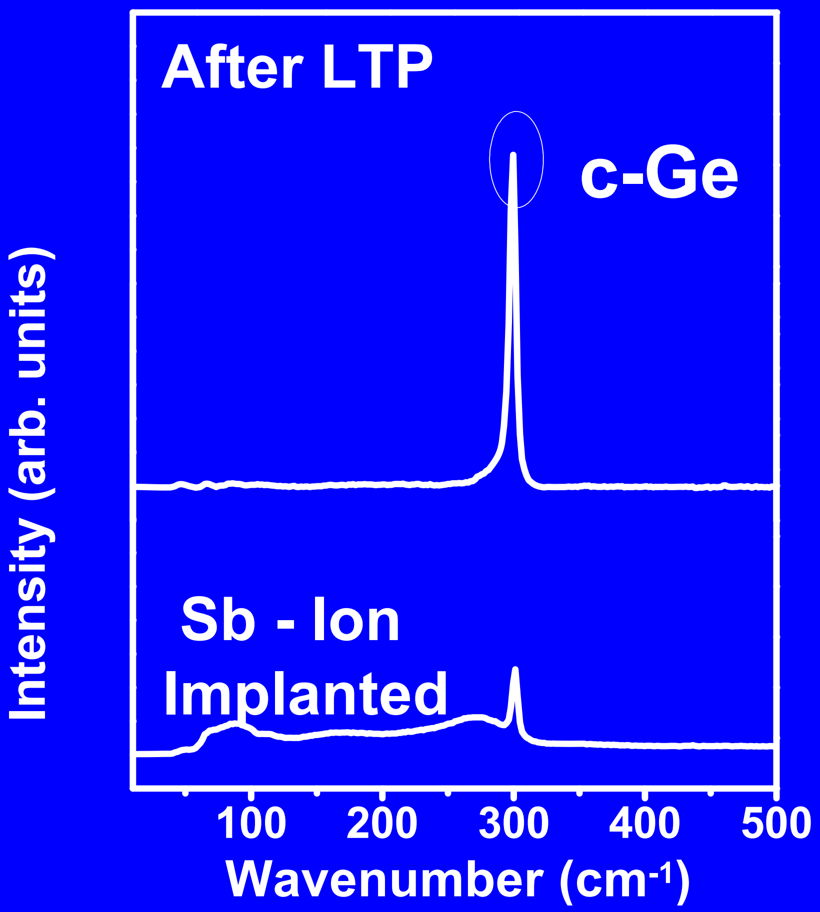


Sb implantation provides the lowest sheet resistance (as implanted junction depth is similar for all species)

Sheet Resistance and TEM

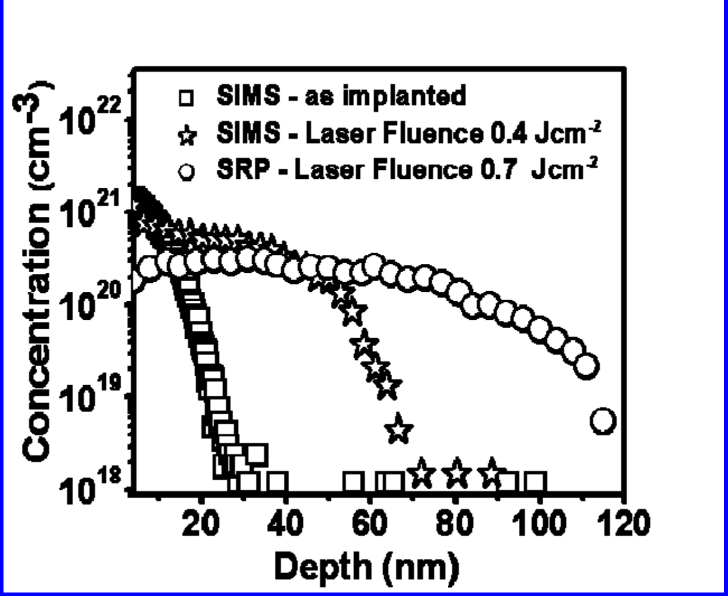


Crystallinity of LTP Junctions



Crystallinity restoration confirmed using Raman

Dopant Activation

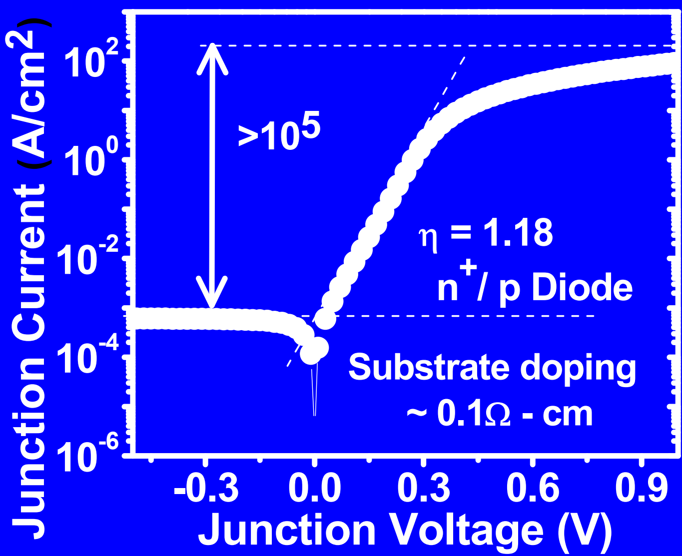


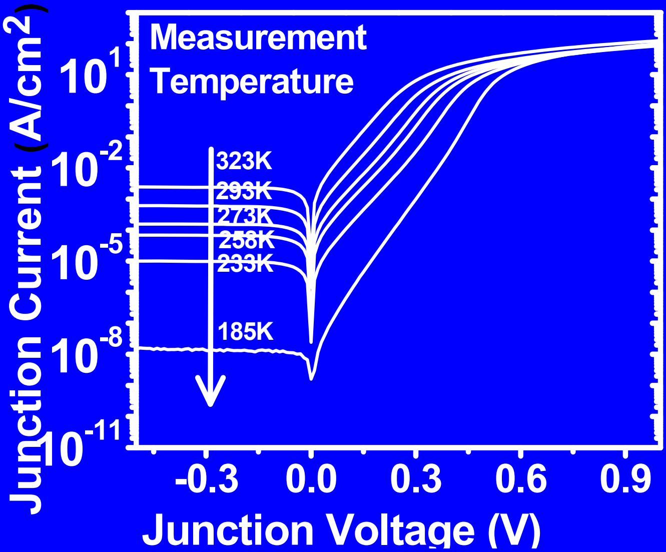
Doping Method	Annealing Method	Dopant Activation(cm^{-3})
Ion Implantation	RTA	Sb- 8×10^{18} / As 8×10^{18}/ P-2×10^{19} /B-1×10^{20} [1]
Ion Implantation	Flash Anneal	P - 6×10^{19}[2]
In-situ doping	Thermal	P-1×10^{19} [3]
Gas Phase Doping	RTA	As-1×10^{19} [4]
Ion Implantation	Furnace Anneal	P – 8×10^{18}[5]
Ion Implantation	LTP	Sb > 1×10^{20}

Dopant Activation > 1×10^{20} cm^{-3}

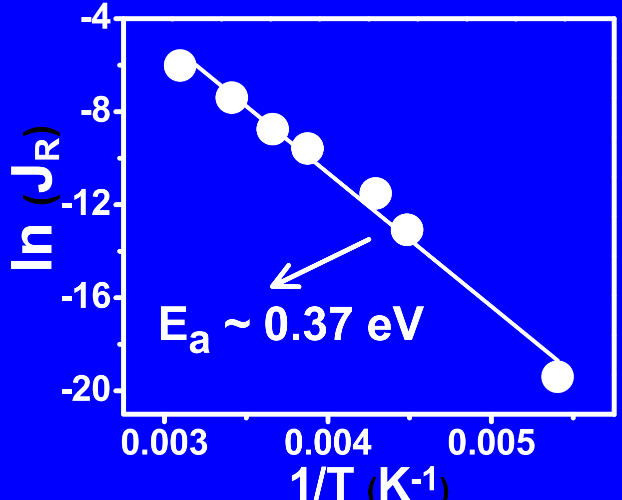
[1] C.O.Chui, et al. APL, 2003, [2] C. Wundisch, et al. APL, 2009, [3]H.-Y. Yu, et al., IEDM' 09, [4] Takagi et al., IEDM'09 [5] D.Kuzum, et al., IEDM'09

N+/P Diode



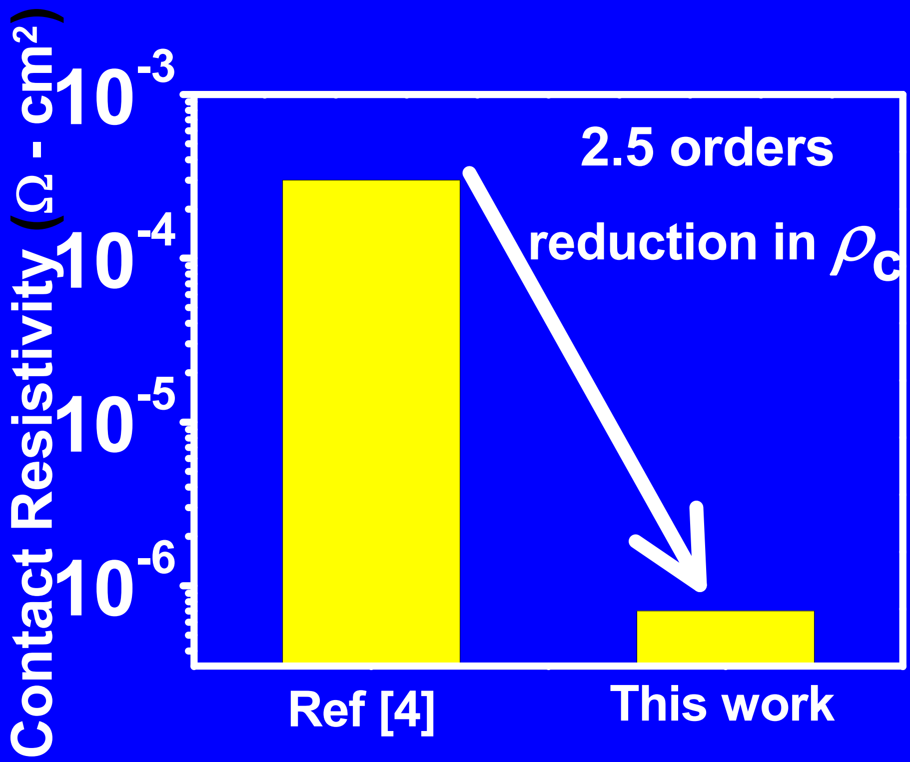


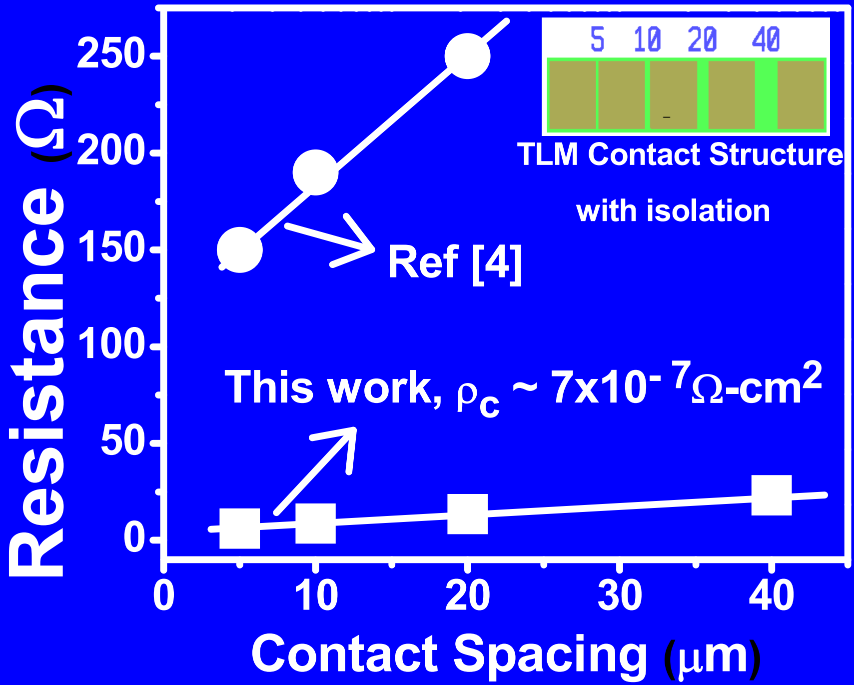
High I_{on}/I_{off}, $\eta < 1.2$



$E_a \sim E_g / 2$, No defect assisted current

Contact Resistivity (ρ_c) & Benchmark

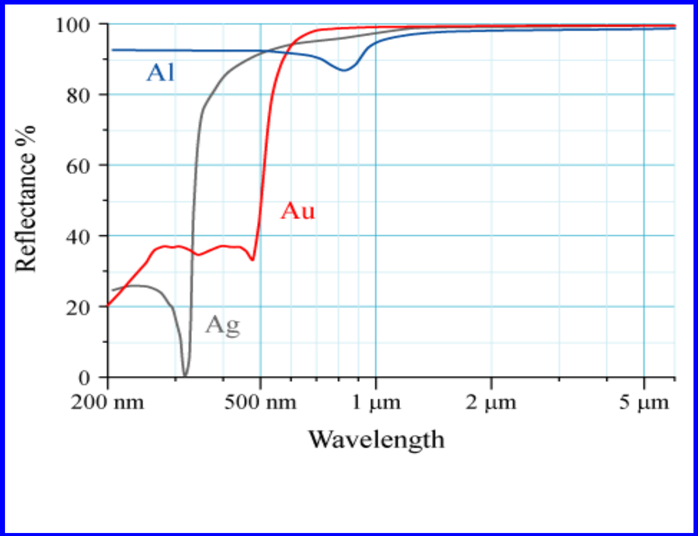


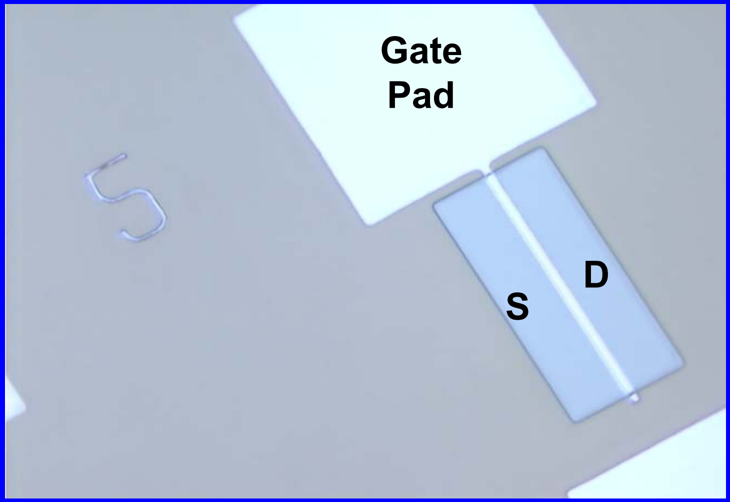


Significant reduction in Metal / N^+ Ge ρ_c of 7×10^{-7} Ω-cm^2

[4] **J. Oh et al.,** VLSI 2009, p. 238

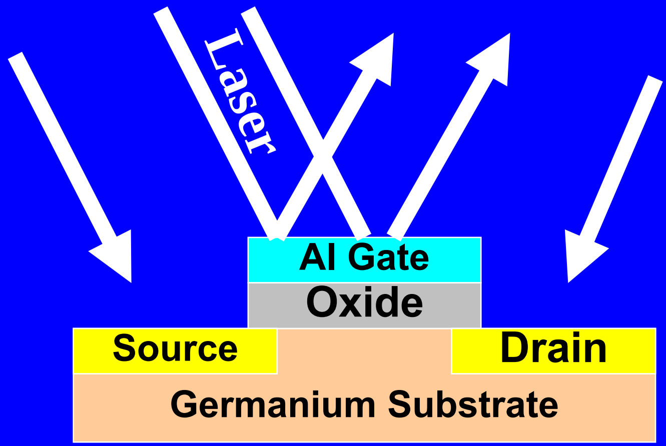
Gate First MOSFET Process





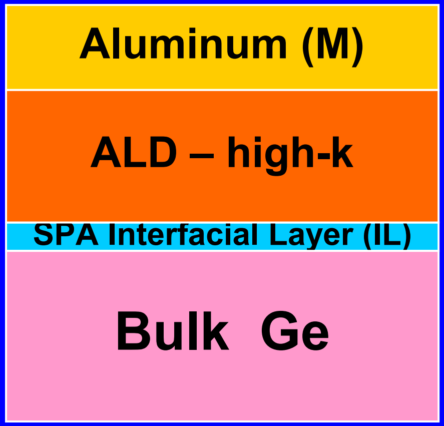
Aluminum (low ψ_m) reflective across a wide wavelength range

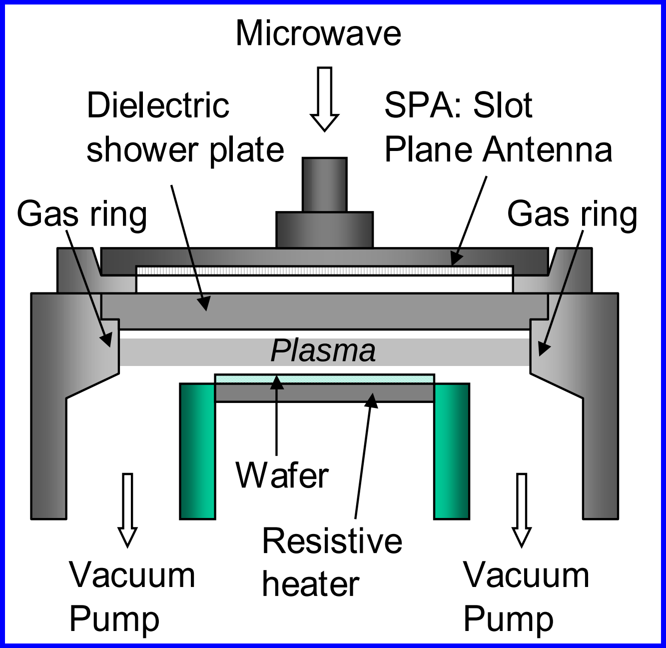
Bright Field Image: Single pulse laser shot
No visible damage effect on transistor structure



Process Flow for MOSFET

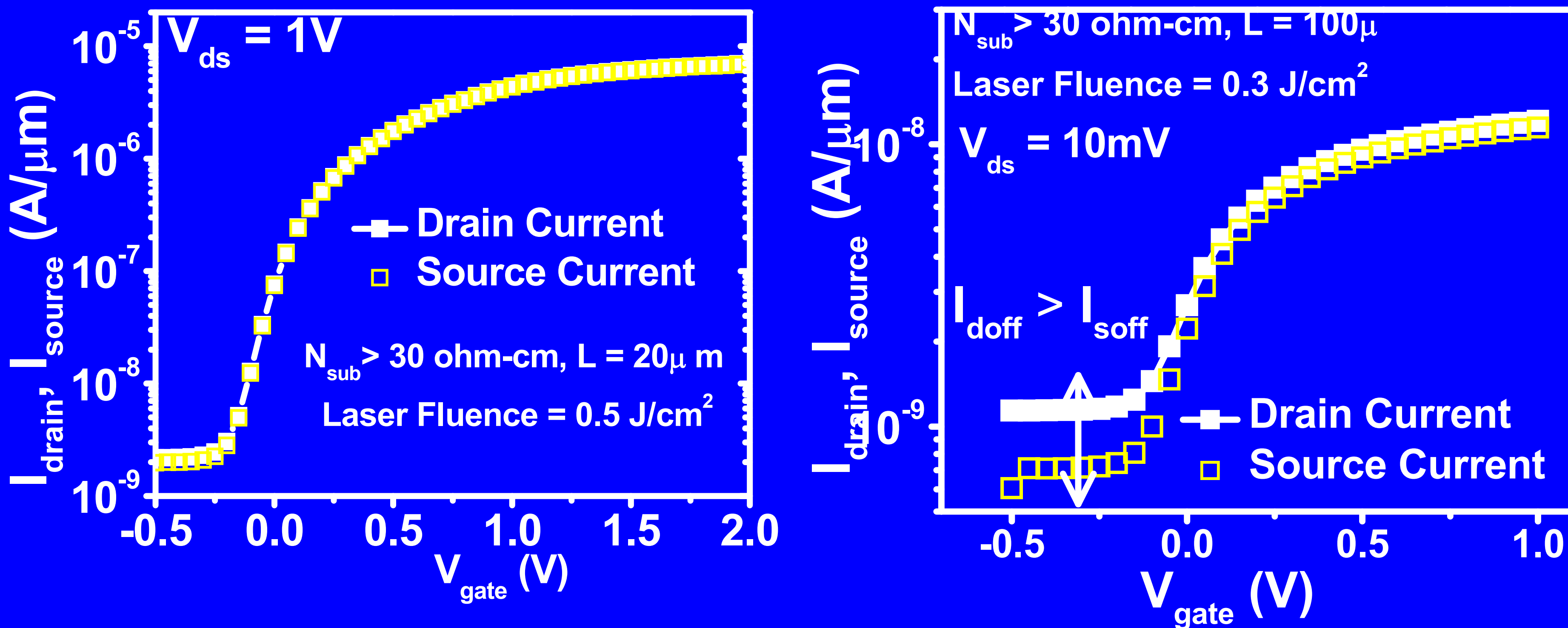
- Ge surface clean (cyclic HF, HCl last)
- SPA 1nm ultra-thin GeO_2 IL
- TMA+O_3 5nm ALD Al_2O_3
- 150nm Al ebeam evaporation
- PMA: FGA 400C, 30min
- Metal Gate Patterning
- S/D Doping: Sb – 30 keV, $1x10^{15}$ cm^{-2}
- Laser Thermal Processing (LTP)
- HF/HCl contact cleaning
- Ti (5 nm)/Al(95 nm) contact metal





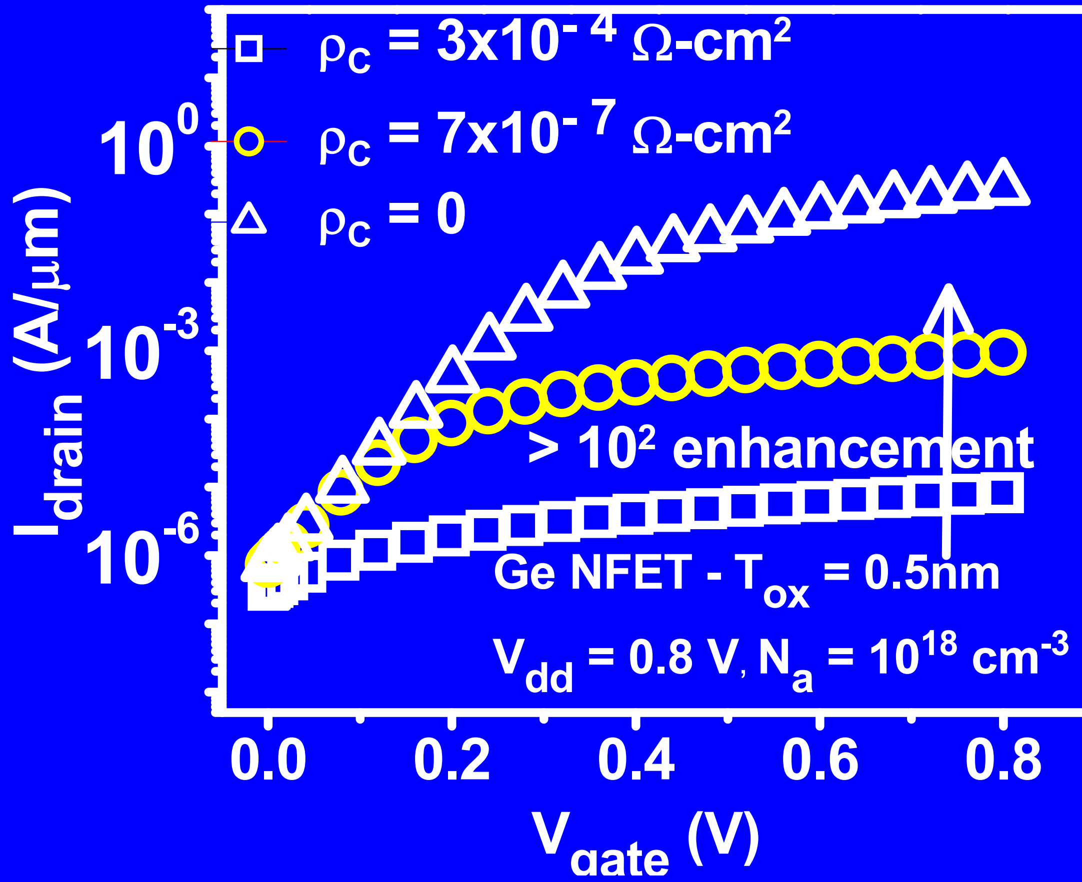
M. Kobayashi et al, VLSI Symp. 2009

MOSFET results



Unoptimized laser fluence causes discrepancy between I_{drain} and I_{source} due to high diode leakage

Performance Projections



Drive current enhancement for 22nm HP ITRS node

Contributions

- **First demonstration of High dopant activation (> $1x10^{20}$ cm^{-3}) using Sb dopants (n-type) in Ge**
  - **Well behaved n^{+}/p diodes (I_{on}/I_{off} > $1x10^{5}$, $\eta < 1.2$).**
  - **Lowest contact resistivity for metal (Ti/Al)-n^{+} Ge contacts ($7x10^{-7}$ Ω-cm^{2})**
  - **MOSFET integration**

Thank you for your time & patience !