Review of IEDM 2010 Conference

Susan Felch
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From The Future Si Technology Perspective: Challenges and Opportunities, Dr. Kinam Kim, Samsung

Key technologies for the future Si CMOS era

Example of vertical NAND structures

(a) P-BiCS
(b) TCAT
Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications, Intel
Self-aligned III-V MOSFETs heterointegrated on a 200 mm Si substrate using an industry standard process flow, Sematech.
Self-aligned metal Source/Drain InxGa1-xAs n-MOSFETs using Ni-InGaAs alloy, University of Tokyo

(a) Pretreatment
   (Acetone, NH₄OH, (NH₄)₂S)
   ALD : Al₂O₃ 10 nm

(b) Ni gate evaporation and gate patterning

Ni-InGaAs S/D formation
   - (c) S/D Ni evaporation
   - (d) RTA at 250°C for 1 min
   - (e) removal of unreacted Ni
     (Selective etching)

(f) Electrode formation

- p-InGaAs
- p-InP

- Gate

- Ni for S/D

- RTA

- Ni-InGaAs alloy

- Selective etching
Physical Origin of pFET Threshold Voltage Modulation by Ge Channel Ion Implantation (GC-I/I), Toshiba & IBM

**Fig. 5:** pFET $\Delta V_{TH}$-EOT plots of Al I/I into IL and GC-I/I. Plots of Al-cap on top of HK are also shown as a reference. Large pFET $V_{TH}$ shifts can be realized by both cases, however, huge EOT degradation occurs in the Al I/I case similar to Al-cap trend. On the other hand, GC-I/I induces ~+500mV $V_{TH}$ shift with no $T_{inv}$ increase.

**Fig. 19:** Schematic of Ge pile-up at IL/Si interface. Ge piled-up at IL/Si interface forms fixed charge/dipoles resulting in enhanced pFET $\Delta V_{TH}$ in the case of RTO IL process.
Ground plane implants are In$^+$ and As$^+$
Novel Stress-Memorization-Technology (SMT) for High Electron Mobility Enhancement of Gate Last High-k/Metal Gate Devices, Samsung

Fig. 1. Schematic S/D SMT process flow.

Fig. 4. Mask-edge dislocation image of SMT sample with deep PAI: multiple mask edge defects can be observed.

Fig. 5. Simulated SMT-induced channel stress: deep PAI SMT (multiple mask edge dislocation) shows much higher channel stress than the normal shallow PAI SMT (single mask edge dislocation).
Contact Resistance Reduction to FinFET Source/Drain Using Dielectric Dipole Mitigated Schottky Barrier Height Tuning, Sematech

Fig. 3. Cross sectional schematic illustrating FinFET fabrication using DDM-SBH tuning technique.

Fig. 6. $R_{SD}$ calculation using method described in [9]. Addition of AlO$_x$ in the contact hole results in $\sim$25% reduction in $R_{SD}$. The strong overdrive dependence on $R_{SD}$ is due to underlap architecture.
Strained SiGe and Si FinFETs for High Performance Logic with SiGe/Si stack on SOI, Sematech

Fig. 1. Process flow for four different SiGe/Si stack FinFET

Fig. 17. SiGe (20nm)/Si (20nm) improved mobility on p-FinFET by ~46% compared to Si.

Fig. 19. SiGe (20nm)/Si (20nm) nFinFET shows ~67% degraded mobility relative to Si.
Reliable Single Atom Doping and Discrete Dopant Effects on Transistor Performance, Shinada, Waseda University, Japan

Fig. 1 Single atom doping method for evaluating the influence of various discrete dopant distribution on device performance. Single ions are injected through an aperture into the sample, where they dope the surrounding material. The dopant distribution is then analyzed using a focused ion beam and a liquid metal ion microscope.

Fig. 2 Systematic studies of discrete dopants on transistor performance. Ordered distribution of dopant atom serves to improve the device performance (a). The influence of asymmetric discrete dopant distributions on the electrical properties has been investigated in this work (b, d). Note that the number of single ions is controlled by detecting secondary electrons for all devices.

Fig. 10 Bar chart of $\Delta I_d/I_d$ for devices with ordered (a, b) and random (c, d) distribution of dopants. All devices show the positive variation of $\Delta I_d$ by interchanging source and drain terminals. The current increase is believed to be attributed to the suppression of injection velocity degradation at the source-side due to the asymmetric discrete dopant distribution. $\Delta I_d$ tends to increase with increasing in $V_d$. 