Rapid Thermal Processing 2010

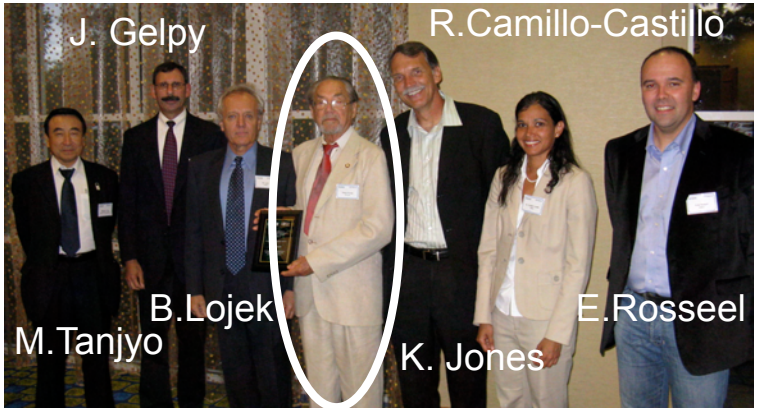
Highlights: Sept 28-Oct 2, 2010, Gainesville FL

Michael Current
Current Scientific, San Jose, CA USA

1. **J.O. Borland:**
   Melt and sub-melt anneals for 22 nm CMOS.
2. **S. Chen/Ultratech:**
   Dual beam laser anneals.
3. **E.Rosseel/IMEC & M.Tanjyo/Nissin:**
   C7 implants for strain and P diffusion control.
4. **K.Huet/Exico, J. Brune/Coherent:**
   Backside laser melt for power switches & sensors.

RTP 1993-2010; 18 years: 822 papers

Bo Lojek
RTP Chairman Extraordinaire



2010 J. Gibbons Award to Si Prussin

RTP Hard Core Group: Friday, Oct 2, 2010

Comparison of Solid Phase Epi (SPE) Non-Melt to Liquid Phase Epi (LPE) Melt Laser Annealing for 22nm Node n+ USJ Formation

J. Borland, J.O.B. Technologies
S. Shishiguchi & N. Matsuzaka, Renesas/Yamagata
M. Hane, Renesas/Albany
M. Tanjyo, Nissin
P. Oesterlini, Jenoptik Innovavent
J. Mayer, EAG

IEEE/RTP- 2010 Sept. 29, 2010

Sub-melt (DSA) & melt (Jenoptik) Anneals

As, As_4, P, P_4, Sb n-type junctions
BF_2, In halos

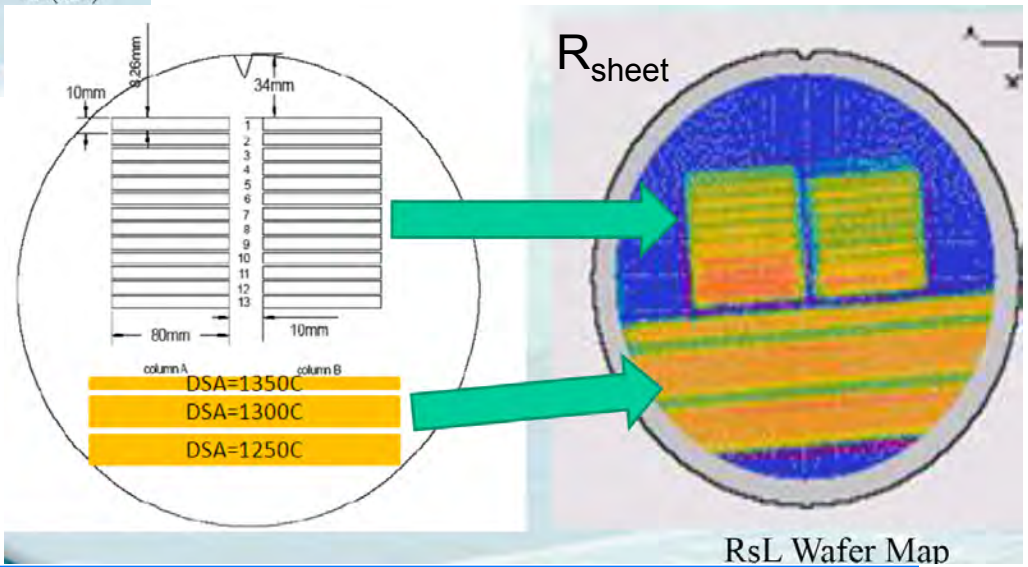
		HALO Implantation	
		BF2-HALO	In-HALO
23-300mm p-type wafers	No HALO	20keV/3E13	45keV/3E13
•Control (n-type wafer)		#1(S6)	#2(S7)
•As (1keV/1E15)	#3(S1)	#4(S2)	#5(S3)
•As (1keV/3E15)	#6(S4)		
•As4 (1keV/1E15)	#9(S5)		
•As4 (1keV/1E15) Cold/ Implant	#26(S12)		
•P (1keV/1E15)	#10(S8)	#11(S9)	#12(S10)
•P (1keV/3E15)	#13(S11)		
•P4 (1keV/1E15)	#14(S15)	#15(S13)	#16(S14)
•P (1keV/3E15)+C(3keV/3E15)	#17(S18)		
•P4 (1keV/1E15)+C16(3keV/3E15)	#19(S19)	#20(S20)	#21(S21)
•P4 (1keV/3E15)+C16(3keV/3E15)	#22(S22)	#23(S23)	#24(S24)
•Sb (4keV/1E15)	#25(S25)		

Nissin Claris Molecular Implanter: As4, As4-cold implant (-30C), P4, Sb and C/C16

Melt laser: 300 ns pulses,
Power increasing to center,
Left: slow scan, right: fast scan

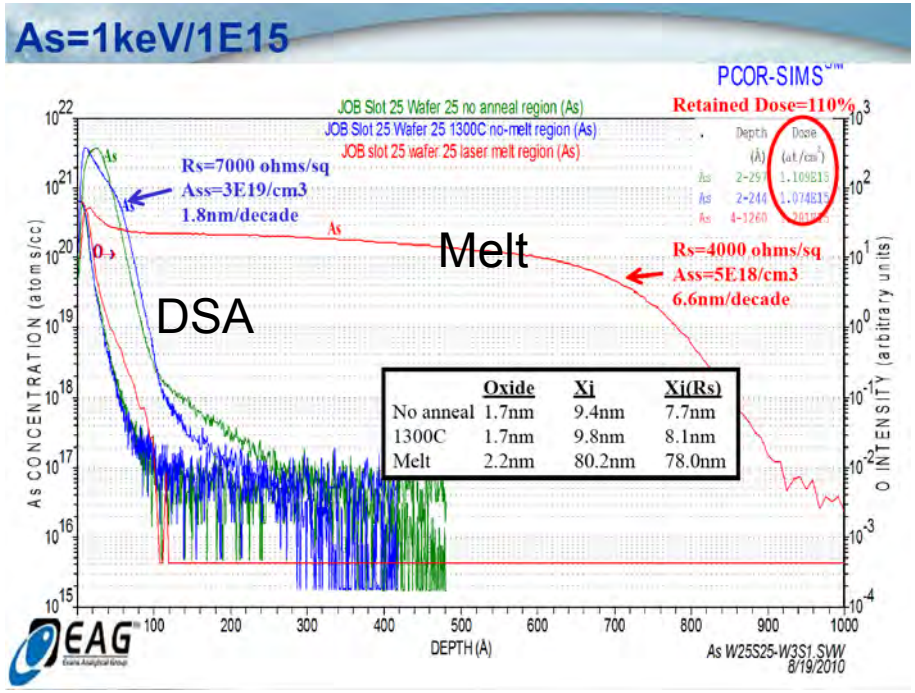
Sub-melt laser: visible laser scan
Thin hot (1350 C) strip near center

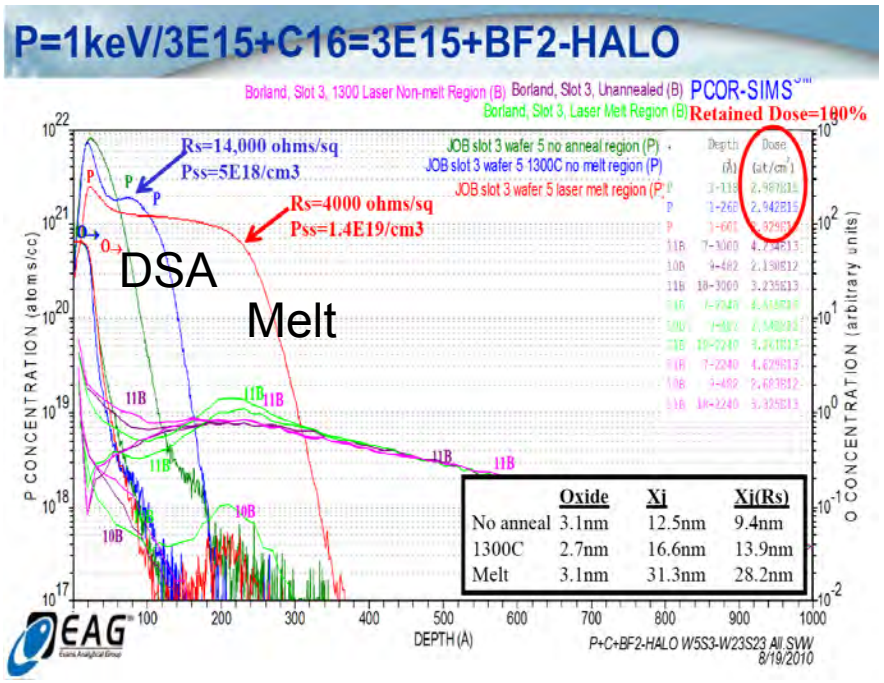
RsL mapping of R_{sheet}
and recombination leakage.



Dopant Diffusion: As & P

Melt laser powers drive dopants deeper than sub-melt.





Rs & Leakage Trends: 1 keV As

1 keV As, 3e15 As/cm²

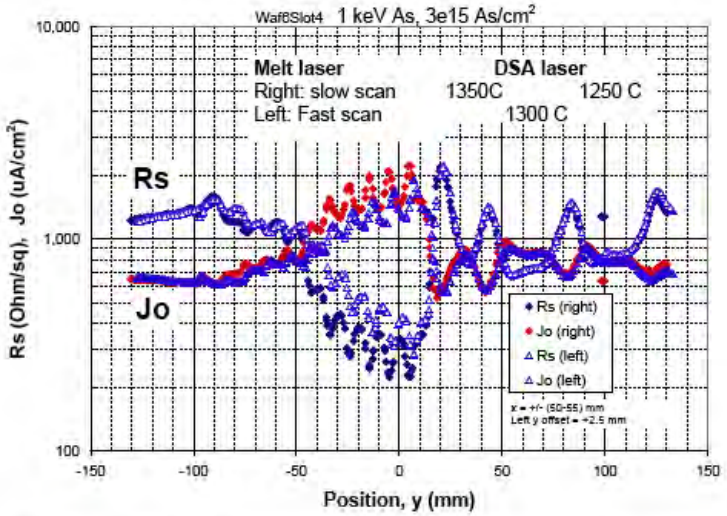
Lower Rs for slower scan (Melt laser right)

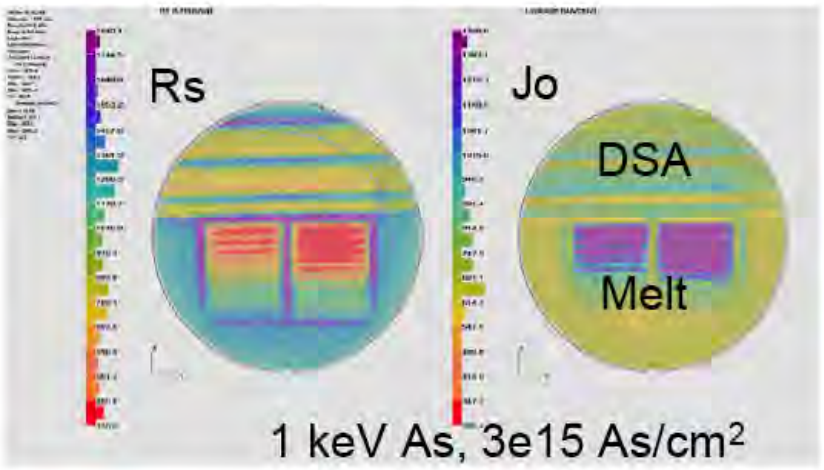
Jo increases for increased melt laser power.

Jo similar for Melt and SPE laser anneals.

Relatively low Jo for all anneals (no halo).

Jo for As x100 times higher than for 1 keV P or 4 keV Sb.





Rs & Leakage Trends: 1 keV Phos

1 keV P, 3e15 P/cm^2

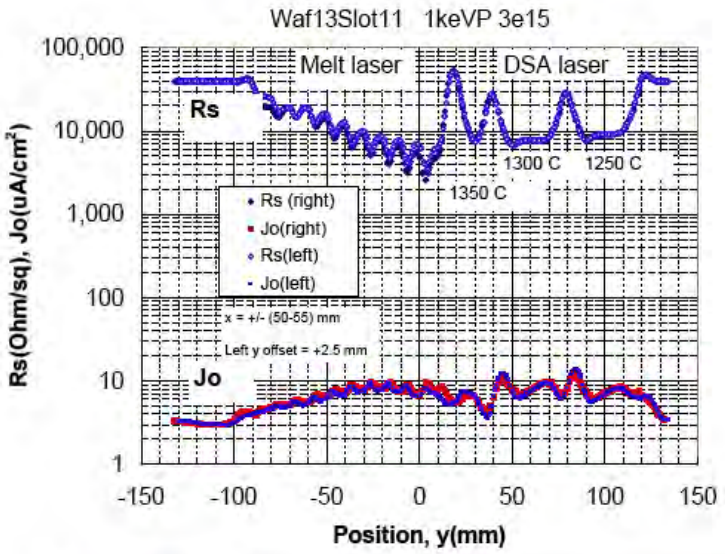
Lower Rs for slower scan (Melt laser right)

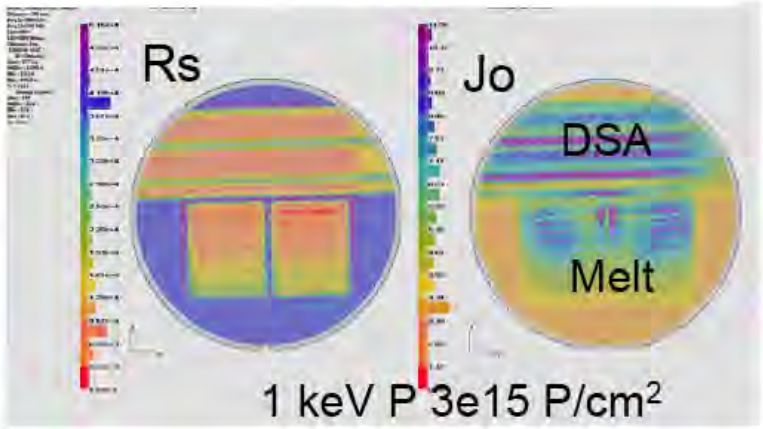
Jo increases for increased melt laser power.

Jo similar for Melt and SPE laser anneals.

Relatively low Jo for all anneals (no halo).

Phos has much higher Rs and lower Jo than 1 keV As.





Rs & Leakage Trends: 4 keV Sb

4 keV Sb, 1e15 Sb/cm²

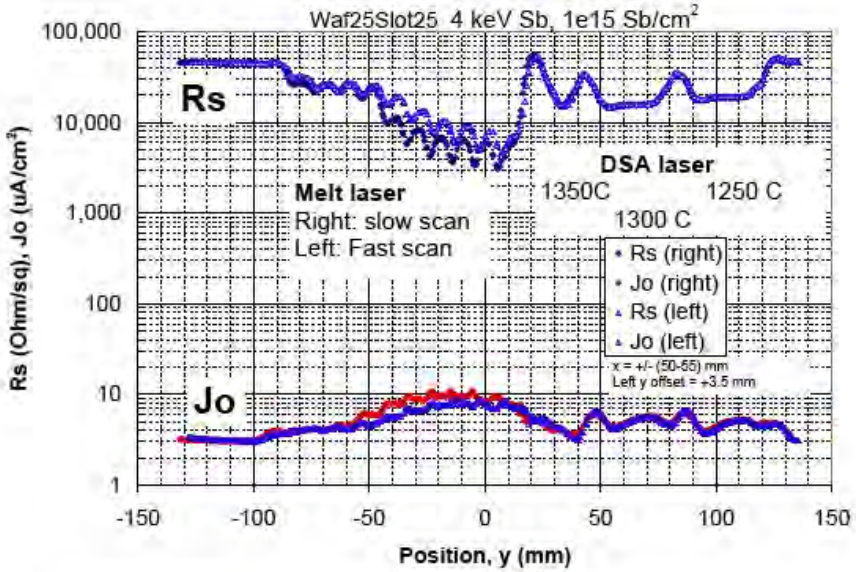
Lower Rs for slower scan (Melt laser right)

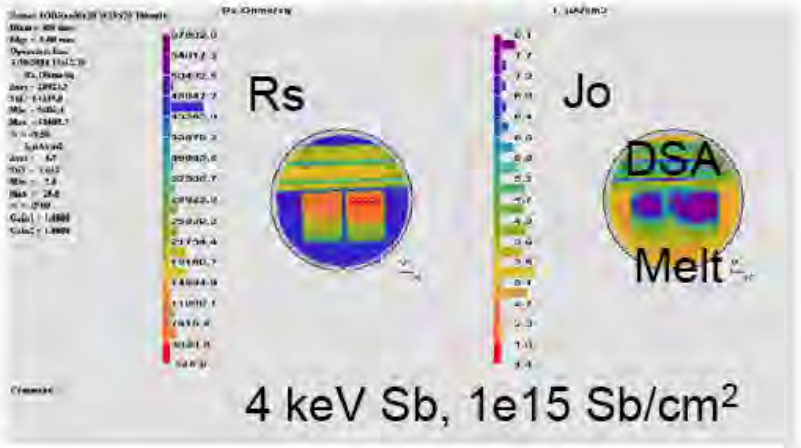
Jo increases for increased melt laser power.

Jo similar for Melt and SPE laser anneals.

Relatively low Jo for all anneals (no halo).

Sb has much higher Rs and lower Jo than 1 keV As. Similar to Phos.

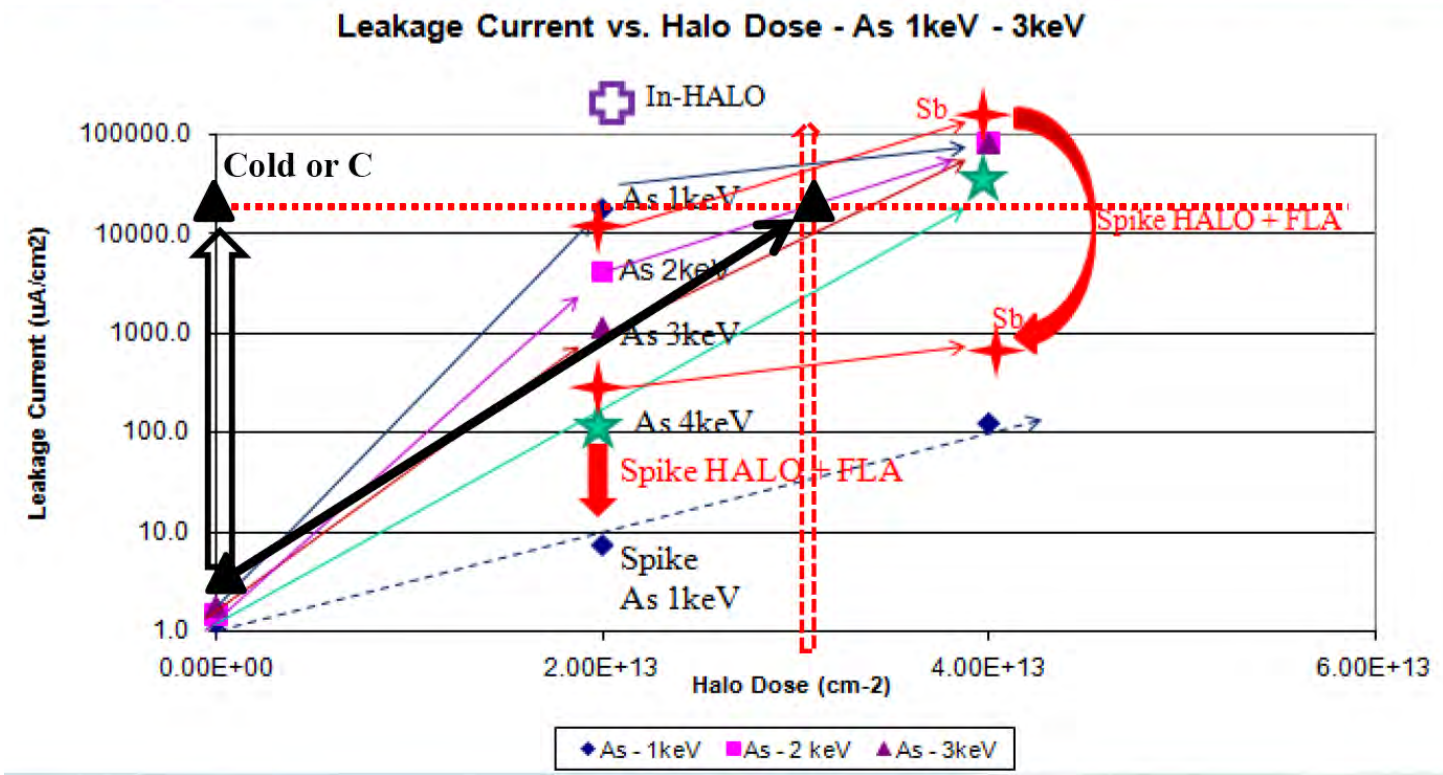




Leakage Currents: Halo Dose

Recombination & trap-assisted tunneling leakage:
Increase with (1) halo dose, (2) damage near Xj, (3) high C dose.
Cryo implants are not guaranteed to be low-leakage!!!

As, P & Sb Effects & With BF2/In HALOs



Ultratech

Characterization of Dopant Activation, Mobility and Diffusion in Advanced Millisecond Laser Spike Annealing

Shaoyin Chen[1], Xiaoru Wang[1], Michael Thompson[2], Yun Wang[1], Cam Lu[1], Jim McWhirter[1]

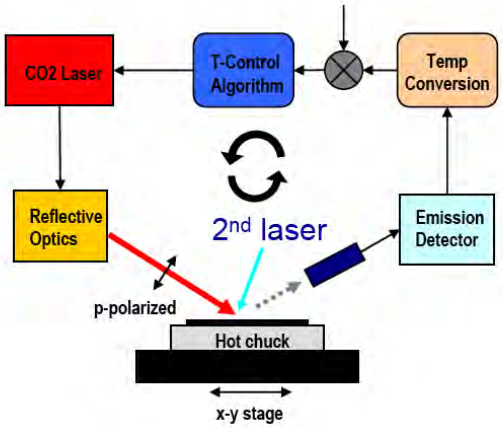
[1] Ultratech Inc., 3050 Zanker Rd., San Jose, CA 95134 USA
[2] Cornell University, Ithaca, NY, USA

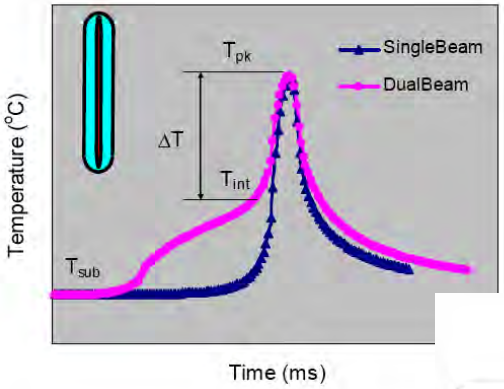
Sep 29, 2010

Dual laser heating: IR & “Pre-Heating”

Broad pre-heat laser extends the available dwell times to >10 ms.

Advanced Dual-Beam LSA System



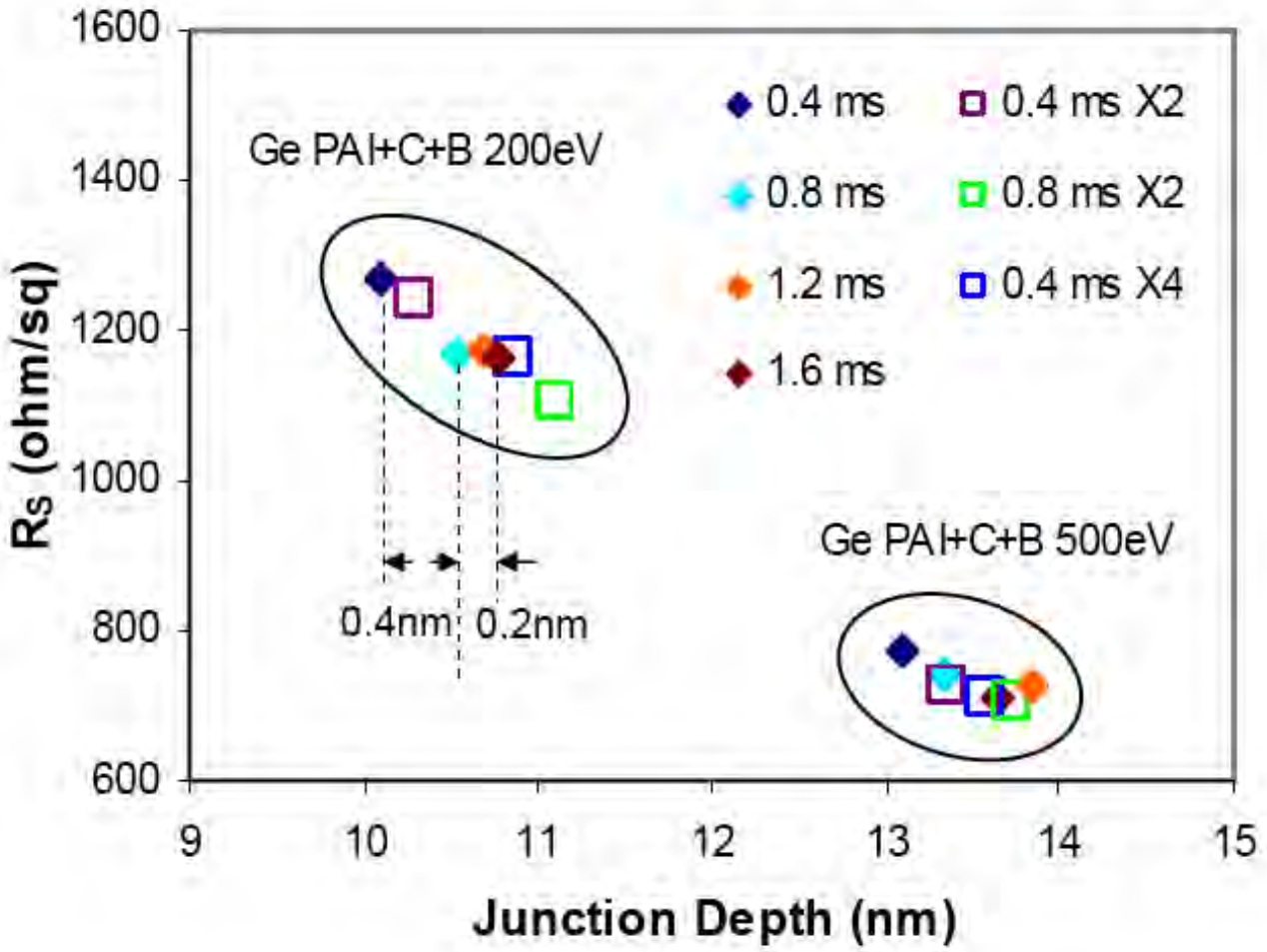


- A 2nd laser is introduced to the conventional SB-LSA system as a pre-heat laser

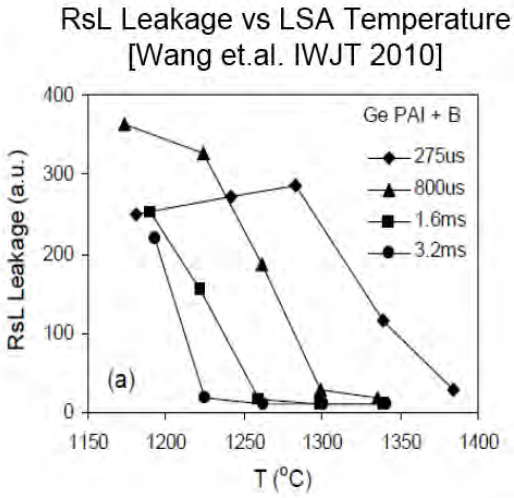
DB-LSA Applications

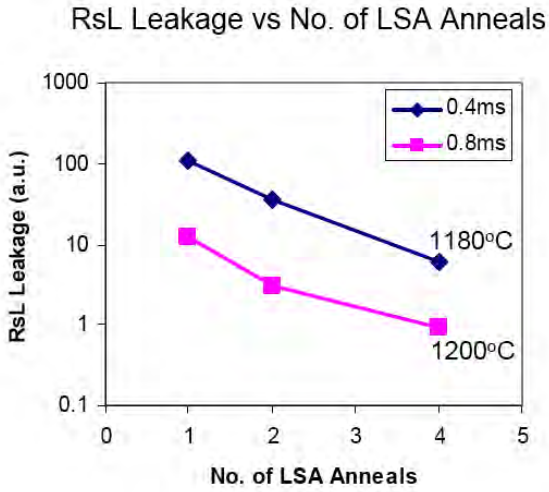
	Low T (Silicide Formation)	Stress Reduction (Junction Formation)	Long Dwell (Defect Annealing)
T_{sub}	< 250°C	~400°C	~400°C
T_{int}	Minimal	Low-Mid	High
Thermal budget	Negligible	Small	Large
T_{pk}	500-900°C	1100-1350°C	1100-1350°C

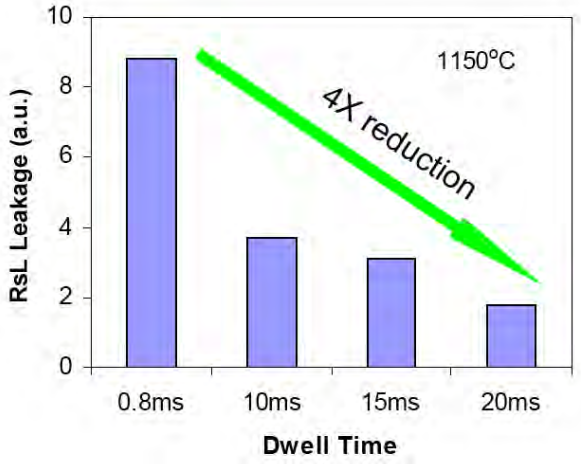
Laser Dwell Time: Rs and Xj “Tuning”



Longer Laser Dwell Reduces Leakage

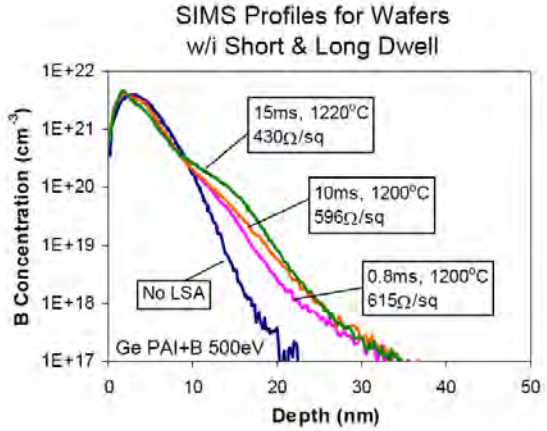






But: Longer dwell times leads to:

1. Deeper junctions
2. Wafer stress, slip & alignment errors (Hebb: RTP09)



ΔXj ~ 4nm for 0.8ms
ΔXj ~ 6nm for long dwell

IEEE RTP2010

Influence of the process sequence and thermal budget on the strain of Si:C stressor layers formed by Ion Implantation

Erik Rosseel[a,1], Claude Ortolland[a], Andriy Hikavyy[a], Tom Schram[a], Annelies Falepin[b], Thomas Hoffmann[a], Bastien Douhard[a], Alain Moussa[a], Wilfried Vandervorst[a,c], Mike Ameen[d], Leonard Rubin[d]

[a]*IMEC, Kapeldreef 75, B-3001 Leuven, Belgium*
[b]*NXP semiconductors, Kapeldreef 75, B-3001 Leuven, Belgium*
[c]*Instituut voor Kern- en Stralingsfysika, KU Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium*
[d]*Axcelis Technologies, Inc., 108 Cherry Hill Drive, Beverly, MA01915, USA*

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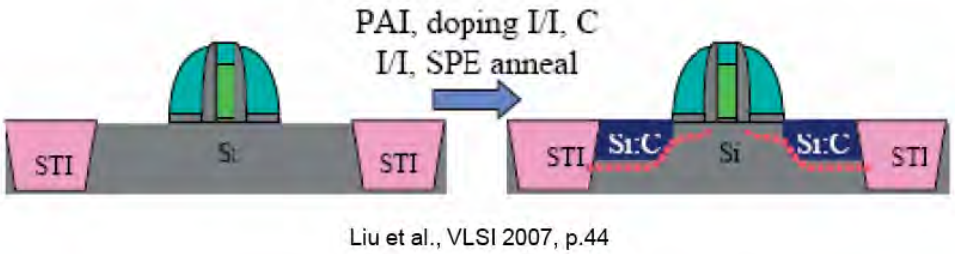
Si:C SD Regions for Tensile nMOS

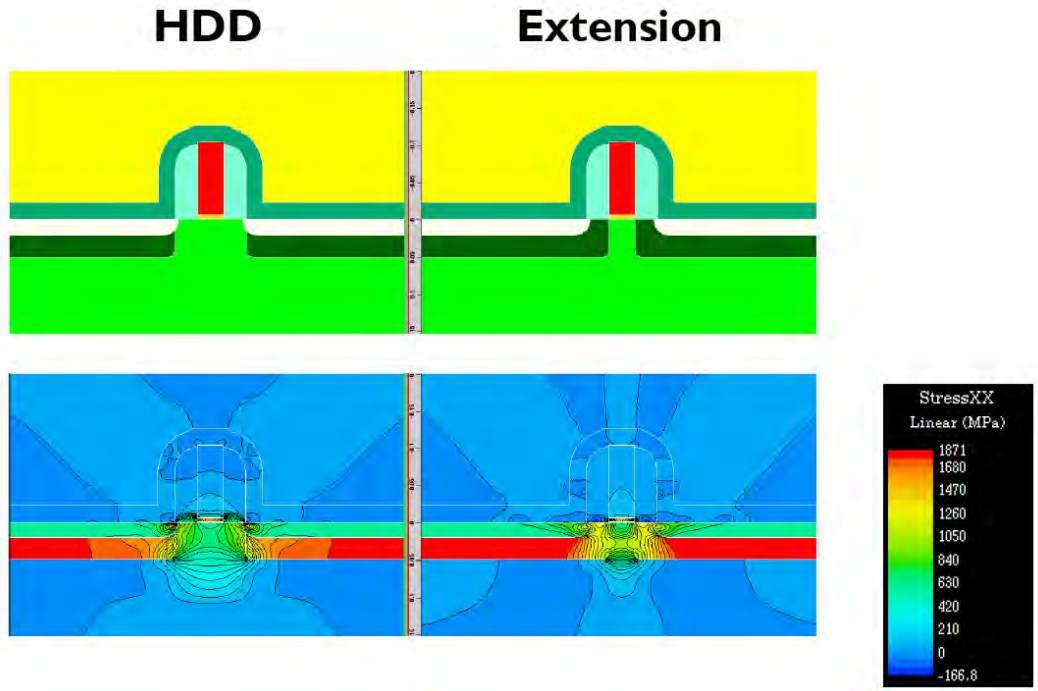
Si:C SD regions give tensile strain in nMOS channels.

Many choices:

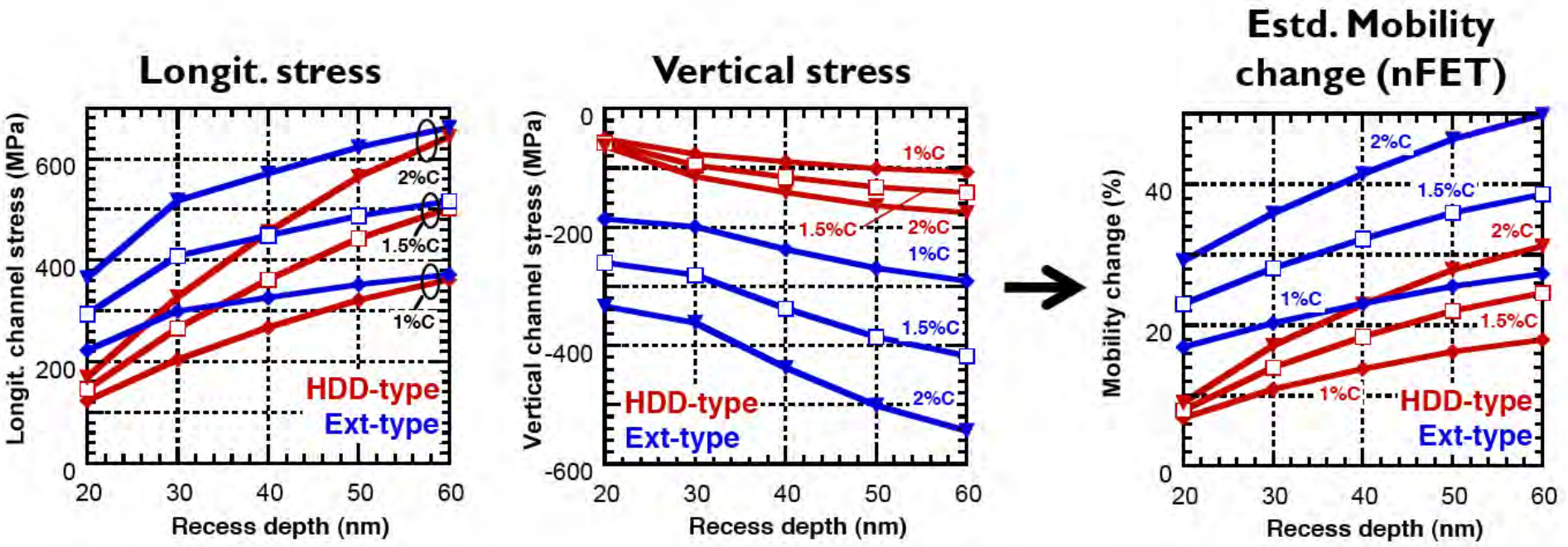
1. C dose & depth (target=2% substitutional C)
2. Si:C lateral position
3. C ion form (C1, C7, ??)
4. Anneal (ms-anneal preferred)
5. Need also to have high n-type dopant (Phos) activation.
6. Can use C to slow P diffusion.



Liu et al., VLSI 2007, p.44



CHANNEL STRESS, LG=35NM



- Ext-type much leads to much higher mobility than HDD-type Si:C S/D, mainly because of higher vertical stress.
- Higher C% leads to significant mobility increase.
- Deeper Si:C S/D leads to higher mobility. Expected to saturate beyond 60nm recess depth.

C Strain Implants for nMOS

EXPERIMENTAL DETAILS

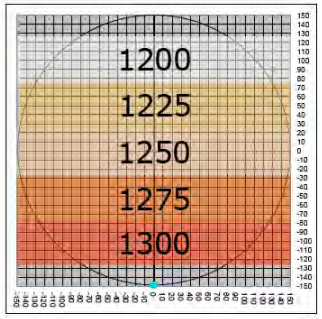
300 mm p-type (001) monitor wafers

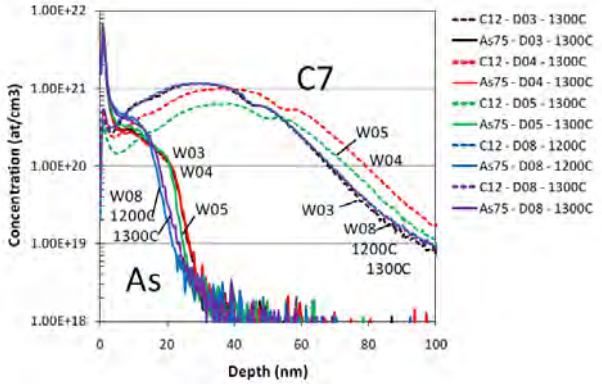
Implants/anneals given at IMEC following implementation of Si:C at EXT/HDD level

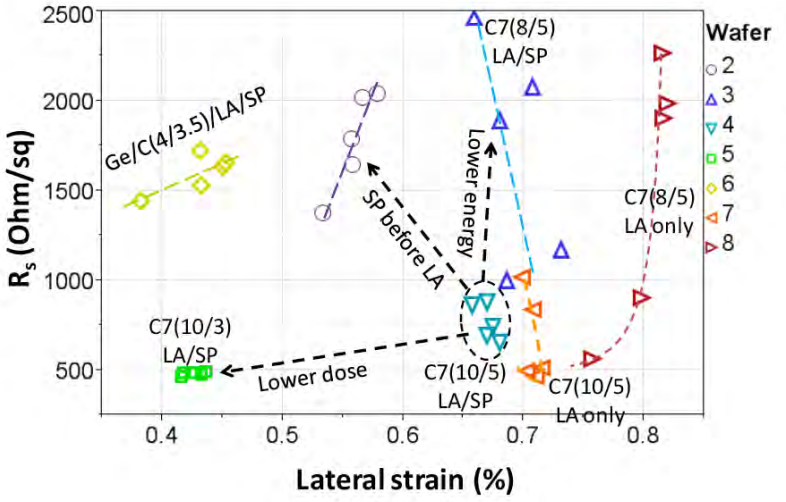
C_7H_7 (91 AMU) implants done at Axcelis with Optima HD Imax high current implanter

Annealing done at IMEC using laser anneal (DSA) or Spike anneal (Levitor)

Characterization of Rs with M4PP (Capres) and strain with HR-XRD (Bede) and SIMS (Atomica).





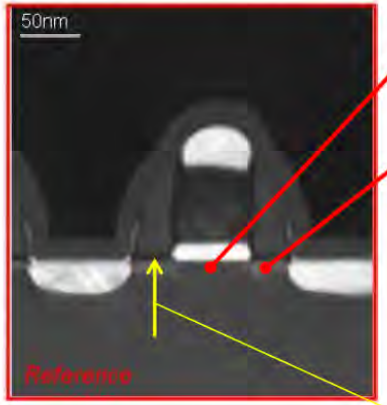


* SDE strain more effective than HDD.
* C_7 better for strain than Ge/C_1.
* Spike anneals are not good for strain.

Best trade-off for C7 (10keV, 5e15) and large Tp

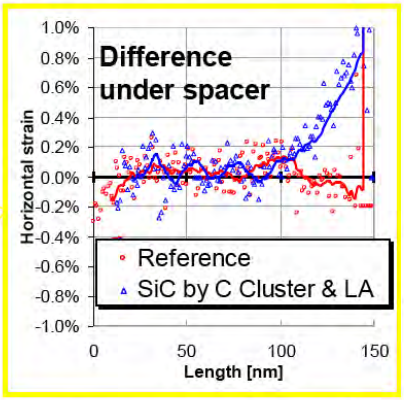
TEM: Nano-Beam Diffraction

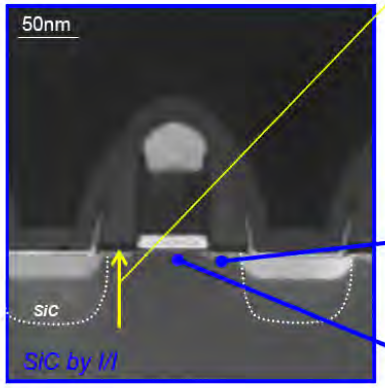
STRAIN MEASUREMENT BY NBD*



Horizontal:~+0.6%
Vertical:~-0.4%

Horizontal:~0.0%
Vertical:~0.0%





Horizontal:~+0.4%
Vertical:~-0.2%

Horizontal:~+0.6%
Vertical:~-0.4%

Under gate (1):
No difference between Reference and Si:C

Under spacer (2):
Tensile strain in plane & compressive strain out plane is observable for Si:C

* thanks to
Paola Favia, Hugo Bender

imec

Cluster Carbon Implantation for NMOS Fabrication Improvements

M.Tanjyo, H.Onoda, T.Nagayama, N.Hamamoto, S.Umisedo, Y.Koga, H.Une, N.Maehara, Y.Kawamura, Y.Hashino, Y.Nakashima, T.Igo, M.Hashimoto, N.Tokoro, N. Nagai

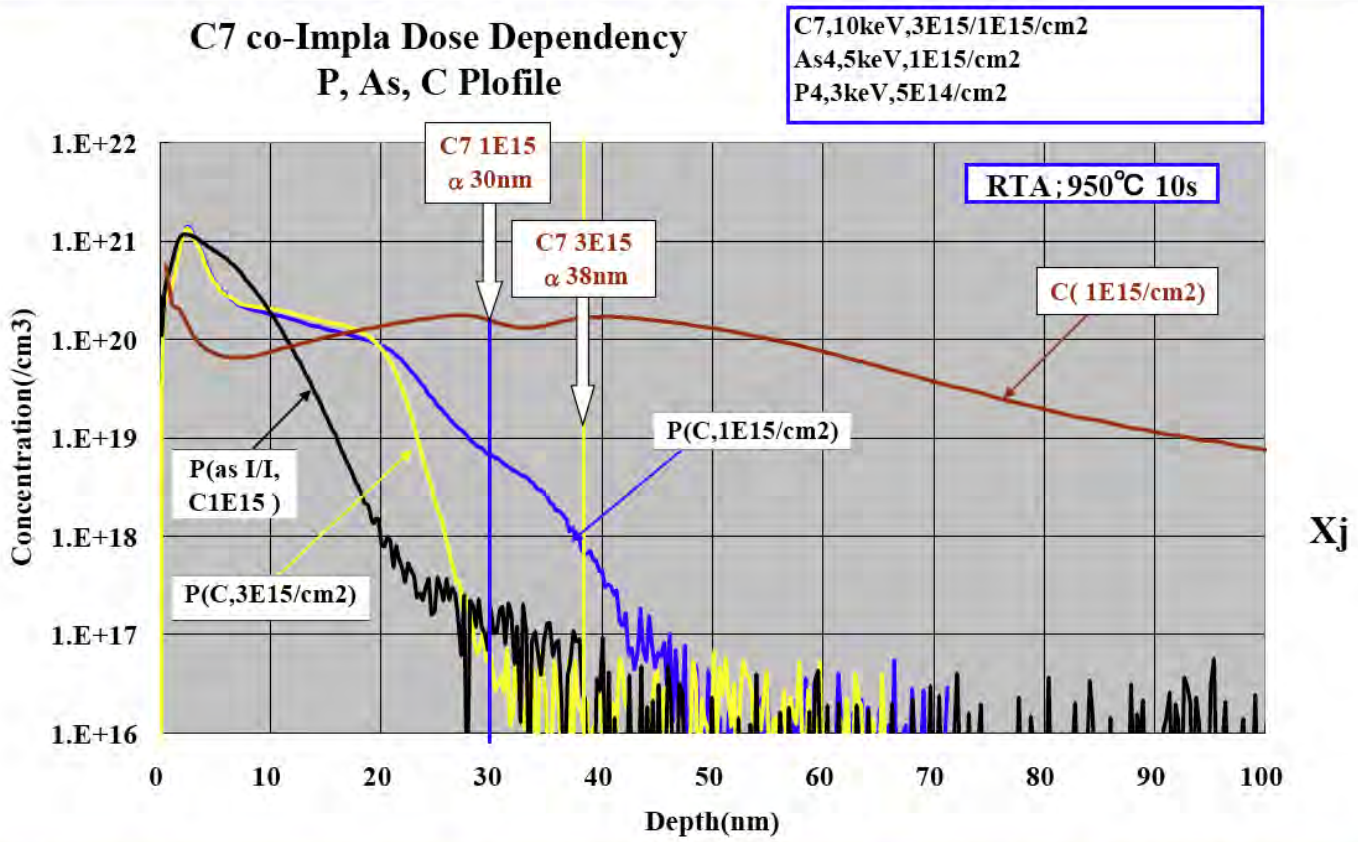
Nissin Ion Equipment Co., Ltd, 575 Kuze-Tonoshiro-cho, Minami-ku, Kyoto, 601-8205 Japan,

Tanjo_Masayasu@nissin.co.jp

P_4 & C_7 Profiles

C7 Dose Dependency, co-Implant SIMS

NISSIN ION EQUIPMENT CO.,LTD.
Cluster CLARIS

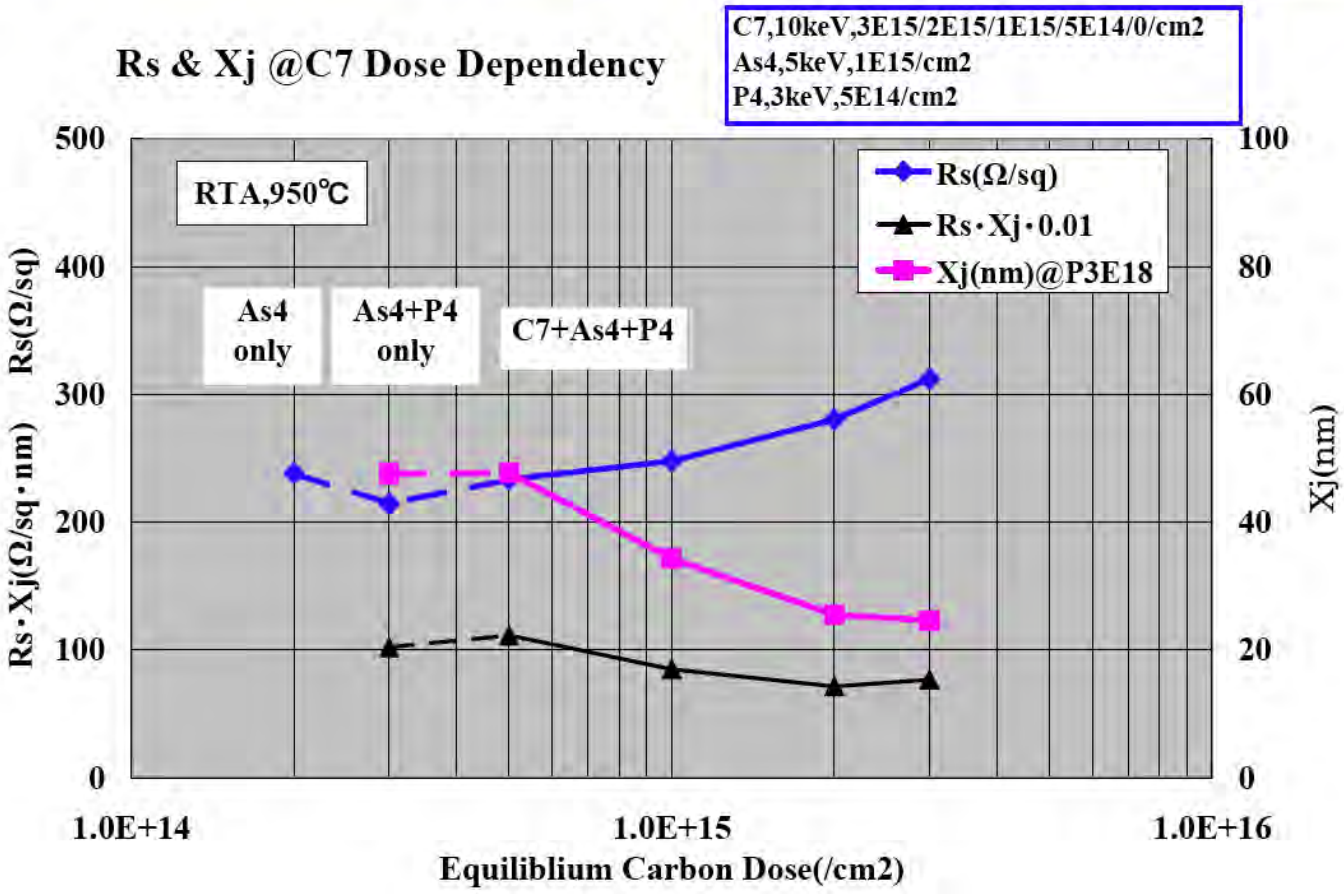


To make a boxlike profile, carbon α layer should cover the P EORD area.

C Dose Effect on Rs, Xj

C7 Dose Dependency, Rs & Xj

NISSIN ION EQUIPMENT CO.,LTD.
Cluster CLARIS



EXCICO

FULL DEVICE EXPOSURE LASER THERMAL ANNEALING: HIGH PERFORMANCE AND HIGH YIELD JUNCTION FORMATION PROCESS

K. Huet, C. Boniface, R. Negru, P. Aing, J. Venturini

EXCICO

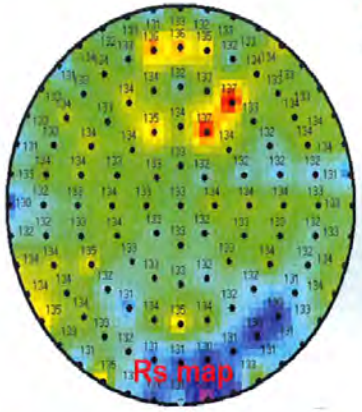
13-21 Quai des Grésillons Gennevilliers 92230 France

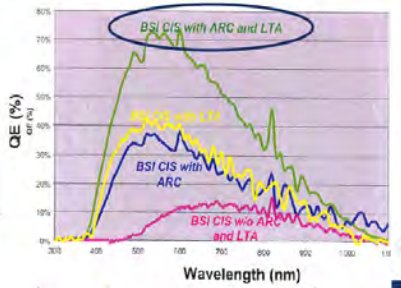
www.excico.com

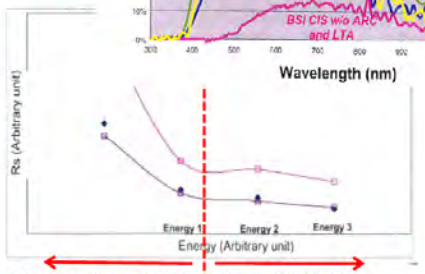
Backside Melt Junctions

EXCICO

Use case: Backside illuminated CMOS Imaging Sensors







1.5% Rs uniformity

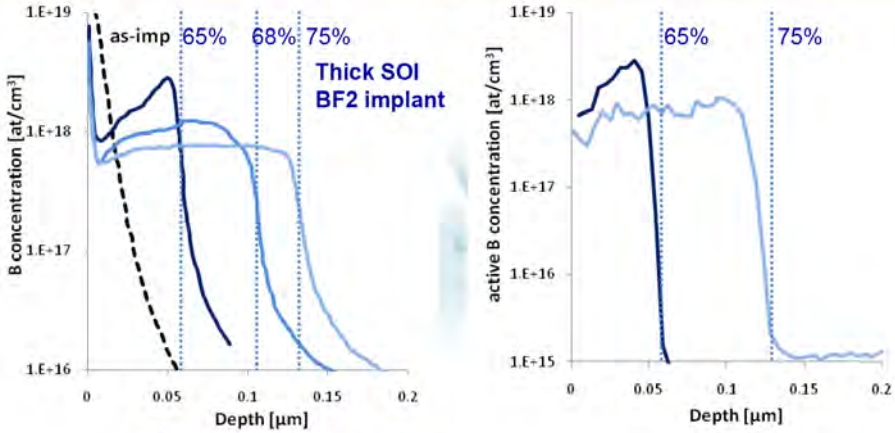
Non Melt regime:
X High variability

Melt regime:
✓ Reduced variability
⇒ Large process window

IISW conference (Bergen, Norway, June 09)

EXCICO

Junction dopant profiles



⇒ Activation rate ~85%
⇒ Shallow junction
⇒ Box shaped for melt deeper than implant tail

Full die exposure with step-and –repeat good for Rs uniformity.

Excico Melt Laser Tool

EXCICO

Laser Thermal Annealing Tool

LTA Laser Thermal Annealing 15-05

Ultra low thermal budget annealing tool

- ✓ **Time at temperature ~100ns**
- ✓ **3D integrated junction process on any substrate**
- ✓ **Process stability below 1.5%**
- ✓ **Variable field size**

Activation of Silicon Wafer by Excimer Laser

Rainer Paetzel[1], Jan Brune[1], Frank Simon[1], Ludolf Herbst[1]
Masashi Machida[2], Junichi Shida[2]

1) Coherent GmbH 2) The Japan Steel Works Ltd.

JSW - ELA system for semiconductor annealing

- Wafer size: 200mm (300mm)
- Laser irradiation ambient: Nitrogen / Air
- Cassette to cassette wafer transfer module
- Full automatic handling with SMIF Pod , Foup , open cassette or manual loading
- Monitor & logging functions
- Irradiation laser power auto calibration
- Process & operation log function
- SECS (Semiconductor Equipment Communication Standard)
- Conformity for SEMI standard
- 200mm wafer throughput up to >120 wph possible

LineBeam Series 3 – Standard ?

- LB250 – i.e. 250 mm x 400 µm and >>650 mJ/cm²
  (other lenghts available)
- Standard was LB370 – with 375 mm x 400 µm and > 450 mJ/cm²
- State of the art: LB465 - i.e. 465 mm x 350 µm
- In qualification: LB750 – i.e. 750 mm x 350 µm

Standard LB375

- Table 1: Main optical specifications of the Line Beam System

Specification	Value
Line Length, LA	200 mm, Top Hat
LA Uniformity	< 2.5%, 2 sigma
Line Width, SA	140-160 µm @96% int.
Slope width SA (10% to 90% intensity)	< 80 µm
Energy Density, ED	1.5 J/cm²
Pulse Length	30 ns (FWHM)

COHERENT.

RTP10: Gainesville, Florida

Si Prussin/UCLA Masayasu Tanjyo/Nissin

Will the RTP series be re-born as part of IIT12 ? Stay tuned.