Advanced Anneal Solutions for Silicides

Shankar Muthukrishnan

RTP Anneals GPM

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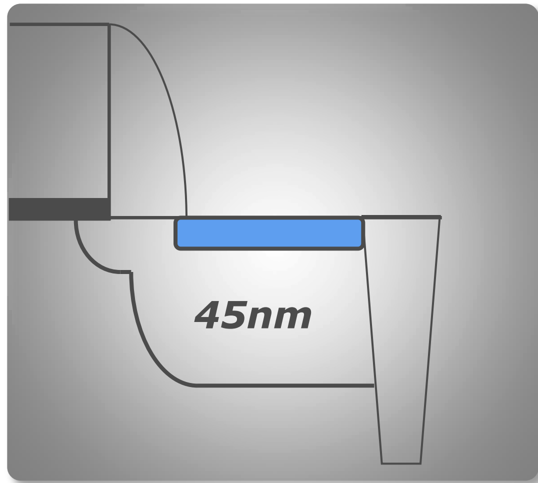
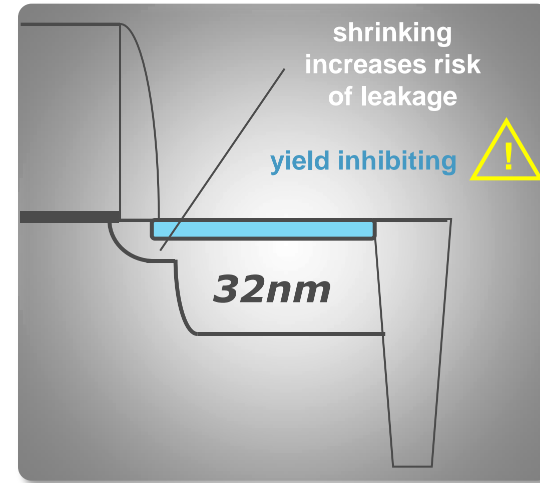
Challenges Scaling Nickel Silicide Contacts





- Diffusion control for thinner layer formation
- Silicide-Silicon interface morphology
- Avoiding yield limiting piping defects, especially with proximity to SDE, channel
- Sensitivity to agglomeration

Improved silicide contact is key to scaling

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Integration Alternatives to Suppress NiSi Piping

- Pre amorphous implant (PAI)
- Pre clean using “flourine” dry etching
- Co implant dopant in substrate (F, C)
- Nickel alloy (Pt)
- **Modifying anneals**

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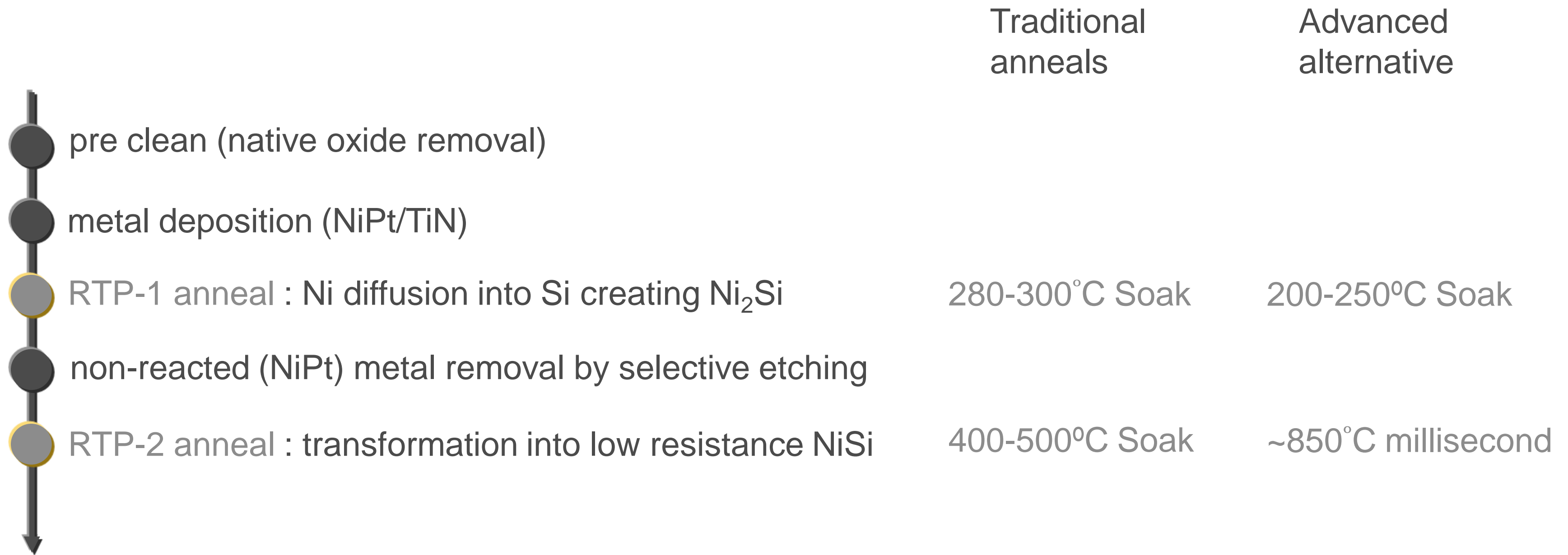
Nickel-Silicide Process Steps

NiPt Salicide Flow:



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Soak to Millisecond Transition for Silicides

	Logic (65nm)	Logic (45nm)	Logic (32nm)
Ni Silicidation / Diffusion	Soak	Low temp Soak	Low temp Soak
NiSi Phase Transformation	Soak	Soak or Millisecond	Millisecond

- **Driven by**
  - Enabling thinner silicides without comprising conductivity or yield
- **Millisecond Provides**
  - Improved Yield performance
  - Improved Junction Leakage performance
  - Fewer leakage-inducing defects through steep temperature profile

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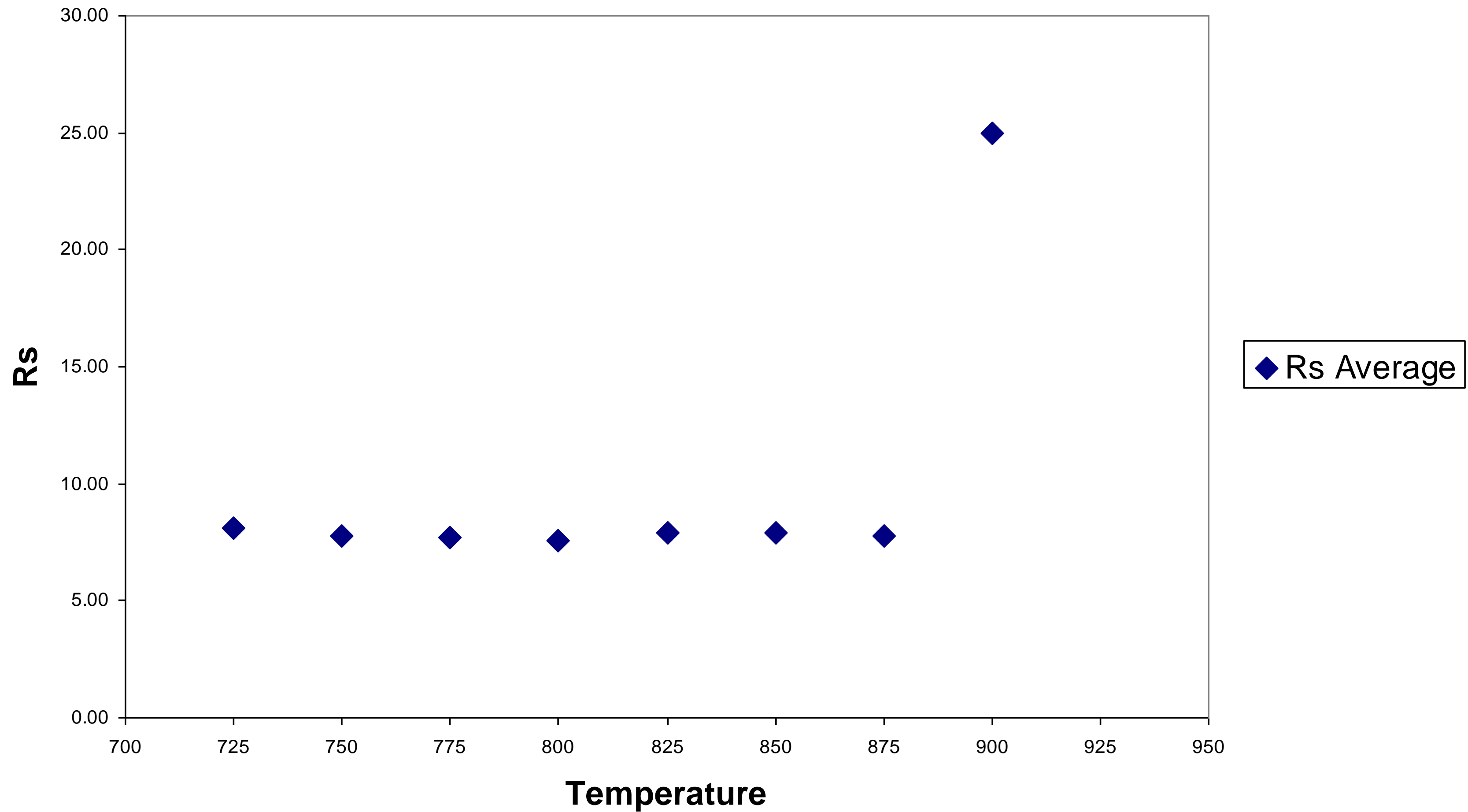
Nickel Silicidation Transformation Curve



Large process window available for RTA 2

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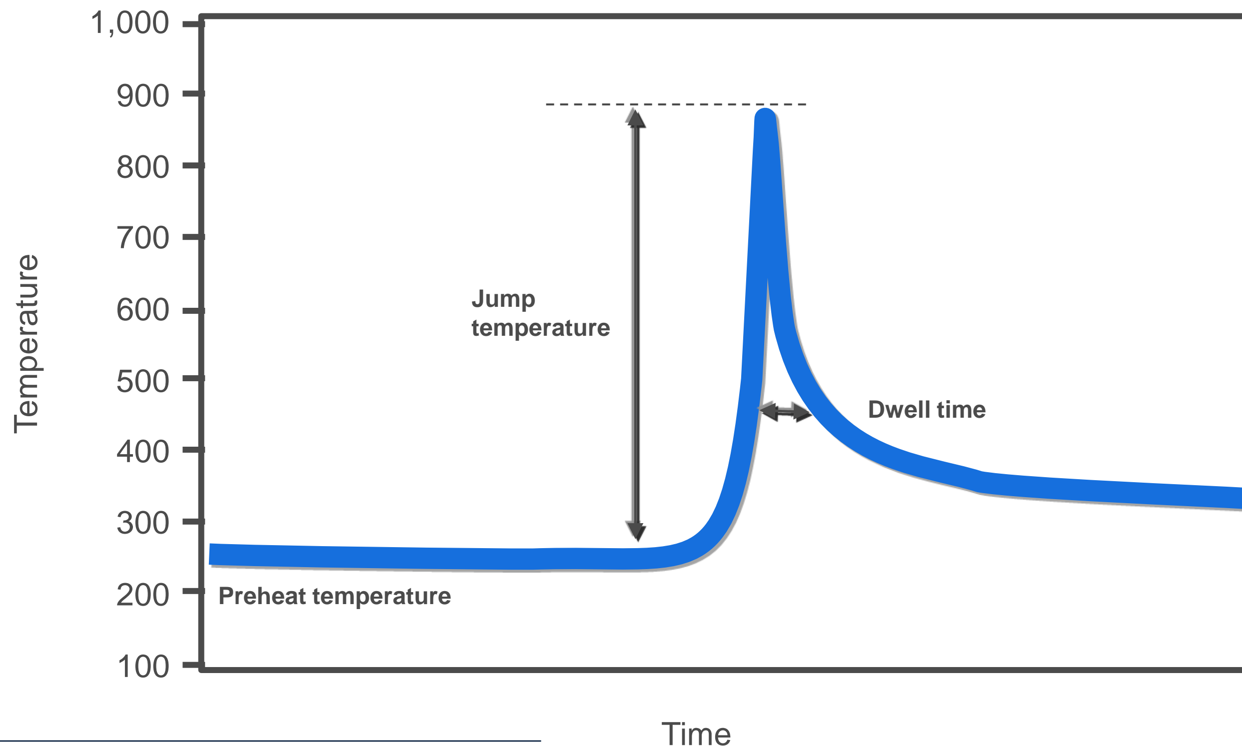
The Ideal Time-Temperature Profile for NiSi

Key parameters to consider

Preheat : Must be low enough to avoid uncontrolled diffusion

Jump temp : Must be high enough to enable optimal activation w/o wafer breakage or agglomeration

Dwell time : Must be short to avoid wafer bow and breakage



Above profile is key to enabling optimal nickel silicide

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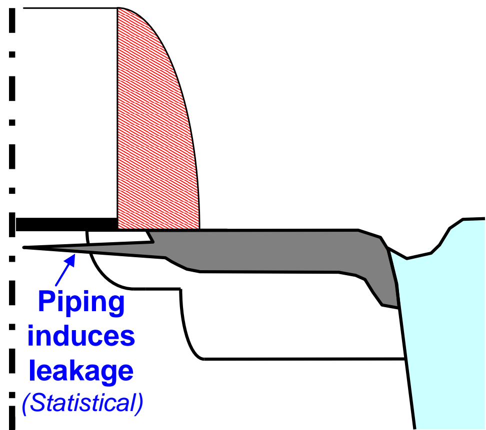
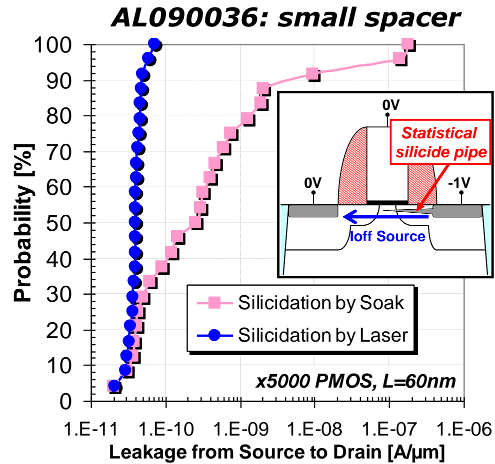
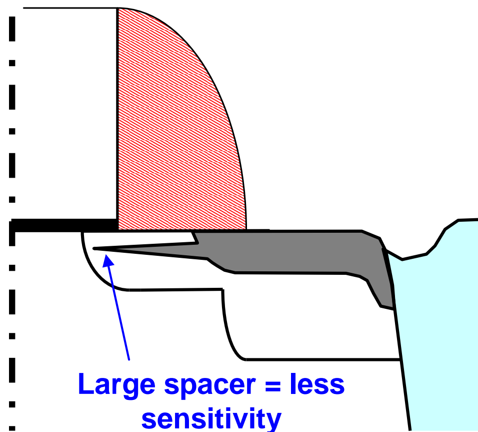
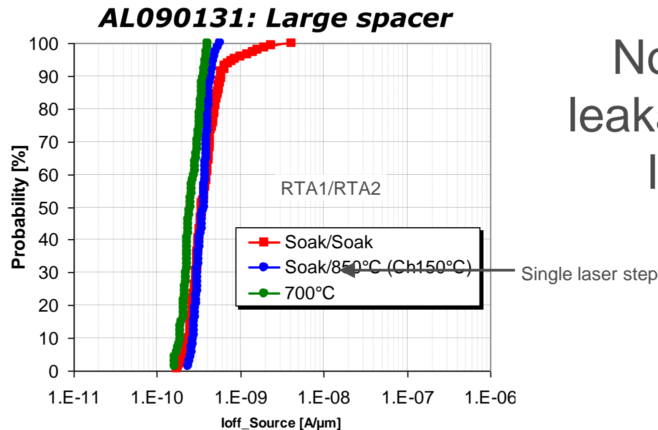
Yield Results and Scaling Impact for NiSi Process





Scaling spacer affects RTA2 leakage, but not DSA2





No difference in leakage when using large spacer

Data source : IMEC IEDM 2009

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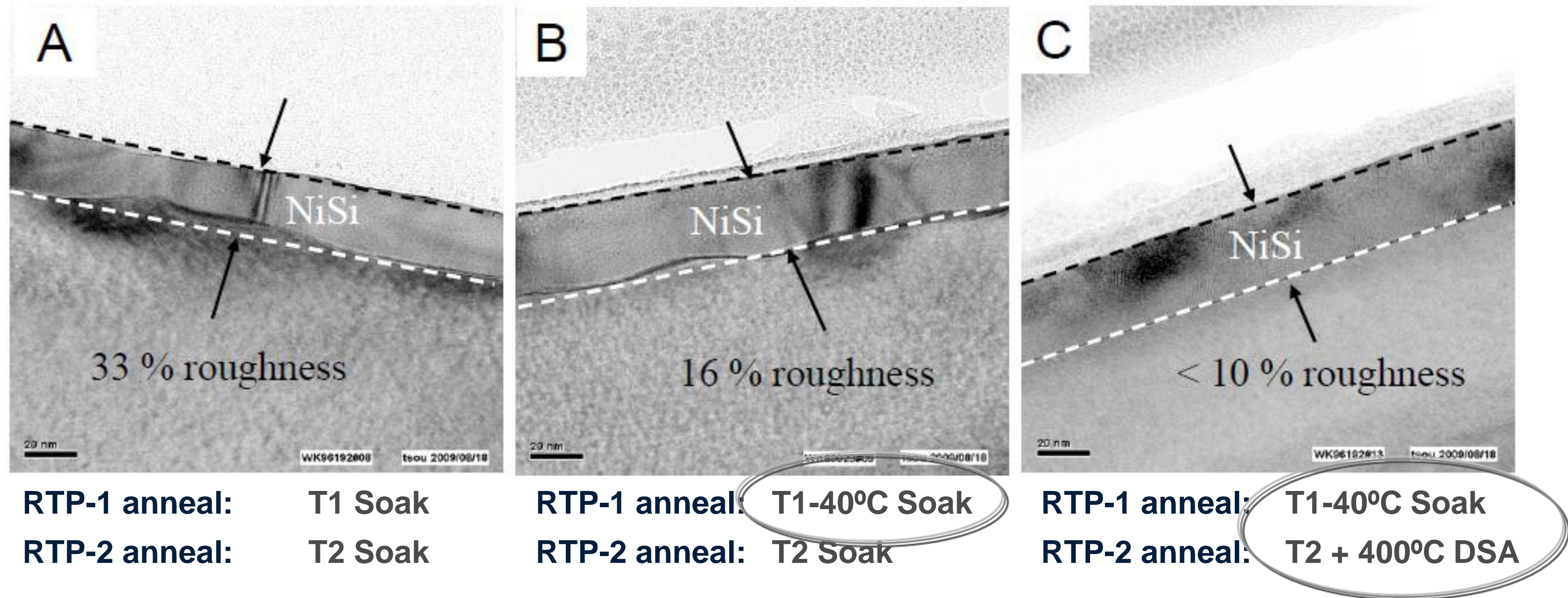
Results: NiSi Morphology Improvement



Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*, Dr. Chen et al. Co-published by UMC / Applied Materials

Process B (lower RTP-1 Soak) roughness reduced vs process A (baseline)
Process C (lower RTP-1 Soak + DSA RTP-2) achieves lowest roughness

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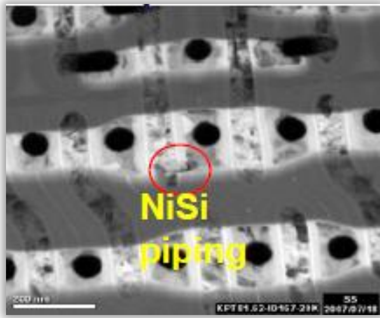
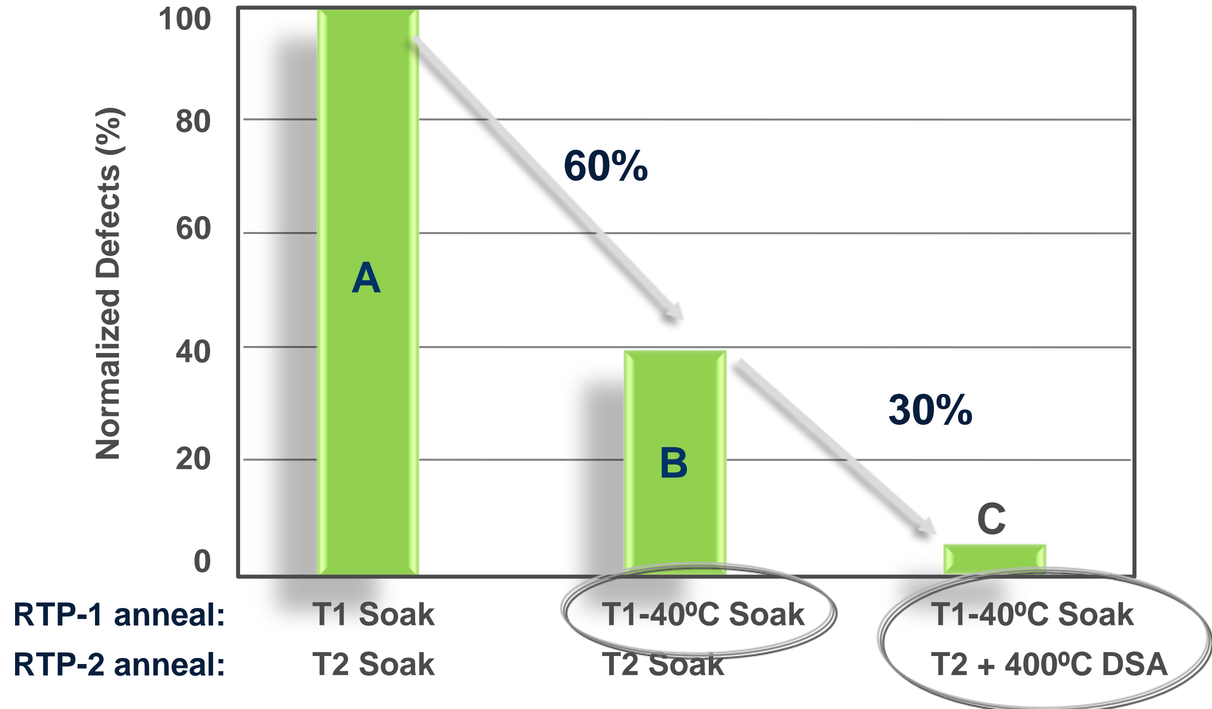
Results: NiSi Piping Defects Reduction





Based on e-beam Bright Voltage Contrast (BVC) measurement count on a pattern wafer, post CMP

Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*,
Dr. Chen et al. Co-published by UMC / Applied Materials

Process B (lower RTP-1 Soak) achieves lower defect count than baseline
Process C (lower RTP-1 Soak + RTP-2 DSA) achieves lowest piping defect count

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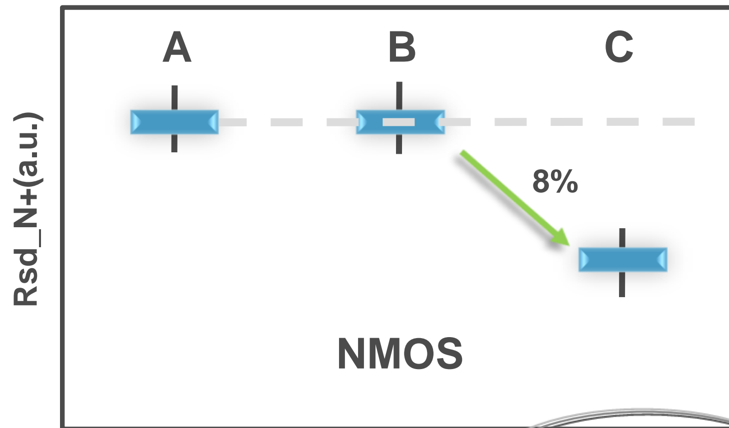
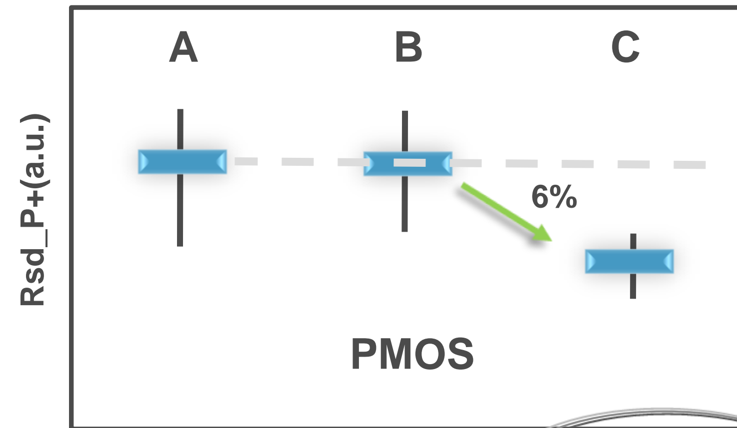
Results: Electrical Performance – $R_{S/D}$





	NMOS A	NMOS B	NMOS C	PMOS A	PMOS B	PMOS C
RTP-1 anneal:	T1 Soak	T1-40ºC Soak	T1-40ºC Soak	T1 Soak	T1-40ºC Soak	T1-40ºC Soak
RTP-2 anneal:	T2 Soak	T2 Soak	T2 + 400ºC DSA	T2 Soak	T2 Soak	T2 + 400ºC DSA

Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*,
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The series S/D Rs (Rsd) decreased using DSA

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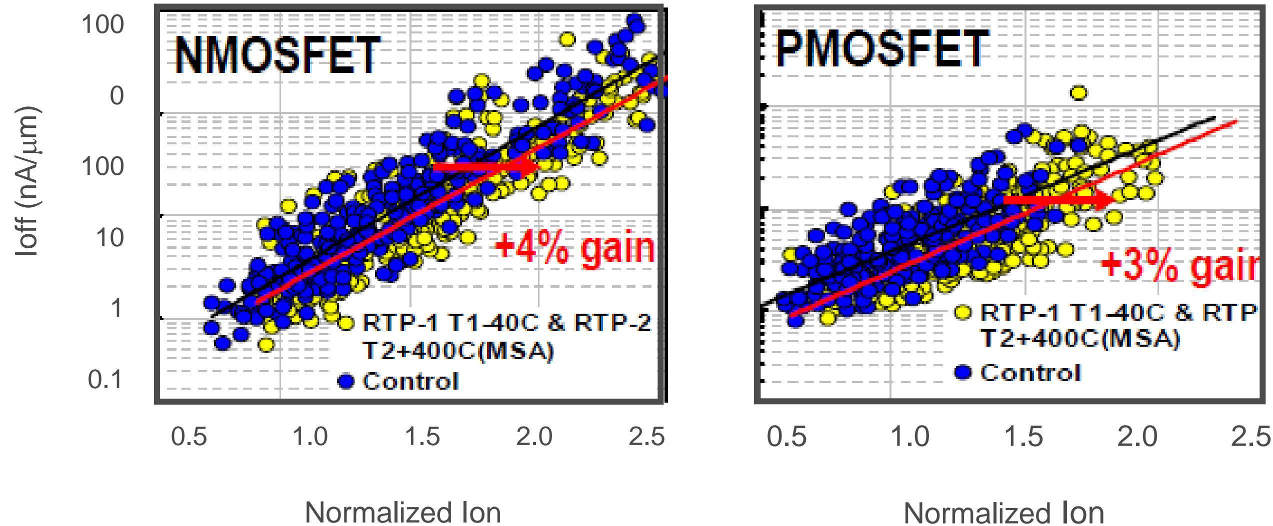
Results: Electrical Performance – I_{on}/I_{off}

RTP-1: Soak @ T1-40ºC
RTP-2: Millisecond (T2+400ºC)



NMOS gain = 4%	PMOS gain = 3%

Source: IEEE - RTP2009 Conference, *Advances on 32nm NiPt Salicide Process*, Dr. Chen et al. Co-published by UMC / Applied Materials

Drive current gain achieved by enhancing nickel silicide contact using millisecond annealing with low temperature RTP-1 Soak

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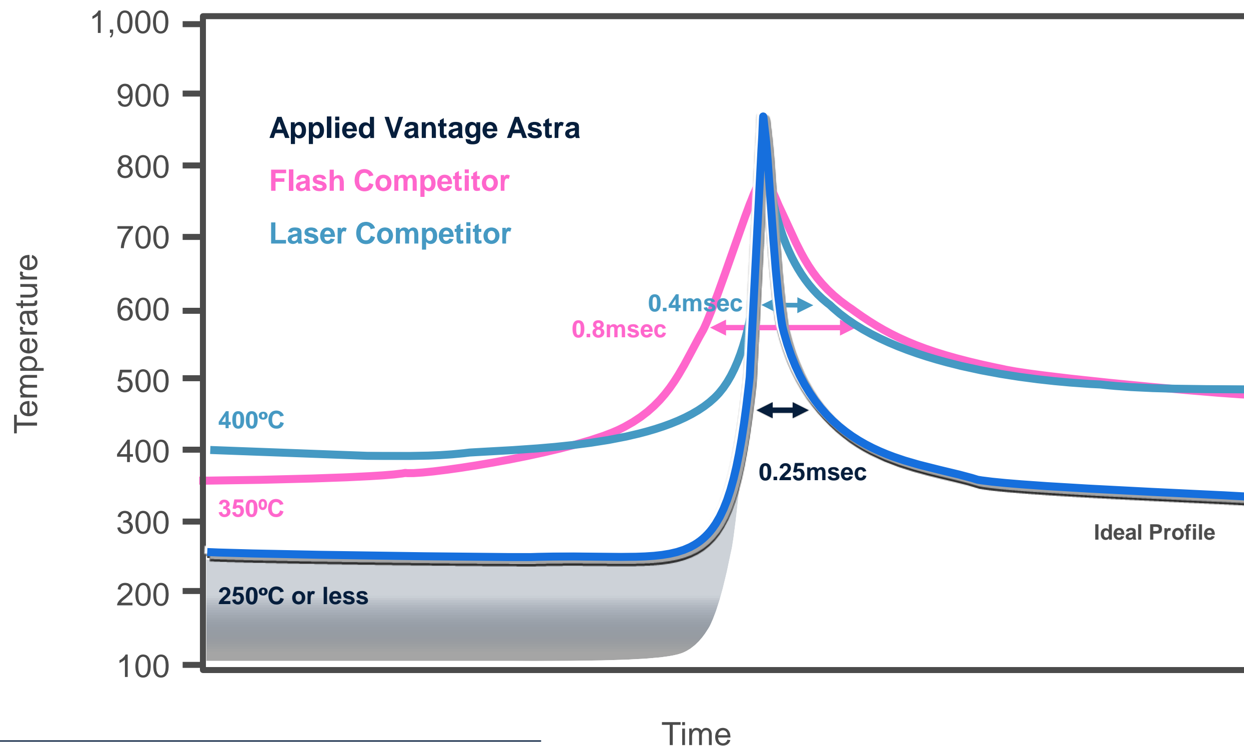

Delivered by Applied Materials' Vantage Astra system

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Applied Vantage® Astra™ DSA System

- **Uniquely powerful silicidation**
  - Up to 5% greater device speed
  - Higher yields enabled by up to 15x lower leakage
  - Less wafer stress
- **Versatile dynamic millisecond anneal**
  - Broad range of processing conditions
  - Ambient control
  - Extendible to high-k/metal gate applications
- **Compact, reliable, cost-effective**
  - Simple, compact and smart chamber design
  - Solid-state laser with prolonged lifetime
  - > 40 WPH per two- chamber system
  - Compatible with an RTP chamber on same system as hybrid

FAST. SMART. RELIABLE.
Simply Better Anneal

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Vantage Astra DSA System Photos

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into industries.™