22nm & 15nm Node Junction Scaling Options

John Borland

J.O.B. Technologies, Aiea, HI

July 15, 2010

Outline

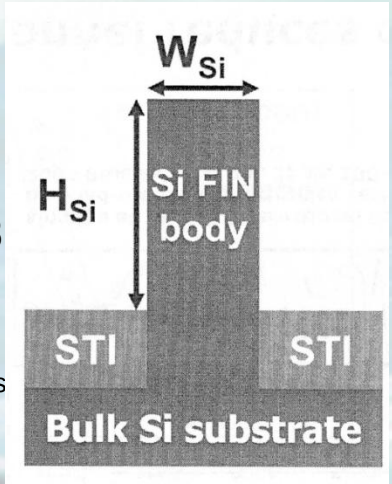
- **Introduction**
  - **Technology Roadmap Options**
- USJ Technology:
  - p+ USJ 22nm node and beyond
  - n+ USJ 22nm node and beyond
- Strain Technology
  - pMOS 22nm node and beyond
  - nMOS 22nm node and beyond
- Summary

Summary of Planar CMOS –vs-FinFET

- **VLSI Sym 2008:** Planar CMOS to 22nm Node
  - Intel said SRAM needs Bulk FinFET/Trigate at 16nm or Floating Body Cell FD-SOI (Mark Bohr)
- **IEDM 2008:**
  - Intel: Stated that FinFET not ready for 22nm node manufacturing (K. Kuhn).
- **VLSI Sym 2009:**
  - IBM: TC Chen stated at 16nm node body controlled devices (FD-SOI or FinFET) will be required to extended CMOS to 11nm CMOS

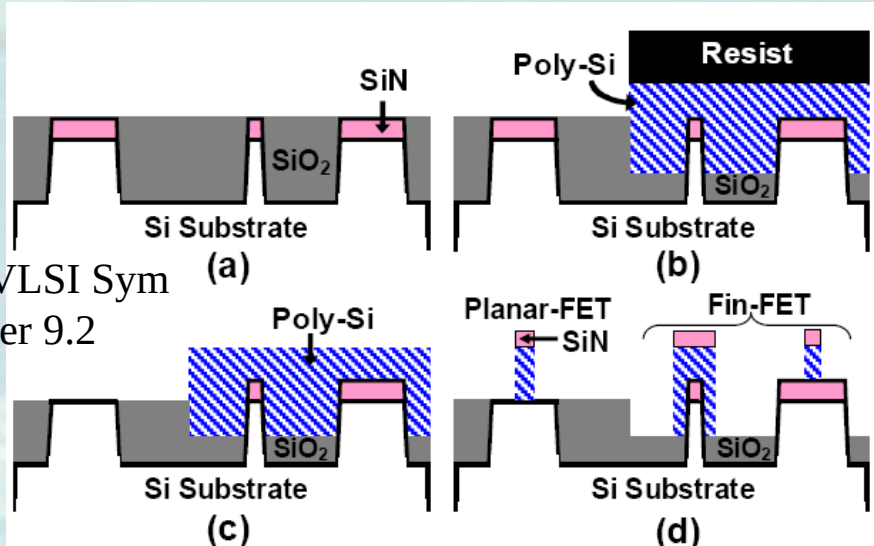
-TSMC April 2010: Planar bulk at 20nm node 5th gen SiGe & 2nd gen Hik/MG, 14nm node maybe FinFET (S.Y. Chiang)

Intel, VLSI Sym 2008 short course



J.O.B. Technologies Marketing, Sales & Technology)

Toshiba, VLSI Sym 2006, paper 9.2



FD/SOI With Dielectrically Isolated Back Gates

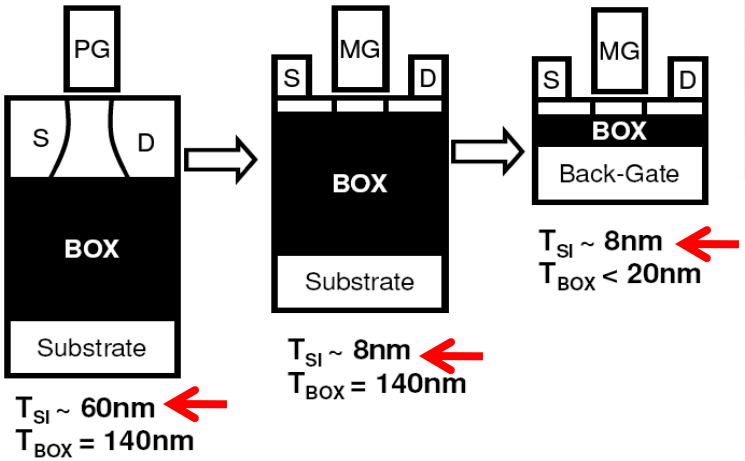


Fig.5. Possible device roadmap to enable back-gating at post 32 nm nodes.

G. Shahidi, IBM, VLSI Sym 2010, paper 13.5

IBM/YH, VLSI Sym 2010, paper, 4.4

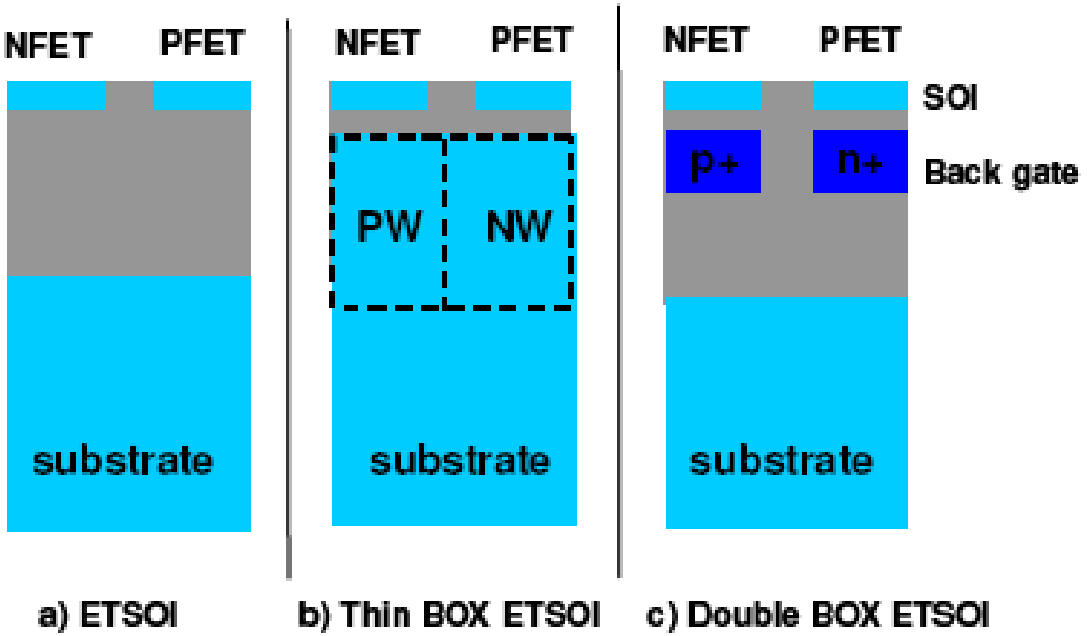


Fig. 1. Schematic view of fully-depleted thin SOI CMOS structures: (a) on thick BOX (b) on thin BOX with junction isolated back gate (c) on double BOX with dielectrically isolated back gate.

Hybrid Localized SOI/Bulk Technology Using Buried SiGe Layer/Channel

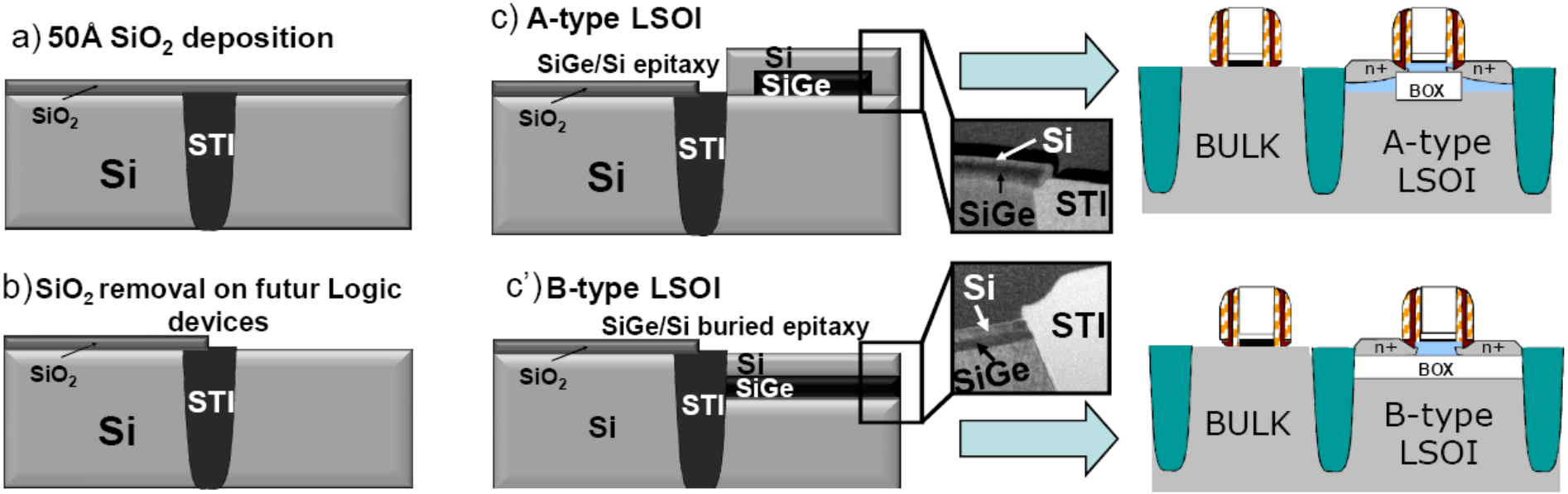


Fig.2: Key steps for the co-integration. The thick SiO_2 layer (50Å) is used as hardmask for future I/O devices (a,b). Then, selective SiGe/Si epitaxy is performed for the LSOI structures: folded epi for the A-type transistors (c), or buried facet-free epi for the B-type devices (c').

ST/LETI, VLSI Sym 2010, paper 6.2

Ultra-Thin-Body & Box (UTBB) FD-SOI And Localized SOI (LSOI)

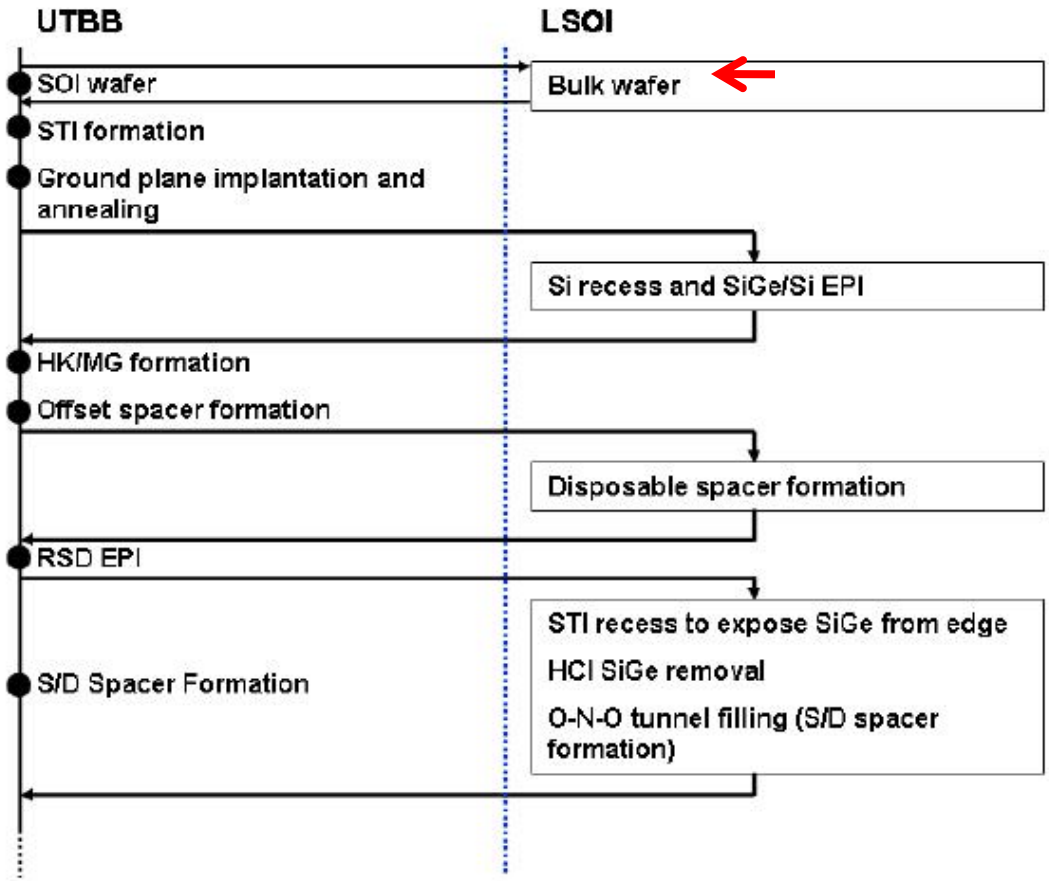


Fig.1 UTBB and LSOI integration schemes

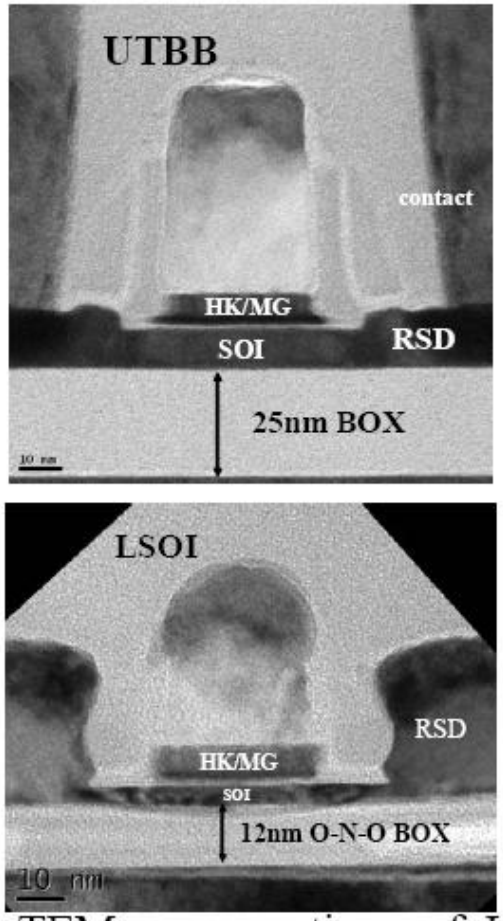


Fig. 2 TEM cross-sections of UTBB and LSOI, featuring 25nm L_G.

Intel's 15nm Node Floating Body Cell (FBC) FD-SOI With Back Gate Doping

Intel, VLSI Sym 2010, paper 15.1

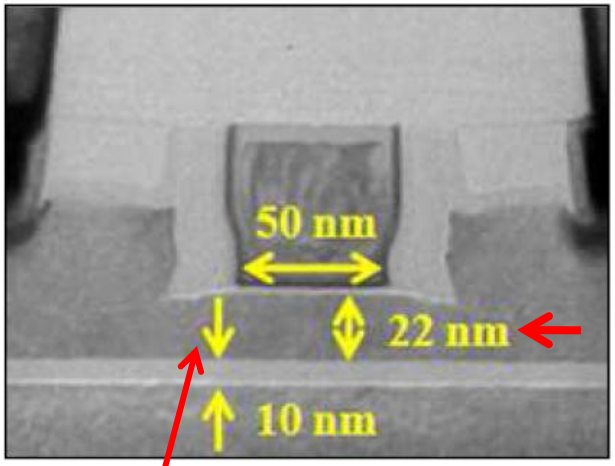


Fig. 4 A typical TEM micrograph of a 10-nm BOX FBC device, nominally targeted at L_g=50 nm and T_{si}=25 nm.

Tip implant before spacer

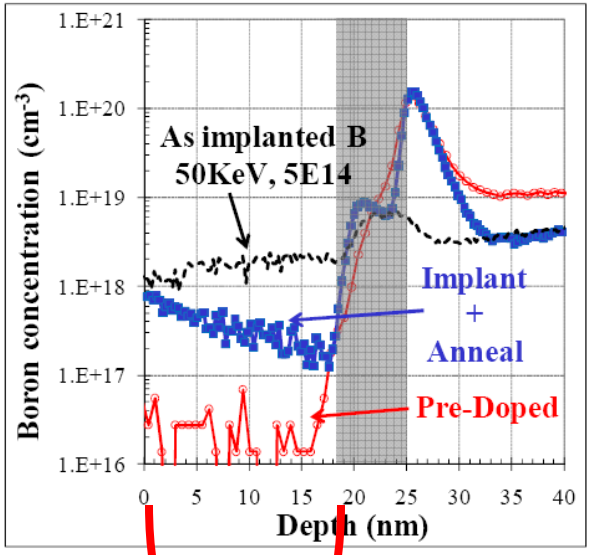


Fig. 6 Boron SIMS profiles: as-implanted B (dashed line), post-implant and anneal, and pre-doped SOI.

Intel's Silicon on Replacemet Insulator (SRI) FBC Using SiGe Etching For LSOI

Intel, VLSI Sym 2010, paper 15.4

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

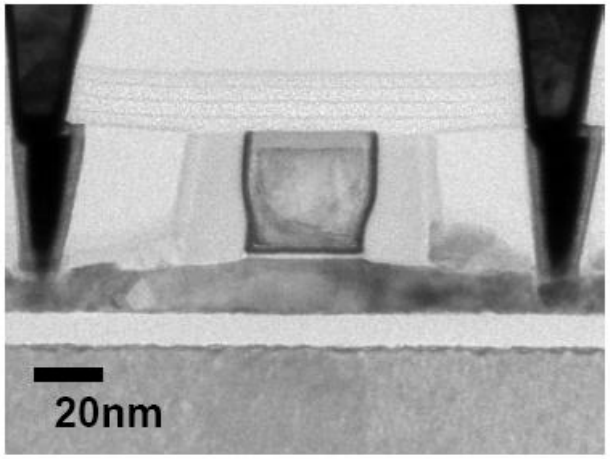


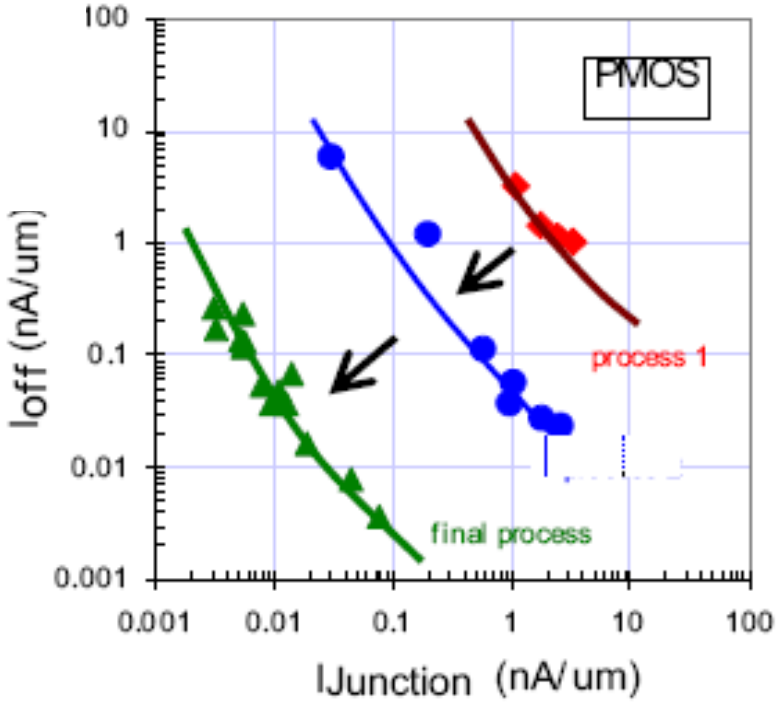
Fig. 4 TEM micrograph of 15-nm node SRI FBC device: L_g=51 nm, W=77 nm, T_{Si}=25 nm, and T_{BGox} =12nm.

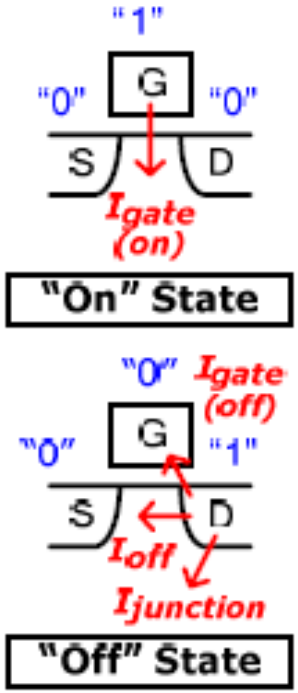
Trench process
Poly dep/pattern/etch
Oxide recess
SiGe etch
Gap fill
Trench refill/CMP
BG doping
Standard logic process

Fig. 1. Process flow. SRI process is highlighted.

IEDM-2009: Intel 32nm Node Low Leakage Junctions

- Isolation (wells, Vt)
- *Oxide I/O gate growth*
- *Oxide I/O gate patterning*
- Dielectric growth
- Poly-Si dep
- Poly-Si patterning
- Logic S/D extension- HP/LP
- *ULP S/D extension*
- *I/O S/D extension*
- Spacer dep/patterning
- S/D formation
- Poly-Si Gate Removal
- Metal Gate Replacement
- Contact Formation





$$I_{total} = \tfrac{1}{2}(\text{“On” state leakage}) + \tfrac{1}{2}(\text{“Off” state leakage})$$

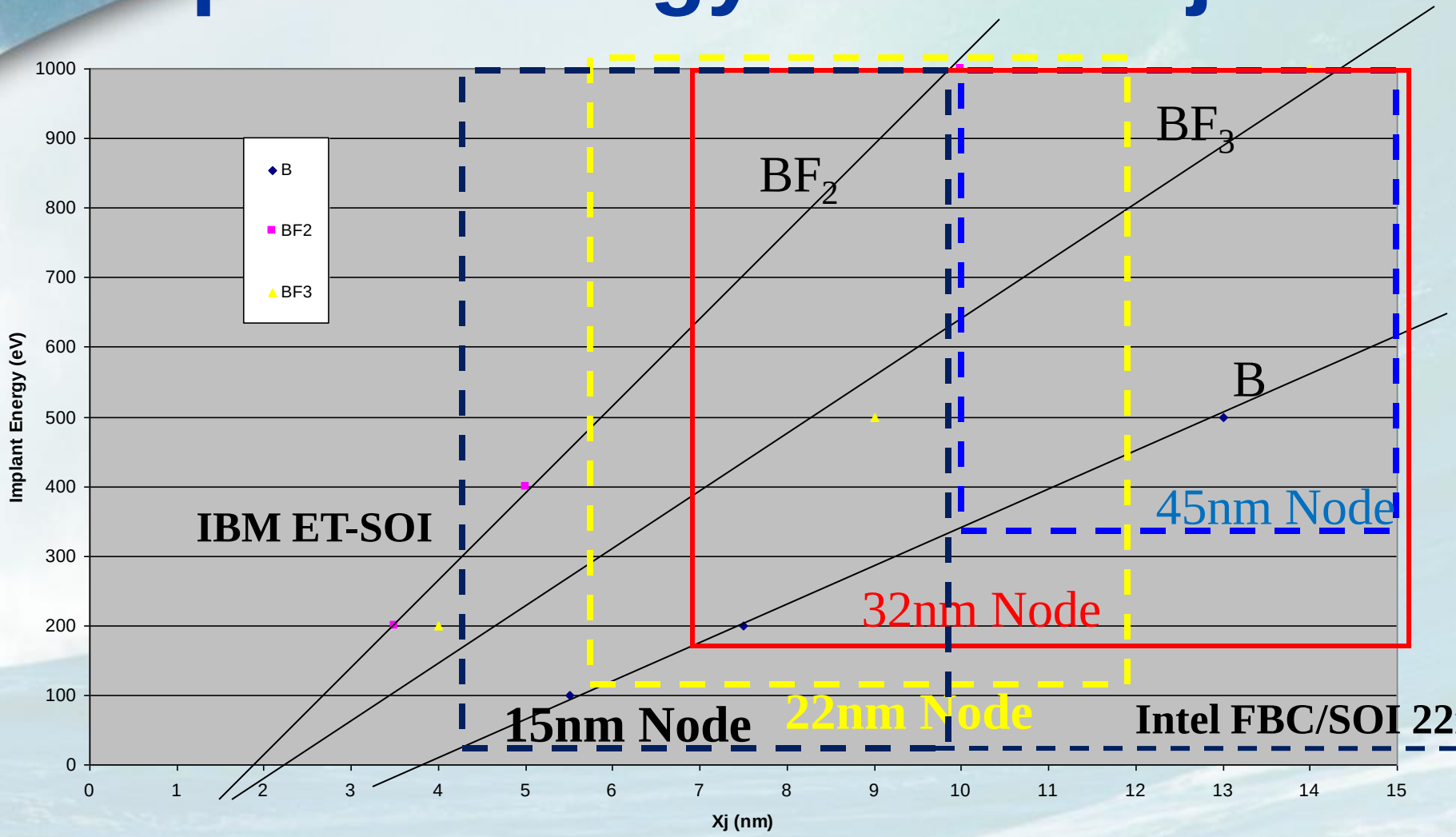
Fig. 6 Ioff vs. Ijunction trade-off and total leakage (Itotal) optimization for the final process

J.O.B. Tech
Marketing, S
Technology

Outline

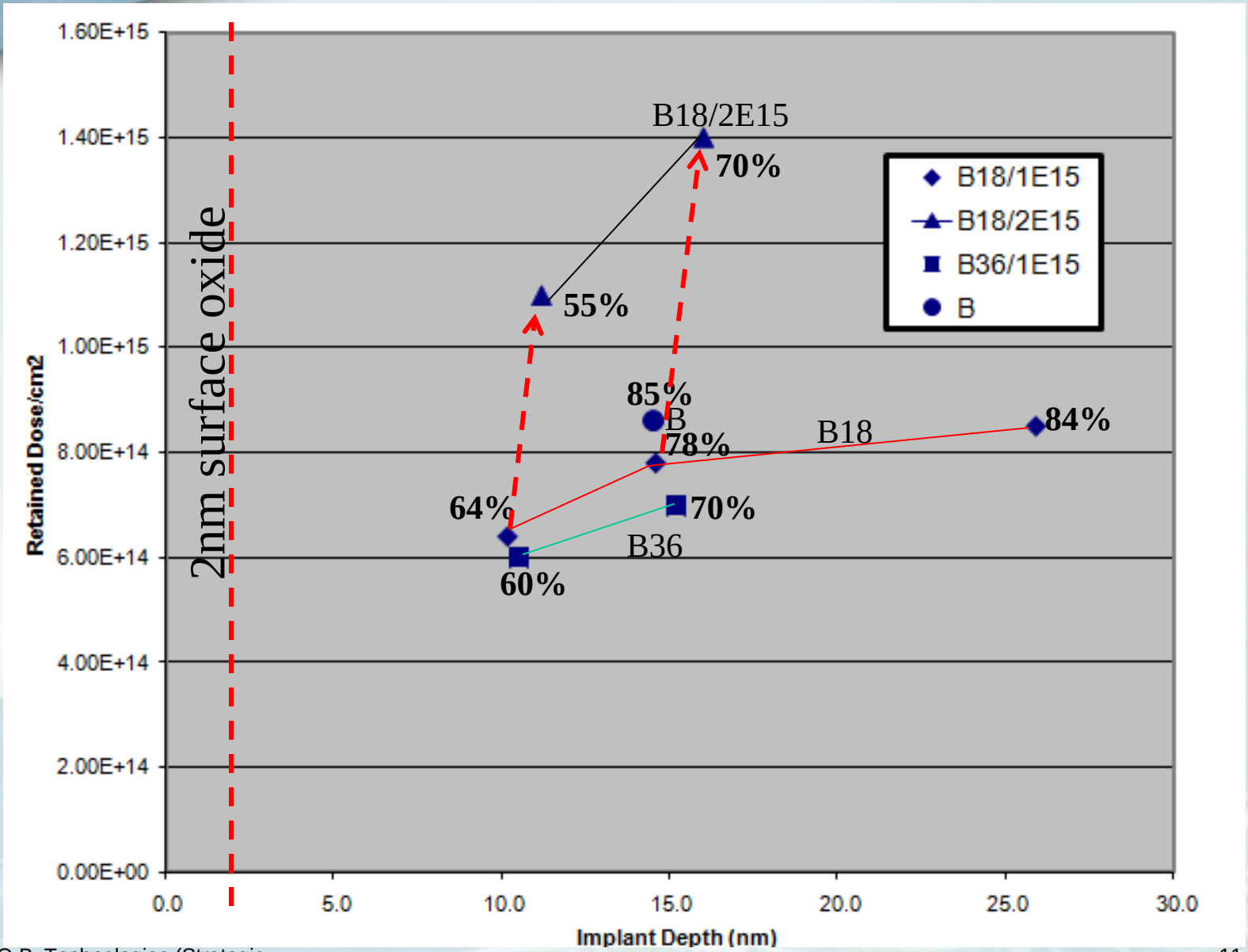
- Introduction
  - Technology Roadmap Options
- **USJ Technology:**
  - **p+ USJ 22nm node and beyond**
  - **n+ USJ 22nm node and beyond**
- Strain Technology
  - pMOS 22nm node and beyond
  - nMOS 22nm node and beyond
- Summary

Implant Energy Versus Xj



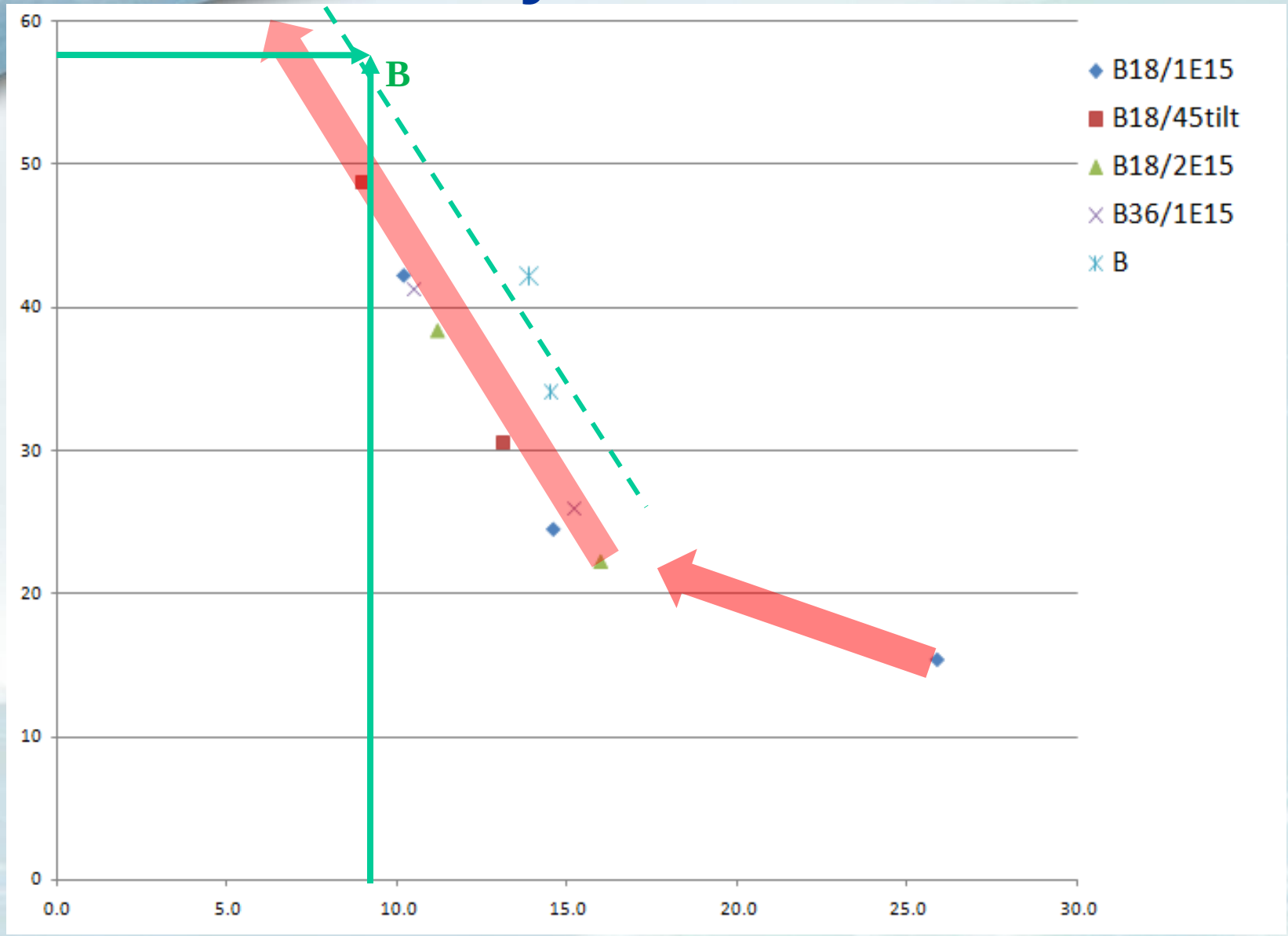
Borland, Semiconductor International, Dec. 2006, p.49

B, B18 & B36 Total Retained Dose (2nm oxide)

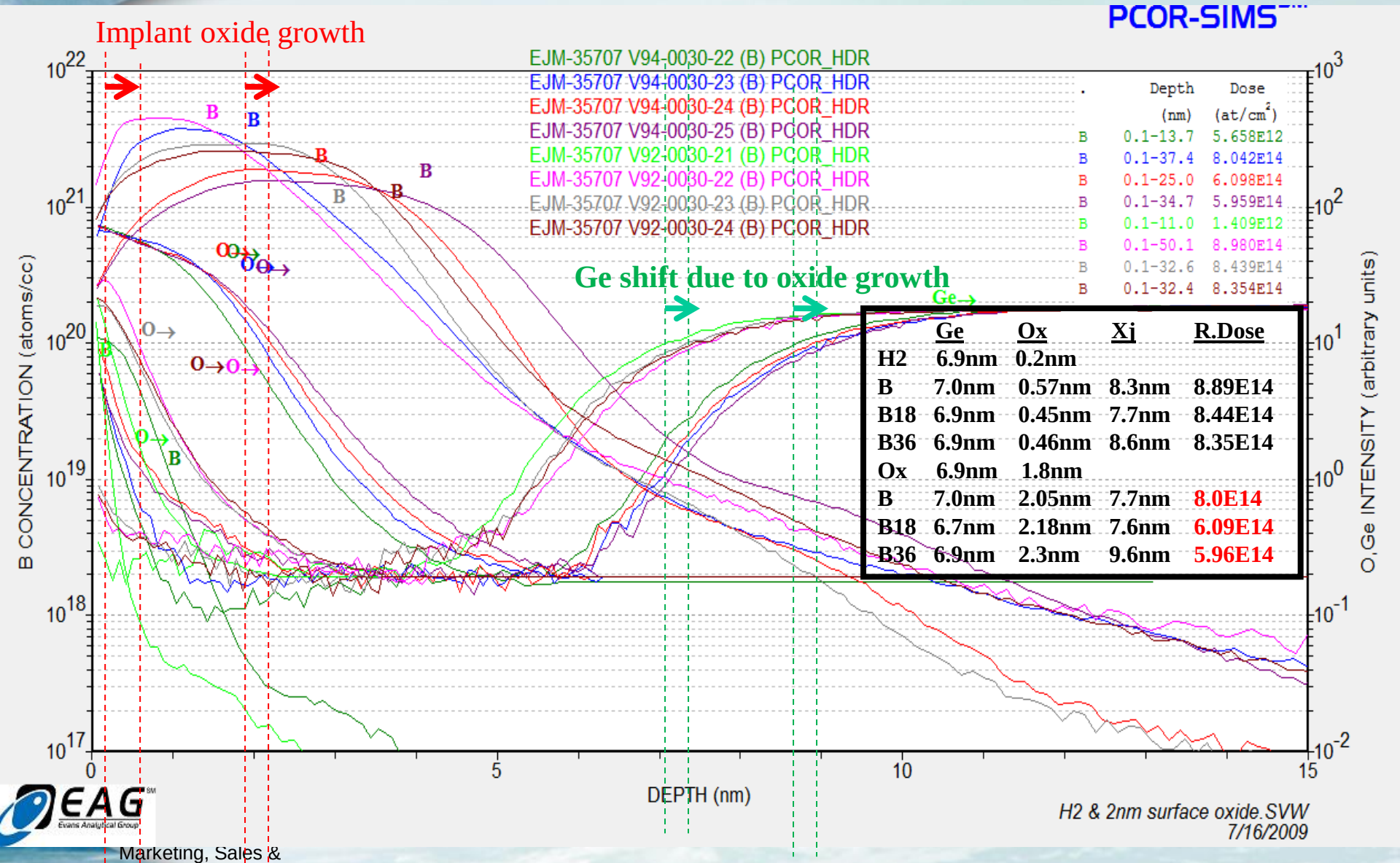


Borland et al., JOB

PCOR-SIMS Analysis



Proof Of Surface Reflectance/Backscatter On Retained Dose Limit & Implant Oxide Growth



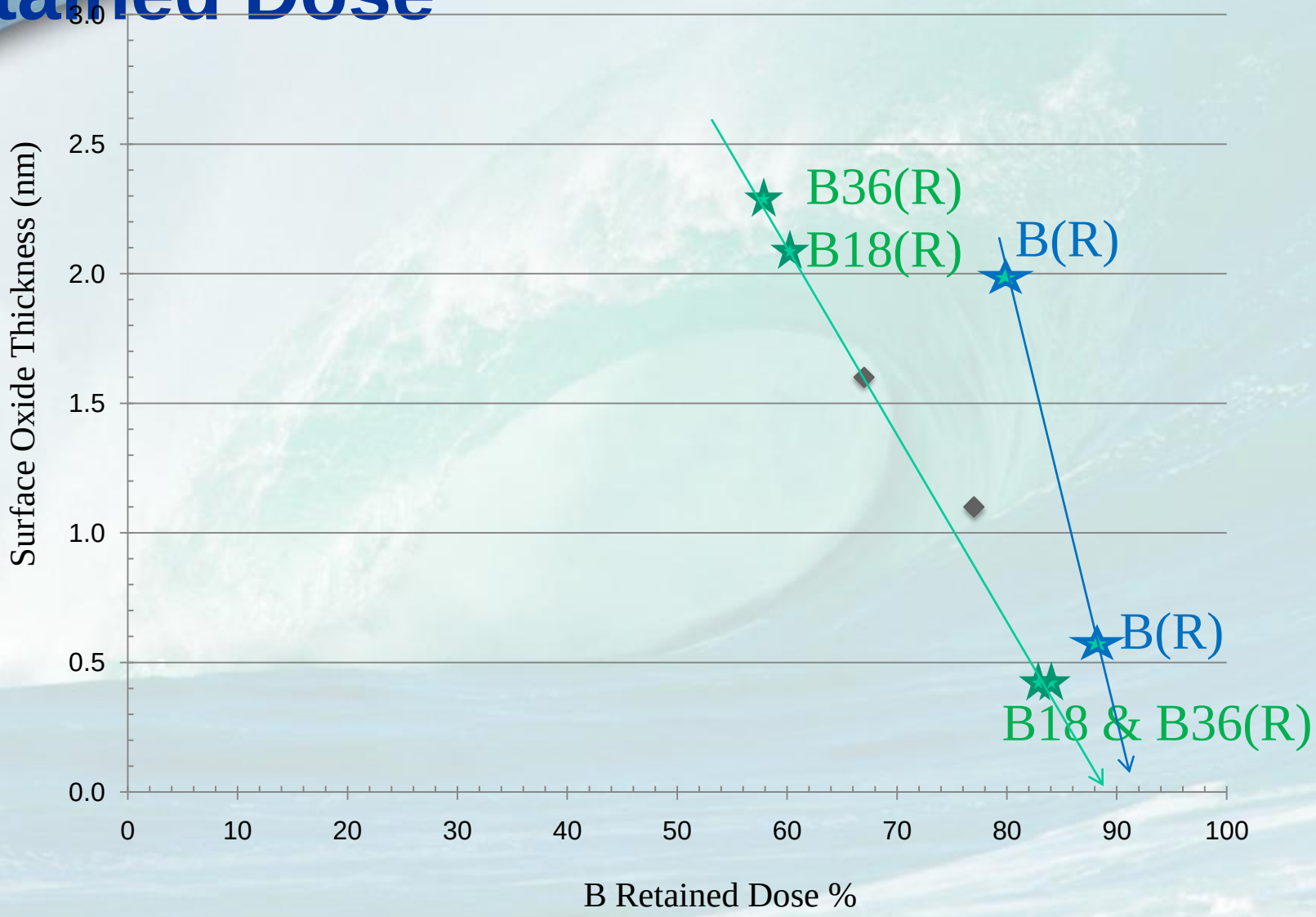
	Depth (nm)	Dose (at/cm²)
B	0.1-13.7	5.658E12
B	0.1-37.4	8.042E14
B	0.1-25.0	6.098E14
B	0.1-34.7	5.959E14
B	0.1-11.0	1.409E12
B	0.1-50.1	8.980E14
B	0.1-32.6	8.439E14
B	0.1-32.4	8.354E14

	Ge	Ox	Xj	R.Dose
H2	6.9nm	0.2nm		
B	7.0nm	0.57nm	8.3nm	8.89E14
B18	6.9nm	0.45nm	7.7nm	8.44E14
B36	6.9nm	0.46nm	8.6nm	8.35E14
Ox	6.9nm	1.8nm		
B	7.0nm	2.05nm	7.7nm	8.0E14
B18	6.7nm	2.18nm	7.6nm	6.09E14
B36	6.9nm	2.3nm	9.6nm	5.96E14

EAG Evans Analytical Group

Marketing, Sales & Technology)

PCOR-SIMS Analysis Of Surface Oxide & Retained Dose

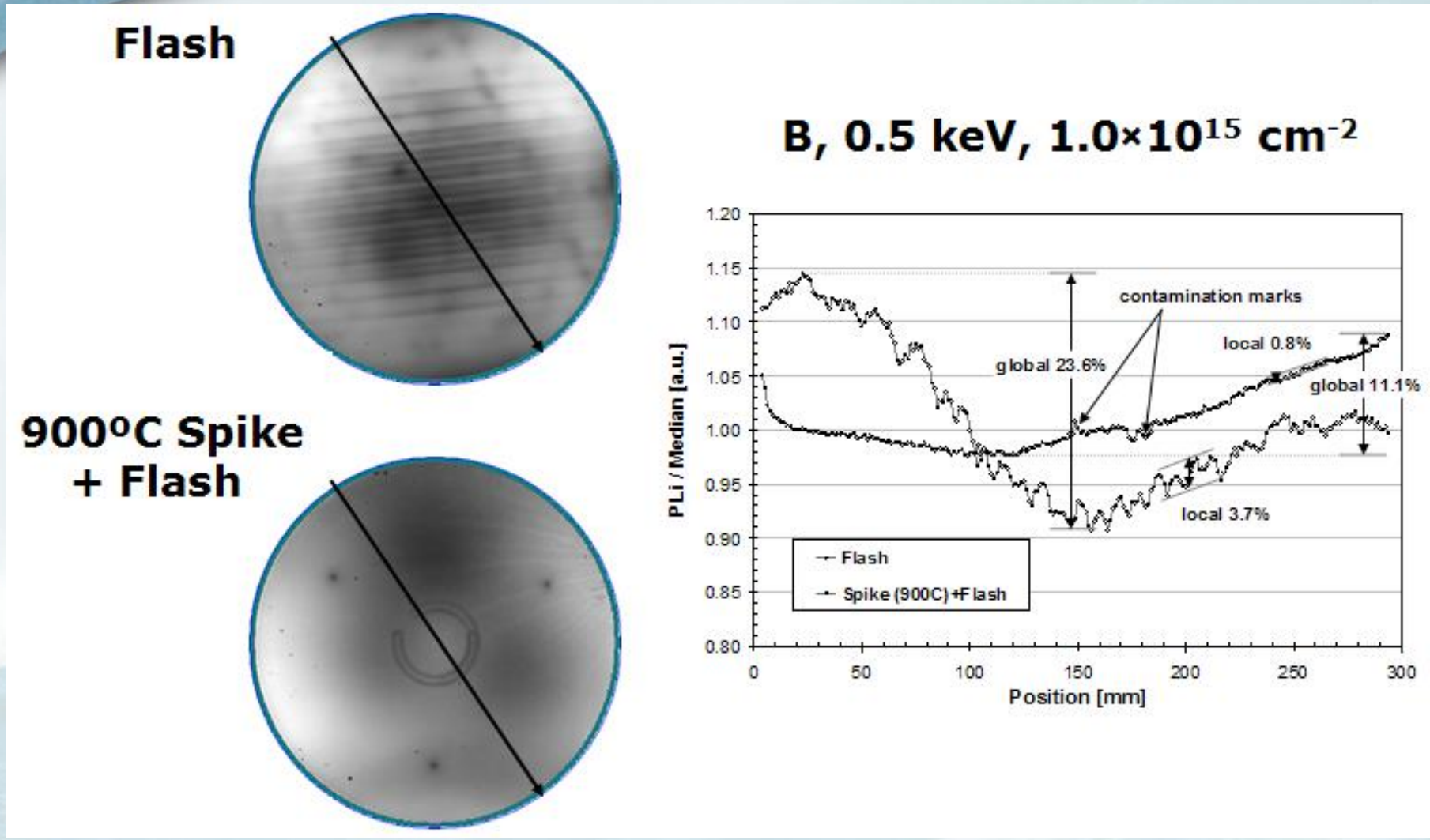


Borland et al., JOB

Lower Residual Implant Damage & Improve Device Leakage

- Improve self-amorphization to reduce residual implant damage with MSA
  - Lower implant wafer temperature (cold or cryo-implantation) -10^{o}C to -160^{o}C using chilled water of liquid nitrogen wafer cooling
  - Use molecular dopants (B18H22, B36H44, As4 or P4) improves self-amorphization
  - Use heavier ions low dose for PAI & optimize amorphous depth (In, Sb or Xe) at <5E13/cm2
- Stable defects and reduction in residual implant damage thereby improving junction leakage
  - Higher MSA peak temperature >1300^{o}C
  - Pre/post MSA diffusion-less spike/RTA 850-900^{o}C

PLi Of Flash And 900C Spike+Flash



Borland et al., JOB/Selete, IWJT 2007

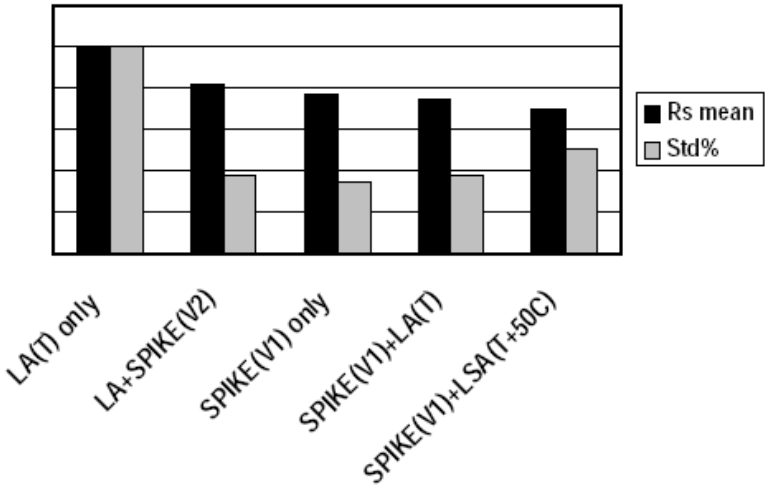


Figure 3. Final Rs and standard deviation using different post-implant anneal processes.

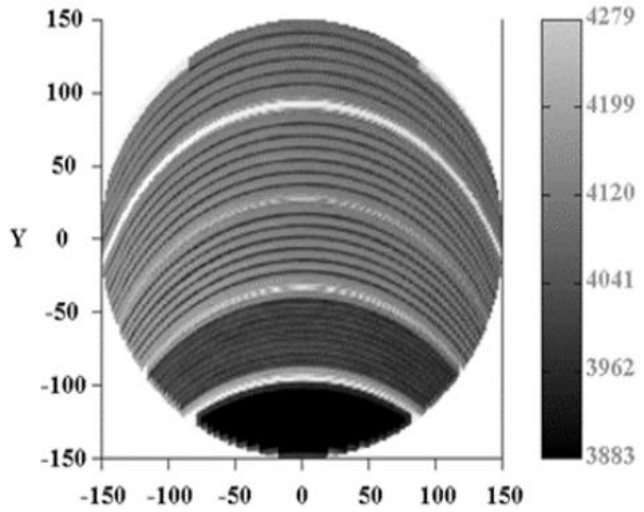


Figure 9. MOR map showing impact of laser beam overlap on micro non-uniformity. The laser beam overlap for the five laser scanning zones (from top to bottom) are 0, 5%, 10%, 40% and 50%, respectively.

Radiance spike/RTA signature

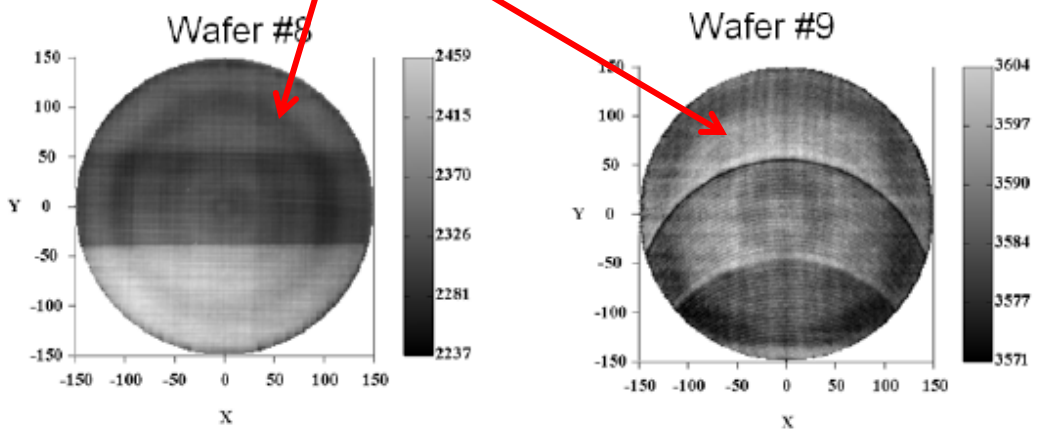


Fig.10: Thermwave mapping for wafer #8 (left) and wafer #9 processed with sRTA+ 3zone LSA

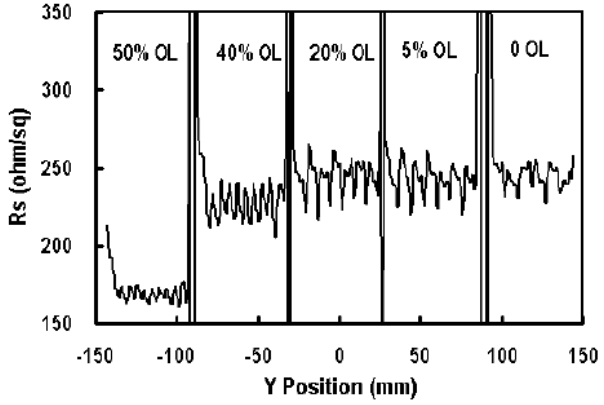
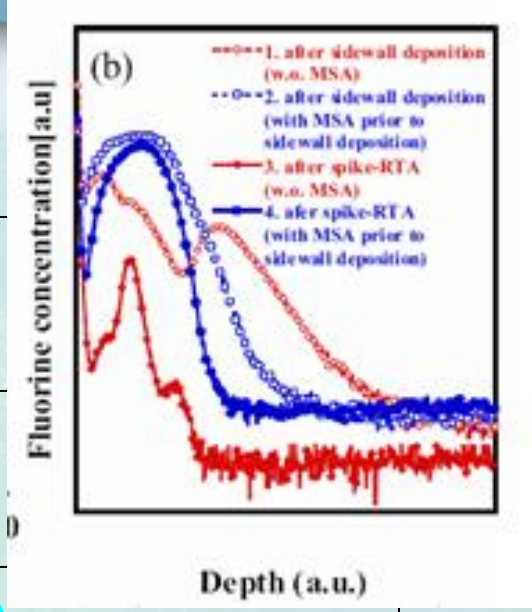


Figure 10. High resolution Rs scan across five zones with different amount of beam overlap, showing impact of laser beam overlap on micro non-uniformity.

Extension Results (Leakage)

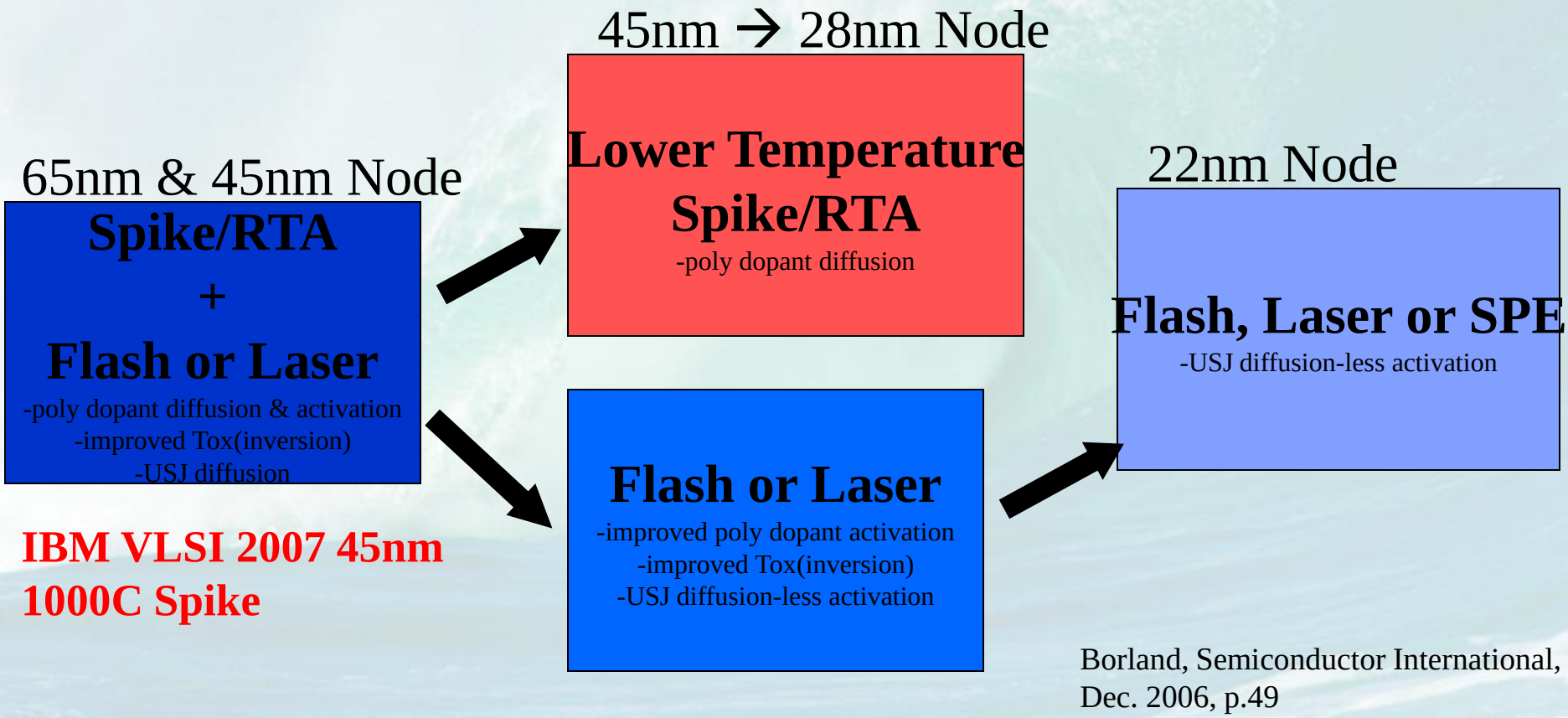


Yamamoto et al., IWJT 2008, MSA pins F in substitutional site and degrades leakage!

RsL Junction Leakage Current (A/cm2)

Borland & Kiyama, JOB/DNS, IIT-2008

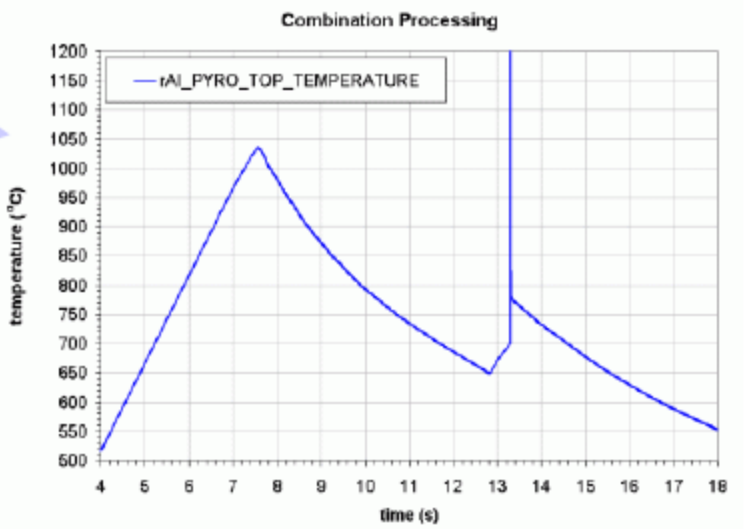
Poly & USJ Activation Roadmap

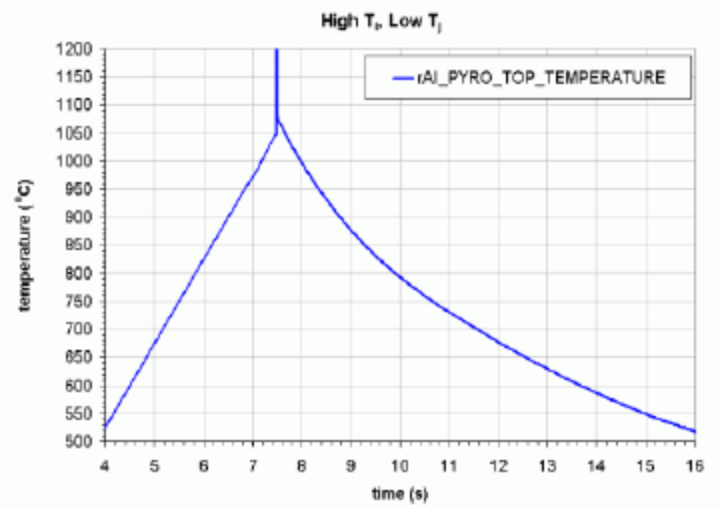


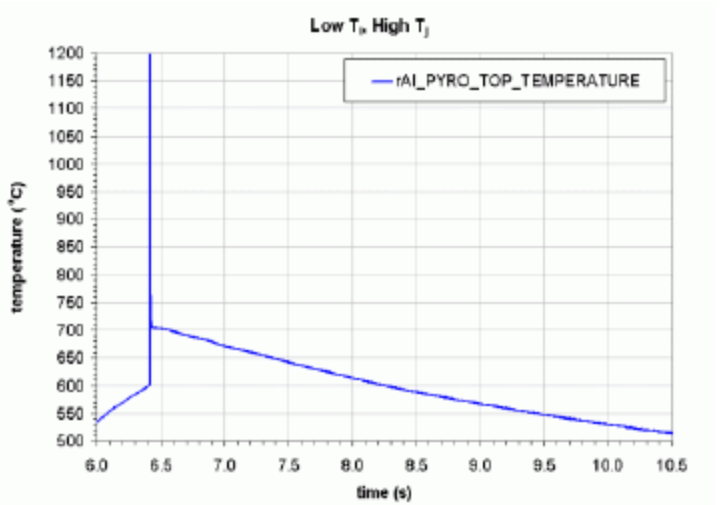
Borland, Semiconductor International, Dec. 2006, p.49

Anneal Process Flexibility

Novel combination processes can be run to combine spike + flash







Unmatched process flexibility

A Partner You Trust.
Performance You Value.

mattson

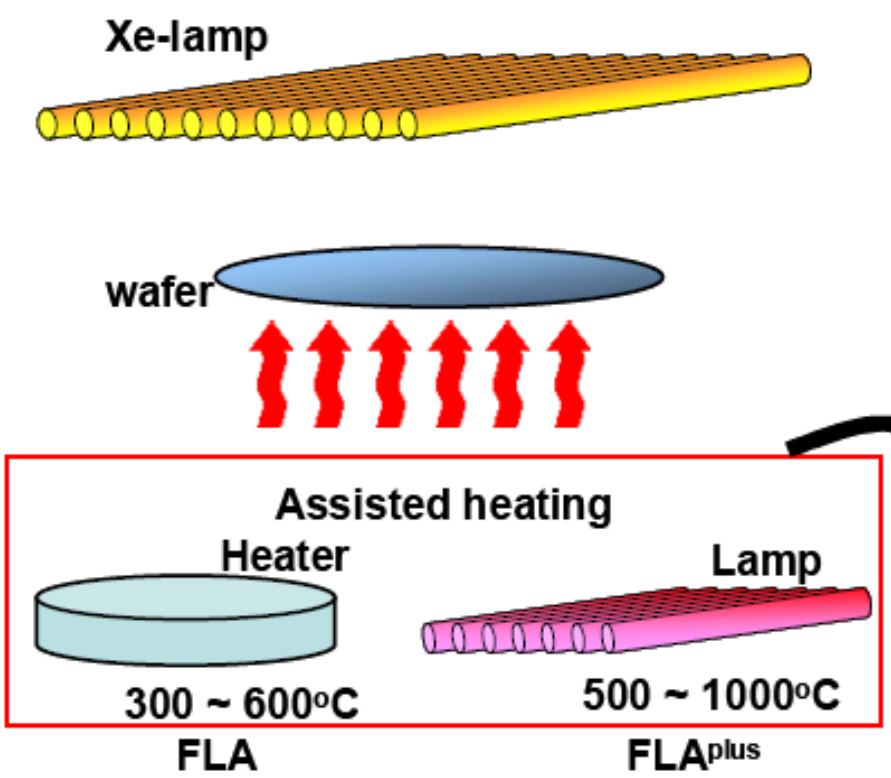


Fig. 1 Schematic drawing of FLA systems: (a) conventional heater-assisted type and (b) lamp-assisted type (FLA^{plus}).

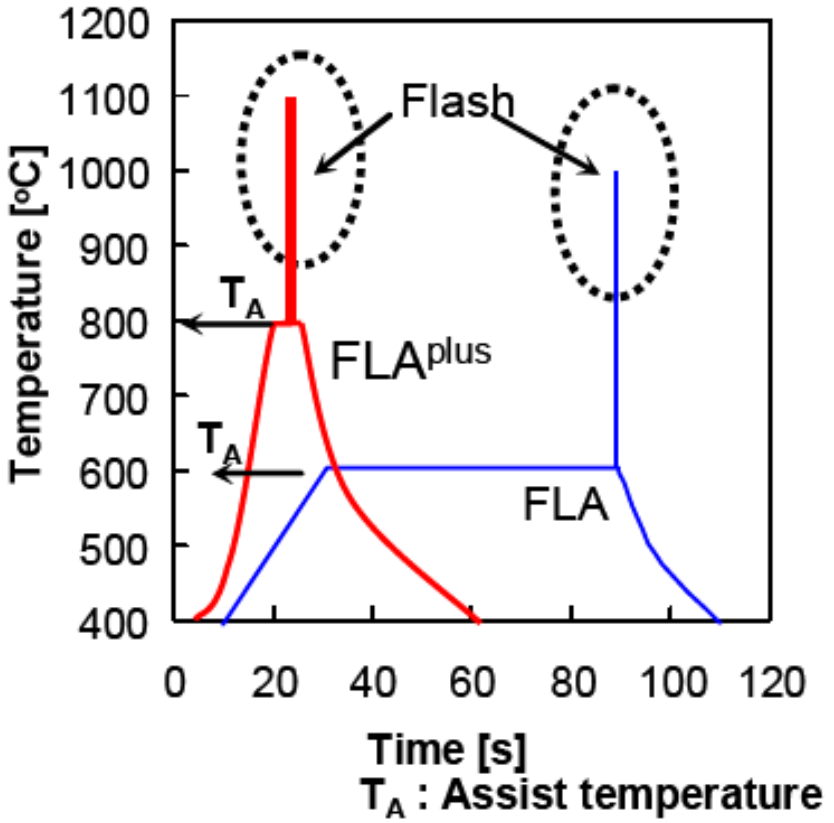
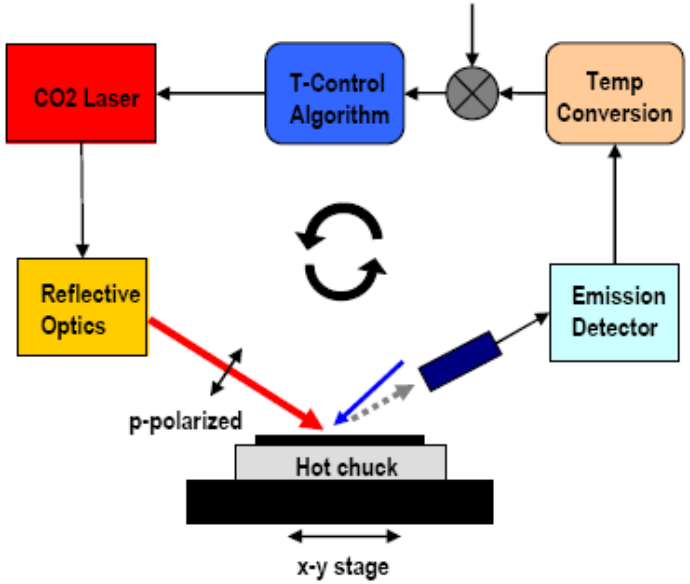
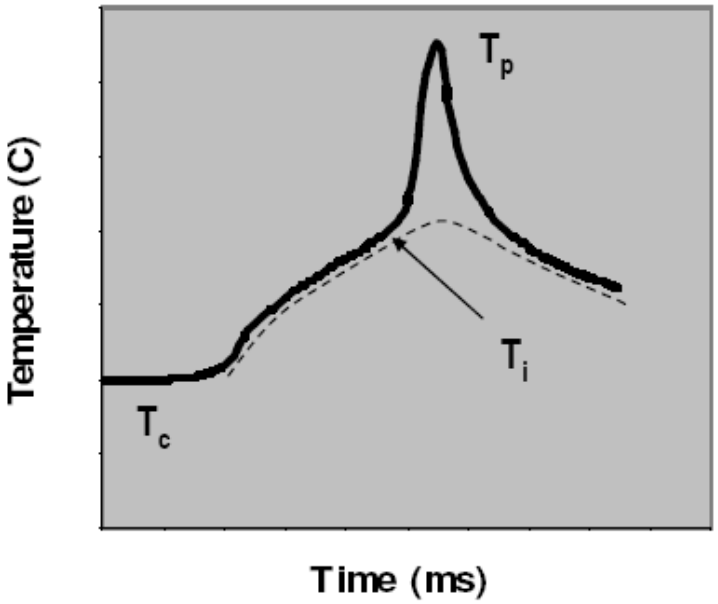


Fig. 2 Typical temperature profiles of conventional FLA and FLA^{plus}. The higher assist temperatures (T_A) used with FLA^{plus} allow higher peak temperatures to be reached in shorter times compared to conventional FLA.

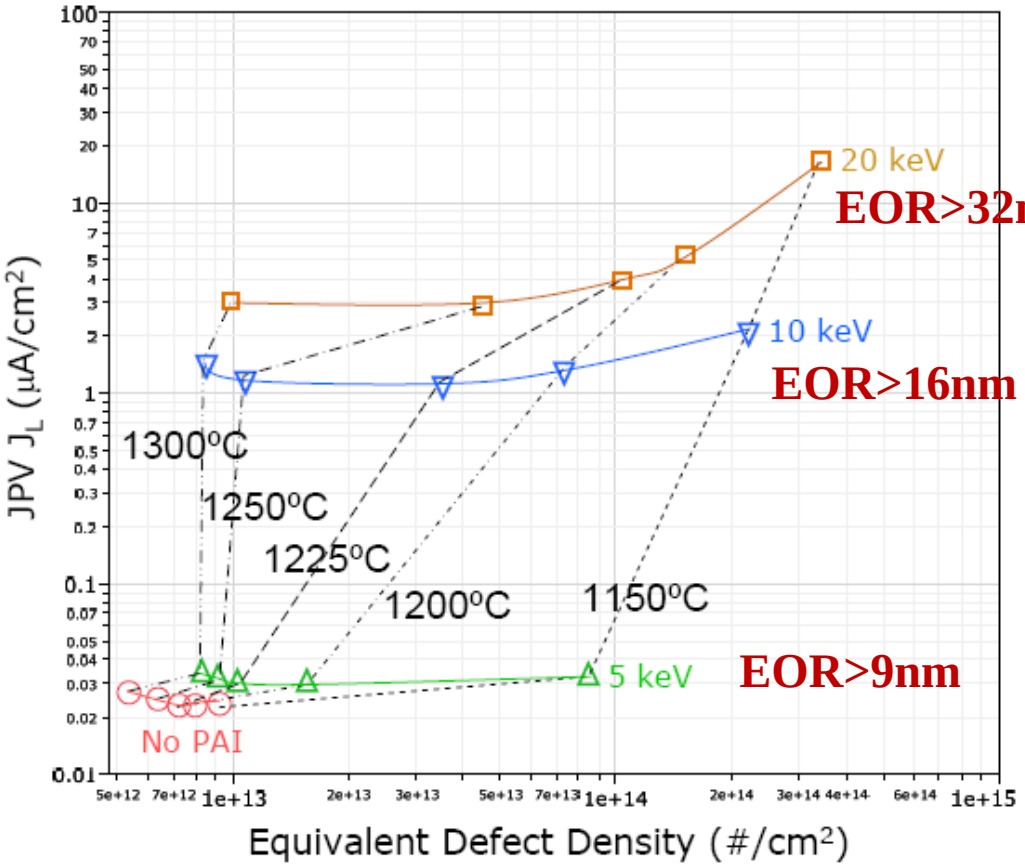
LSA Theory of Operation
Dual Beam Configuration

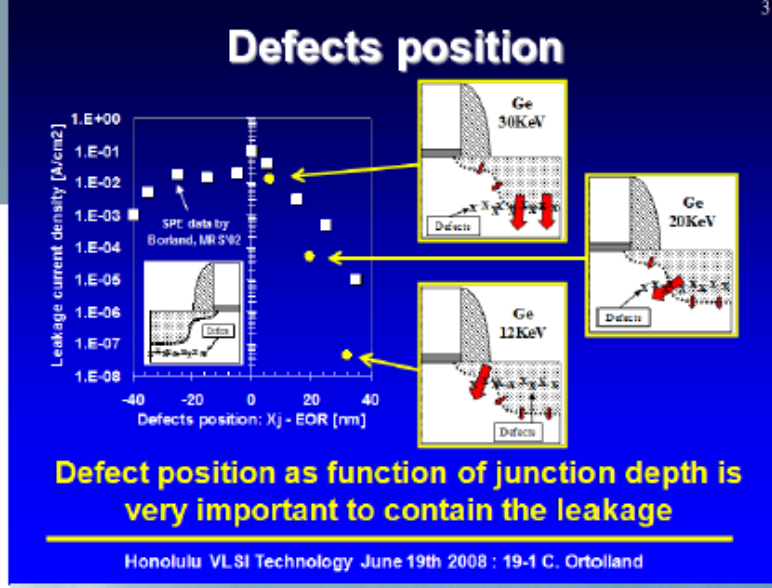


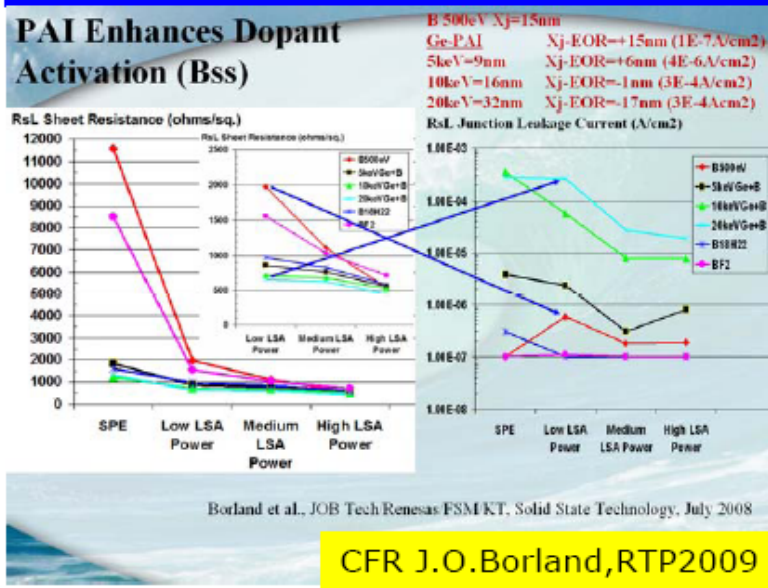


- **Dual beam configuration covers the long dwell time and low temperature regimes.**

JPVLeakage versus EDD

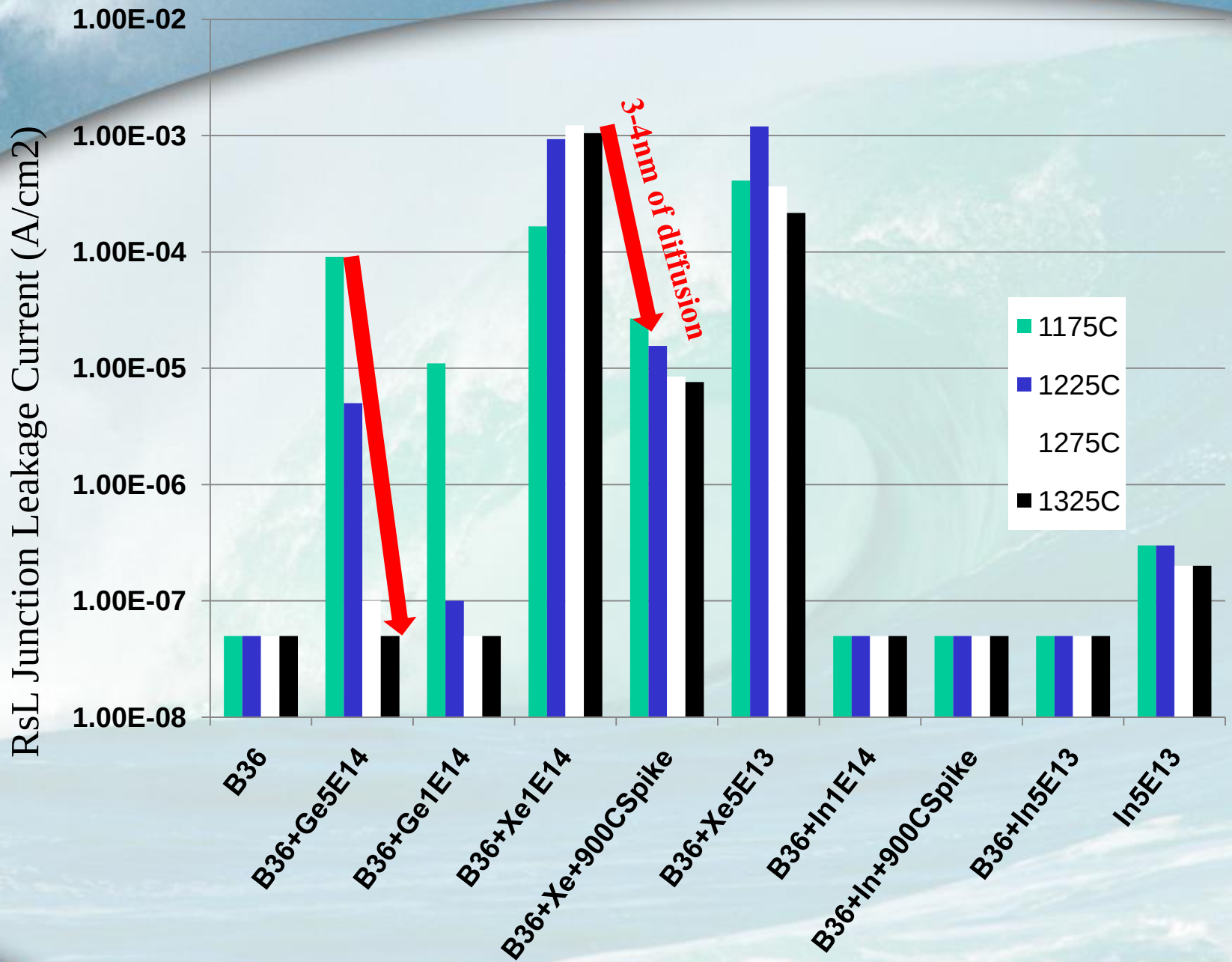




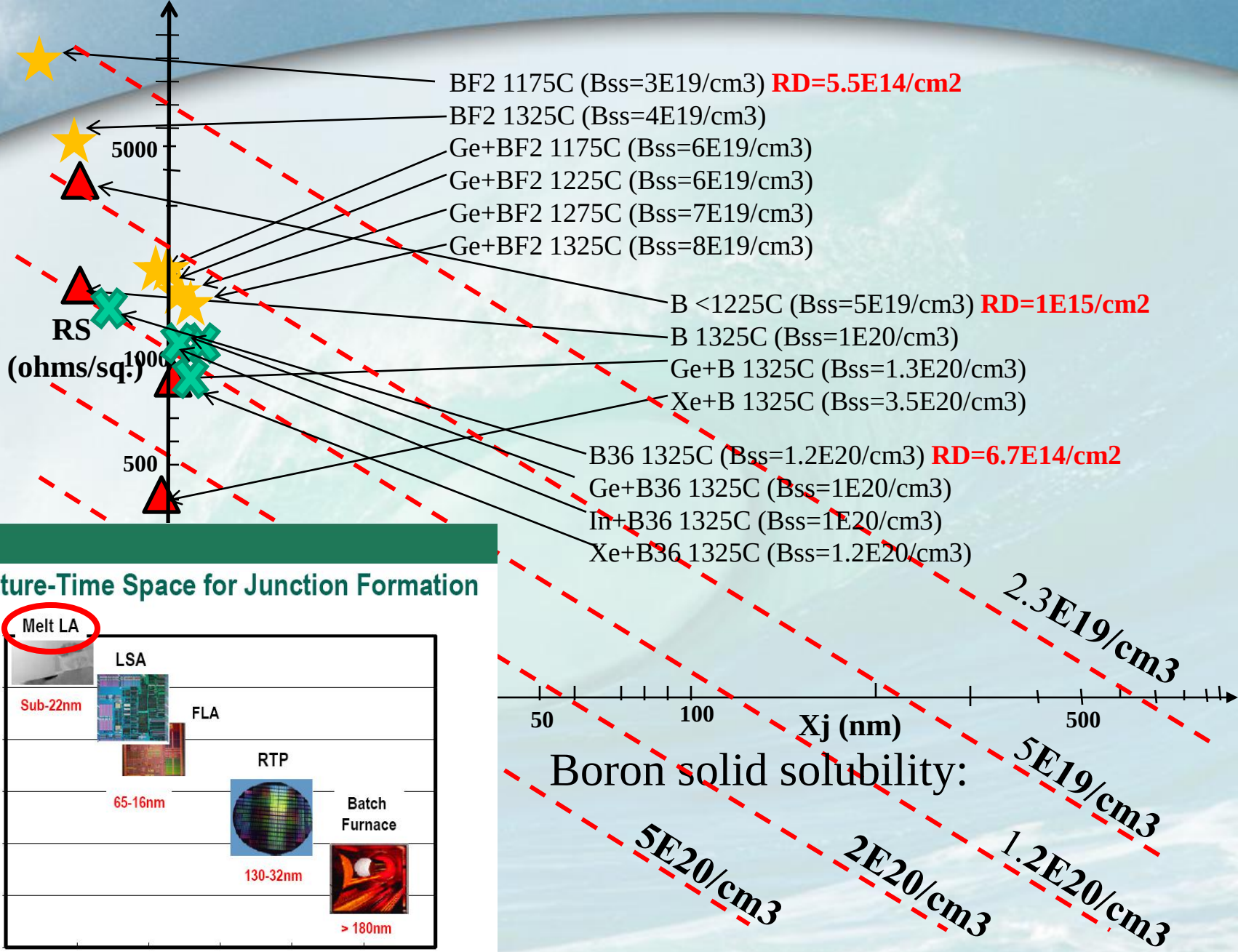


CFR J.O.Borland,RTP2009

- Defect dissolution is not the only parameter
- Xj position with respect to the EOR position important as well



Borland et al., IEEE-RTP-2009



Boron solid solubility:

Borland et al., RTP-2009

Ultratech

Temperature-Time Space for Junction Formation

Boron Dopant Activation With Laser Melt

1E15 dose: Rs=205 Bss=1.7E20/cm3
2E15 dose: Rs=132 Bss=3E20/cm3
4E15 dose: Rs=91 Bss=4E20/cm3
1E16 does: Rs=73 Bss=5E20/cm3

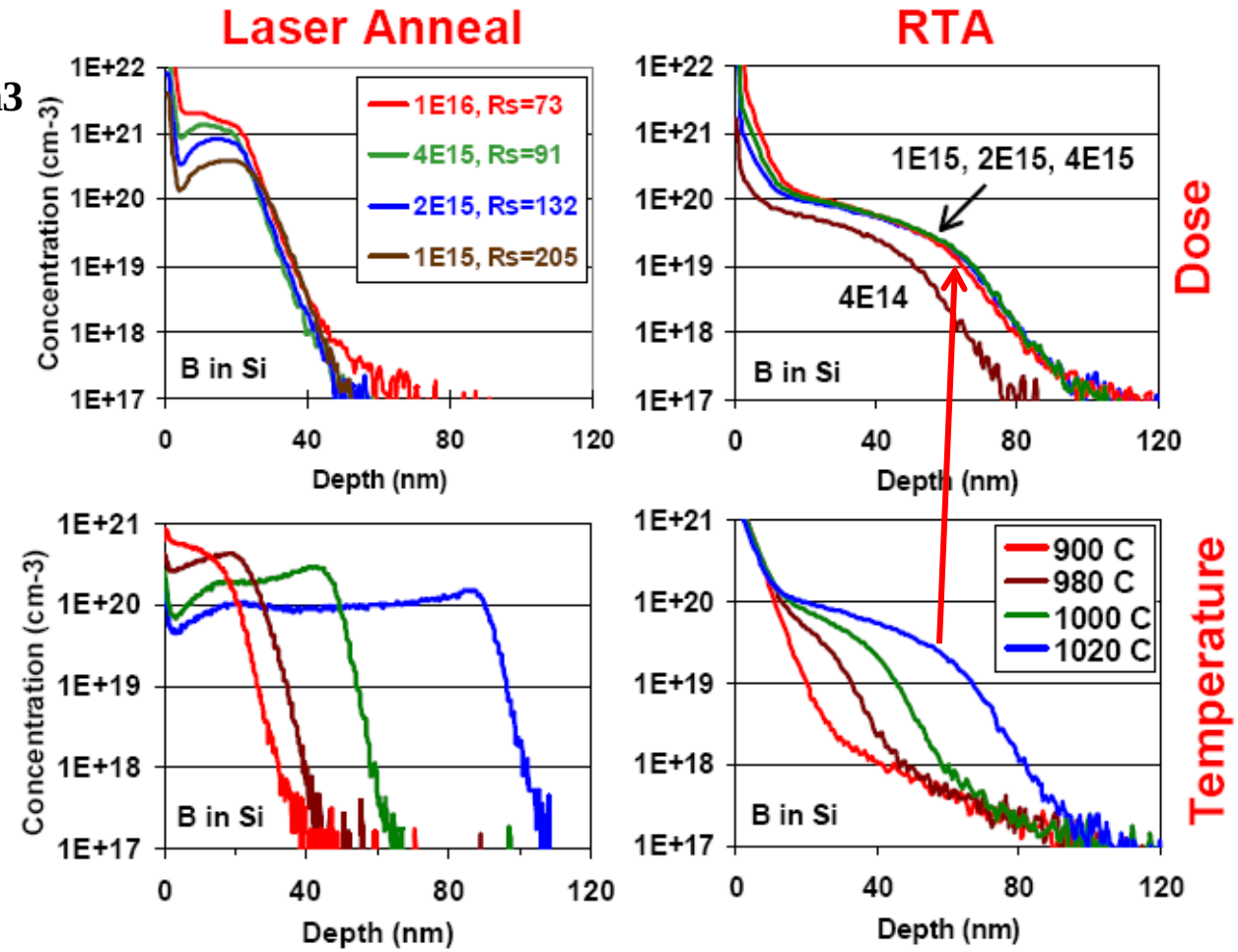


Fig. 11 – Laser melt anneal, showing increased abruptness and non-equilibrium enhanced activation (superactivation).

K. Kuhn, Intel, IWJT-2010 paper K2

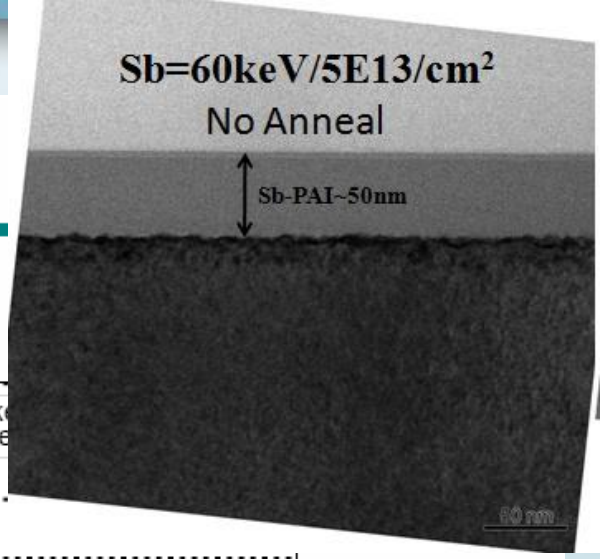
22nm Node Dopant Options: Enhanced SDE & HALO Dopant Activation/Amorphization

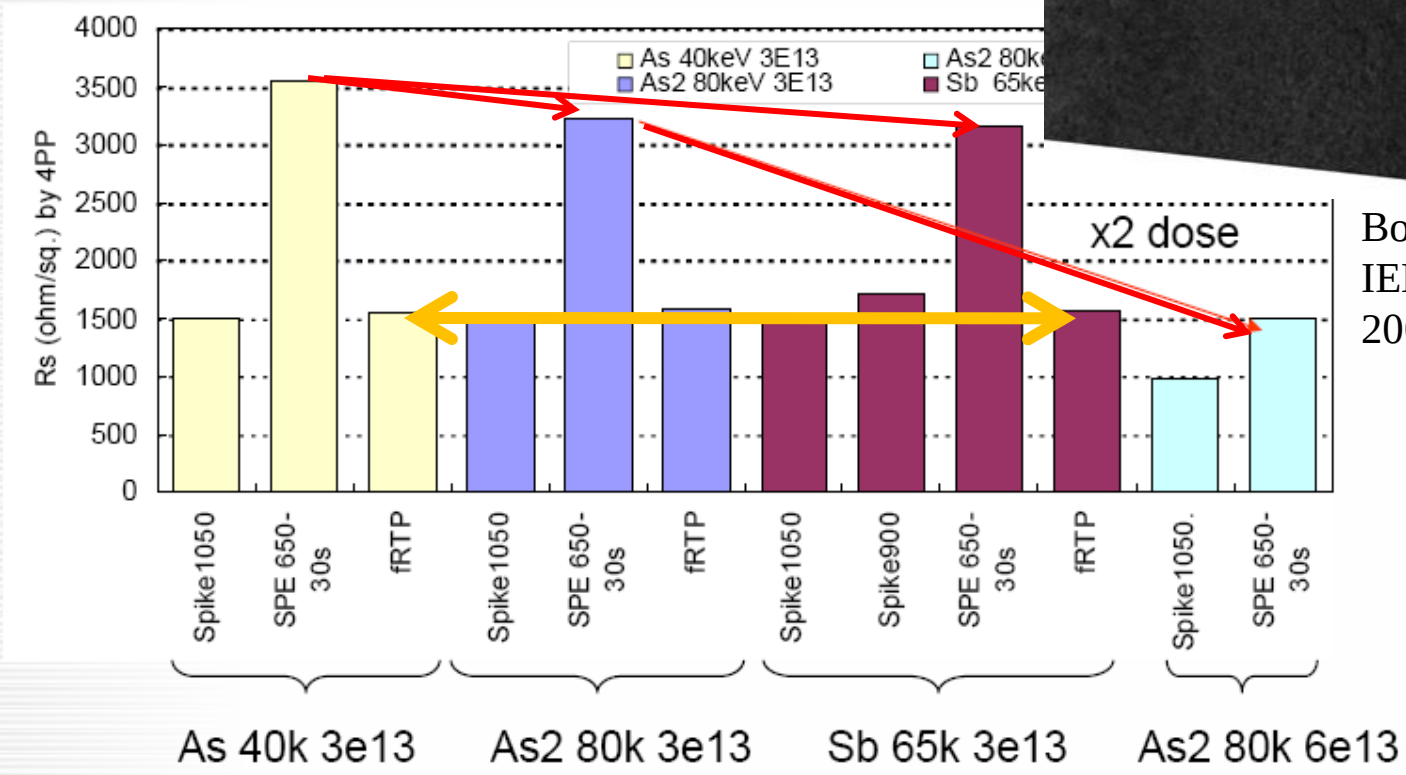
<850C Spike/RTA
>1350C Flash or Laser

- pMOS
  - **pSDE (1-3E15/cm2 dose limited by Bss?)**
    - **B**: **100eV/1E15** (need PAI?)
    - **BF2: 500eV/1E15** (dose lose!)
    - **B18: 2keV/5E13 (self-amorphization)**
    - **B36H44: 4keV/2.5E13 (self-amorphization)**
  - HALO (3E13/cm2 dose)
    - **As**: 20keV/3E13
    - **As2**: 40keV/1.5E13
    - **As4**: 80keV/7.5E12
    - **Sb**: 35keV/3E13 (self-amorphization)
- nMOS
  - nSDE (1E15/cm2 or > dose)
    - **As**: 1keV/1E15
    - **As2**: 2keV/5E14
    - **As4**: 4keV/2.5E14
    - **P**: 500eV/1E15
    - **P2**: 1keV/5E14
    - **P4**: 2keV/2.5E14
    - **Sb**: 1.7keV/1E15 (self-amorphization)
  - **HALO (3E13/cm2 dose)**
    - **BF2**: 20keV/3E13
    - **In**: 45keV/3E13 dose (self-amorphization but **limited by Inss?) In+B!**
    - **B18**: 80keV/1.5E12

N-Halo (As, As2, Sb)

Rs dependent on anneal conditions and ion species





Borland et al., IEEE/RTP-2009

Sheet resistance by SPER is much higher

⇒ The increasing of the As halo dose reduces the Rs by SPER

Mineji et al., NEC/JOBTech/Nissin, IWJT-2007

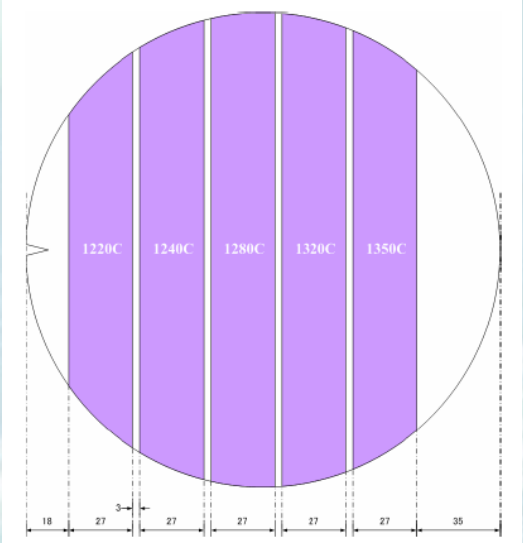
For 22nm Node p+ USJ Formation Using PAI & HALO Implantation With Laser Annealing

John O. Borland, J.O.B. Technologies, Aiea, HI
John Marino, EAG, East Windsor, NJ
Michael Current, Frontier Semiconductor, San Jose, CA
B.L. Darby, University of Florida, Gainesville, FL

IIT June 8, 2010

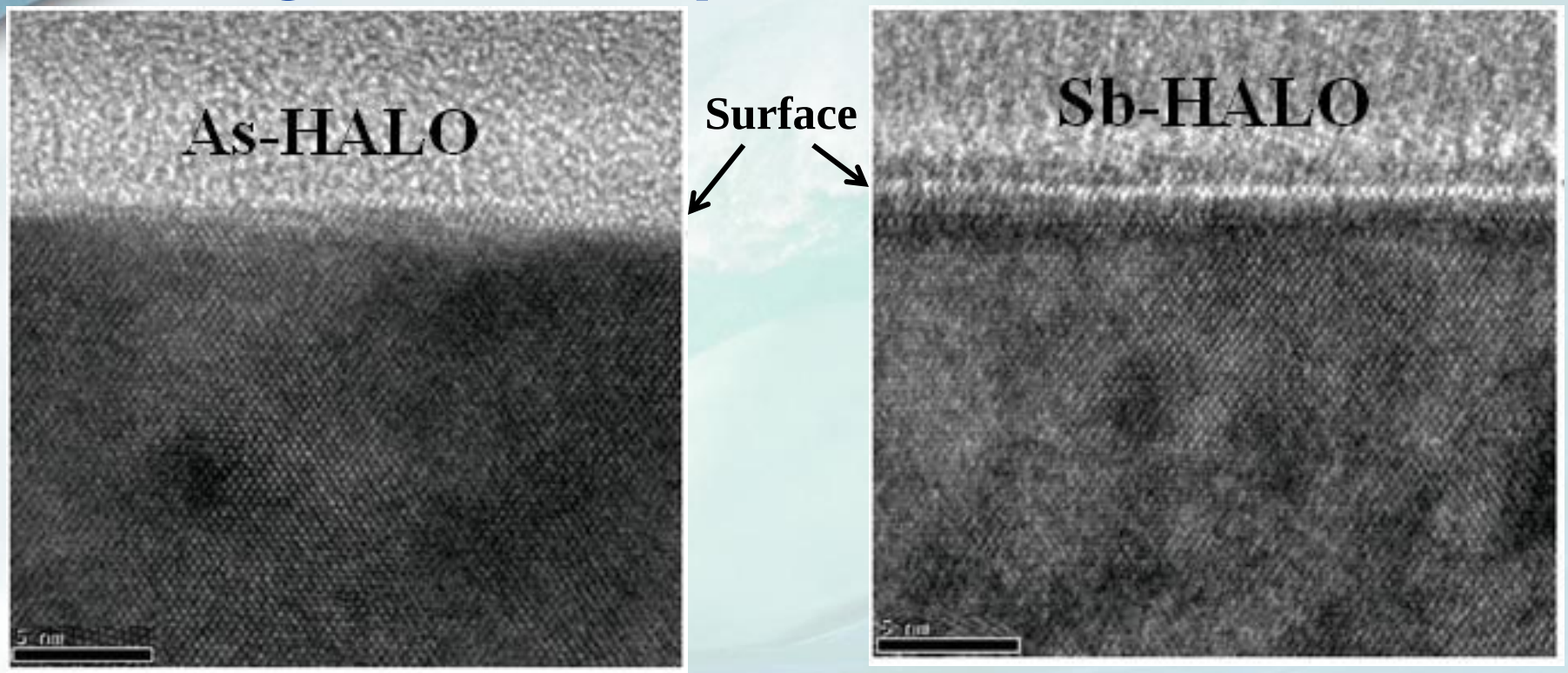
Experimental Matrix Split Conditions

	No HALO	20keV/3E13 As-HALO	35keV/3E13 Sb-HALO
•B (200eV/1E15)	X	X	X
•With Ge-PAI (3keV/5E14)	X	X	X
•With Ge-PAI (10keV/5E14)	X	X	X
•With Xe-PAI (5keV/5E13)	X	X	X
•With Xe-PAI (14keV/5E13)	X	X	X
•With In-PAI (5keV/5E13)	X	X	X
•With In-PAI (14keV/5E13)	X	X	X
•With B36 (100eV/1E15)	X	X	X
•With B36 (500eV/5E13)	X	X	X

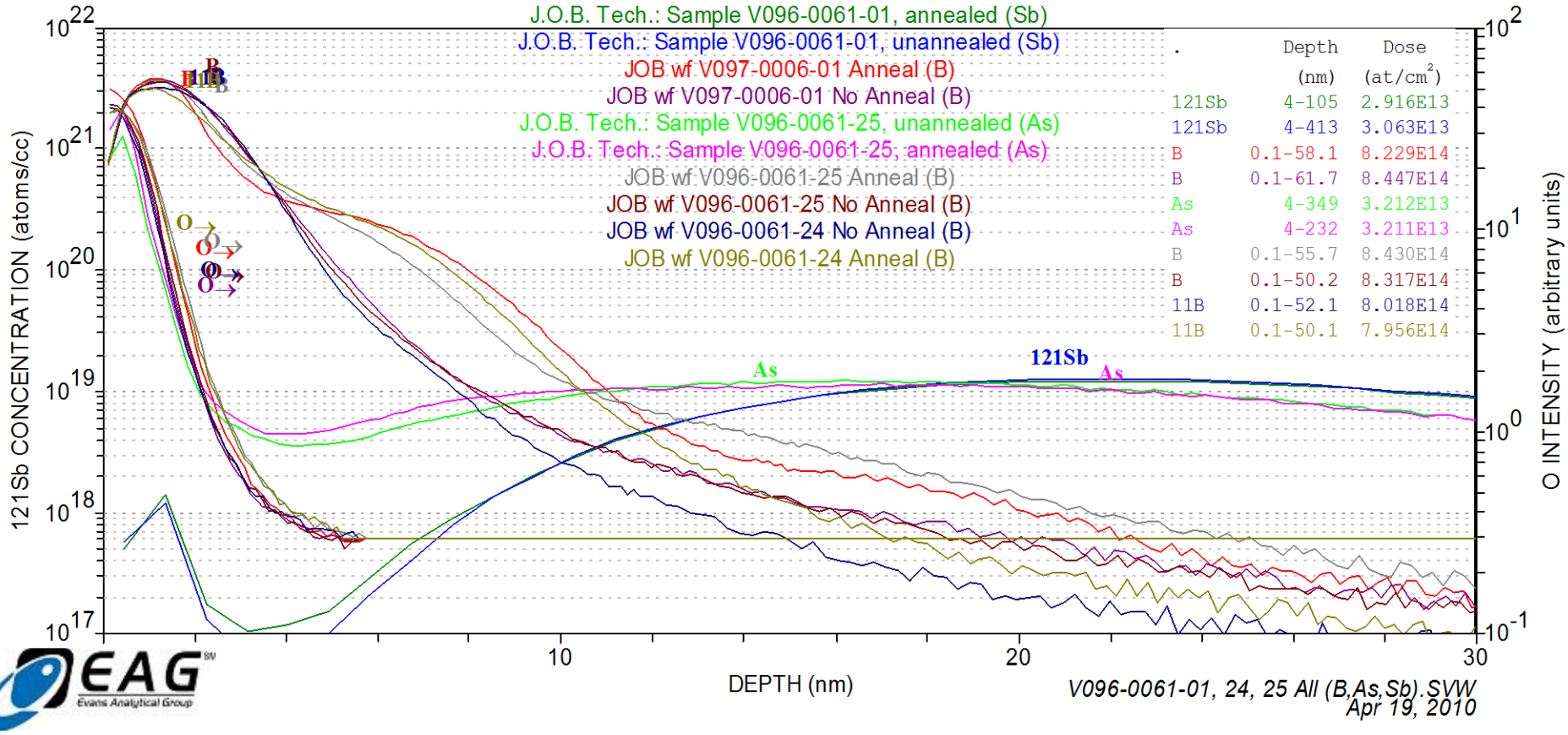


Laser Anneal Pattern

X-TEM Results For As-HALO & Sb-HALO Showing No Amorphization



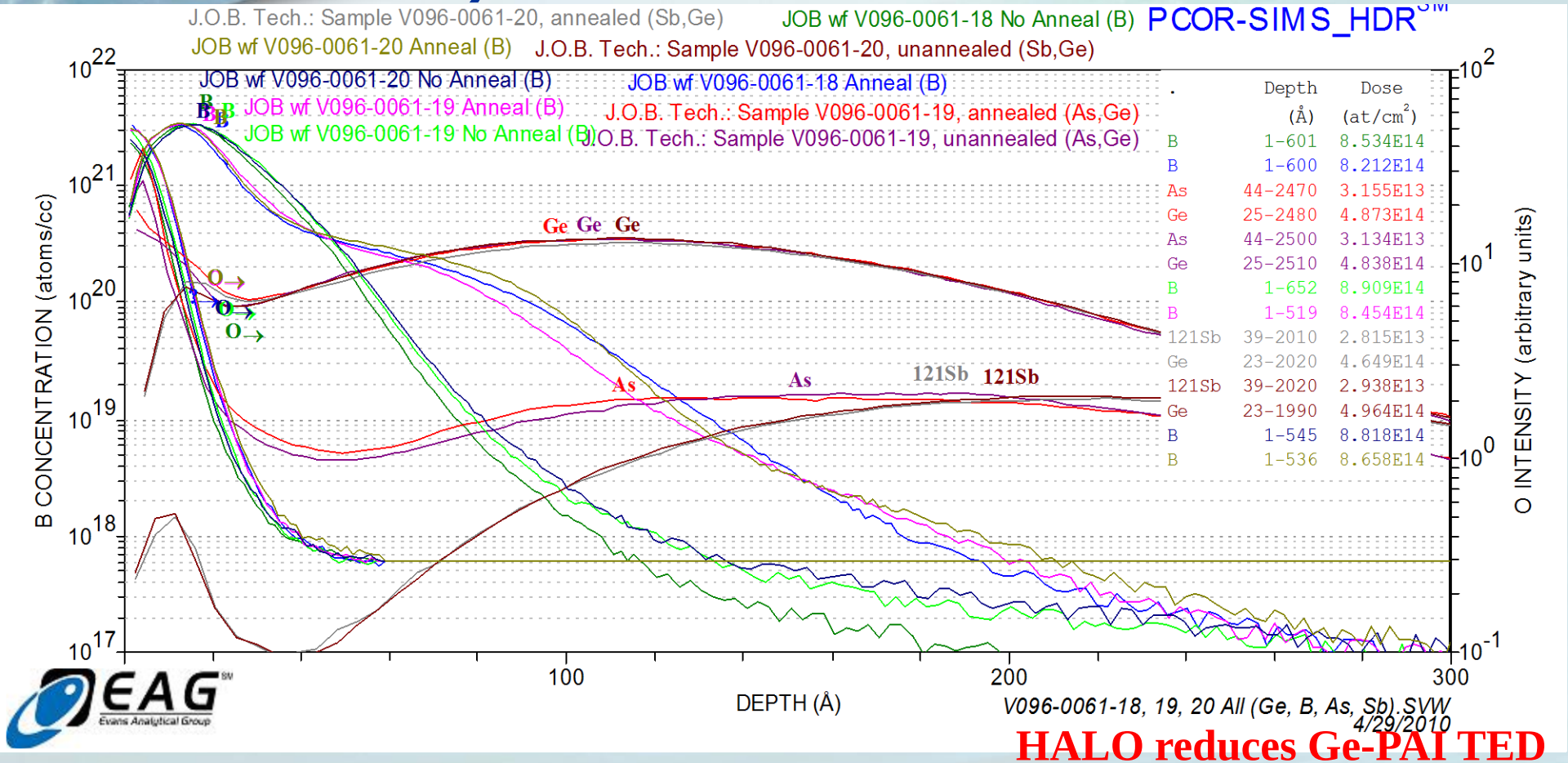
No PAI: B, As & Sb HALO



Condition	Native oxide	Xj	B-Diffusion
B	2.4nm	8.7nm	3.0nm
As-HALO	2.2nm	10.0nm	3.5nm
Sb-HALO	2.0nm	9.8nm	2.4nm

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Ge-PAI: B, As & Sb HALO



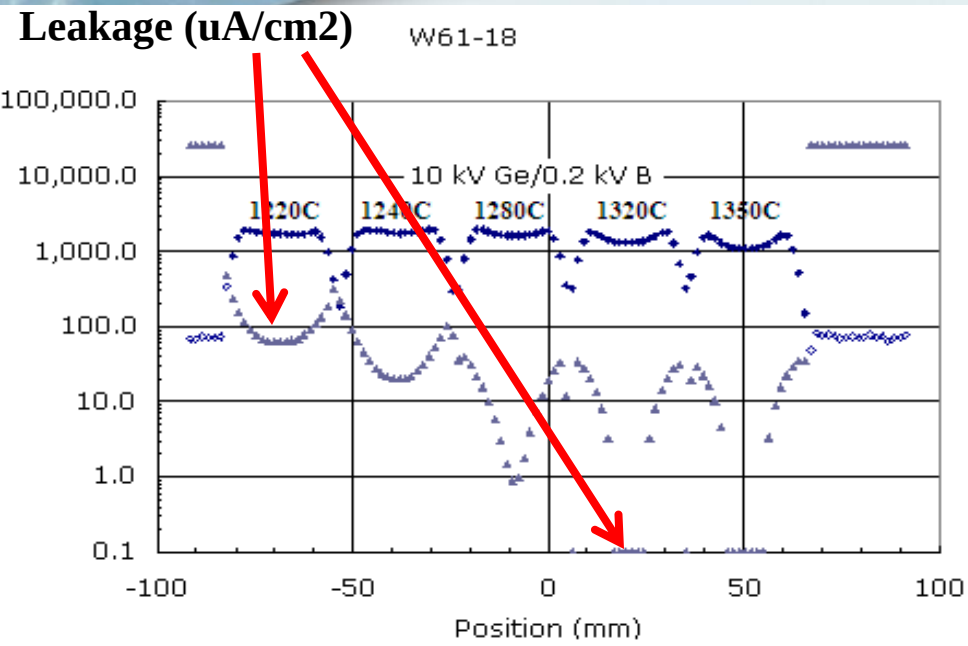
	Depth (Å)	Dose (at/cm²)
B	1-601	8.534E14
B	1-600	8.212E14
As	44-2470	3.155E13
Ge	25-2480	4.873E14
As	44-2500	3.134E13
Ge	25-2510	4.838E14
B	1-652	8.909E14
B	1-519	8.454E14
121Sb	39-2010	2.815E13
Ge	23-2020	4.649E14
121Sb	39-2020	2.938E13
Ge	23-1990	4.964E14
B	1-545	8.818E14
B	1-536	8.658E14

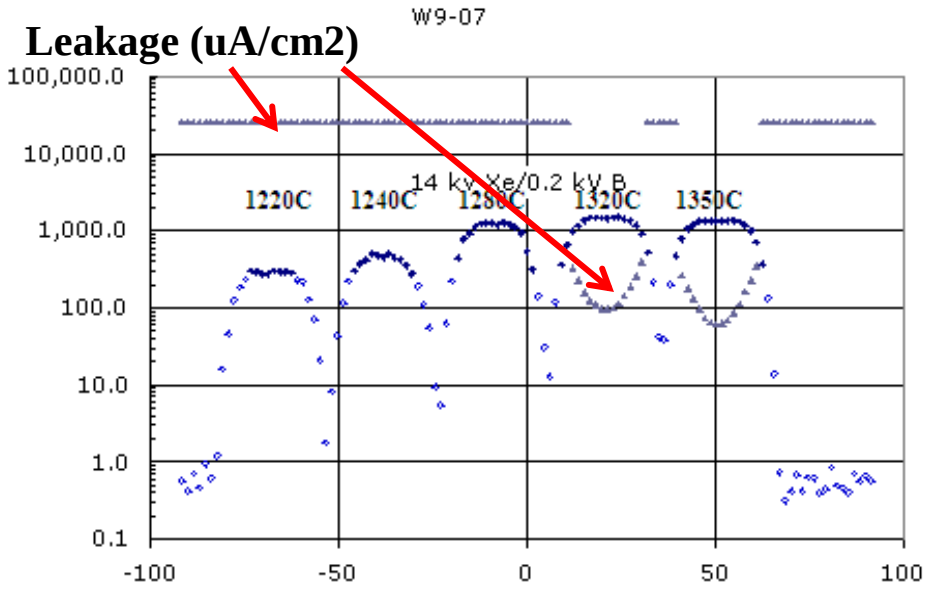
HALO reduces Ge-PAI TED

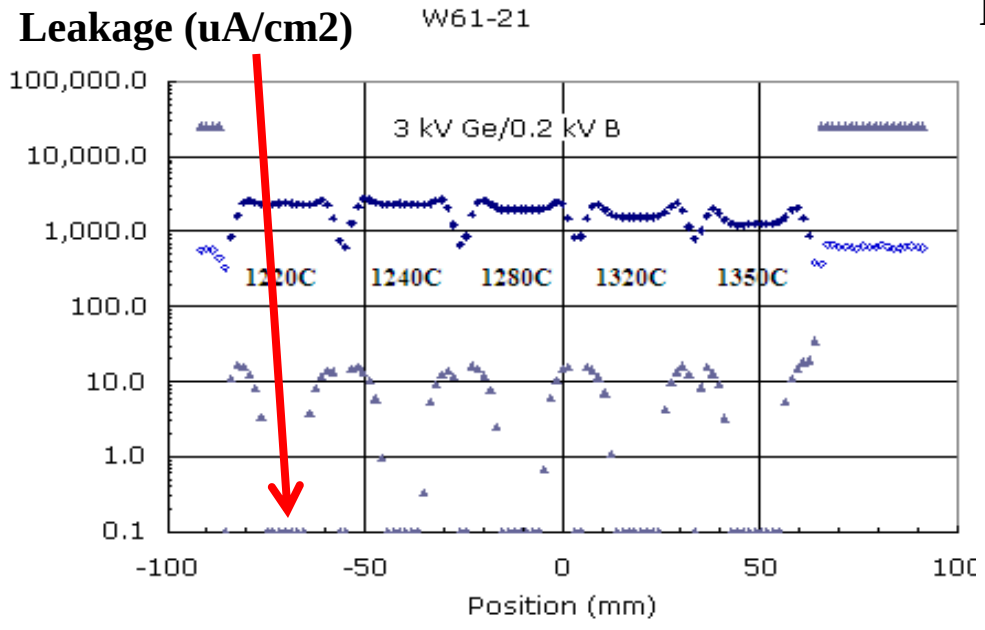
Condition	Native oxide	Xj	B Diffusion
B	1.9nm	8.3nm	6.1nm
As-HALO	2.2nm	9.0nm	5.0nm
Sb-HALO	2.1nm	8.5nm	5.5nm

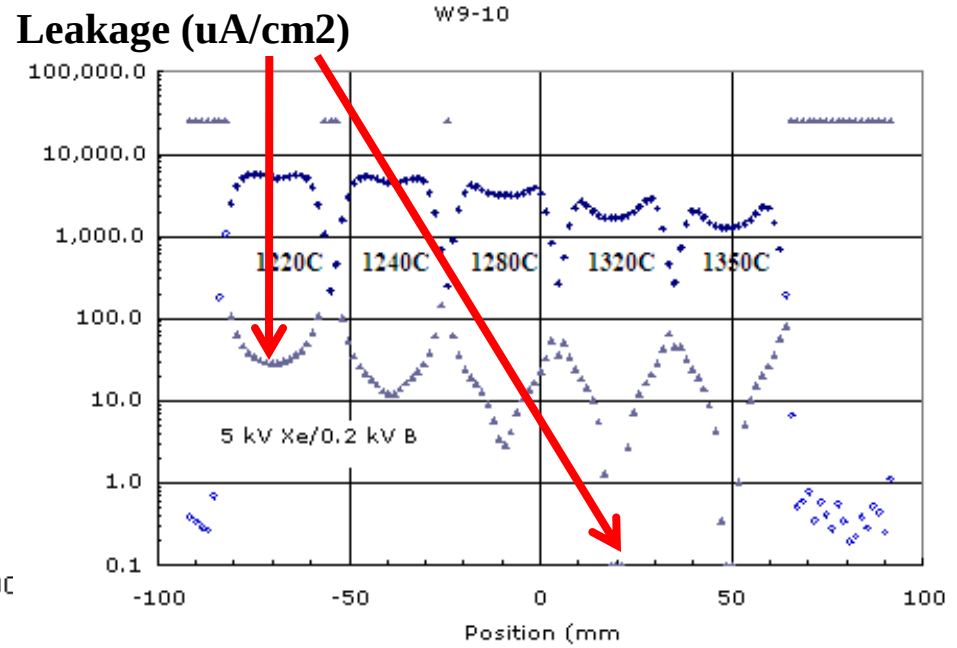
J.O.B. Technologies (Strategic Marketing, Sales & Technology)

No HALO Rs & Junction Leakage

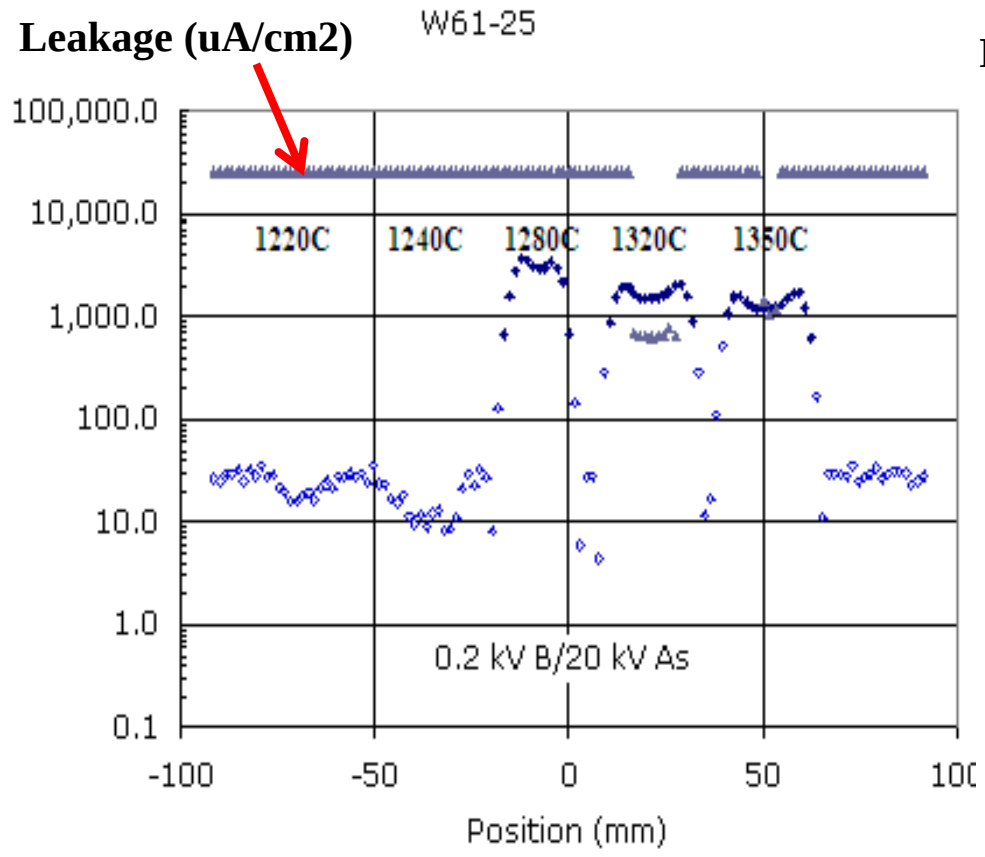


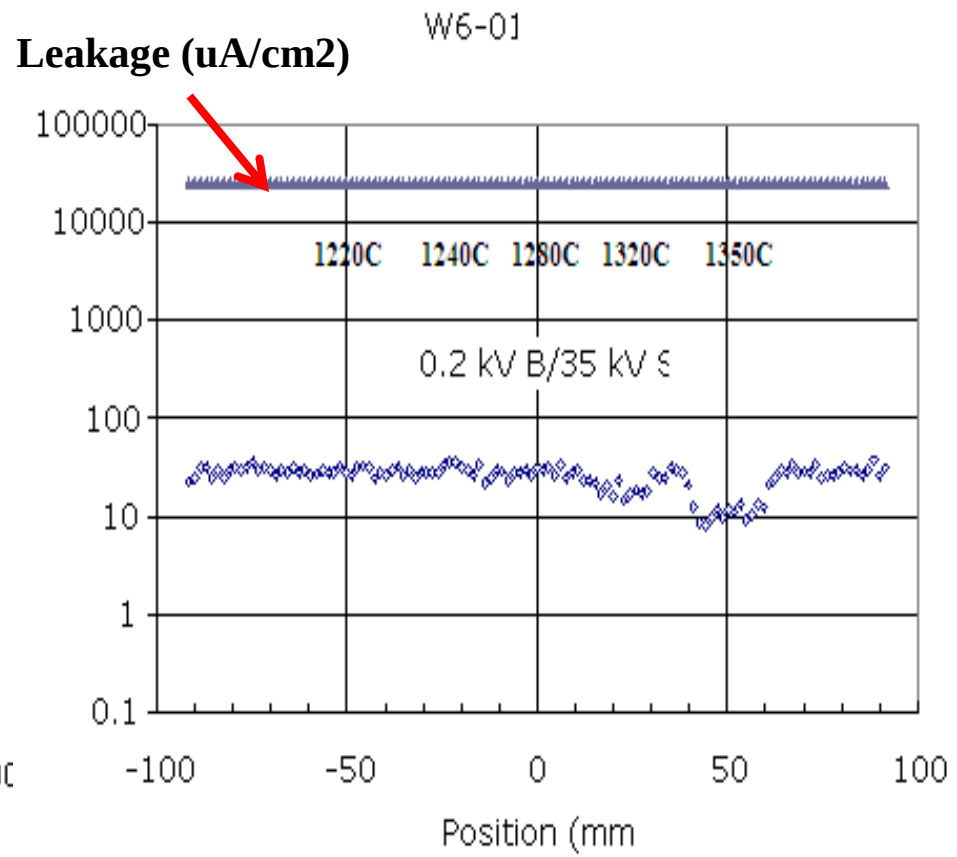






As & Sb HALO Rs & Junction Leakage





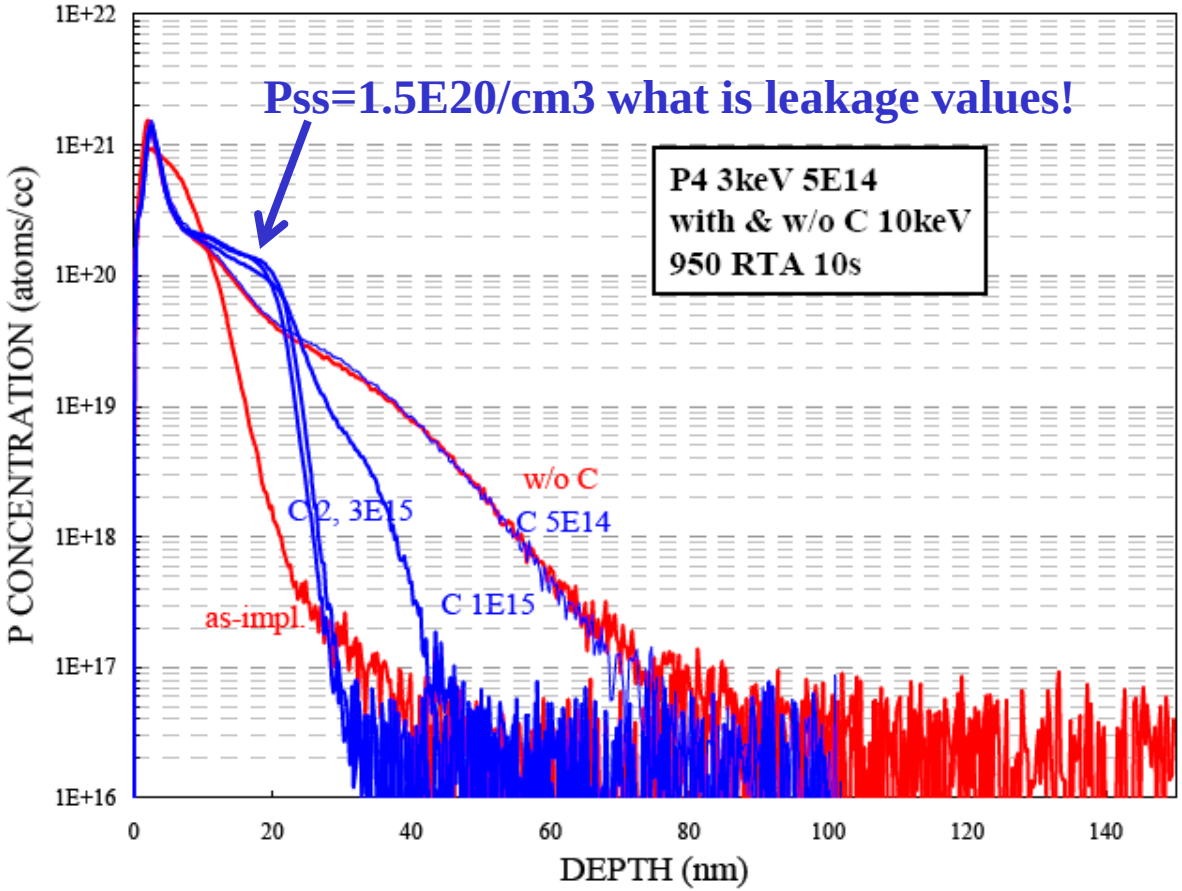


Fig. 5 shows P_4 profiles at equivalent 3keV@5E14/cm2 with and without C_7 at various dose @ equivalent 10keV after RTA 950°C 10sec, which were measured by SIMS.

Box-like profile for P when C dose increases between 1-2E15/cm2

Nagayama, Nissin, IWJT-2010 paper 3.4

Dopant Solid Solubility Limits In Silicon

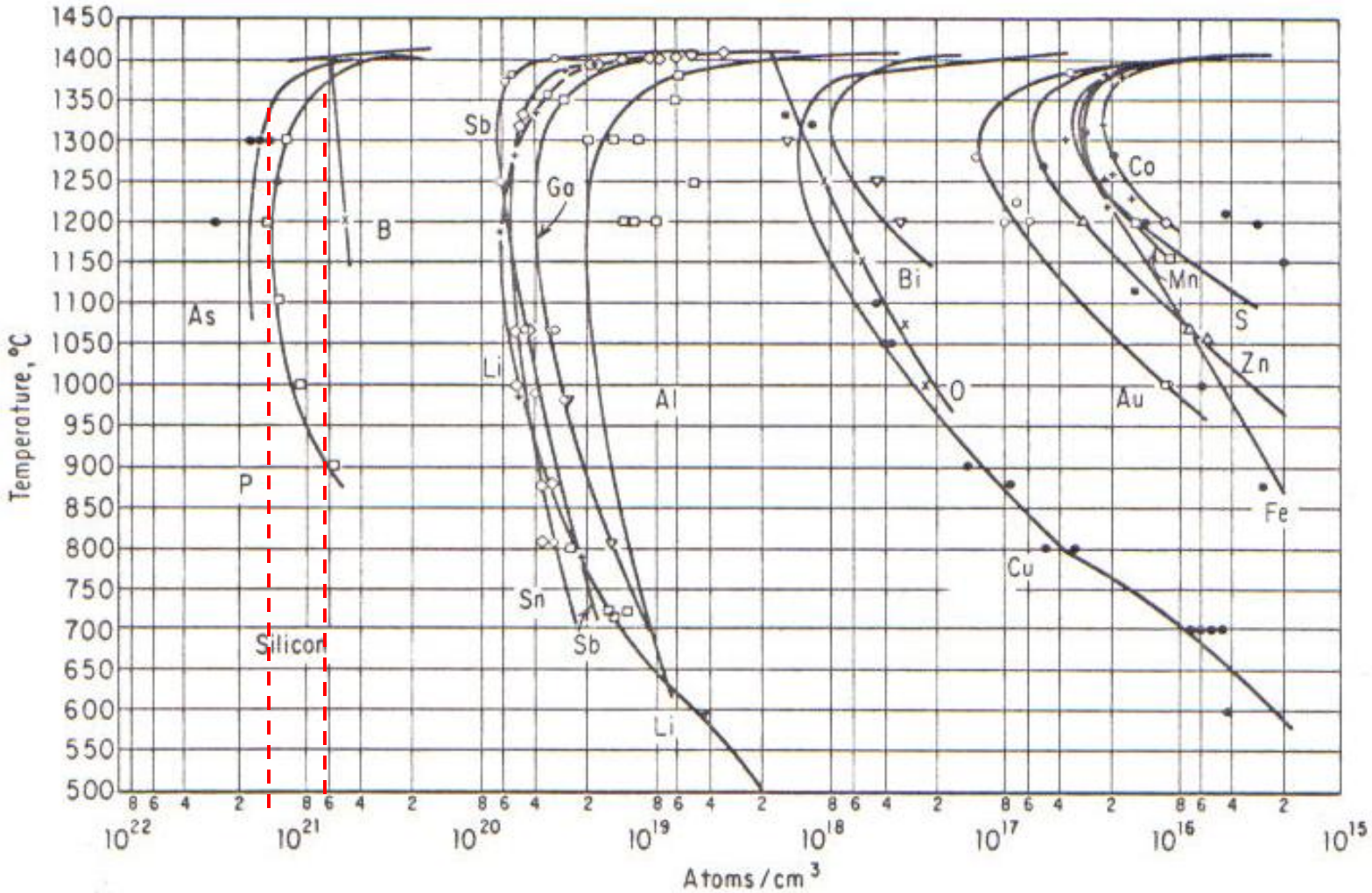


Fig. 11-50. Solid solubilities of impurity elements in silicon. (*From "Solid Solubilities of Impurity Elements in Germanium and Silicon" by F. A. Trumbore, Bell System Tech. J., vol. 39, pp. 205–233, 1960. Used with permission.*)

Higher n+ Phos. Dopant Activation >1.8E21/cm3!

How to get Pss=>1.8E21/cm3?
Compare 1350C to Melt (>1407C)

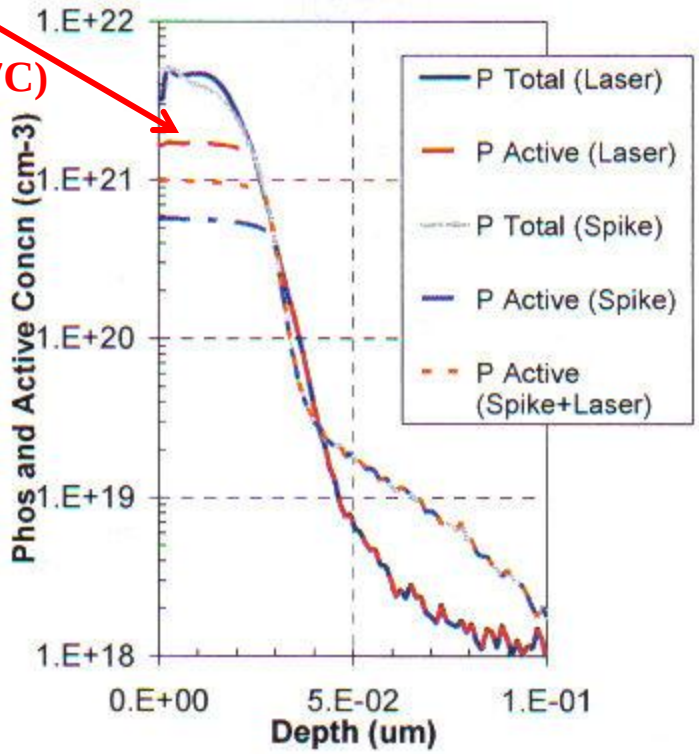
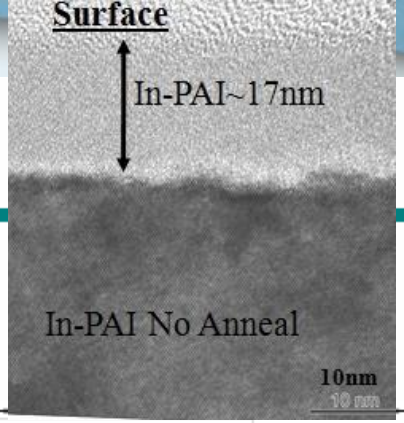


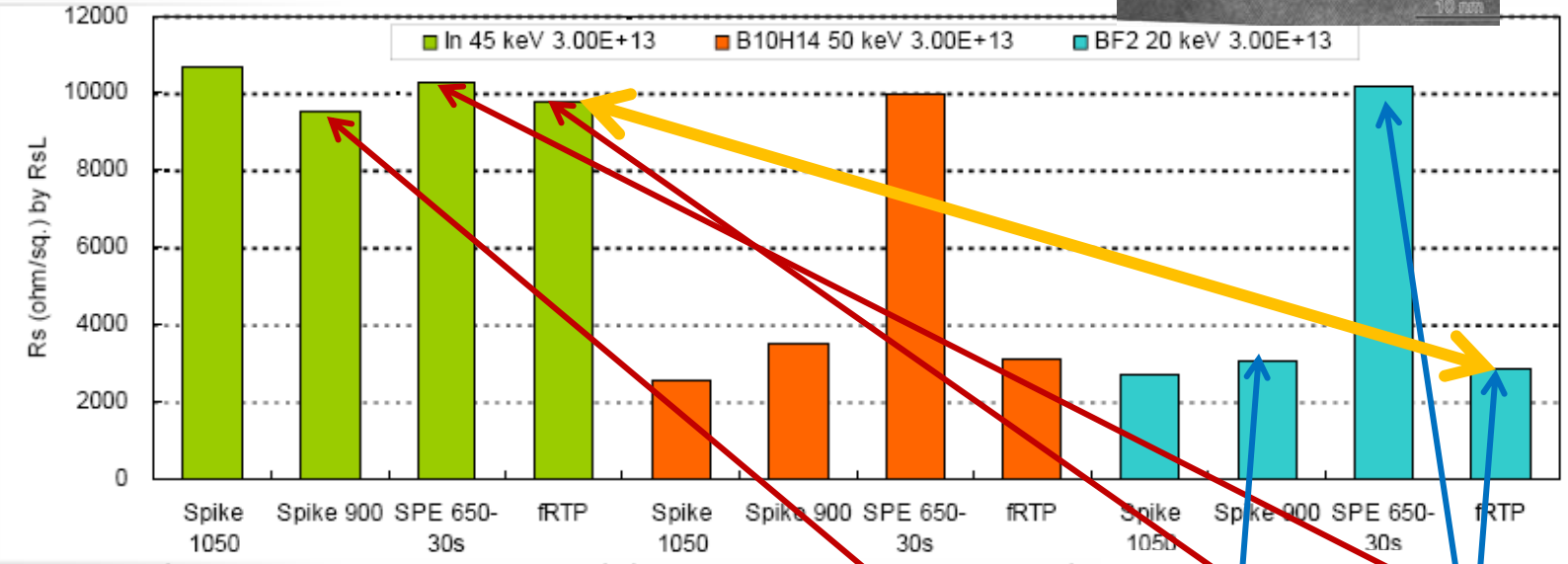
Figure 5: Chemical P from SIMS and active P from simulation matching of Hall data. Best activation was for laser annealing-induced solid phase regrowth. Laser also increased activation after 950C spike annealing.

H. Kennel et al., Intel, NIST meeting, March 2006

P-Halo (In, B10, BF2)

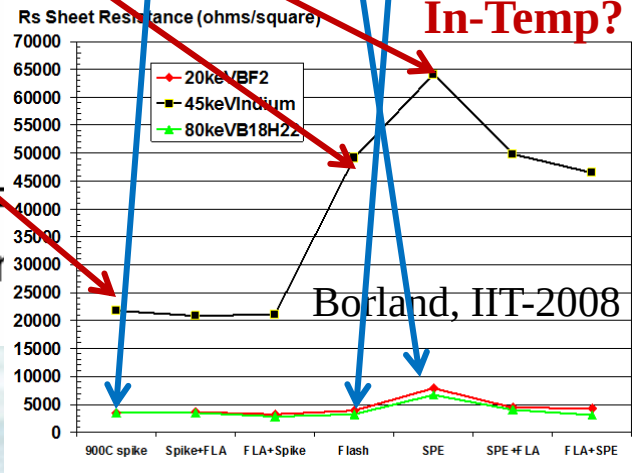


Rs dependent on anneal conditions and ion species



In 45k 3e13 B10 50k 3e13

In-Temp?



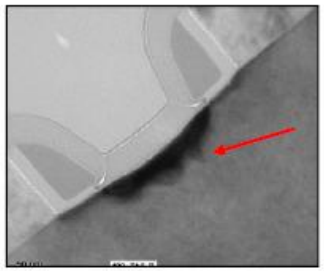
Borland, IIT-2008

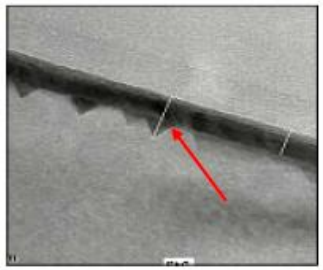
Activation as the halo dopant is not enough by SPE
Indium is independent on the anneal condition ⇒ I
as the halo by SPER

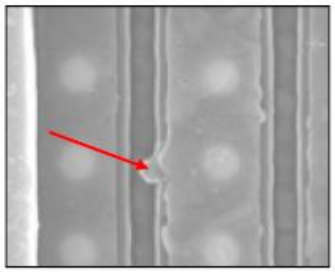
Mineji et al., NEC/JOB/Nissin, IWJT-2007

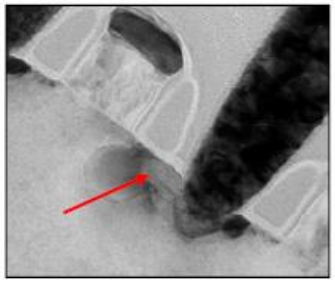
Motivation – NiSi Defect Reduction

- NiSi spiking (PMOS)
- NiSi piping (NMOS)









- The NiSi spiking defects can be well controlled by surface treatment condition, but the piping defect is tough, mainly correlated to implant species, thermal anneal and substrate dislocation/stress.

NiSi Piping Suppression Approaches

- Pre-amorphous implant (PAI)
- Pre-clean by "fluorine" dry etching
- Substrate with dopant (ex: F, C)
- Nickel alloy (ex:Pt)
- Annealing programs

Ni Silicide Improvements With By Shallow Room Temp Si-PAI, Xe-PAI or Cold C-PAI

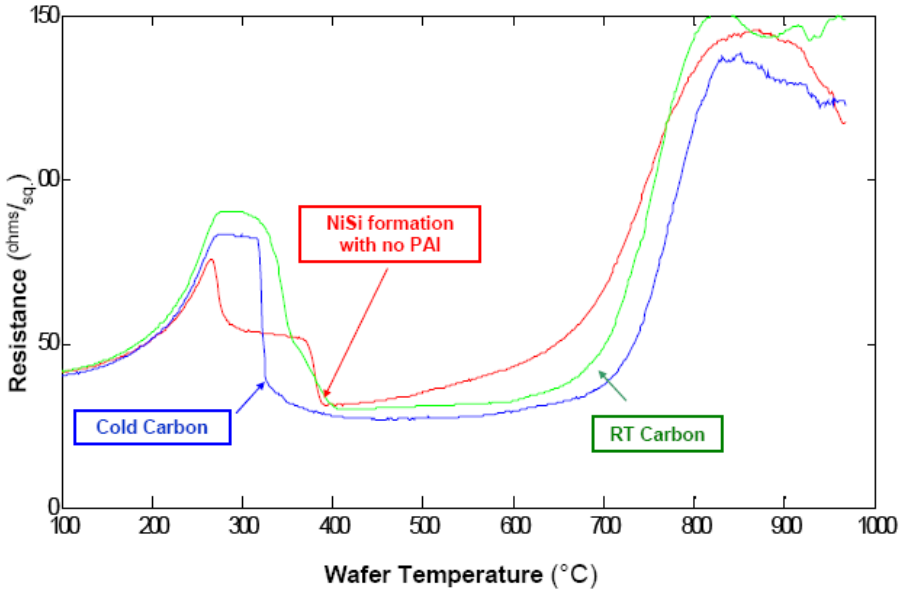


FIGURE 8. Structured wafers results for silicide resistance when preceded by a) no implant (red), b) a room temperature 1keV C 1e15 implant (green), and c) the same C implant at -100°C (blue)

T. Renau, VSEA, IWJT-2010 paper K1

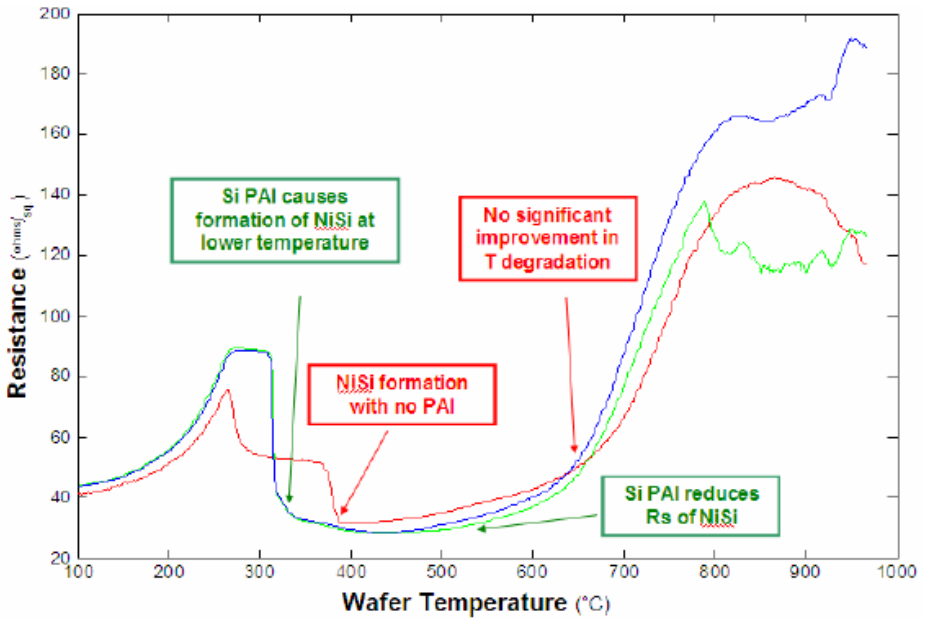


Figure 5. Silicon pre-amorphization implant lowers the silicide transformation temperature as measured by in-situ sheet resistance measurements.

S. Deshpande, IBM, IWJT-2010 paper 4.1

Outline

- Introduction
  - Technology Roadmap Options
- USJ Technology
  - p+ USJ 22nm node and beyond
  - n+ USJ 22nm node and beyond
- **Strain Technology**
  - **pMOS 22nm node and beyond**
  - **nMOS 22nm node and beyond**
- Next

Heated 300C HALO Implantation

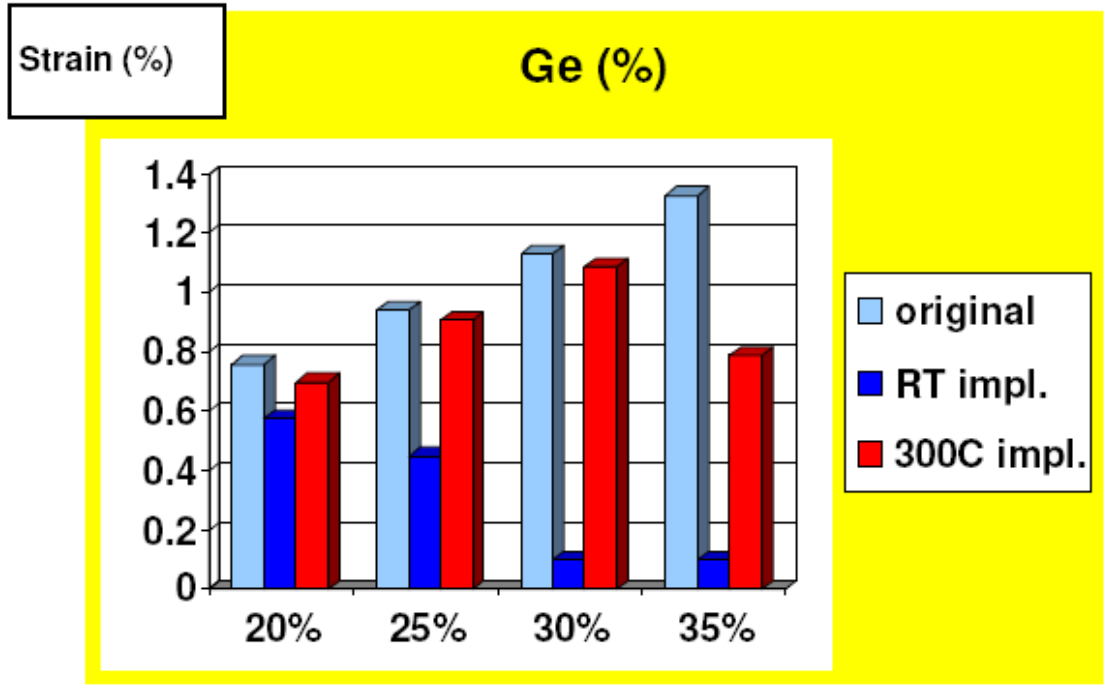


Figure 2. Retained Strain as function of Ge% for RT and 300C As+ halo implant. Process conditions were RTA anneal @ 1080C for 1s and Halo-Implant of As+ @ 2.0E13cm-2, 50 keV and 30 degree tilt.

Issue for eSiGe-SDE or disposable spacer process flow!

S. Deshpande, IBM, IWJT-2010 paper 4.1

eSiGe Strain Relaxation By p+ SDE Implant

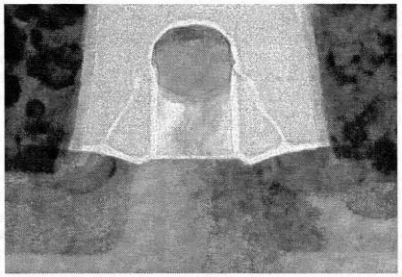


Figure 1: TEM cross section of a diffusionless 38 nm SOI p-MOSFET with the eSiGe stress technique.

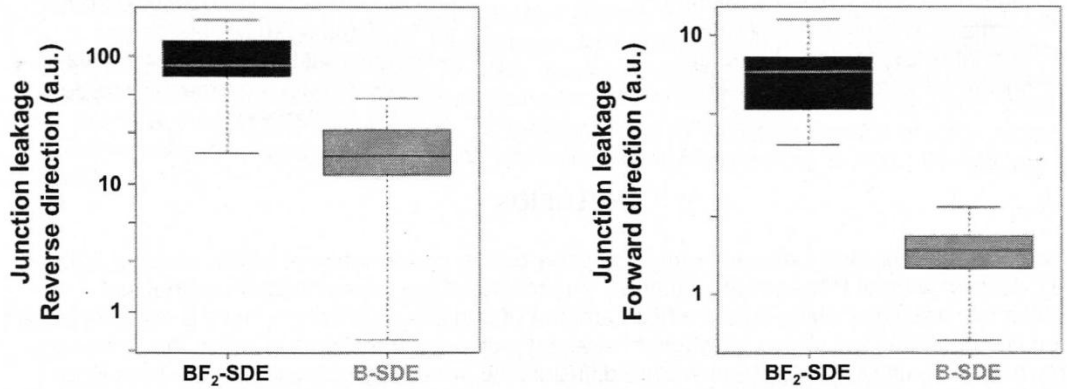


Figure 5: Junction leakage in reverse (left) and forward (right) direction of eSiGe strained p-MOSFET

AMD/Dresden, Insights-2009

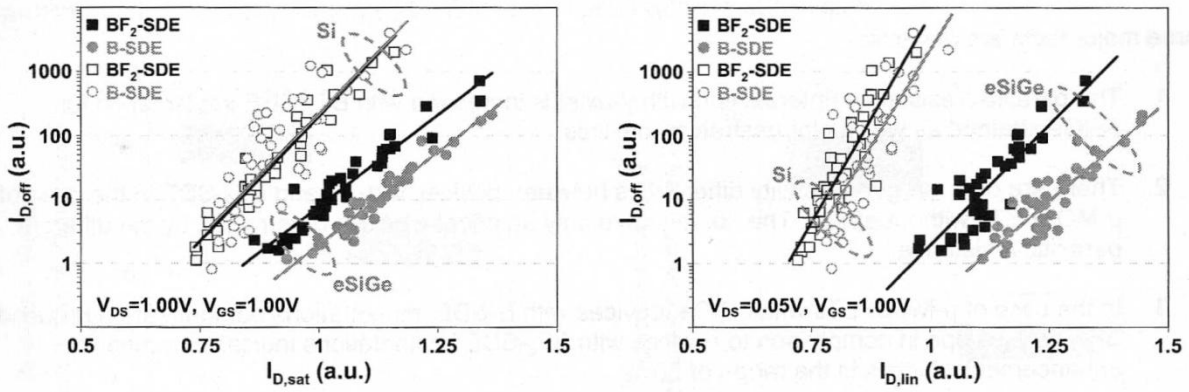
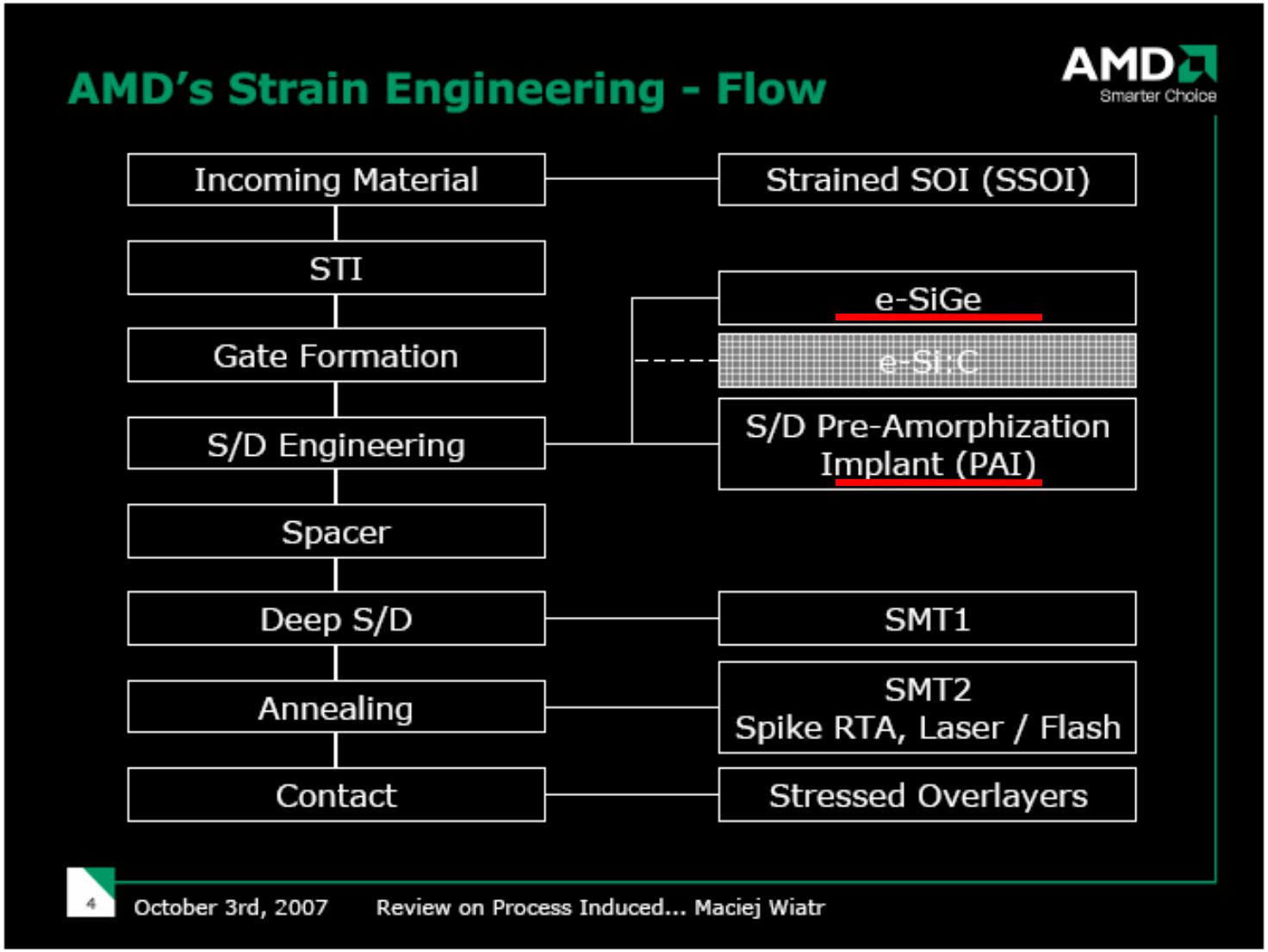


Figure 2: $I_{D,on}/I_{D,off}$ characteristics of p-MOSFET devices with different SDE implantations into Si (open symbols) and eSiGe (filled symbols) S/D areas (left: saturation drain current $I_{D,sat}$; right: linear drain current $I_{D,lin}$).

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

AMD RTP 2007 Paper



April 2010 ECS Meeting Vancouver, Canada

Issue for disposable spacer process flow!

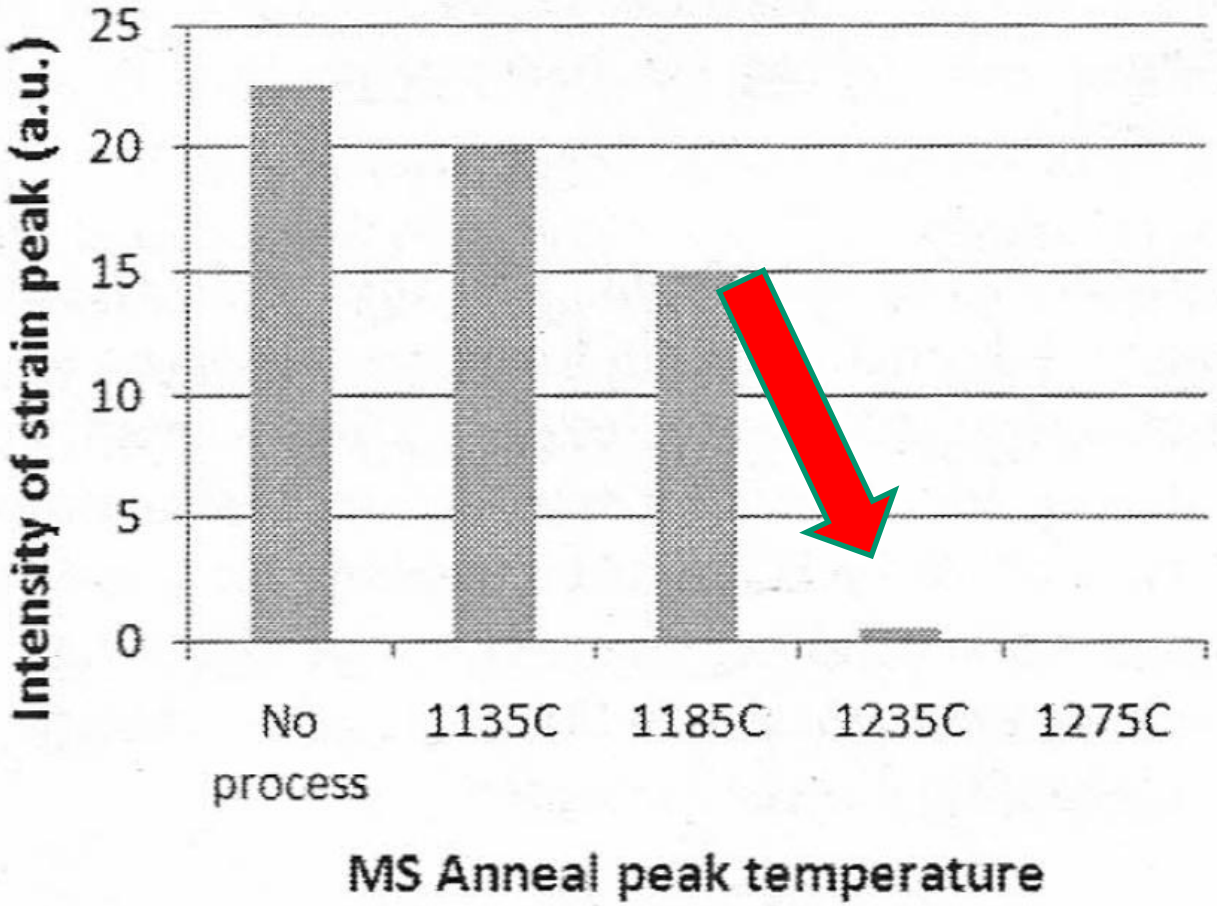


Fig 3: Ge relaxation characteristics with millisecond anneals

S. Govindaraju et al., Intel, ECS Transactions, vol. 28, no.1, p.81, 2010.

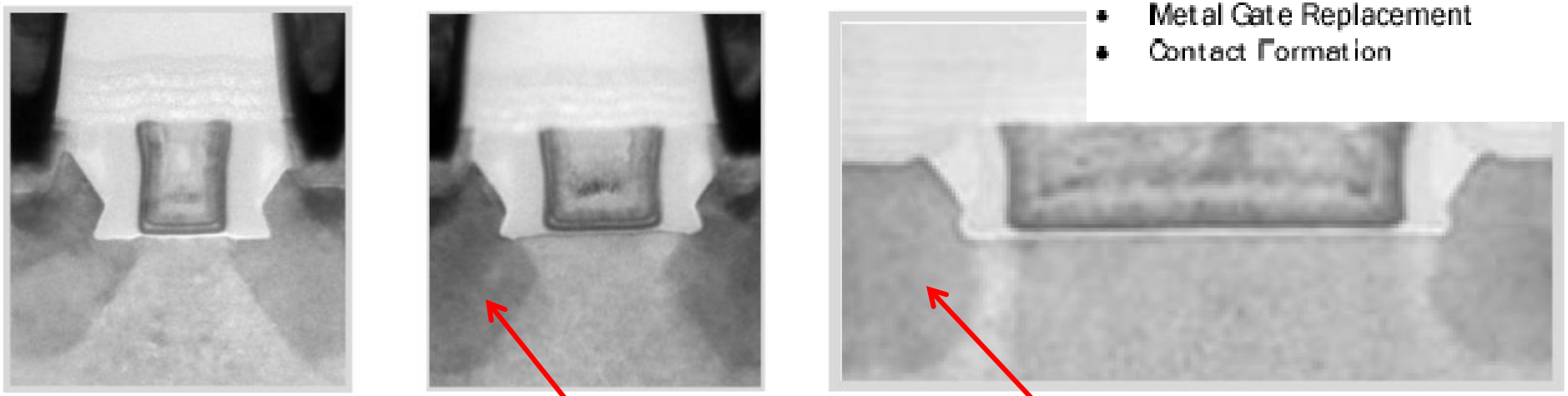
Intel's 32nm Node Low Power RF CMOS SOC Technology

- Isolation (wells, Vt)
- *Oxide I/O gate growth*
- *Oxide I/O gate patterning*
- Dielectric growth
- Poly-Si dep
- Poly-Si patterning
- Logic S/D extension- HP/LP
- *ULP S/D extension*
- *I/O S/D extension*
- Spacer dep/patterning
- S/D formation
- Poly-Si Gate Removal
- Metal Gate Replacement
- Contact Formation

Logic Transistor (HP or SP)

Low Power Transistor (LP)

(1.8



Looks like 45nm eSiGe

Looks like 65nm eSiGe

Fig. 1 Triple transistor architecture.

Intel, VLSI Sym 2010, paper 13.2

April 2010 ECS Meeting Vancouver, Canada

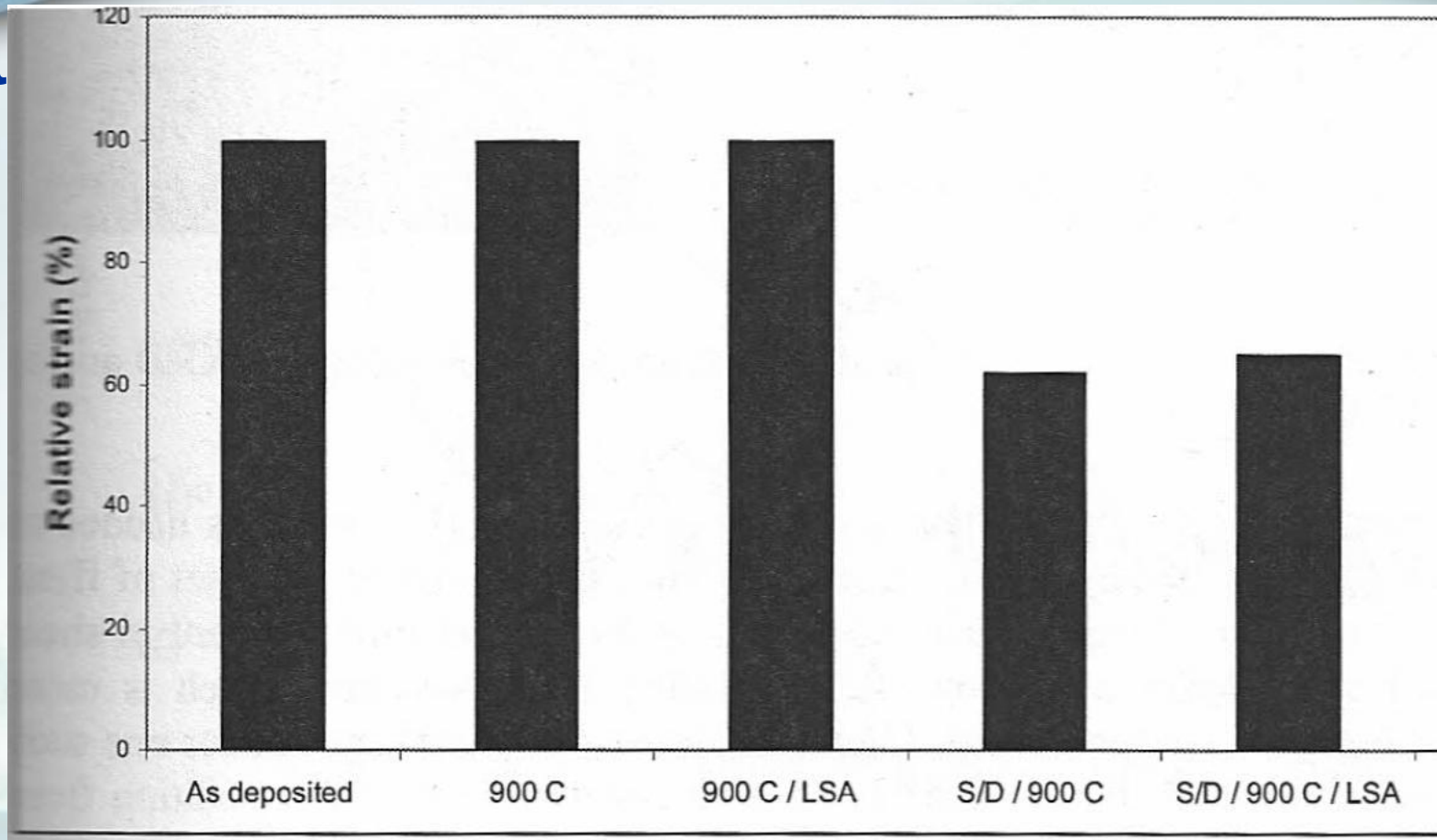


Figure 8. μXRD analysis of strain in a Si:C film after implant and anneals

Dube et al., IBM/GF, ECS Transactions, vol.28, no.1, p.63, 2010.

In-situ SiCP=3E20/cm3 at C=1.7% Also, 1-2wph!

22nm Node n+ SiC Stressor Using Deep PAI+C_7H_7+P4 With Laser Annealing

IEEE/RTP-2009

John Borland[1], Masayasu Tanjyo[2], Nariaki Hamamoto[2], Tsutomu Nagayama[2], Shankar Muthukrishnan[3], Jeremy Zelenko[3], Iad Mirshad[4], Walt Johnson[4], Temel Buyuklimanli[5], Steve Robie[5], Hiroshi Itokawa[6], Ichiro Mizushima[6] and Kyoichi Suguro[6]

1) J.O.B. Technologies, Aiea, HI

2) Nissin Ion Equipment, Kyoto, Japan

3) Applied Materials, Sunnyvale, CA

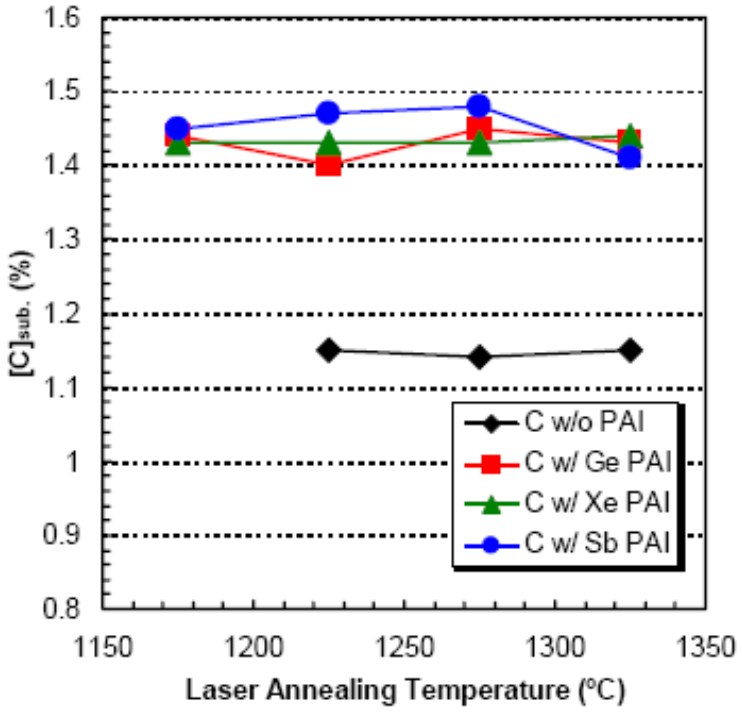
4) KLA-Tencor, San Jose, CA

5) EAG, Sunnyvale, CA

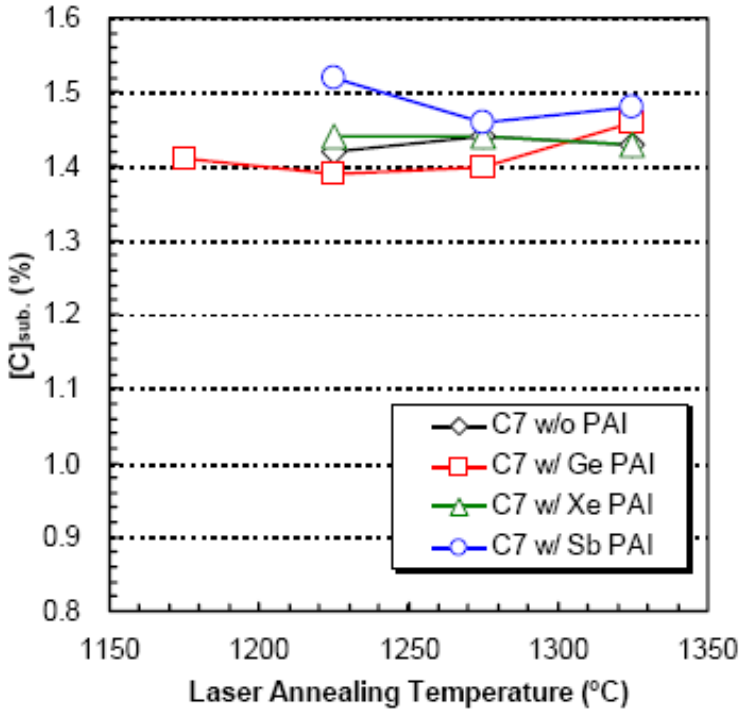
6) Toshiba Corporation, Yokohama, Japan

Substitutionally Incorporated Carbon Concentration ($[C]_{sub}$)

Monomer C + P4

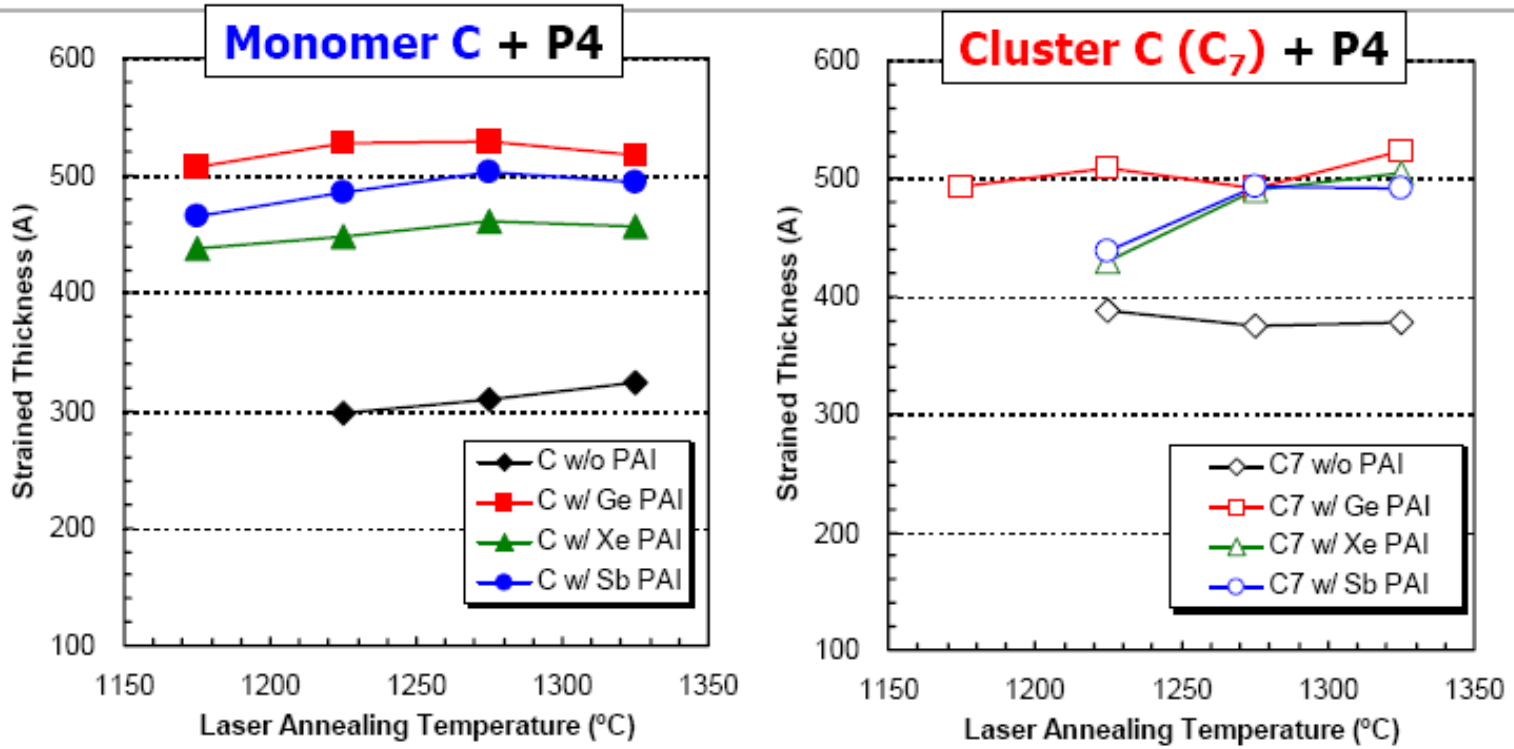


Cluster C (C_7) + P4



- Monomer C^+: without PAI ➔ low $[C]_{sub}$ ➔ P4 effect on [C]sub is small
- Cluster C_7^+: High $[C]_{sub}$ independent on PAI condition
- There is no clear dependence on Laser anneal temperature

Strained Thickness



- PAI causes thicker strained layer. Ge PAI is the thickest.
- In the case without PAI, strained layer for C_7^+ is thicker than that for monomer C^+.
- The higher temperature Laser anneal, the thicker strained layer.
- In the case of C_7^+, Xe PAI and Sb PAI show clear Laser anneal temperature dependence of the strained layer thickness

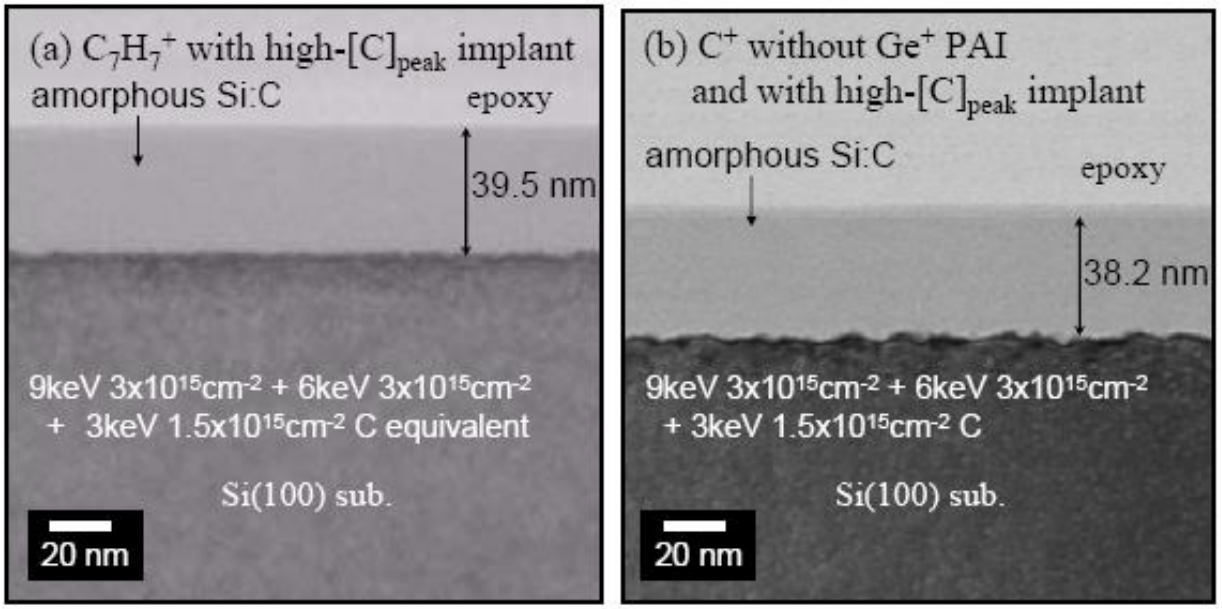
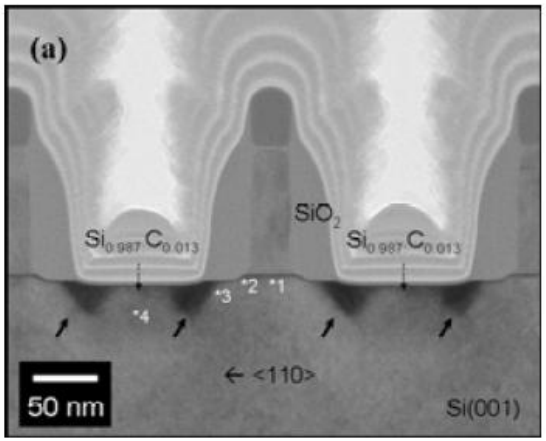


Figure 2 Cross-sectional TEM images of as-implanted sample with high $[C]_{peak}$: (a) $C_7H_7^+$ implant, and (b) C^+ implant.

Keep Csub to <1.3% and use 850C SPE+MSA

Itokawa, Toshiba/IBM, IWJT-2010 papers 3.2 & 6.14



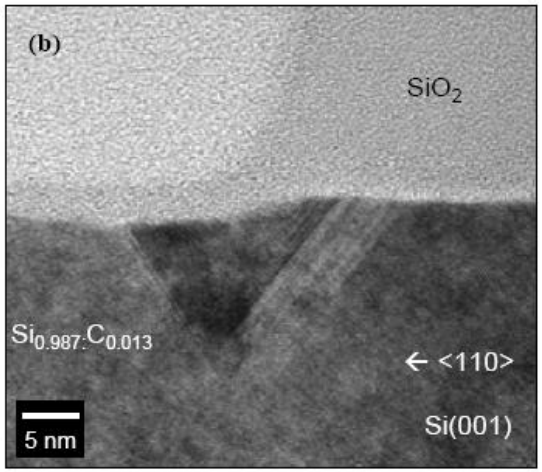


Figure 7. Cross-sectional TEM images of e-$Si_{0.987}$:$C_{0.013}$ S/D stressor in 45nm bulk nMOSFETs with <110> channel direction was formed by cryo-implantation of C^+ into amorphized Si layer and regrowth with laser annealing at 1300 °C. **(a)** Low-magnification and **(b)** high-magnification at gate-edge.

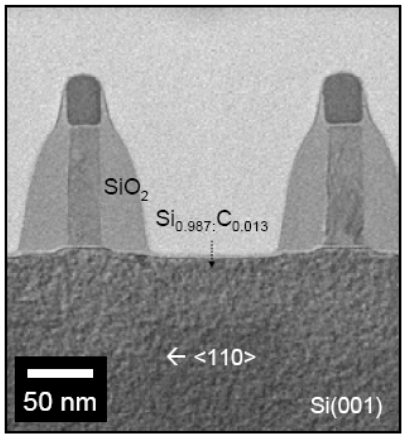


Figure 10. Cross-sectional TEM image of e-$Si_{0.987}$:$C_{0.013}$ S/D stressor in 45nm bulk nMOSFETs with <110> channel direction was formed by cryo-implantation of C^+ into amorphized Si layer and regrowth with laser annealing at 1300 °C combined with SPE annealing at 850 °C for 40 s.

OK to have 1% C in channel under the gate stack (mid-5^{2} E19/cm3)?

SUMMARY

- 22nm Node (2011-2012)
  - Planar Bulk CMOS by Intel & IBM/Alliance Foundry
  - Planar PD-SOI by IBM/Alliance
  - USJ <10nm using MSA+spike/RTA diffusion-less annealing
    - p+(B, B_{10} or $B_{18/36}$)
    - n+(As or P+C)
  - Channel mobility enhancement
    - pMOS: eSiGe or SiGe-channel
    - nMOS: eSiC by Epi or C+P implant
- 15nm Node (2013-2015) & 11nm Node (2015-2017)
  - Planar CMOS:
    - Hybrid bulk and localized FD-SOI with back-gate (Intel & IBM/Alliance Foundry)
    - FD-SOI with back-gate: IBM/Alliance
  - FinFET CMOS?