

Recent Advances in Flexibly Shaped Pulse Flash Annealing - FSP FLA

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Agenda

- **DNS Flash Annealing Overview**
 - 4 generations of FLA
- **mS Annealing Challenges**
- **Flexibly Shaped Pulse Flash Annealing (FSP FLA) of HikMG Structures (SELETE)**
 - Maximizing Mobility
 - Minimizing BTI Degradation
 - Maximizing Device Performance
- **Mitigating mS Anneal Induced Misalignment (Toshiba)**
- **Summary**

Annealing History

Anneal Technology	Timing	Market Leader
Horizontal Furnace	Hour	SVGi, Bruce, TEL
Vertical FR Furnace	< Hour	TEL, Hitachi-Kokusai
RTP	Minute	AG, AST, Peak ...
Spike RTP	Second	AMAT
FLA	mS	DNS
LSA	μ S	Ultratech
Melt Laser	nS	Sopra (XeCl Excimer)

FLA Configurations

Fixed Pulse – Hot Plate



Programmable Pulse Hot Plate Assist



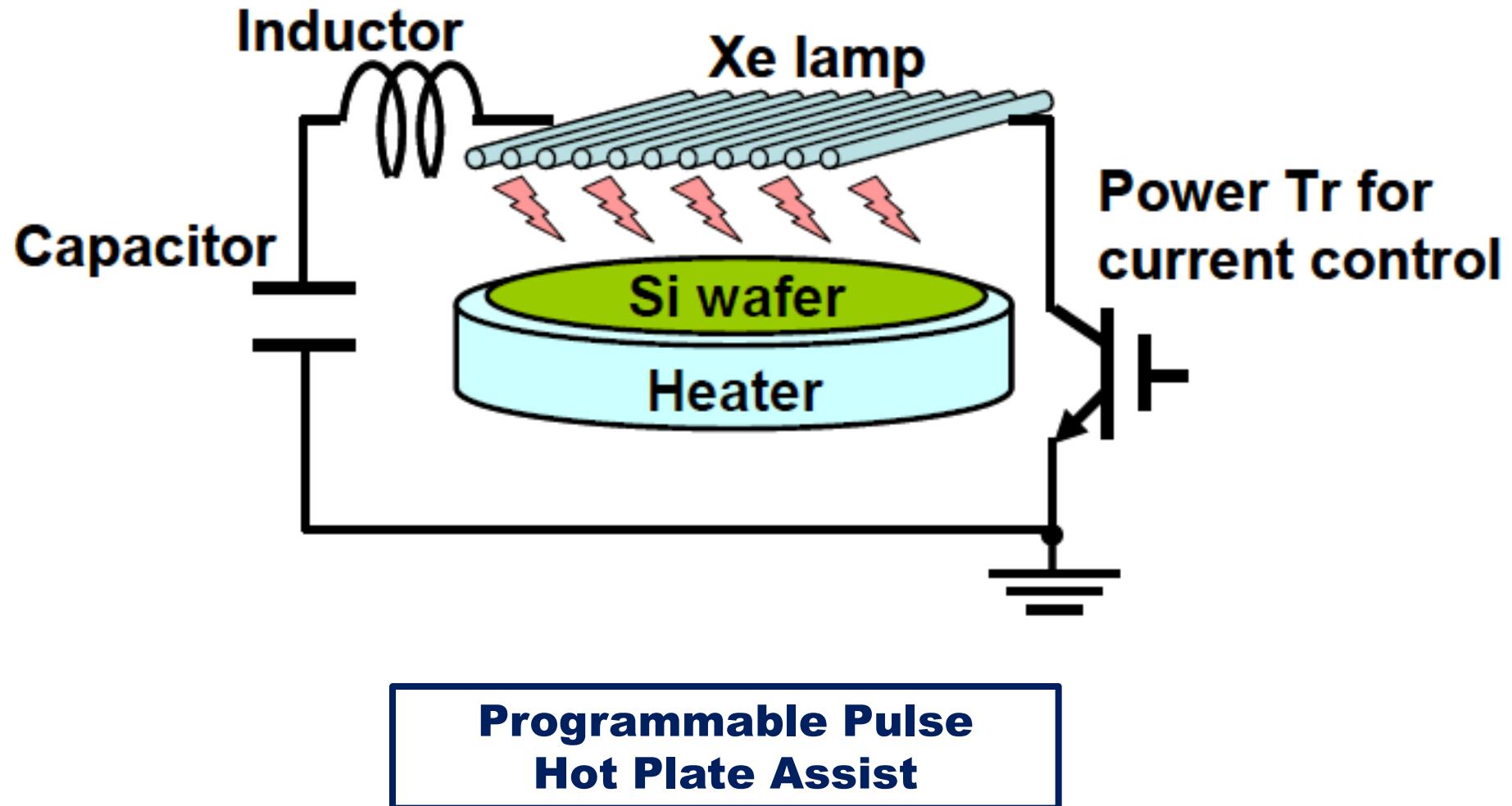
Fixed Pulse – Lamp Assist



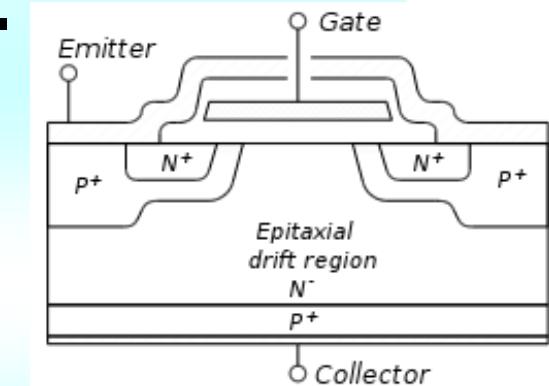
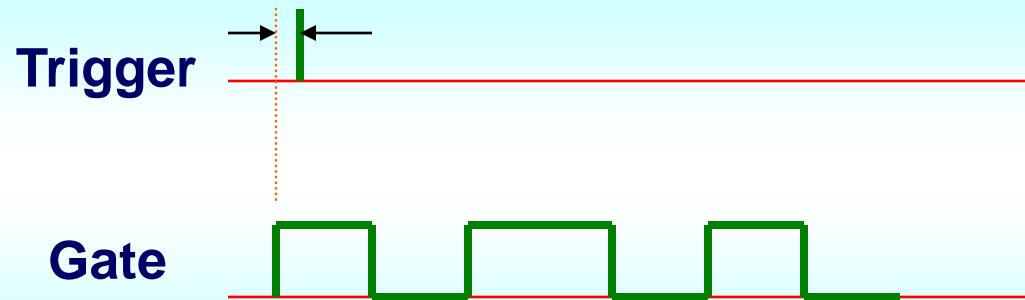
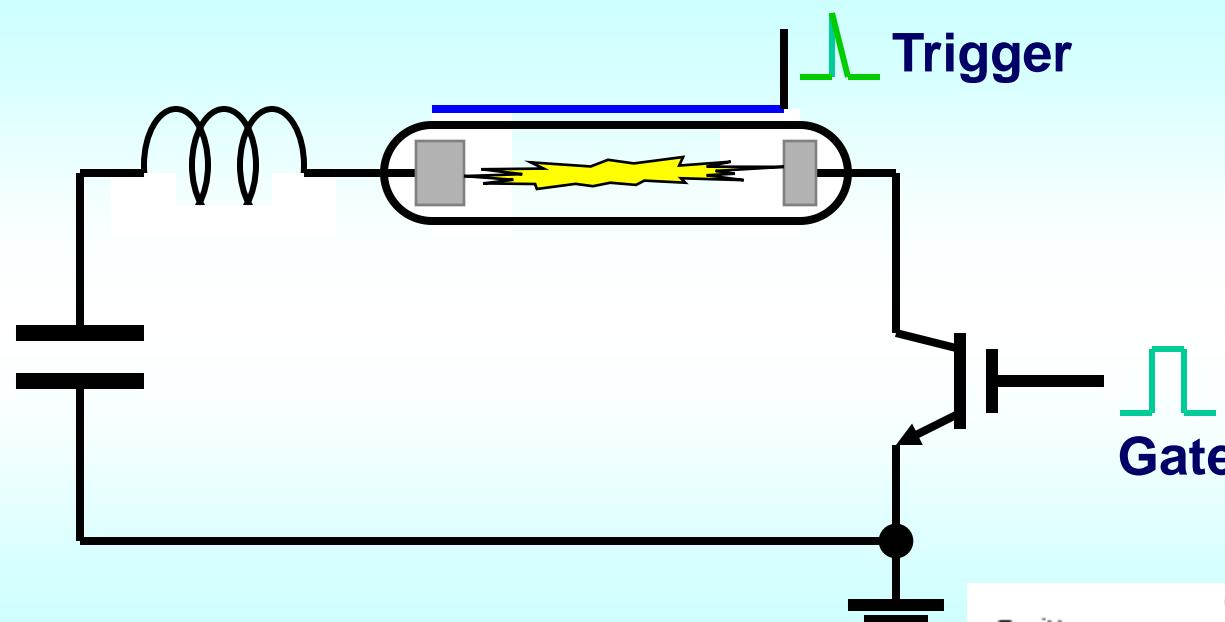
Programmable Pulse Lamp Assist



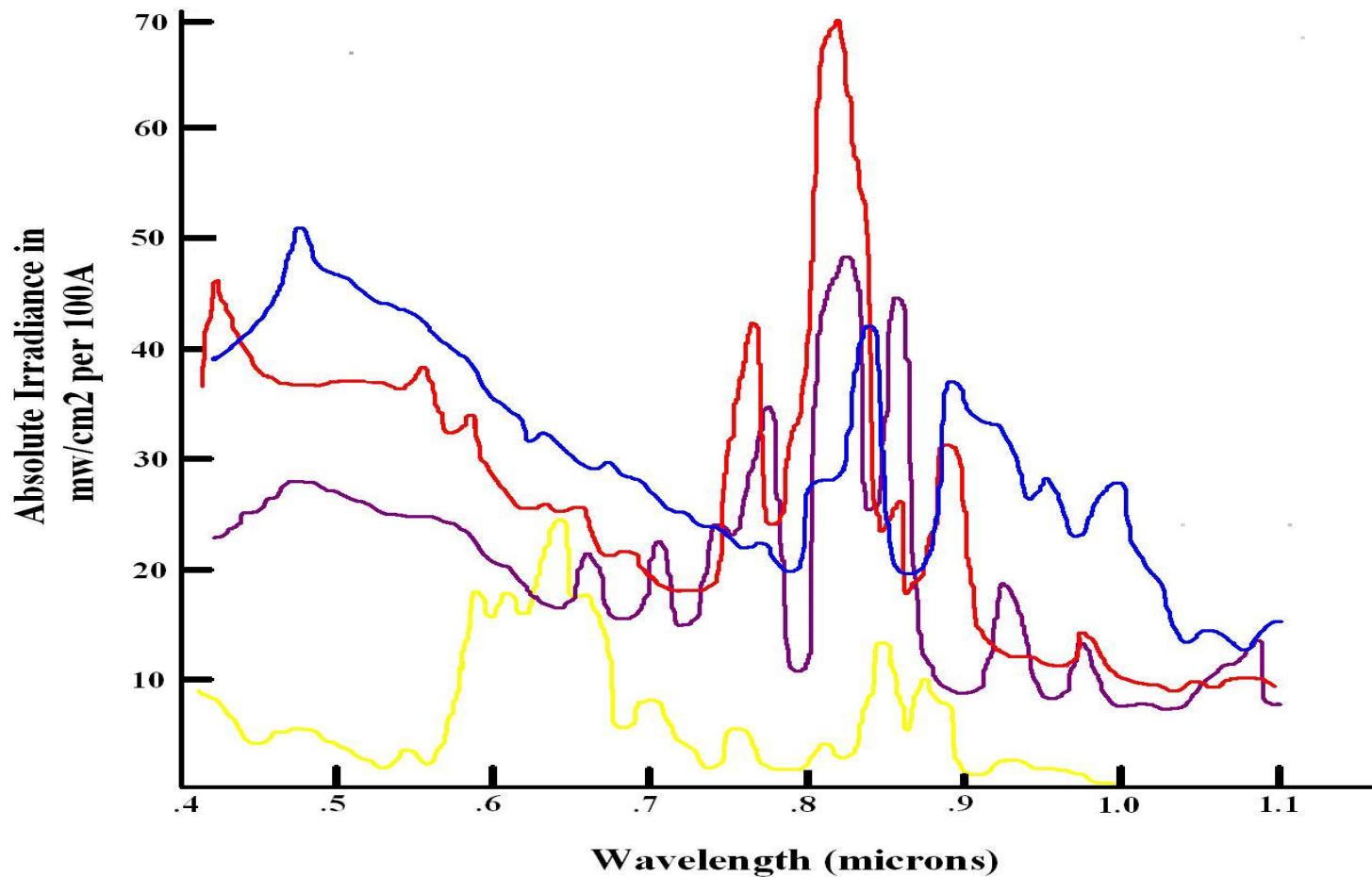
FSP-FLA Schematic - SSA



Pulse Width Control with IGBT & Chop



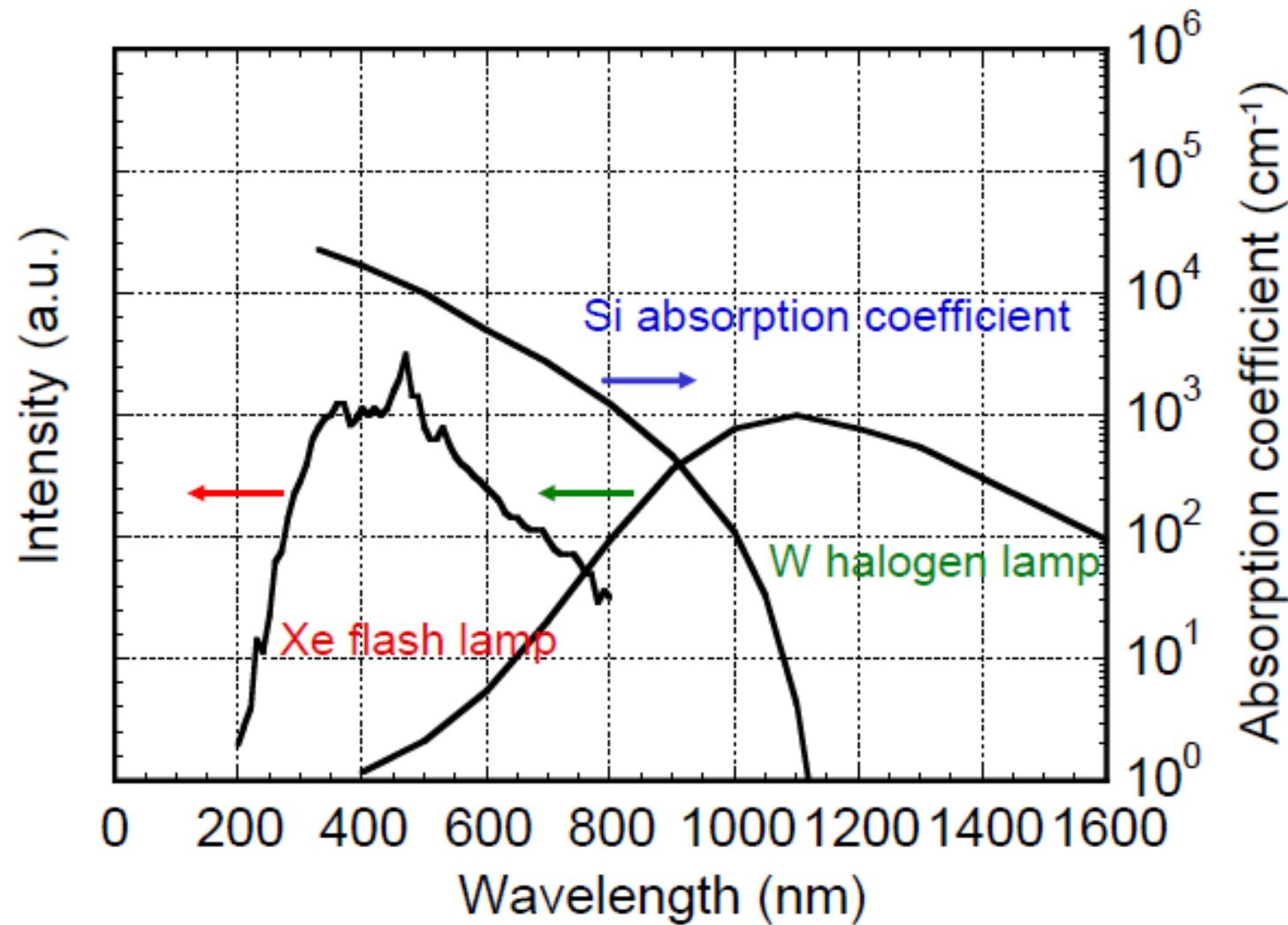
Rare Gas Flash Lamp Spectrum



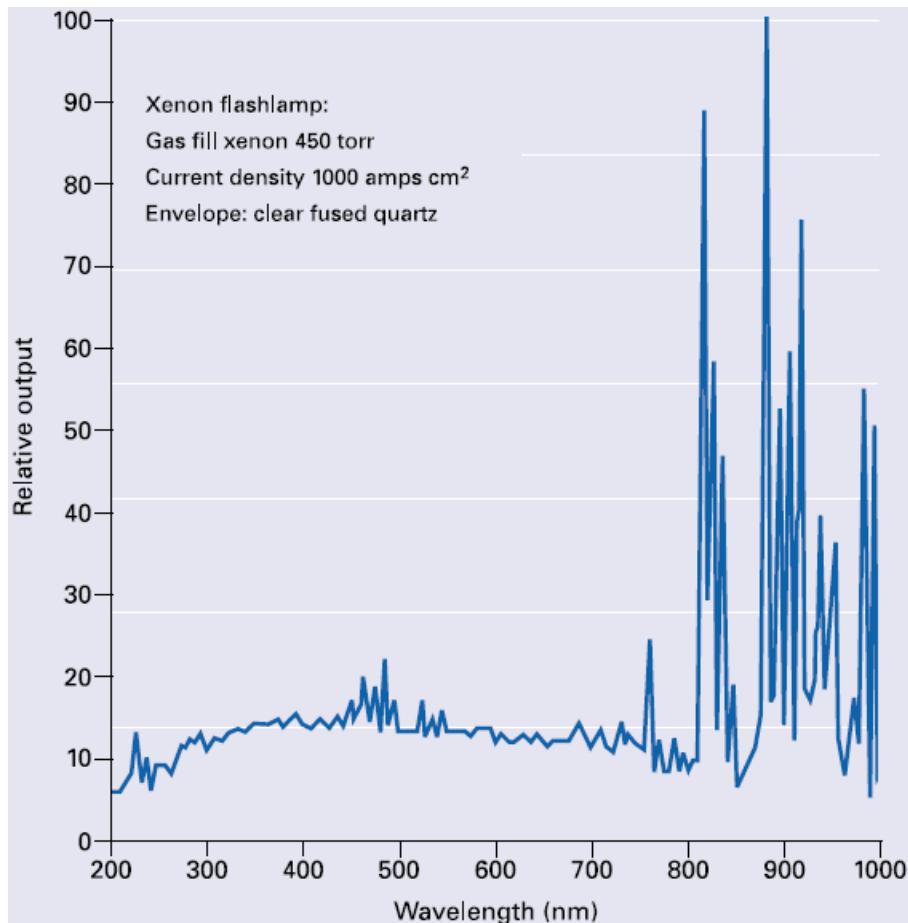
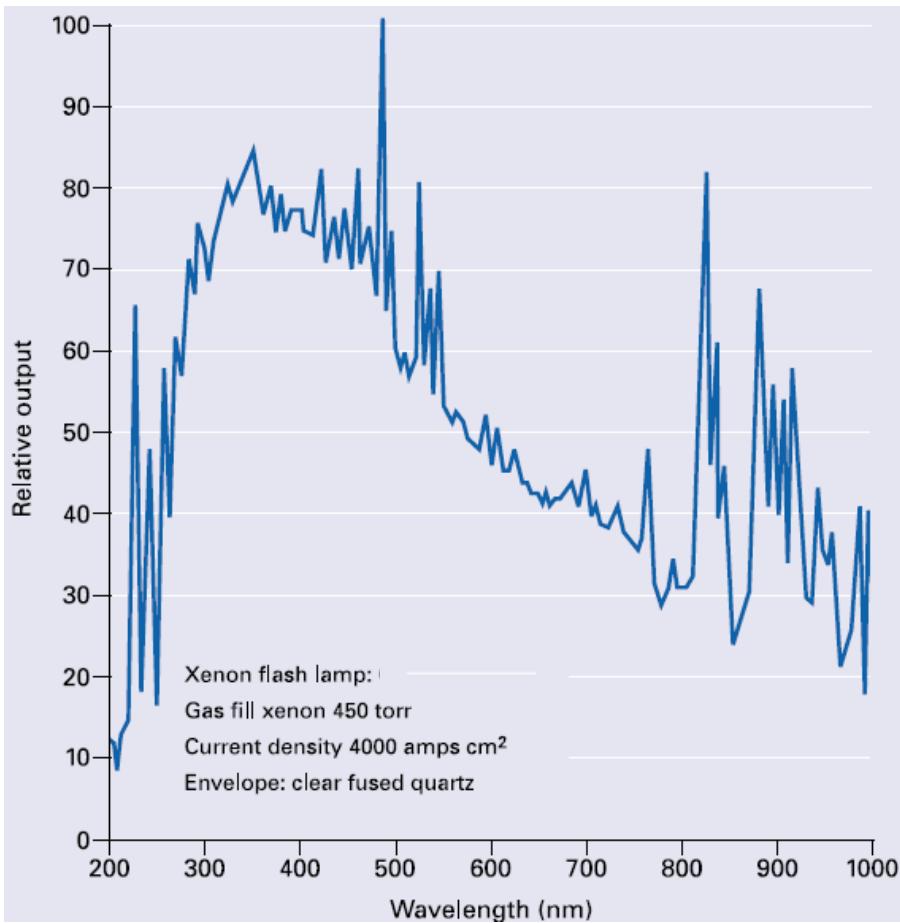
- █ - Xenon (500 Torr)
- █ - Krypton (750 Torr)
- █ - Argon (750 Torr)
- █ - Neon (750 Torr)

**Flashtube Spectral Output
For Various Gases
at 2400 A/cm²**

FLA Wavelength Characteristic



Current Density Impact on Spectrum



Various Pulse Scoped Wave Forms

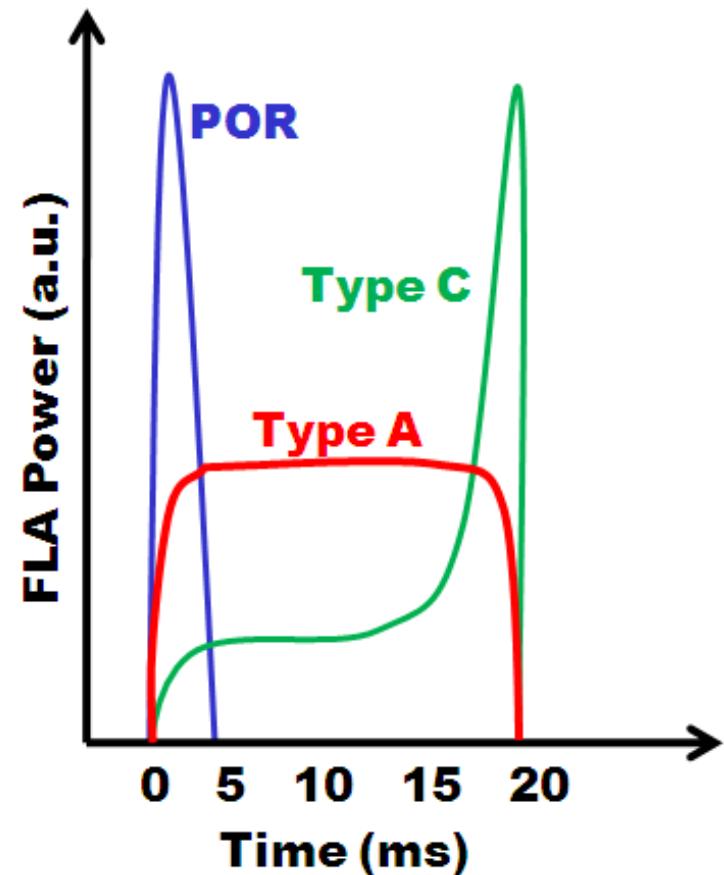
◆ Type A (trapezoidal waveform)

- Pulse condition
300A-15ms, 400A-20ms, 300A-40ms, 200A-
60ms, 150A-85ms

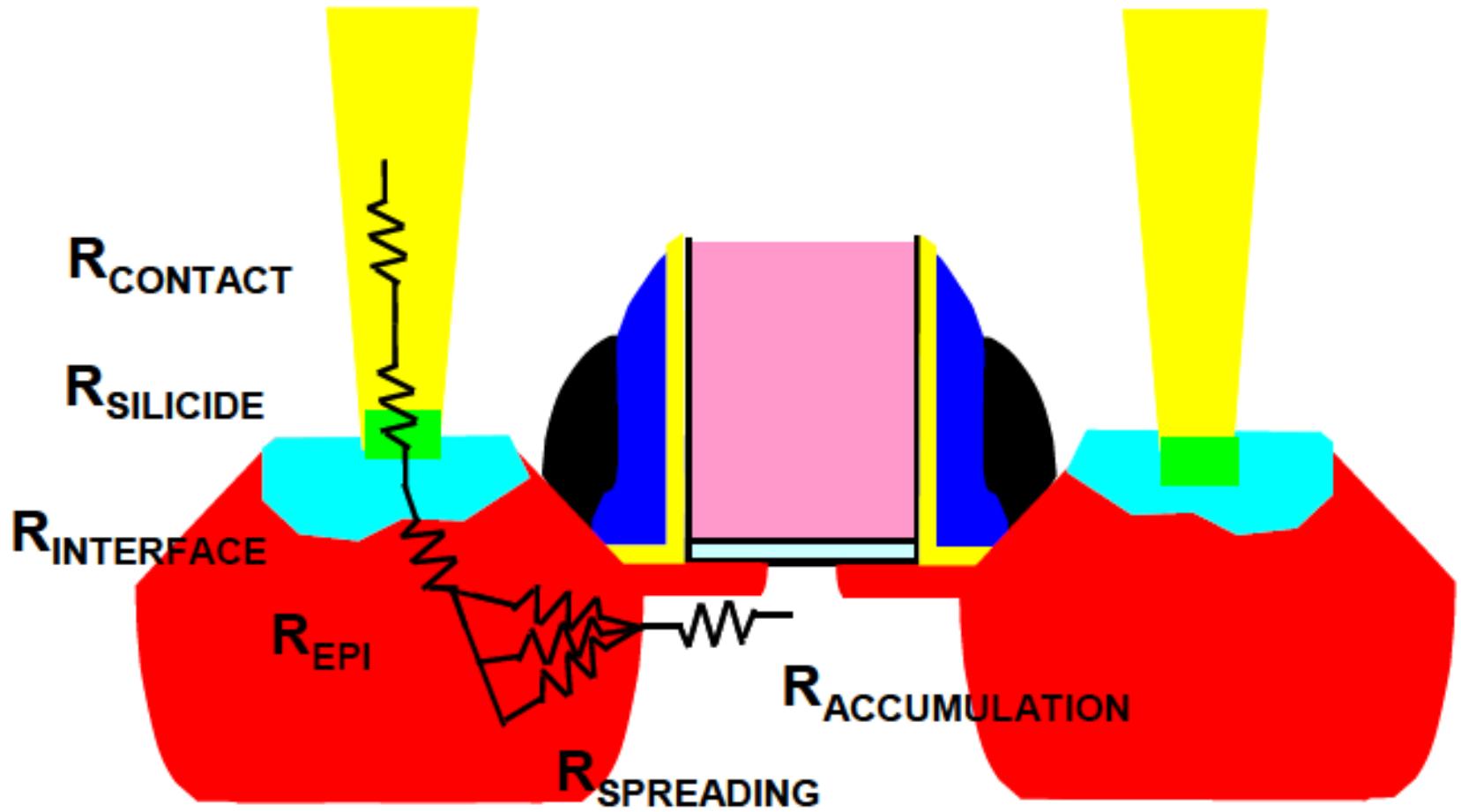
◆ Type C

(10-20msec Trapezoidal + 3msec)

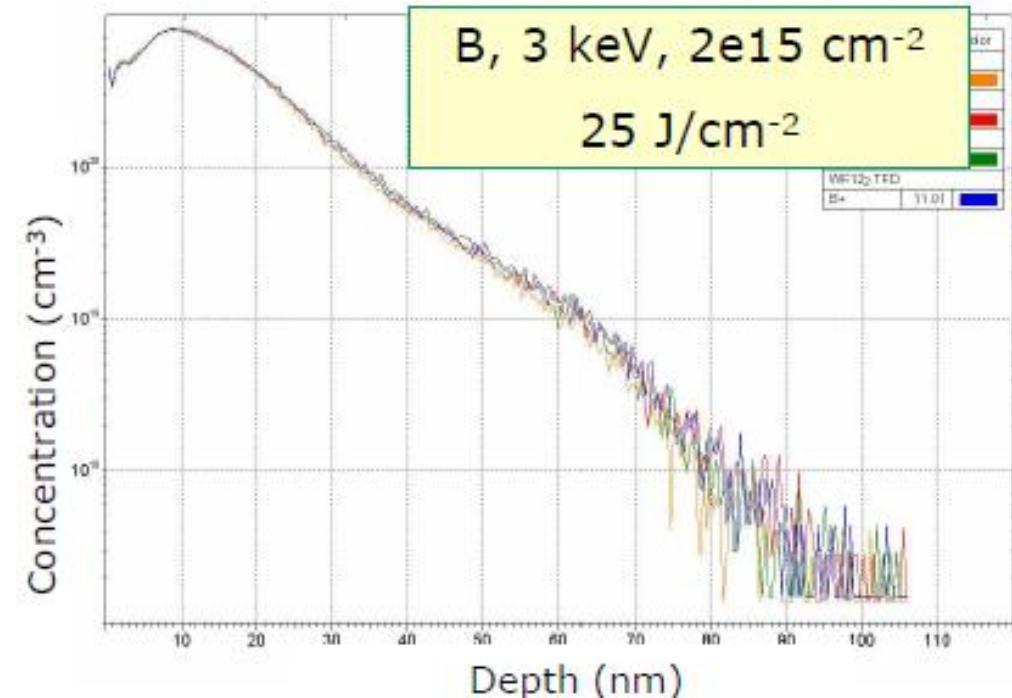
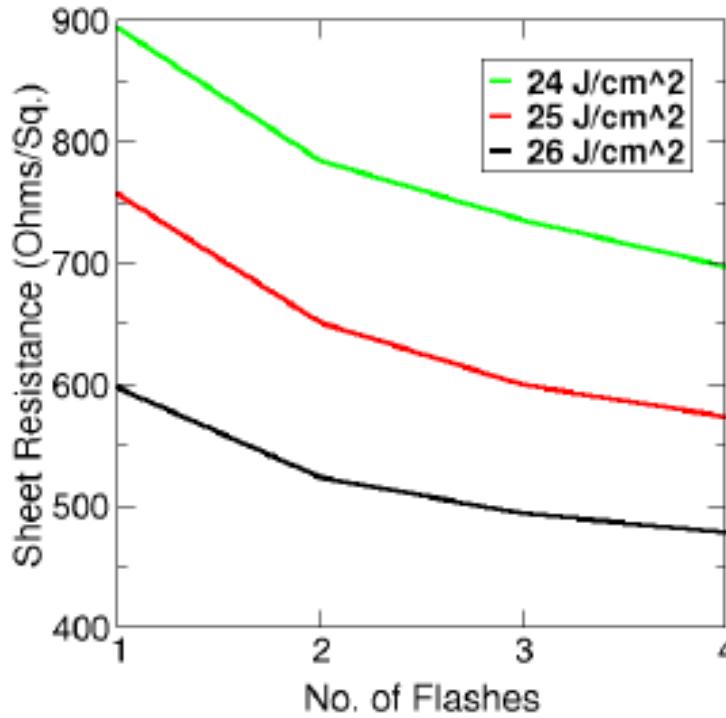
- Pulse condition 10ms + 1000us~4000us pulse
20ms + 2000us



Planar Resistive Elements



FLA Dopant Activation



- Higher power / wafer temperature reduces S/D resistance
- Multiple Flash reduces S/D resistance
- Improvement due to “dissolution” of B clusters

Agenda

□ DNS Flash Annealing Overview

- 4 generations of FLA

□ mS Annealing Challenges

□ Flexibly Shaped Pulse Flash Annealing (FSP FLA) of HikMG Structures (SELETE)

- Maximizing Mobility
- Minimizing BTI Degradation
- Maximizing Device Performance

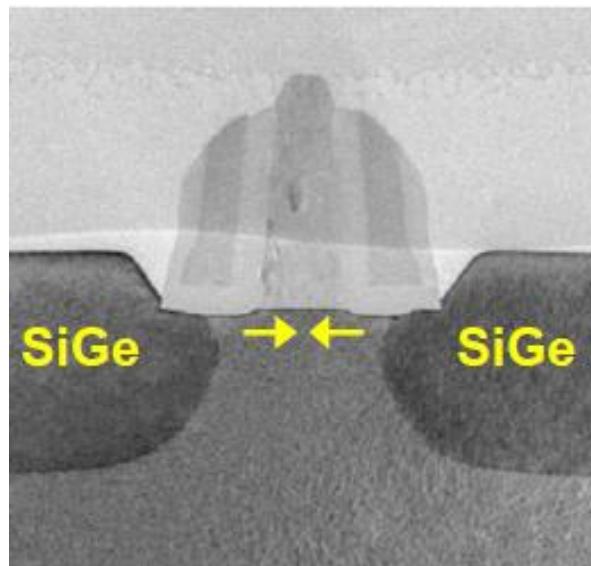
□ Mitigating mS Anneal Induced Misalignment (Toshiba)

□ Summary

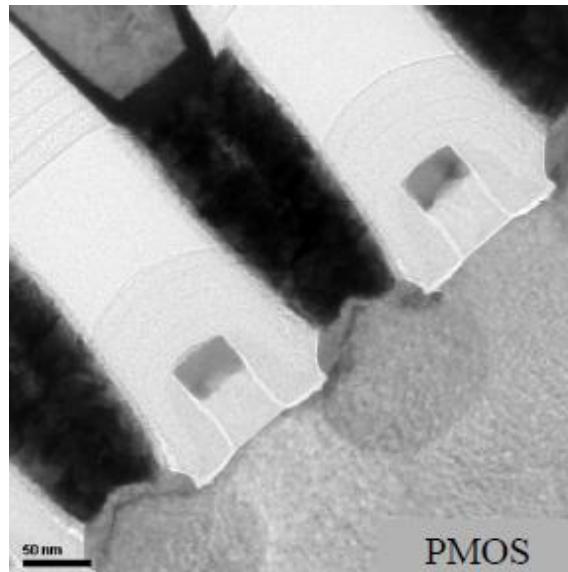
mS Annealing Challenges

- **Wafer Breakage & Defects**
- **Pattern Induced Heating Effects**
- **Mobility Degradation**
 - **Strain Compatible Annealing**
 - **Trap Generation**
- **BTI Degradation**
- **Junction Leakage**
- **Anneal Induced mis-Alignment**

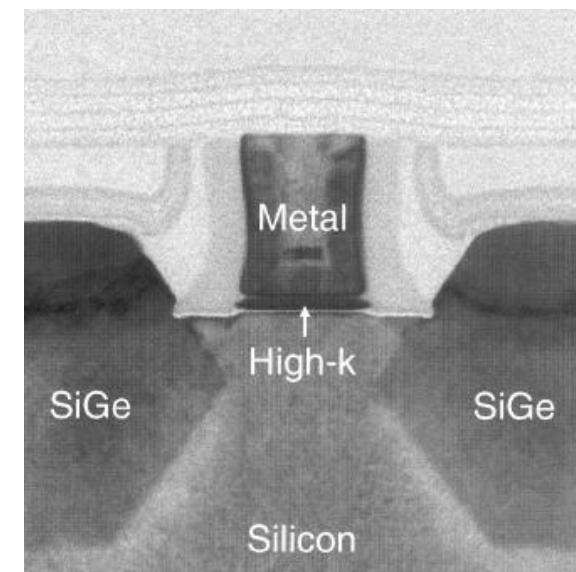
90nm → 65nm → 45nm → 32nm 4 Generations of Strain at Intel



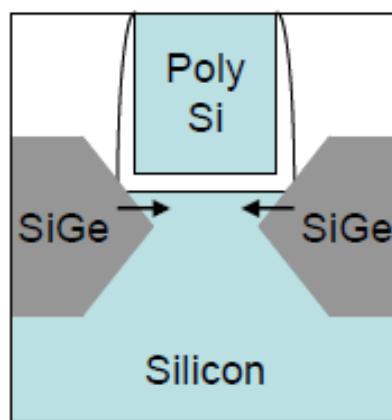
Intel IEDM - '02



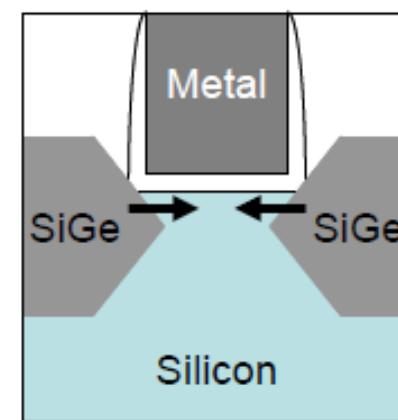
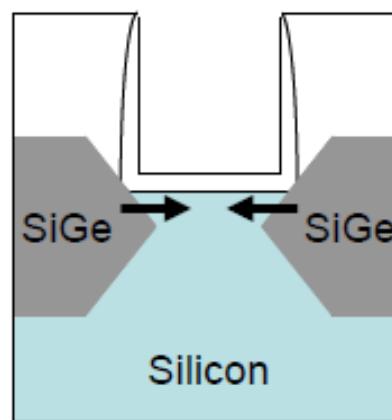
Intel IEDM - '04



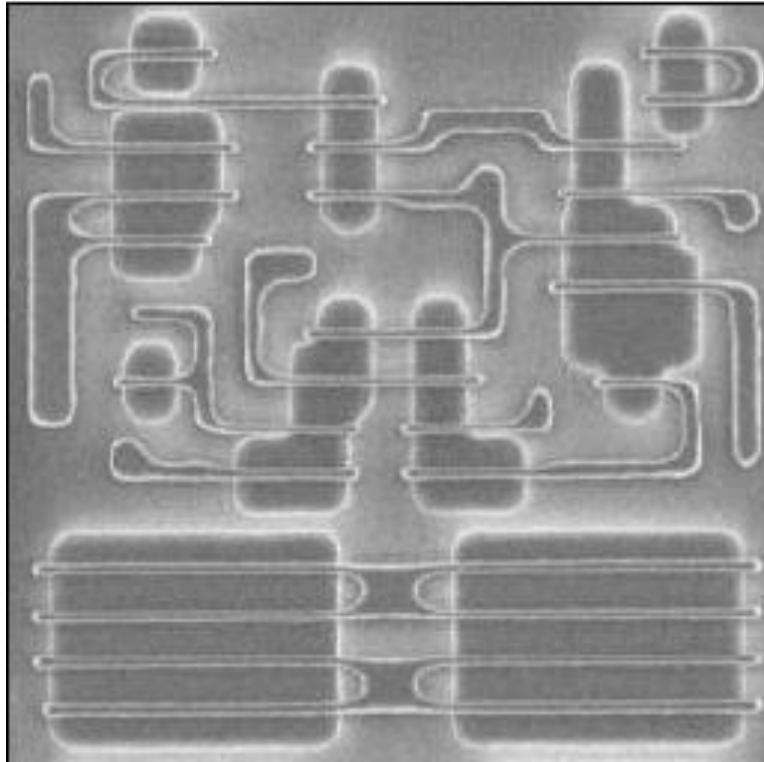
Intel IEDM – '07



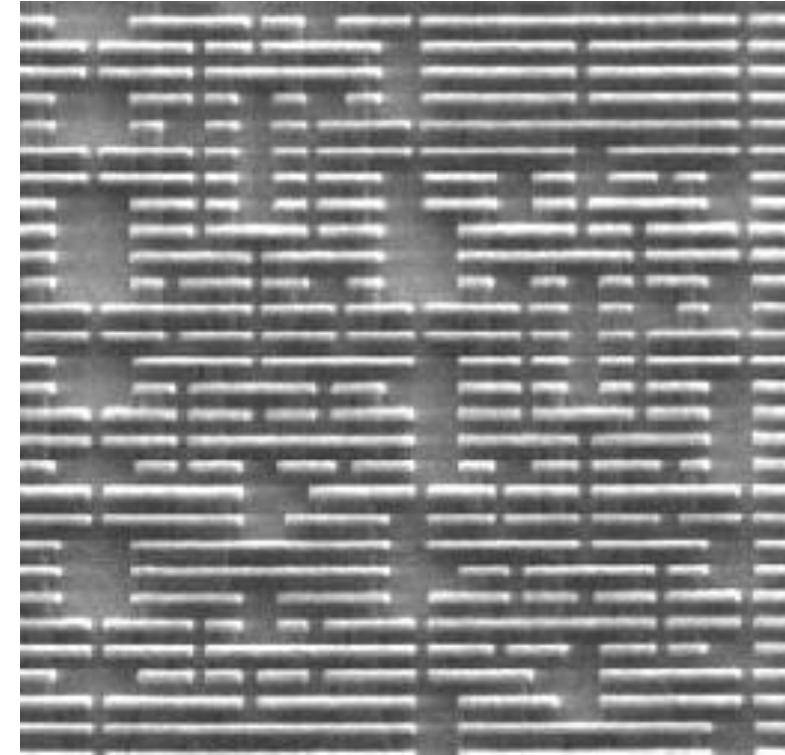
Intel IEDM – '08



65nm → 45nm Layout Changes



- Bi-directional features
- Varied gate dimensions
- Varied pitches



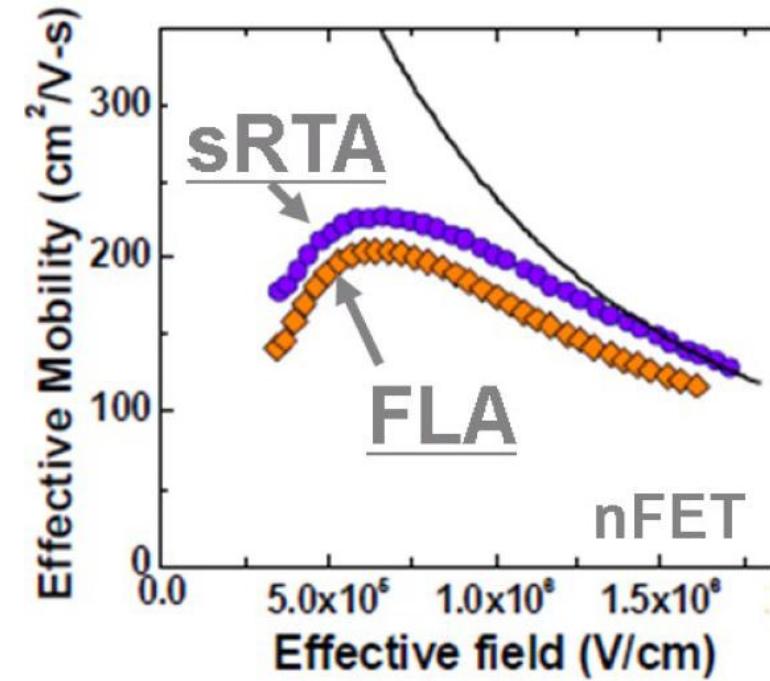
- Uni-directional features
- Uniform gate dimension
- Gridded layout

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Gate 1st HKMG mS FLA Challenge

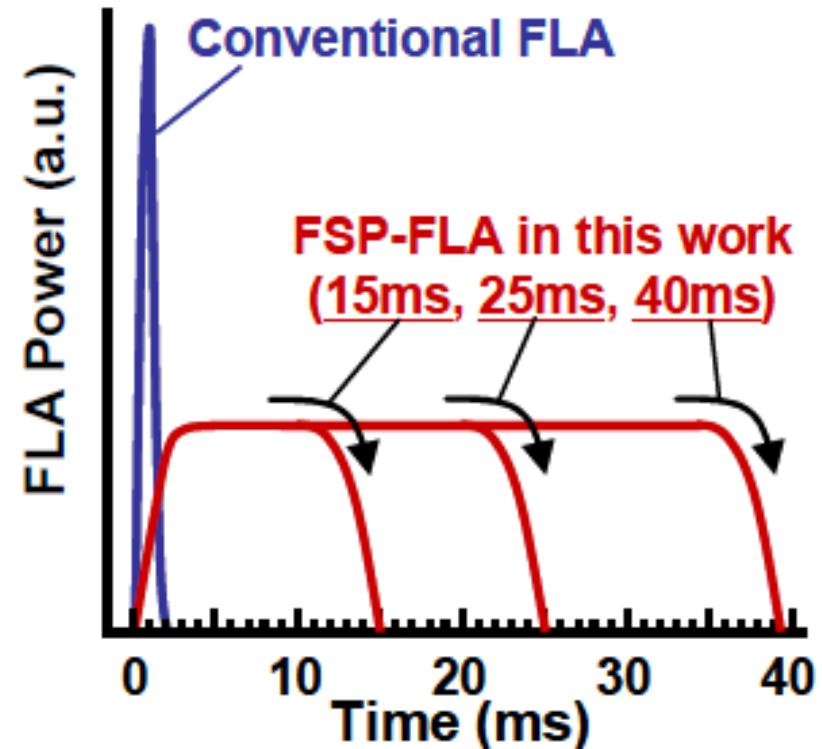
- **HKMG (Gate First) used in 32nm node**
- **POR FLA degrades HKMG device performance**
- **FLA on HfSiO/TiN increases traps**
- **Degrades mobility & BTI**



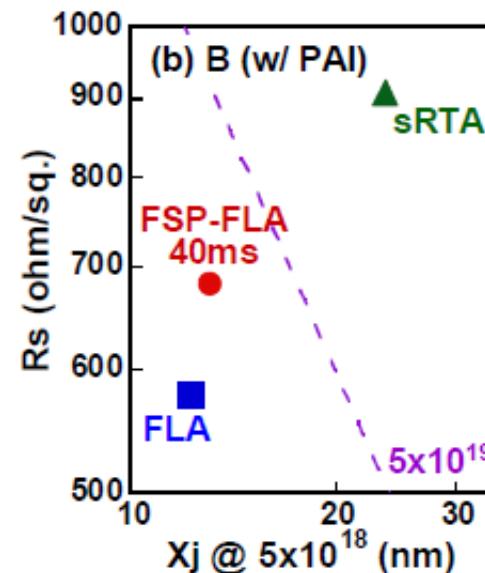
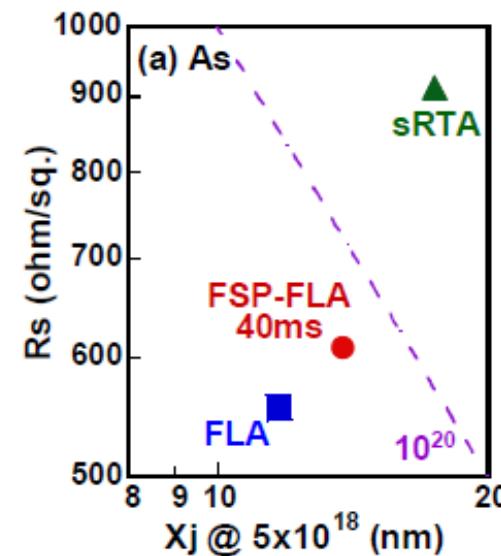
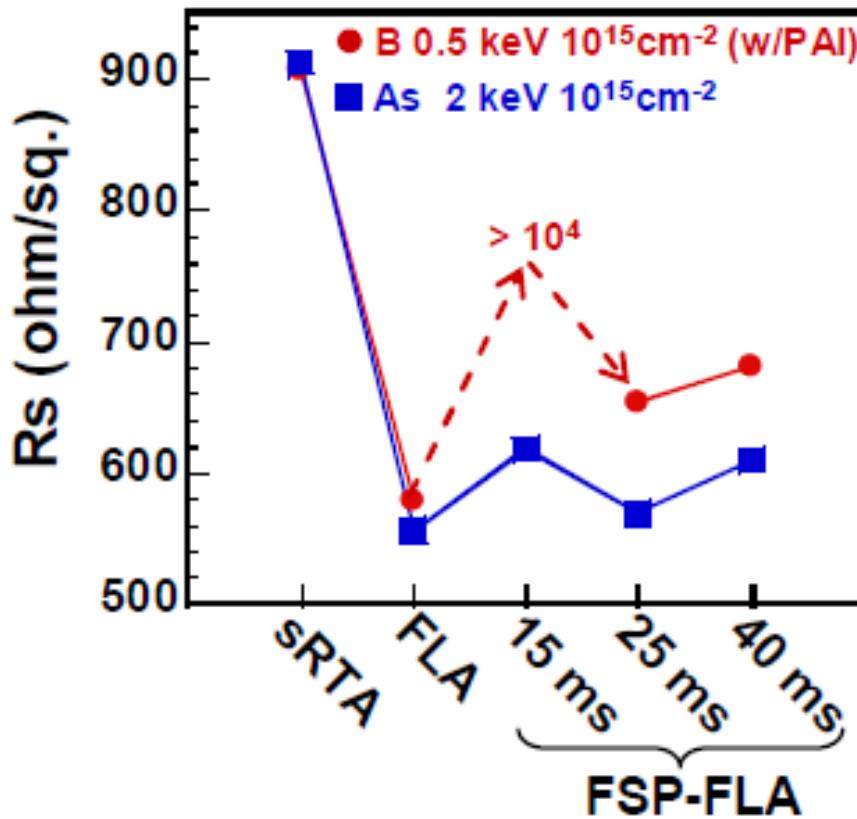
Karla et al., IEDM 2007

FSP FLA Annealed 32nm HKMG

- STI and well formation
- HfSiON/SiO₂ formation
- WFM (TaSiN, TiN) sputtering
- W deposition
- Gate patterning
- Extension, Halo I/I
- Sidewall fabrication
- Deep SD I/I
- SD activation (sRTA, FLA, FSP-FLA)
- Metallization

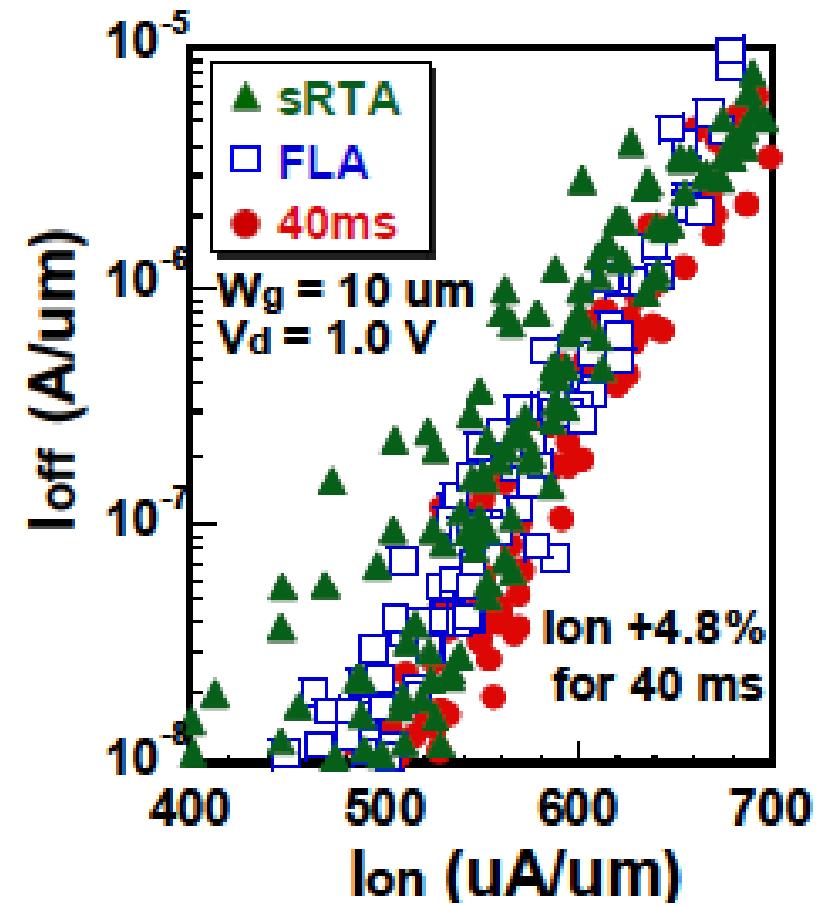
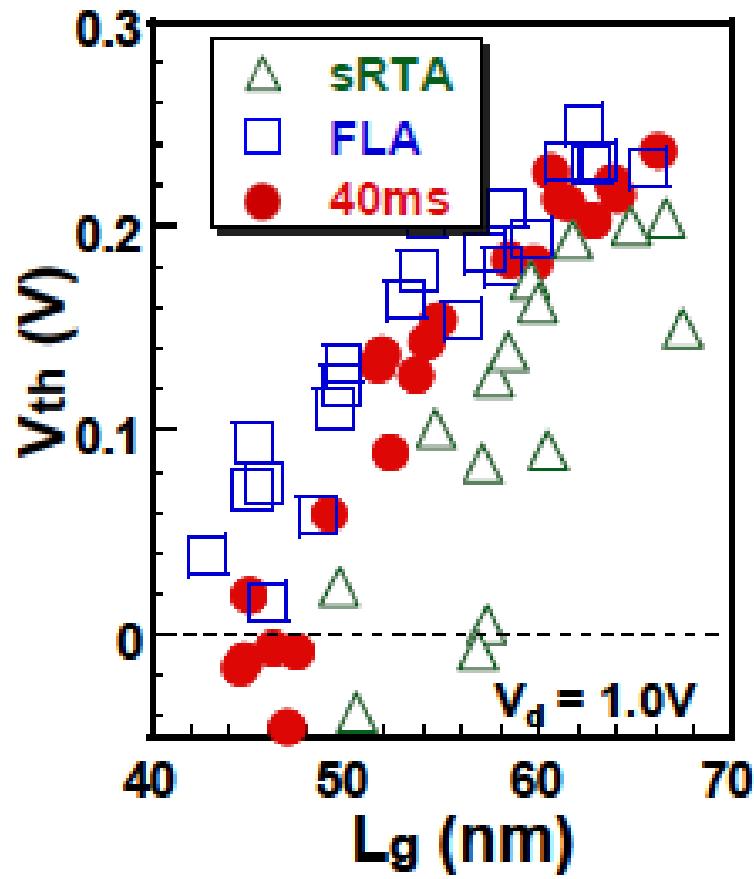


FSP FLA Annealed 32nm HKMG

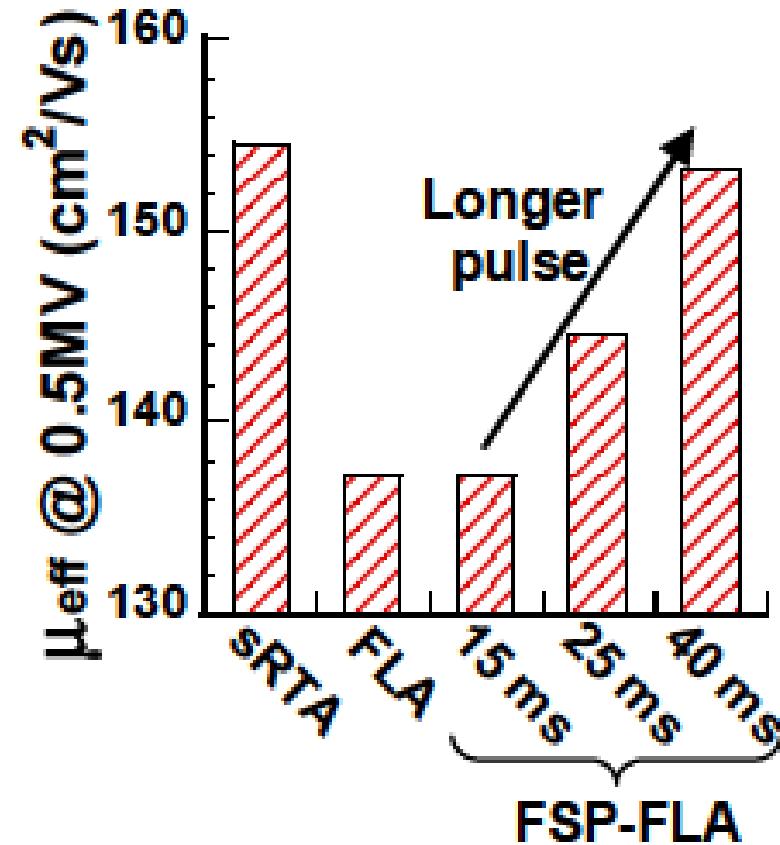
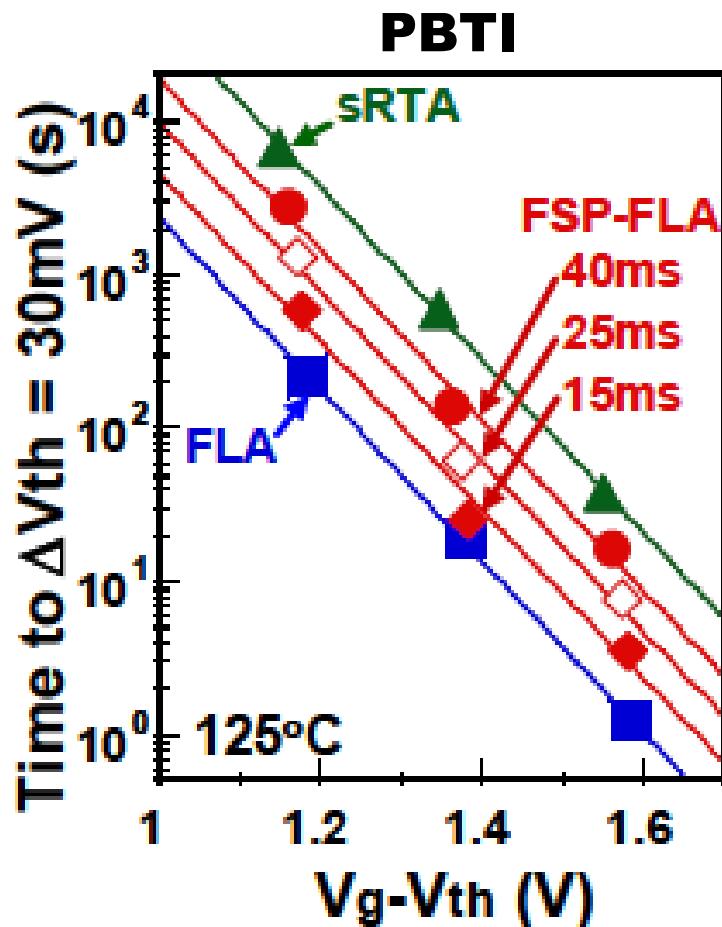


Aoyama et al., IWJT 2009

FSP FLA Annealed 32nm HKMG

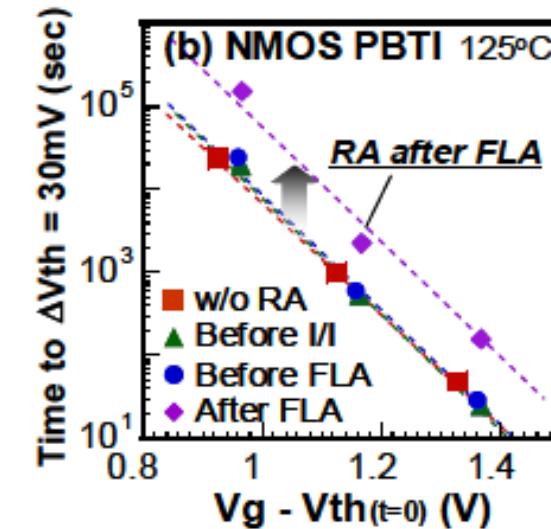
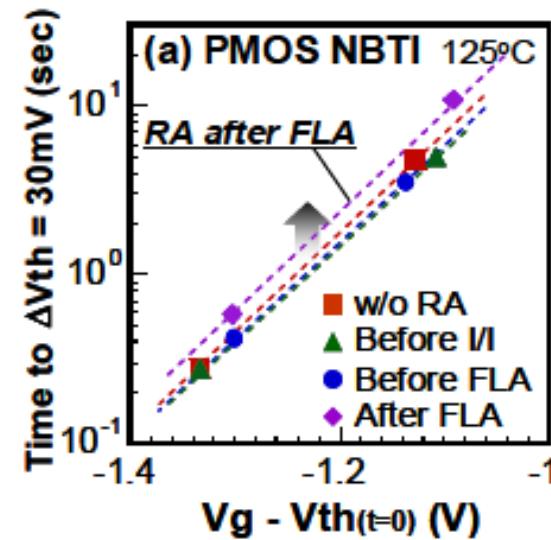
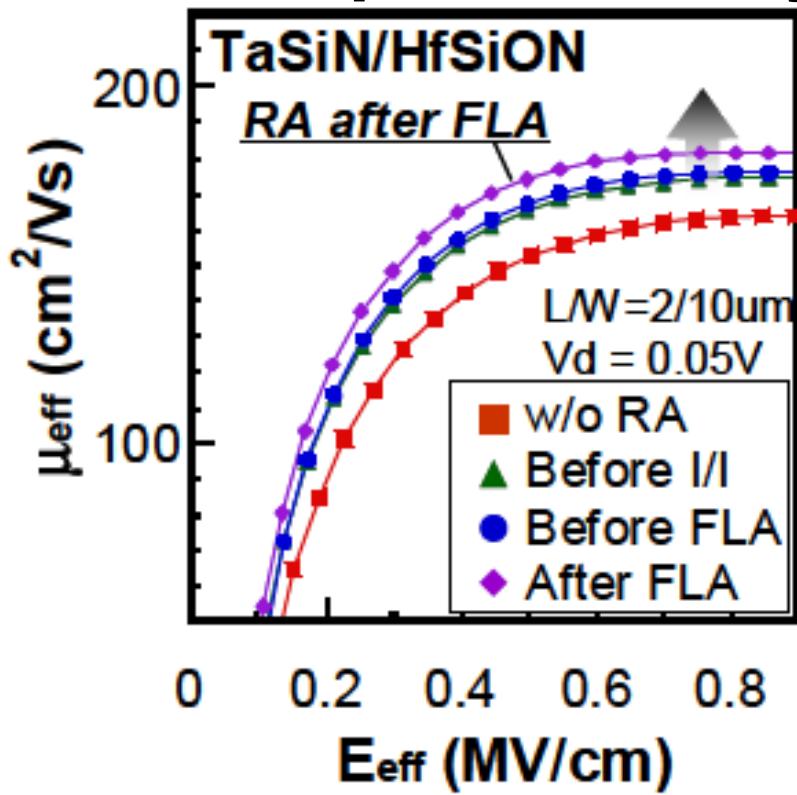


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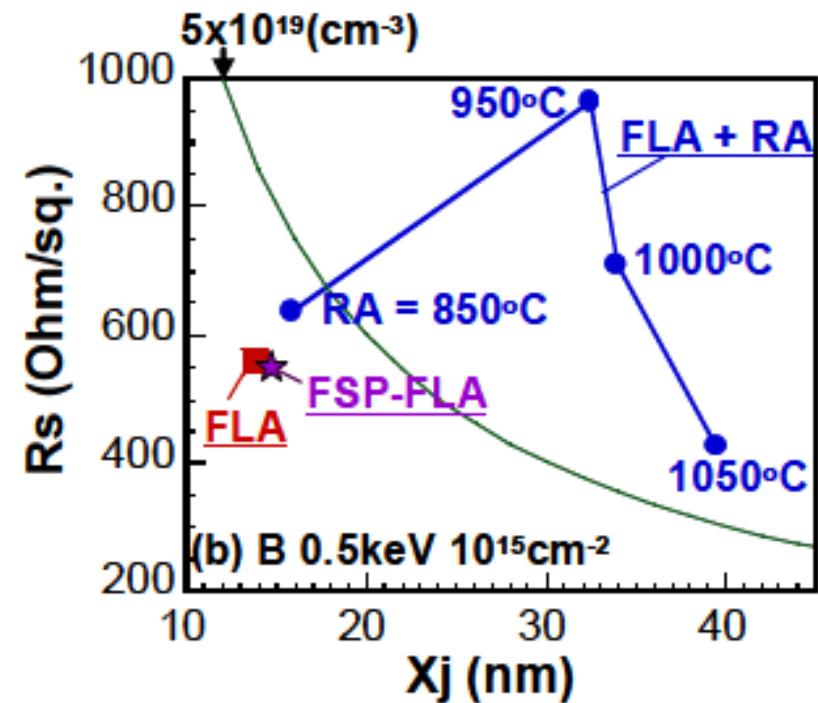
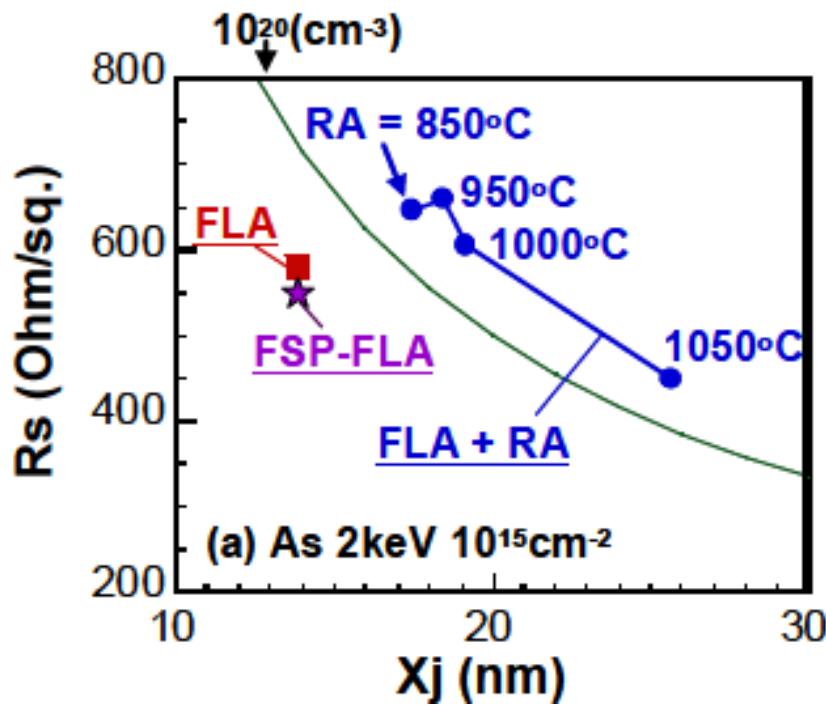


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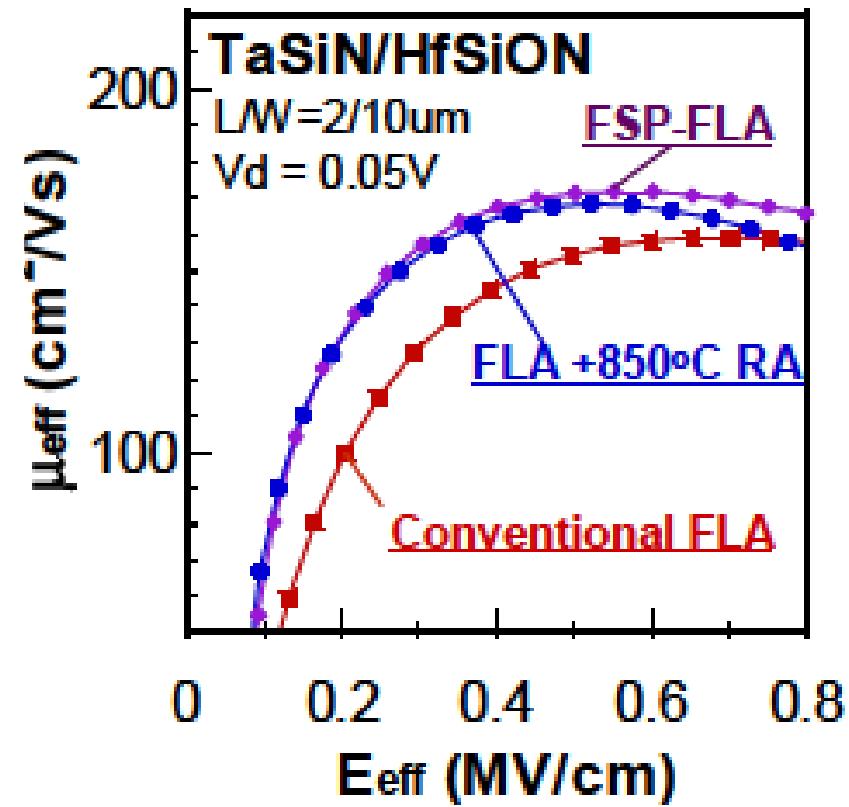
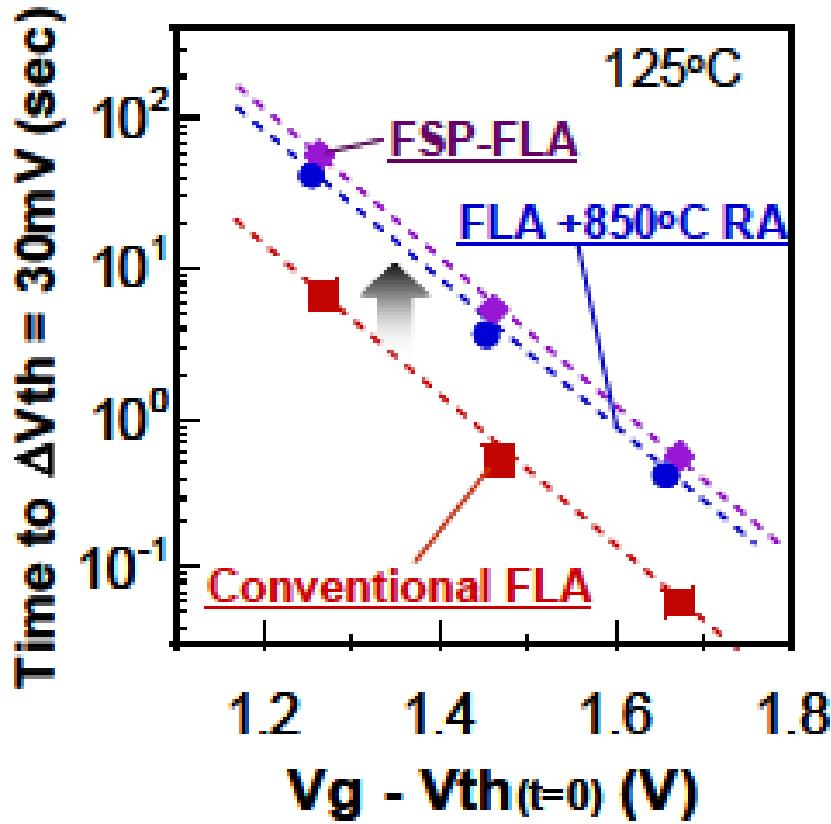
RA impact on Mobility



FSP FLA Annealed 32nm HKMG



FSP FLA Annealed 32nm HKMG

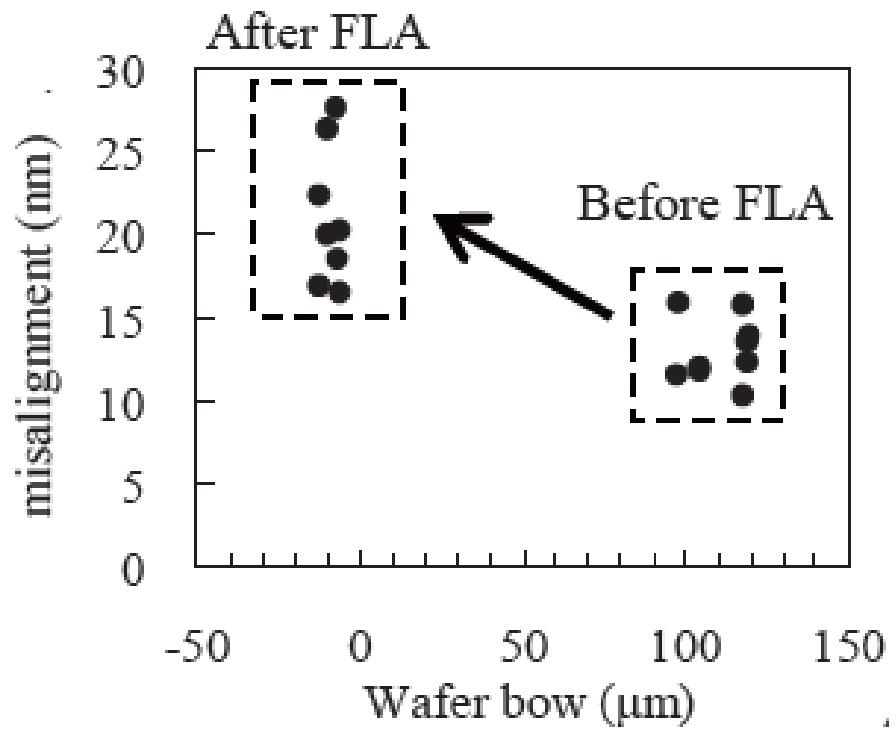


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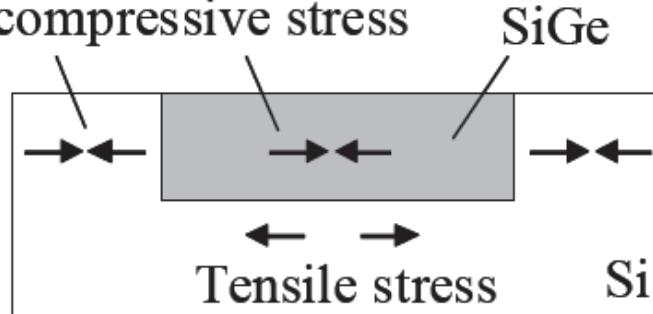
Suppress FLA Induced Mis-Alignment

- STI
- Gate Electrode
- eSiGe S/D
- Halo/Extension Implant
- Sidewall
- S/D Implant
- Spike RTA
- FLA
- NiSi



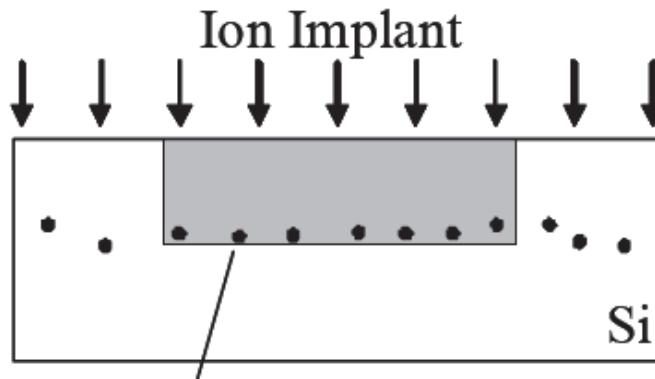
Suppress FLA Induced Mis-Alignment

High compressive stress

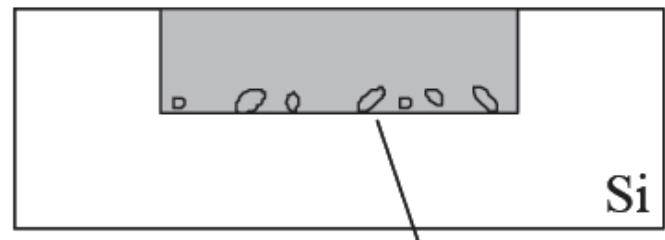


(a) eSiGe

Ion Implant

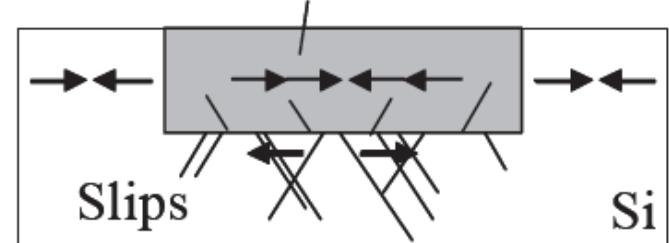


(b) I/I Damage (Interstitials)



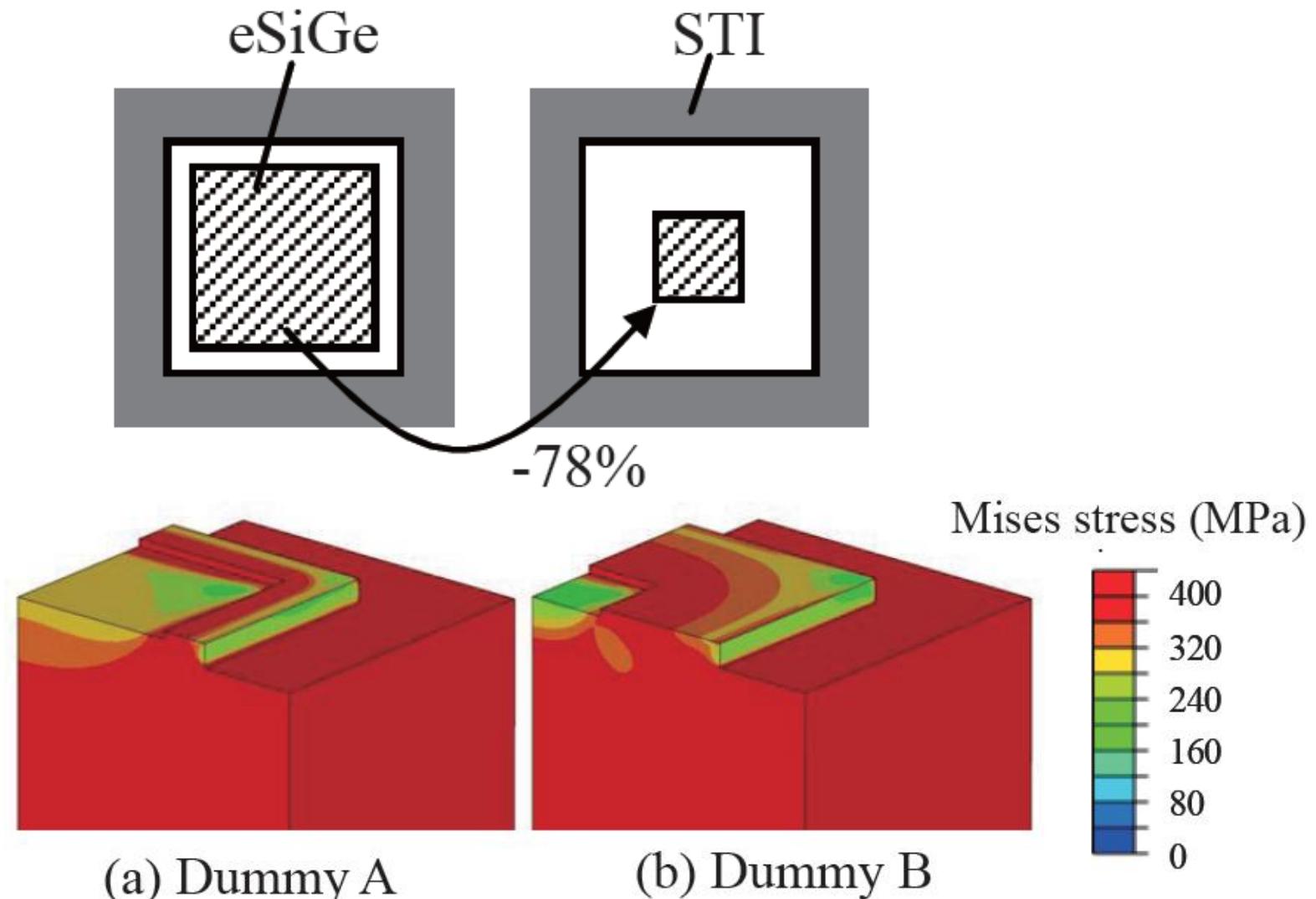
(c) Spike RTA dislocation loops

High compressive stress



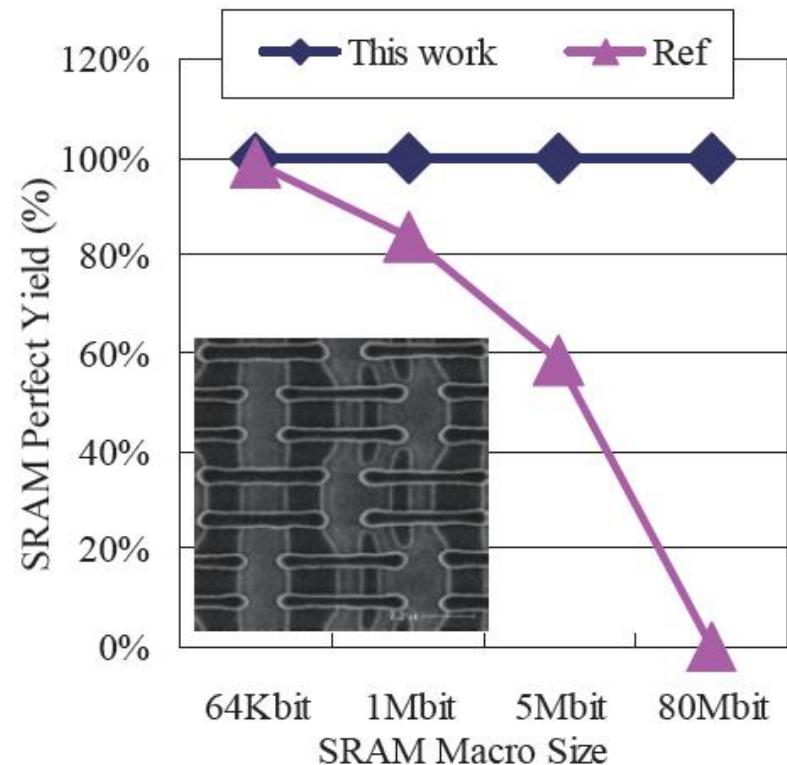
(d) FLA At high temperature

Suppress FLA Induced Mis-Alignment



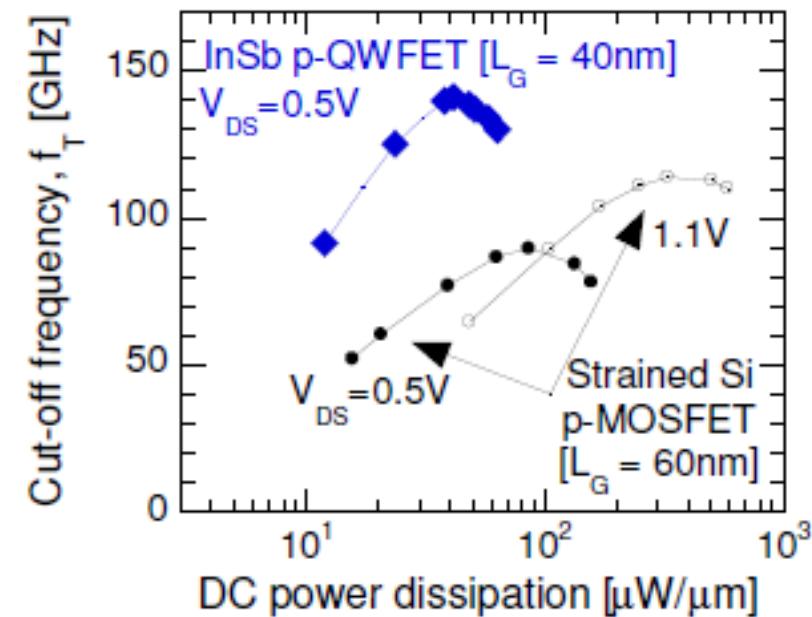
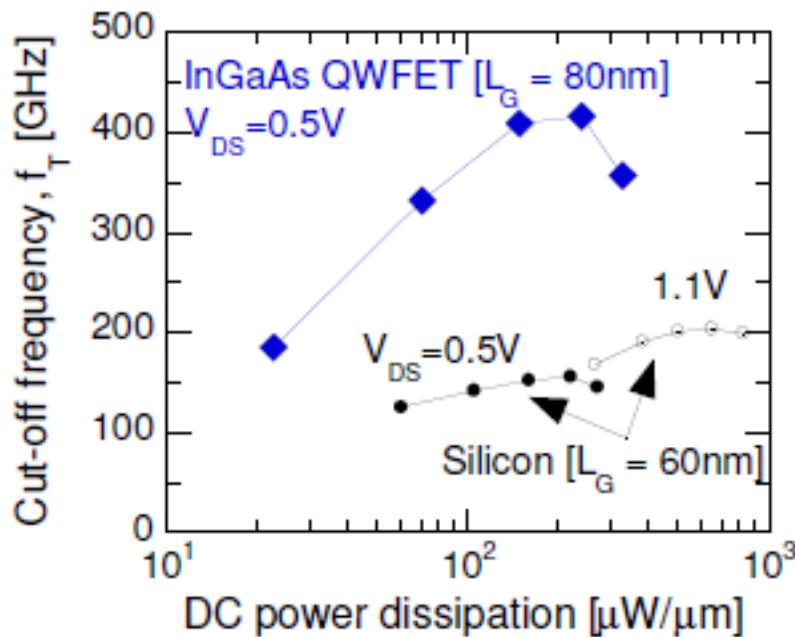
Suppress FLA Induced Mis-Alignment

	Ref.	This work
Dummy eSiGe pattern	A (Fig.11(a))	B (Fig.11(b))
Maximum eSiGe size of transistor	No restriction	< 10um ² (Fig.16)
Random Misalignment (3sigma)	21nm (Fig.4)	11nm (Fig.17)



Scaling – Transistor's Future

III-V Planar Future → The mobility roadmap



InGaAs NMOS QWFET

Peak $f_T > 400\text{GHz}$ at $V_{cc} = 0.5\text{V}$

InSb PMOS QWFET

Peak $f_T > 140 \text{ GHz}$ at $V_{cc} = -0.5\text{V}$

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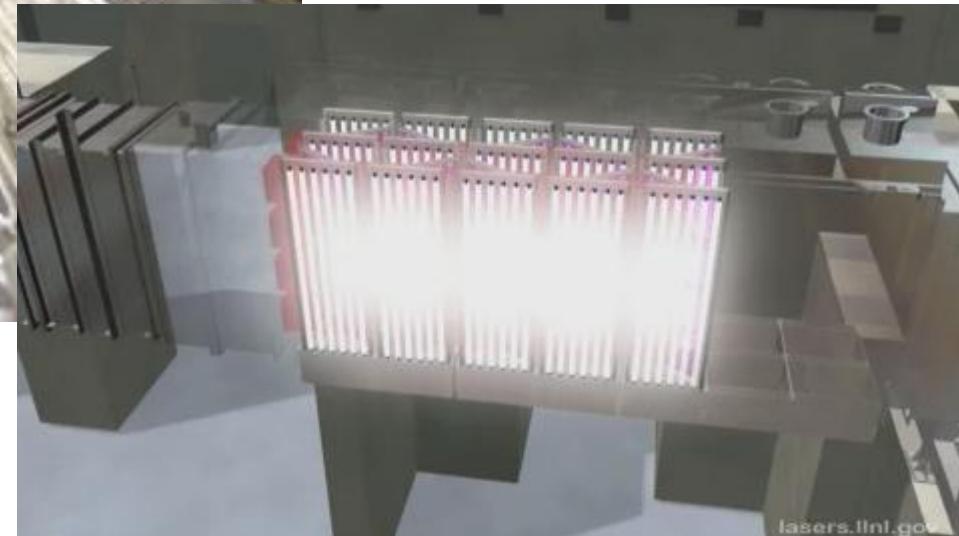
Summary

- **DNS has introduced 4th generation FLA**
 - **FSP-FLA**
- **Lamp Assist minimizes wafer stress**
- **FSP FLA of HikMG**
 - **Maximizes Mobility**
 - **Minimizes BTI Degradation**
 - **Maximizes Device Performance**
- **Integration & design are most important when introducing any new processes**
 - **Minimize misalignment with dummy structure**

Xenon Flash Lamps at NIF



**Xeon pumped
LASER Amplifying
Glass slabs**



Our California neighbors paving the way beyond 450mm

Thank you for your attention

