CMOS Leakage Reduction using Laser Spike Annealing

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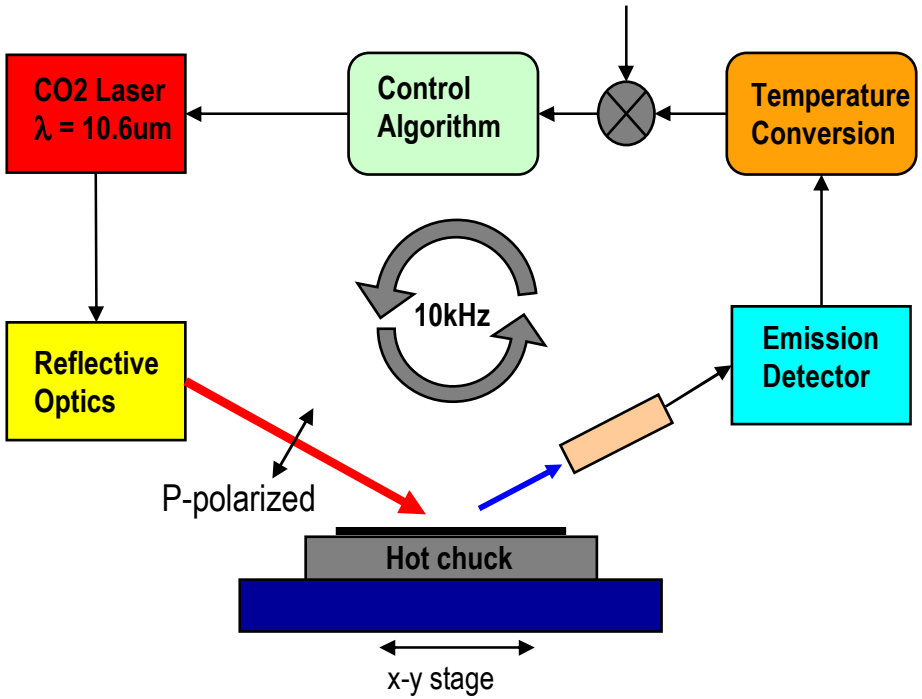
Outline

- Introduction
- Advantages of high annealing temperatures
- HK+MG
- Role of stress for advanced CMOS
- Extendibility to alternate device structures

LSA System Architecture

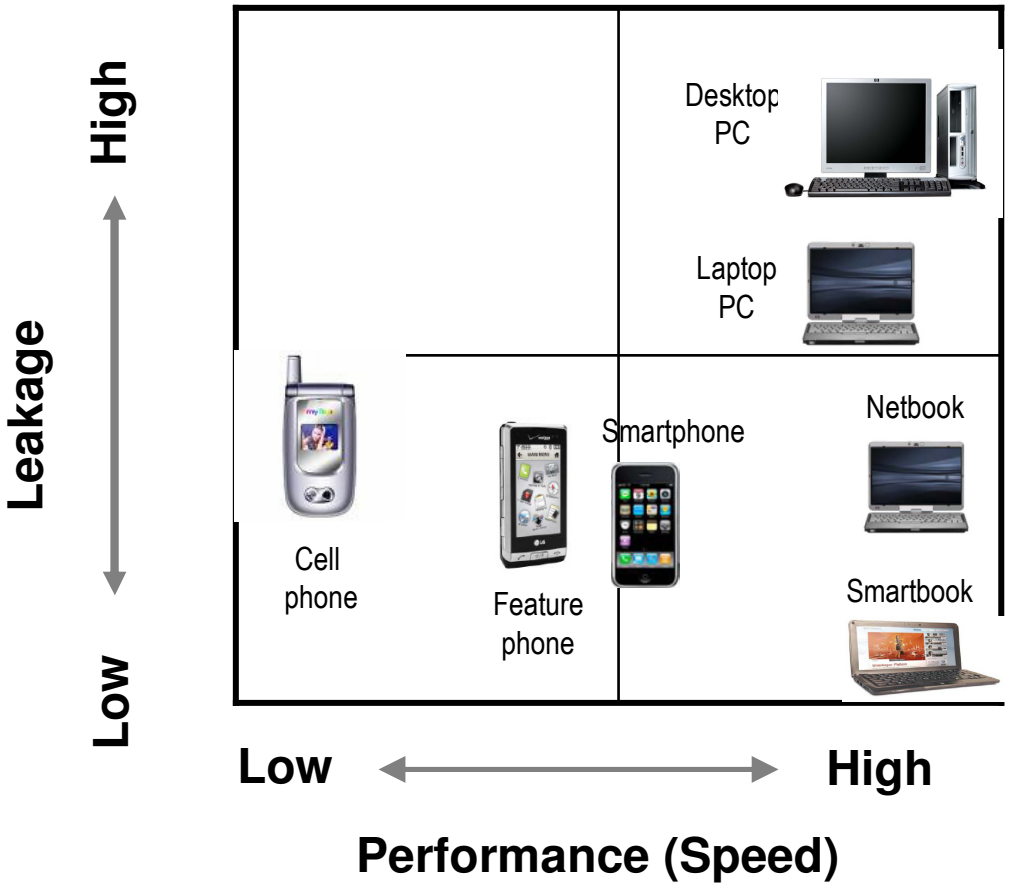


LSA Key Attributes

1. Within-die uniformity
   - Long wavelength,
   - p-polarized
   - Brewster angle
2. Wafer-to-wafer repeatability
   - Temperature feedback control
3. Low stress
   - Flexible dwell time
   - Effective stress dissiptaion

System is designed to minimize within-die and within-wafer variations

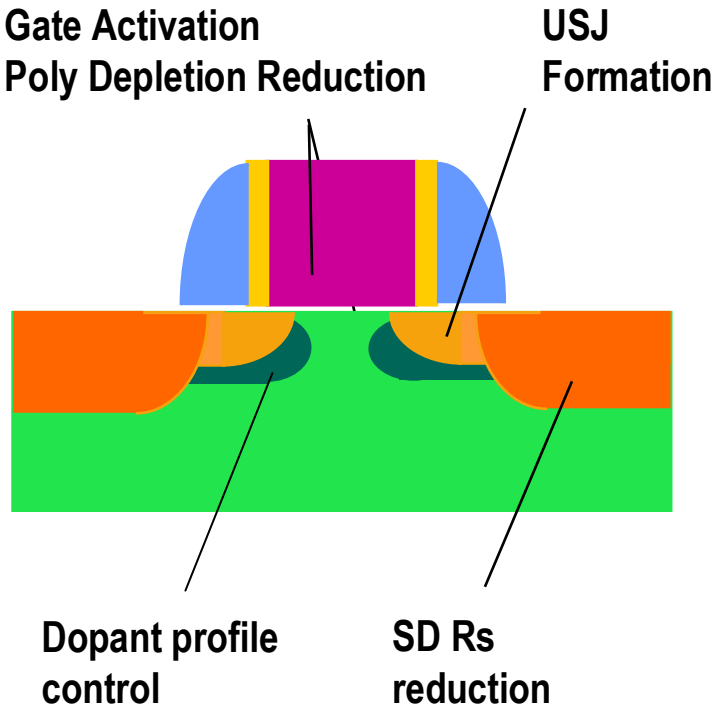
Leakage and Power Requirements for Advanced Devices



Key Highlights

- Trends toward multi-media "connected" devices have placed unprecedented demands on simultaneous power and leakage
- Leakage reduction is critical for:
  - Battery life
  - Cooling requirements

Laser Spike Annealing for USJ Formation



- Thinner Tox_inv due to reduced poly depletion
- Improved Id due to reduced series resistance
- Reduced SCE due to ultra-shallow junction
- Multiple steps being used to maximize gains from LSA
- Tradeoff's between leakage and speed by reverse oxide scaling, junction re-optimization, etc

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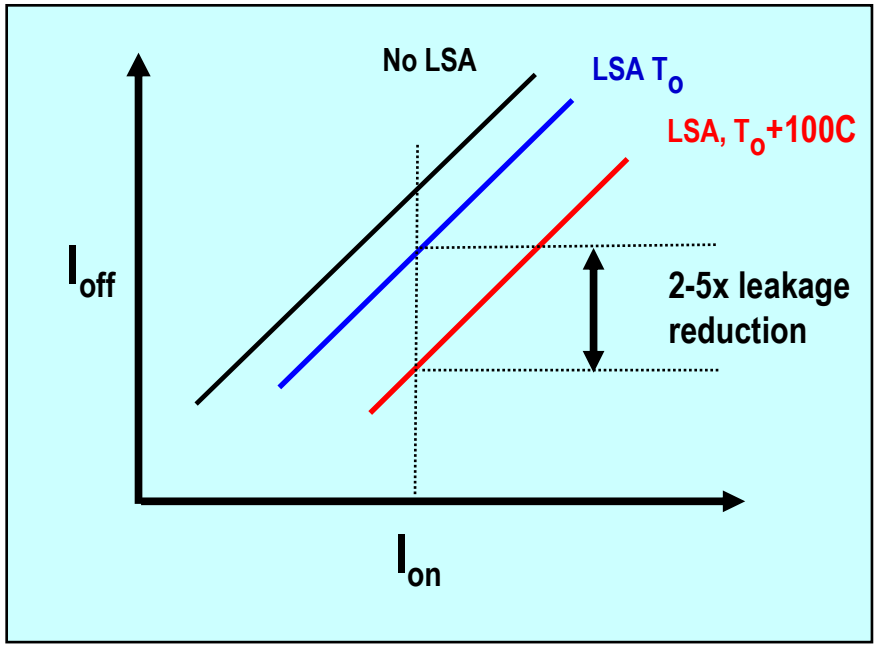
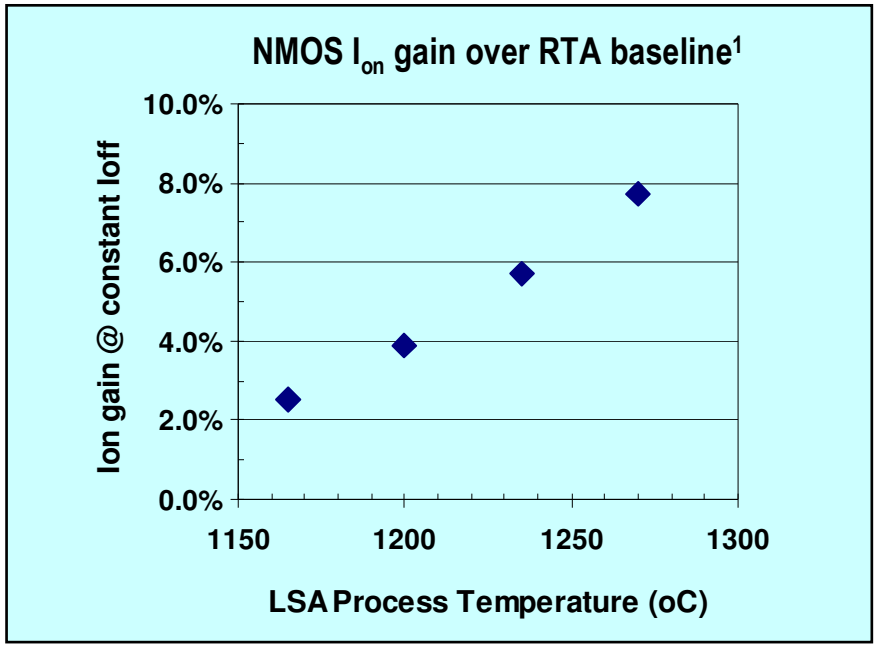
Higher temperatures of LSA gives lower leakage



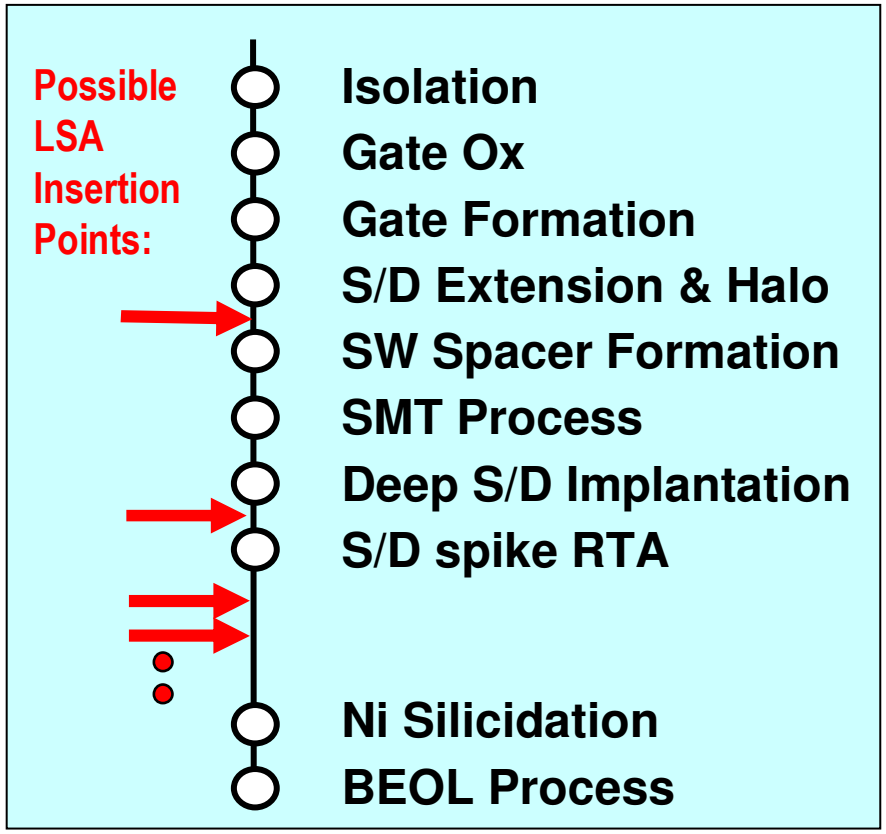
TI Data (Chen et al., RTP2007)



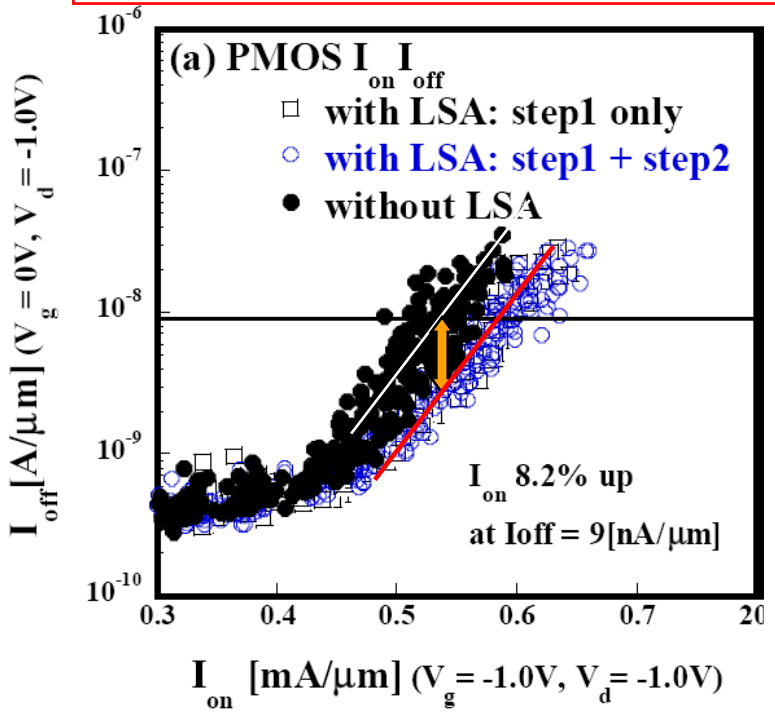
- **Typically, an increase in LSA peak temperature of 100C reduces leakage by 2-5X, depending on device integration (e.g, Adachi et al. Toshiba, IEDM 2005).**

Multiple LSA steps for leakage reduction

Device Flow



PMOS leakage reduction of 3-4X using two-step LSA (Fujitsu, IEDM 2007)

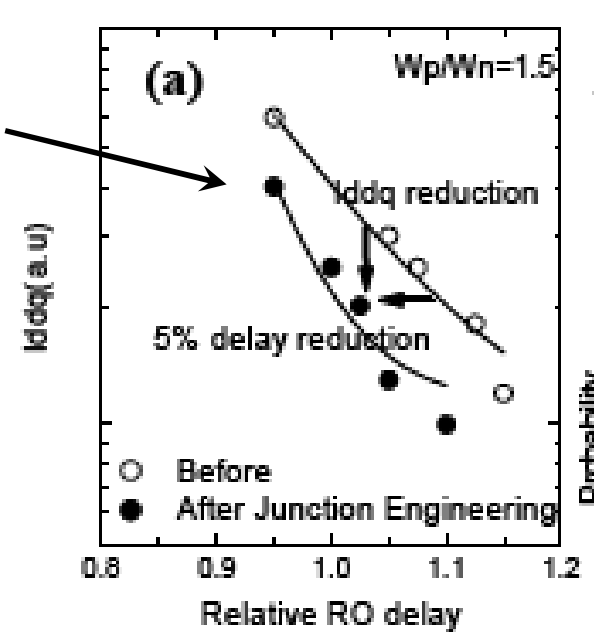


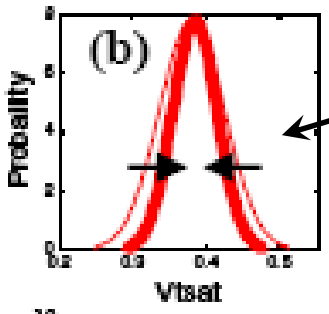
Multiple LSA steps is mainstream for advanced nodes

Vt Variability & Leakage Reduction For Low Power Application (Samsung Results)

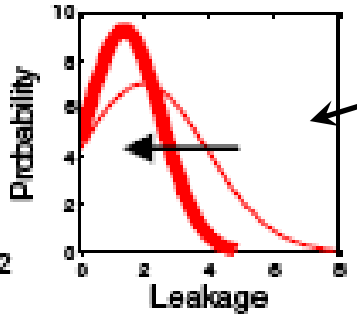
H. Lee et al, Samsung, IEDM2008

Improved ring oscillator performance





Lower Vt variability



Reduced leakage distribution

LSA/Implant optimization gives leakage reduction and improved uniformity

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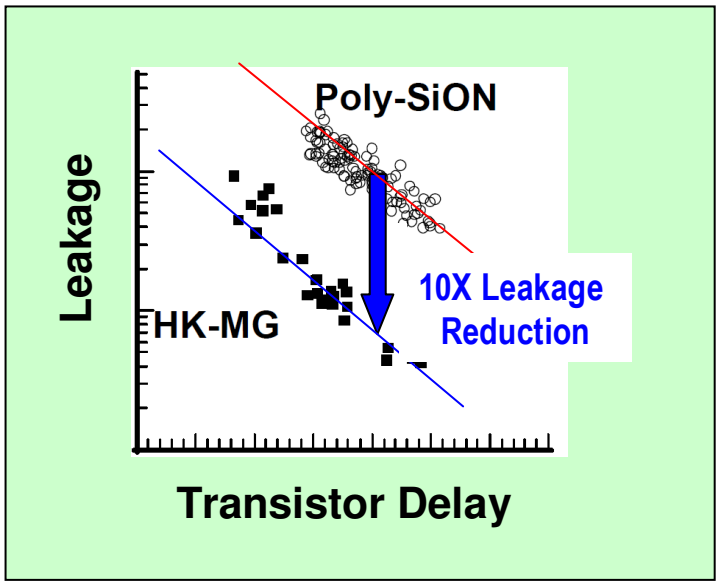
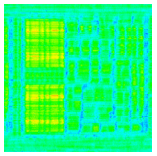
LSA Compatibility with High K + Metal Gate

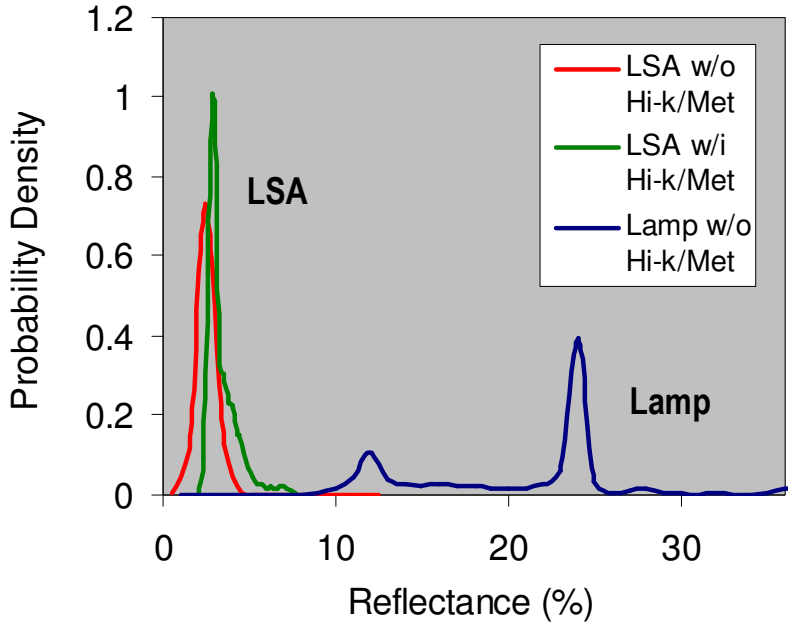
X. Chen et al., IBM, VLSI 2008



Gate first process with LSA

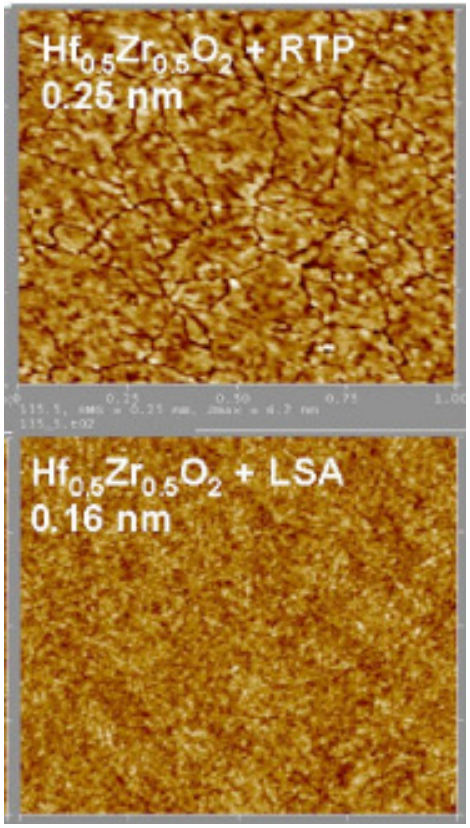


Map of Die Reflectance with LSA

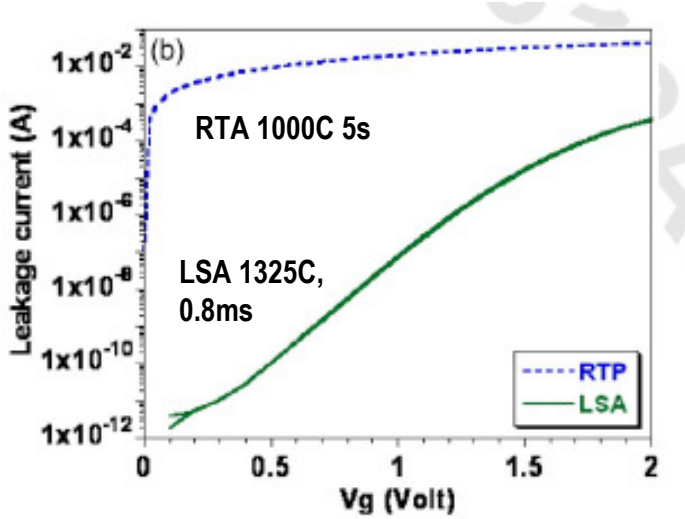


- LSA demonstrated to be compatible with "gate first" HK+MG integration
- Pattern suppression still effective for HK+MG due to small thickness of metal gate

High-k Morphology & Leakage Improvement



(a) AFM morphology



(b) Leakage characteristics

*source: D.H. Triyoso, to be published in APL

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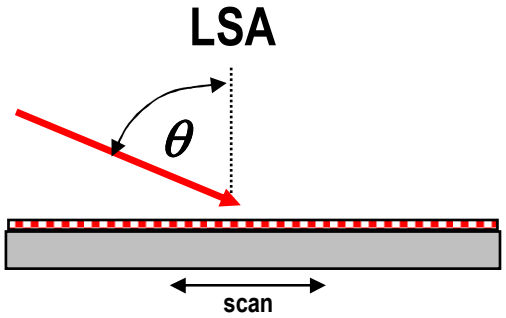
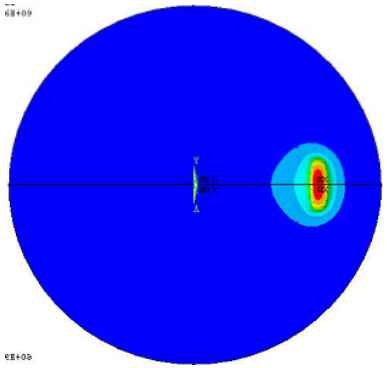
Wafer Stress in LSA



Side view - Wafer held flat on vacuum chuck



Top view: Simulated stress during LSA. Less than 5% of the wafer area is stressed

Temperature gradients

- Minimal pattern effects give uniform stress

Stress dissipation

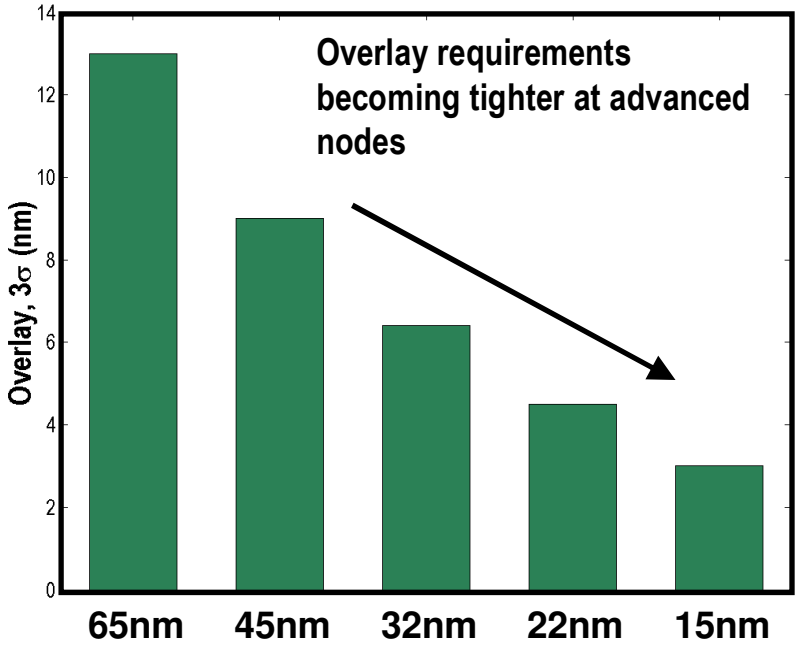
- Stress is localized - minimizes thermal shock.
- Stress is dissipated by rest of the wafer and to wafer chuck

Dwell time

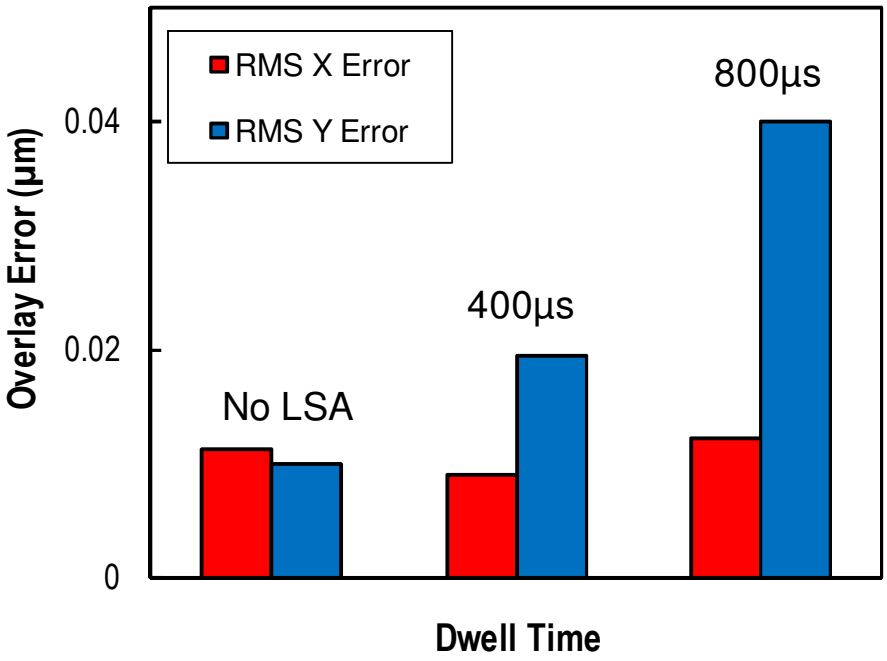
- Dwell time flexibility allows low wafer warpage for critical process steps

Relationship Between Stress & Overlay

ITRS Roadmap

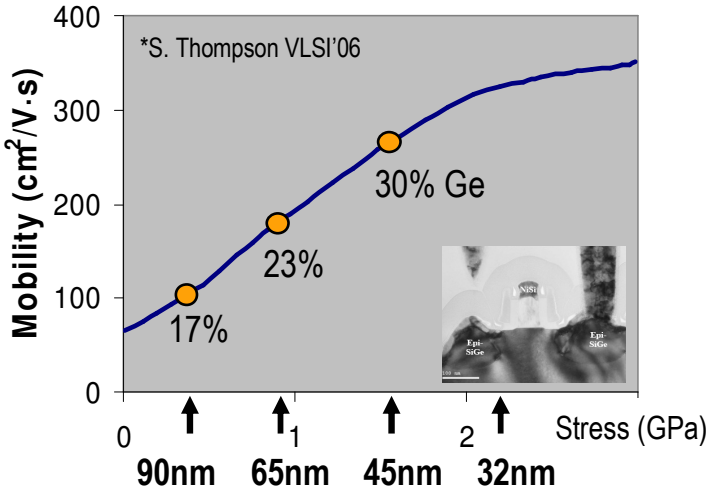


Shetty et al (Ultratech & TI), IWJT2009



- LSA dwell time flexibility critical for compatibility with e-SiGe at sub-65nm
- Same principles apply for Si:C for sub-32nm

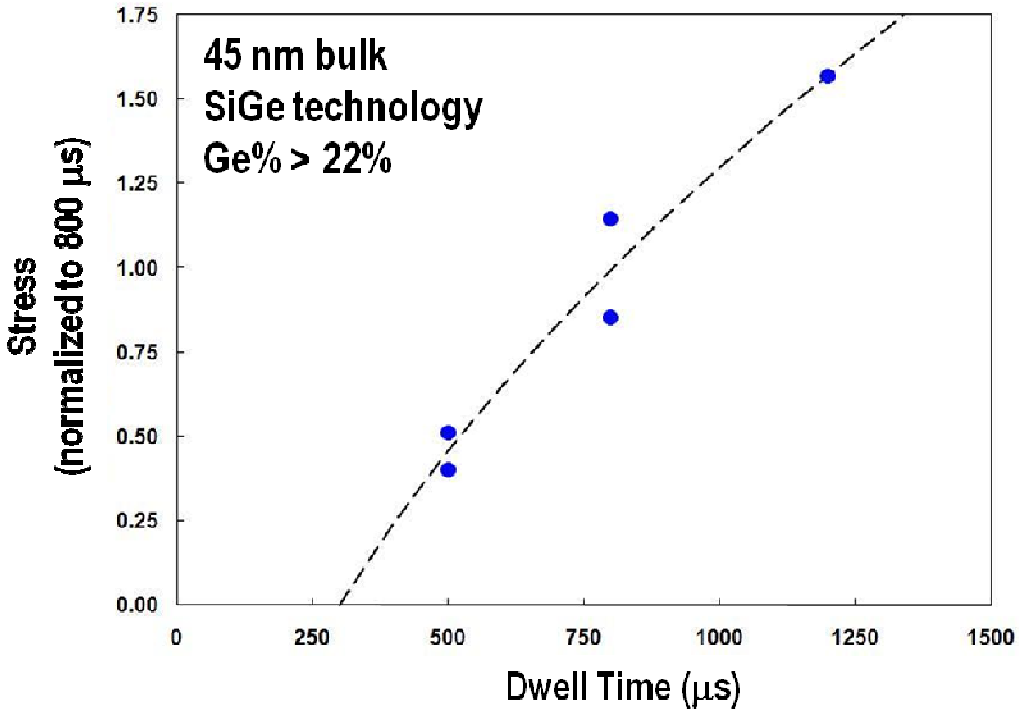
Low Dwell Time for Overlay Improvement



$$\frac{dN(t)}{dt} \propto N_0 \tau_{eff}^{n} \exp\left(-\frac{E_a}{kT}\right)$$

(*Houghton, et al, JAP 1991)

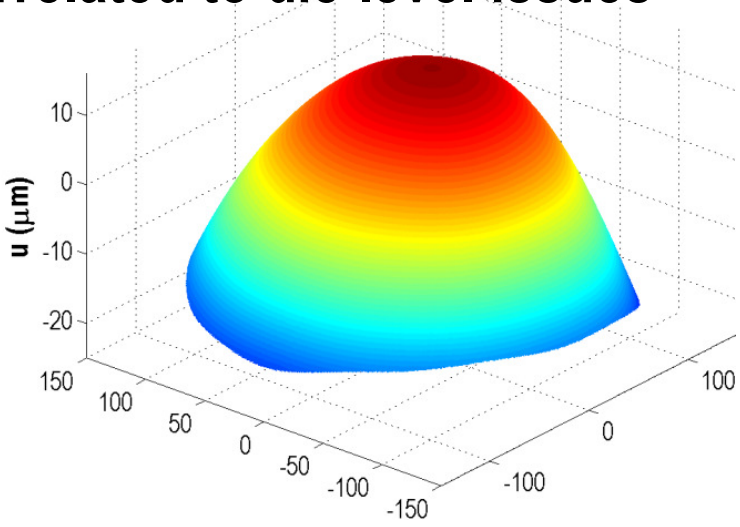
Warpage & stress are reduced at low dwell times



- **Dislocation formation scales exponentially with T and $t^{1/2}$, so reducing time is beneficial for reducing overlay errors**
- **Dislocation formation will become more severe as Ge concentration is increased**

Overview of Coherent Gradient Sensing System

- Measurement technology: Lateral shearing interferometer
  - >700,000 points (310 μm per pixel)
  - Rapid image capture, no scanning
- Analysis and algorithms
  - Full analysis in less than 2 minutes
  - Full wafer stress variations can be correlated to die-level issues

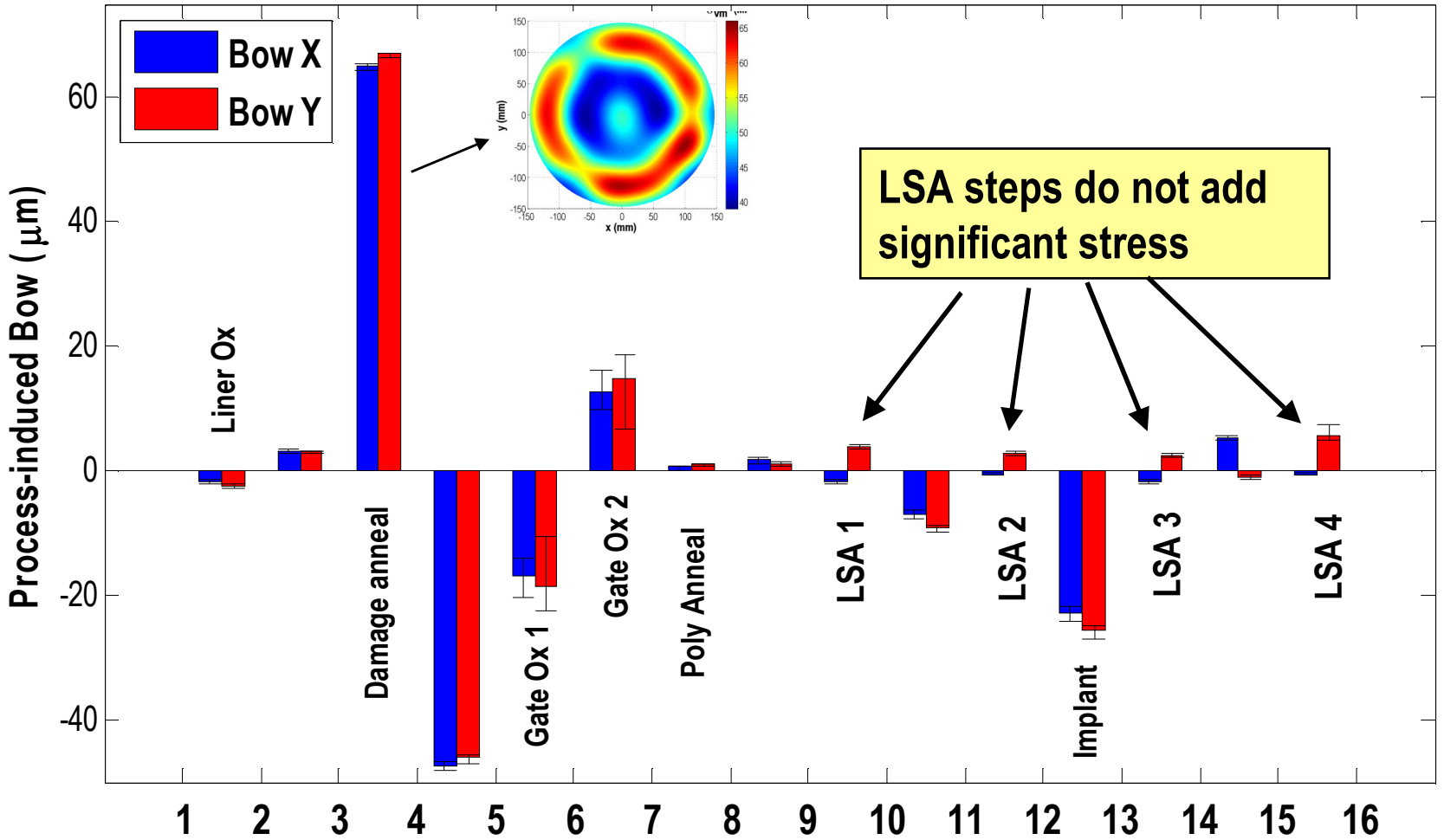


Stress Fingerprinting and Correlation to Leakage

- Coherent Gradient Sensing (CGS) system used to measure wafer level stress at 16 process points in a 65nm DSP process flow
- Measurement points span ~120 process steps from wafer start through source-drain anneal
- Within-wafer and wafer-to-wafer stress variations were characterized for each process or set of processes
- Correlations between electrical parameters & stress were explored
- Parameters: PMOS & NMOS drive current, leakage current, drain current and threshold voltage
- Data used to identify which process steps and stress metrics to which electrical performance is most sensitive

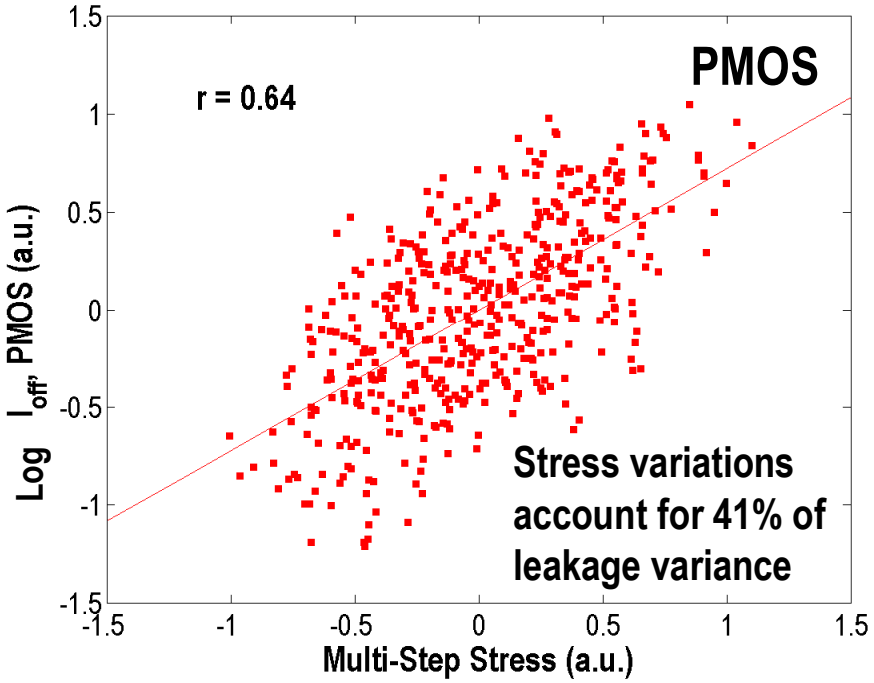
Stress fingerprinting results

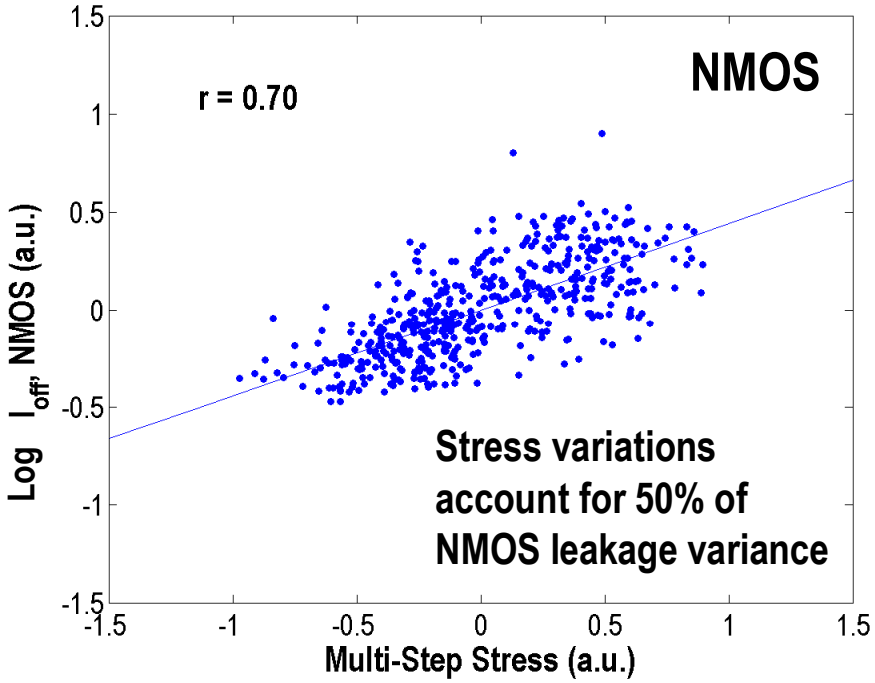
Fingerprinting: Measuring stress & deformation across multiple steps in line



Correlation of stress to leakage current

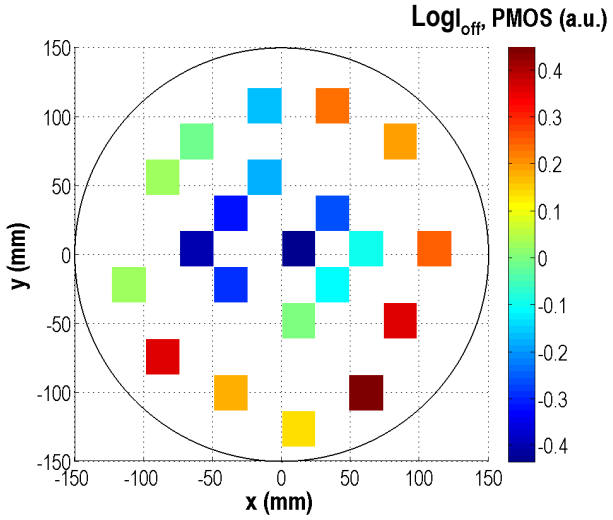
All Points, All Wafers, All Steps



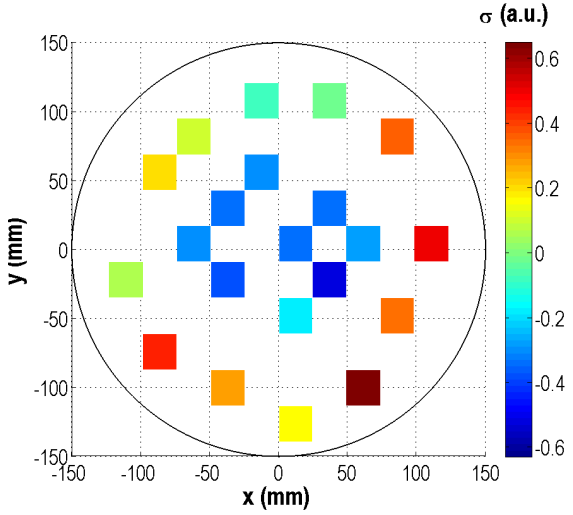


- There is a significant correlation between wafer level stress and leakage
- Most of the leakage variation is due to within-wafer stress variations
- Low stress of LSA does not contribute significantly to stress correlated leakage

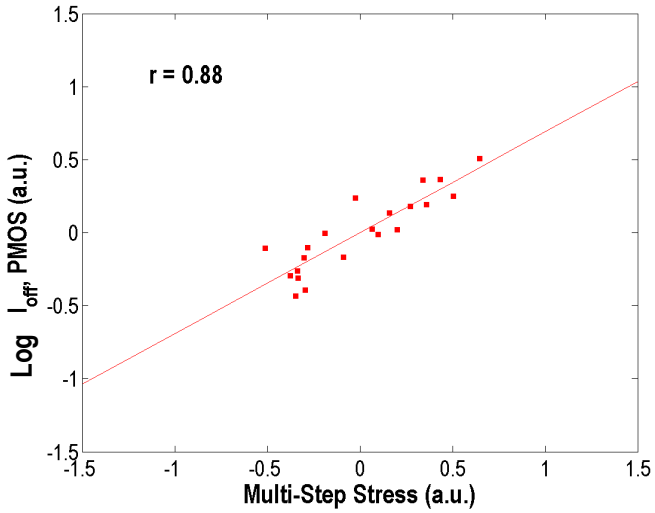
PMOS I_{OFF}: Within Wafer Variation



Within-Wafer Variation of Leakage Current



Within-Wafer Variation of Stress (Multiple Steps)



- Data for each die location represents the average of all 24 wafers in lot
- Within wafer stress variations correspond to leakage current variations

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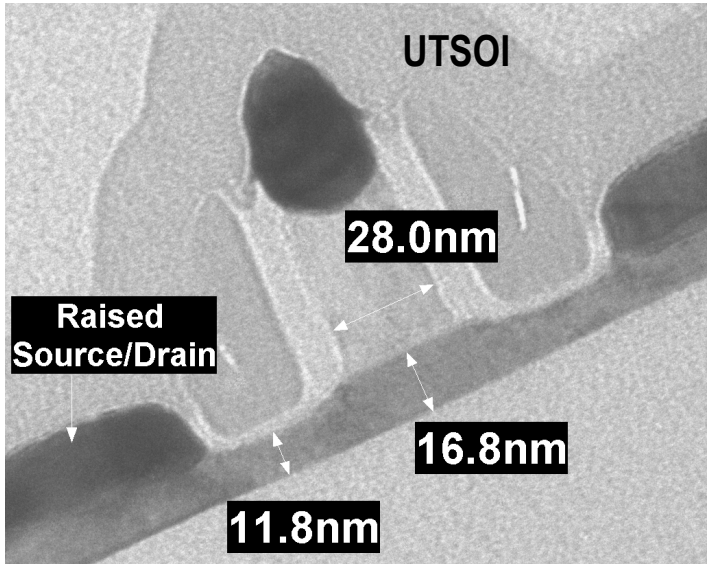
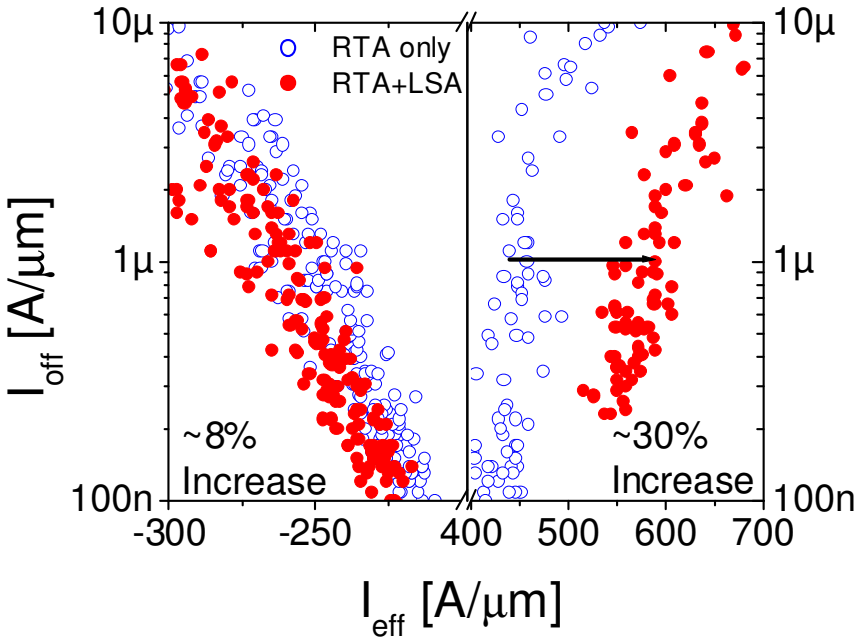
LSA Application To UTSOI

IBM Alliance, VLSI-TSA 2006

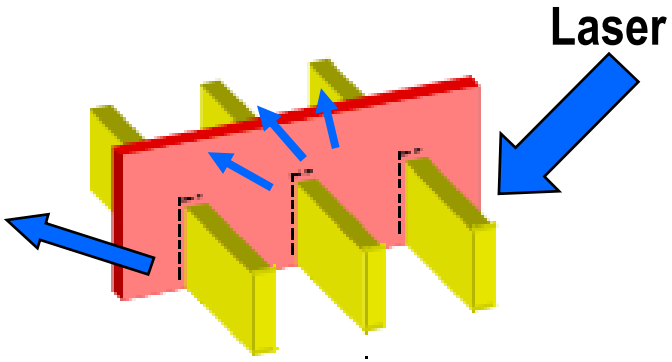




LSA gives 30% enhancement in Ieff & 10% improvement in RO speed for UTSOI

Compatibility With Non-Planar Structures

High aspect ratio fins

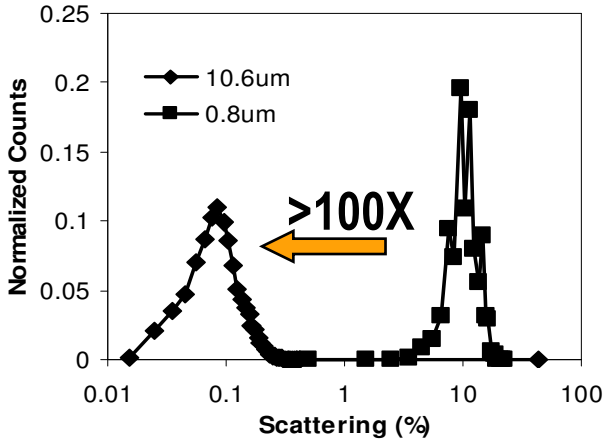


Total Integrated Scattering:

$$TIS = \frac{P_s}{RP_i} \approx \left(\frac{4\pi\sigma}{\lambda}\right)^2$$

σ is rms surface roughness

- Shadowing effects?
  - Thin Si fin is transparent to CO2 wavelength, no shadowing effects
- Scattering effects?
  - Height is still << 10.6um, so scattering is minimal for LSA



- Long wavelength reduces total amount of scattering

Summary

- Market trends create stringent requirements for simultaneous high performance and low leakage for advanced CMOS
- LSA tool architecture has inherent advantages for achieving high anneal temperatures, which can be used to reduce leakage
- LSA is compatible with HK+MG because pattern suppression extends to thin metal layers
- LSA has inherent advantages for low stress which make it compatible with strain engineering techniques, and may reduce leakage correlated with wafer-level stress
- LSA is compatible with transistor architectures that may be used at 22nm