Thermal Processing Issues For 22nm Node Junction Scaling

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Solid State Technology August 2009

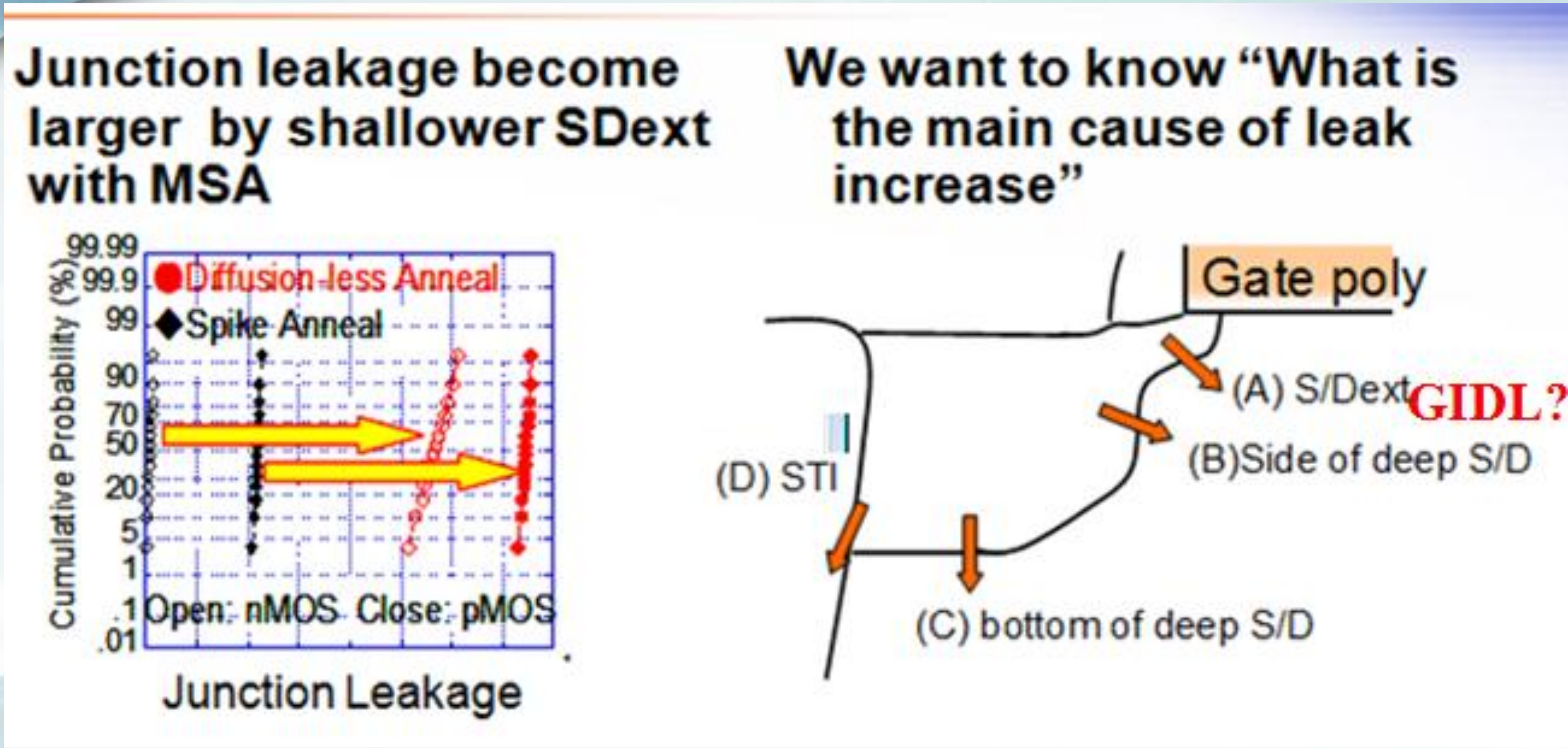
Executive Overview

Junction scaling for 22nm node planar and FinFET CMOS requires low energy implantation but the surface oxide thickness will determine the energy (>83eV) and dose. Engineering the surface amorphous layer maximizes dopant activation, reduces implant damage and junction leakage with sub-melt laser or flash lamp annealing. The annealing process and equipment must be optimized to prevent strain relaxation, high-k/metal gate stack failure and wafer breakage.

Outline

- Executive Overview
- **Introduction**
  - **Defect and junction leakage reduction**
  - **JOB Technologies:**
    - **22nm low defect and leakage p+ USJ**
    - **22nm high activation n+ USJ**
    - **22nm eSiC strain by implant ation**
    - **16nm FinFET high tilt implant retained dose**
- Planar CMOS Doping
- FinFET CMOS Doping
- MSA Process And Equipment Design Issues
- Summary
- Acknowledgements

NEC IEDM-2008: Transistor Leakage (A+B+C+D)



A=HALO (BTBT)
B=HALO & PAI (EOR damage)
C=Residual implant damage & HALO?
D=STI stress induced leakage

Low Damage Implantation

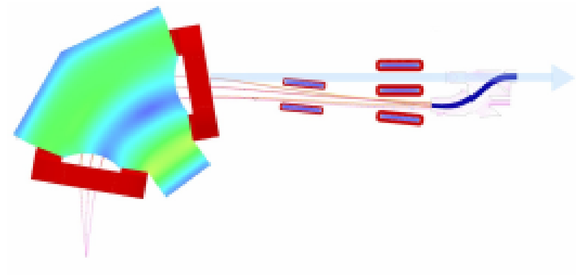
- Improve self-amorphization, lower critical implant doses for amorphization and smooth amorphous interfaces thereby reducing EOR damage and residual implant damage while enhancing dopant activation with MSA
  - Higher implant beam current or dose rate improves self-amorphization
  - Lower implant wafer temperature (cold or cryo-implantation) 0C to -160C using chilled water of liquid nitrogen wafer cooling
  - Use molecular dopants (B18H22, B36H44, As4 or P4) improves self-amorphization
  - Use heavier ions for PAI (In, Sb or Xe), also He-PAI
- Stable defects and reduction in residual implant damage thereby improving junction leakage
  - Higher MSA peak temperature
  - Pre/post MSA diffusion-less spike/RTA<900C

Outline

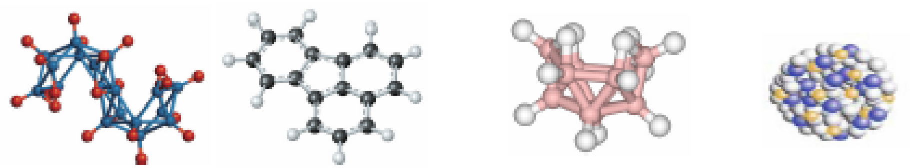
- Introduction
- **Planar CMOS Doping**
  - **22nm and 16nm node**
- FinFET CMOS Doping
- MSA Process And Equipment Design Issues
- Summary & Next

Low Energy Implant Approach

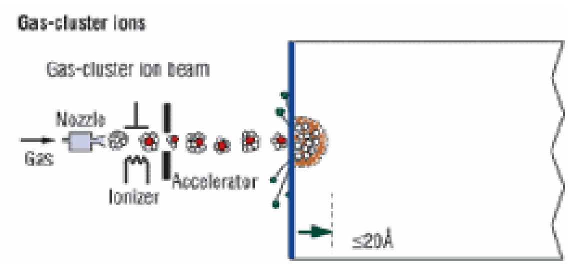
- **Monomer ion beam:**
  - Deceleration of higher energy ion beam



- **Molecular ion beam;**
  - Using $B_{18}H_{22}$, $C_2B_{10}H_{12}$ and $B_{10}H_{14}$
  - Gas-cluster ion

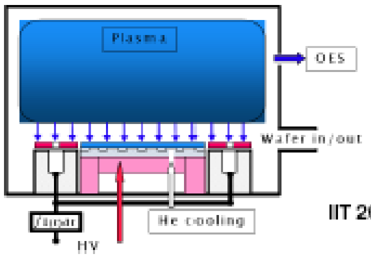


http://www.semequip.com/ http://en.wikipedia.org/wiki/Decaborane



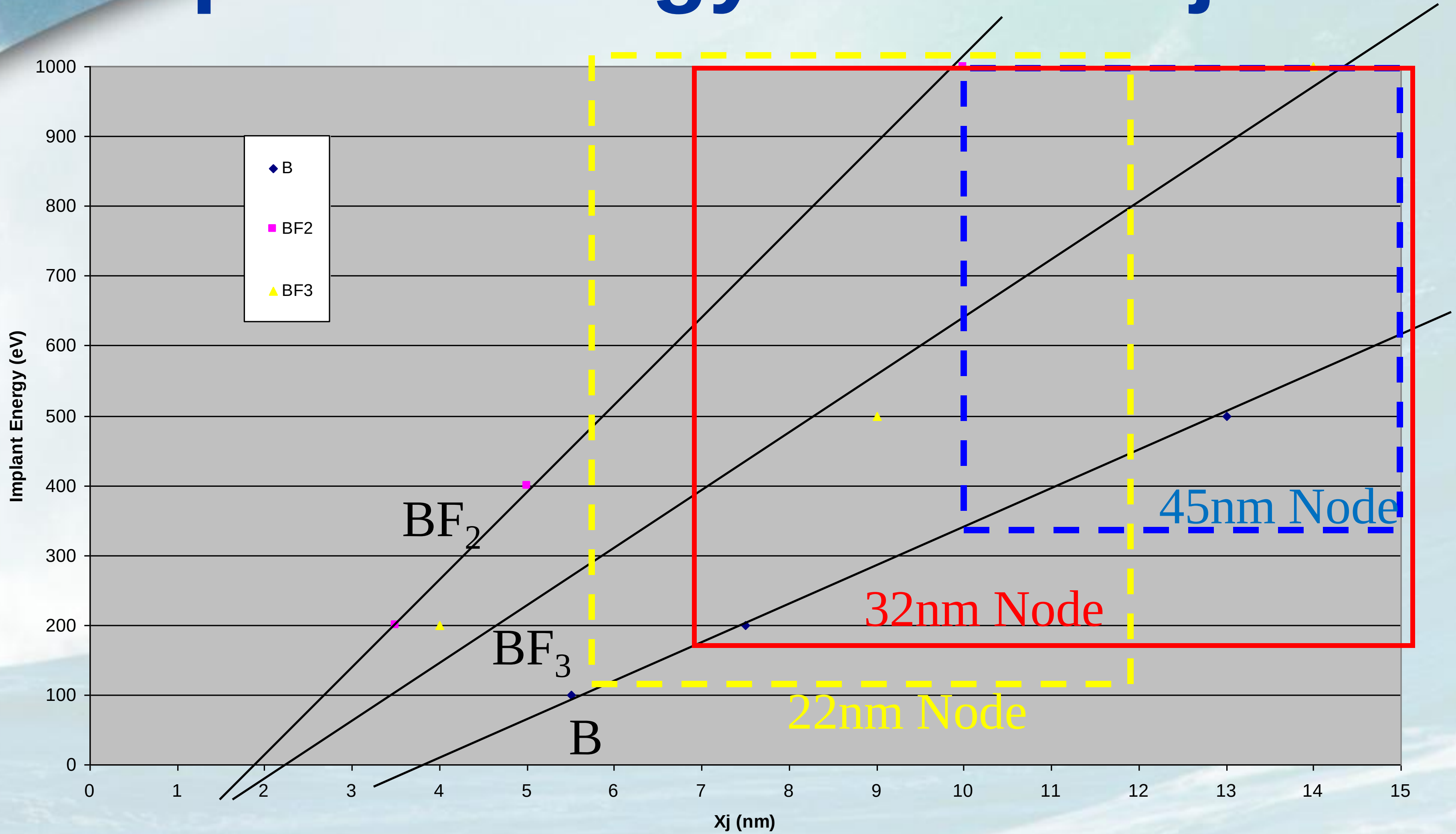
Solid State Technology, May 2004, John Borland,

- **Plasma doping**
  - High density plasma, B_2H_6, BF_3



IIT 2006, E.. Winder

Implant Energy Versus Xj



Borland, Semiconductor International, Dec. 2006, p.49

22nm Node p+ USJ Using Xe-PAI & Laser Annealing

John Ogawa Borland, J.O.B. Technologies, Aiea, Hawaii

Zhimin Wan, AIBT, San Jose, CA

Shankar Muthukrishnan & Jeremy Zelenko, Applied Materials, Sunnyvale, CA

Iad Mirshad & Walt Johnson, KLA-Tencor, San Jose, CA

Temel Buyuklimanli, EAG, East Windsor, NJ

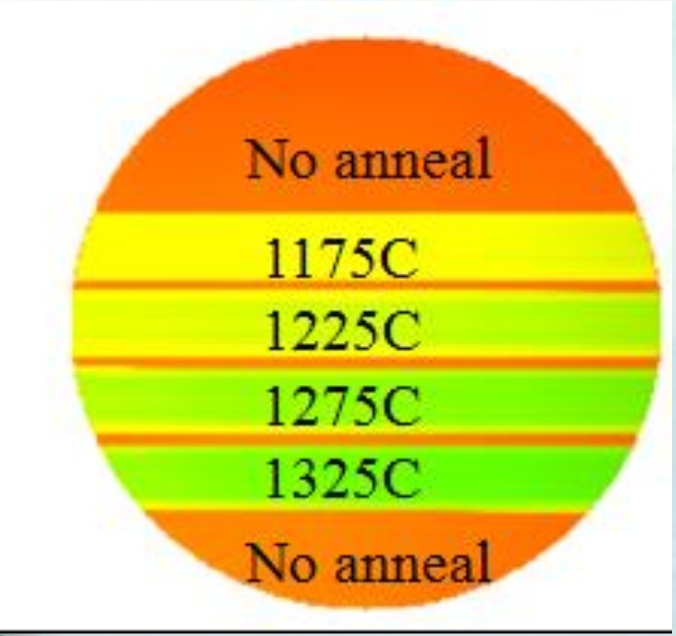
INSIGHTS 2009

April 27, 2009

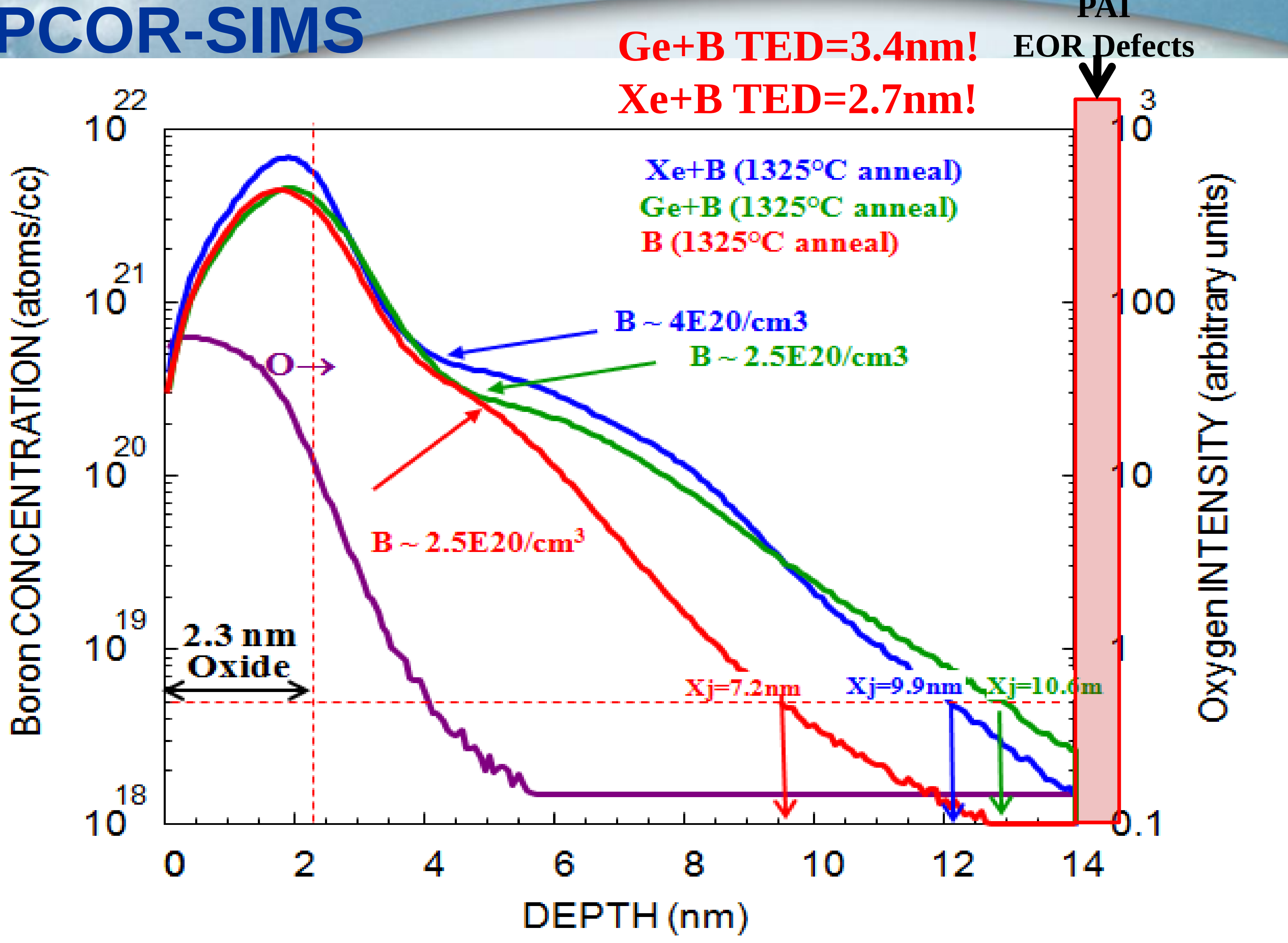
Experimentation & Results

DSA Laser Annealing 1175C→1325C & DSA+900C spike anneal

- **B: 100-350eV/1E15**
  - B, Ge-PAI+B or Xe-PAI+B
- **BF2: 500-890eV/1E15**
  - BF2, Ge-PAI+BF2 or Xe-PAI+BF2

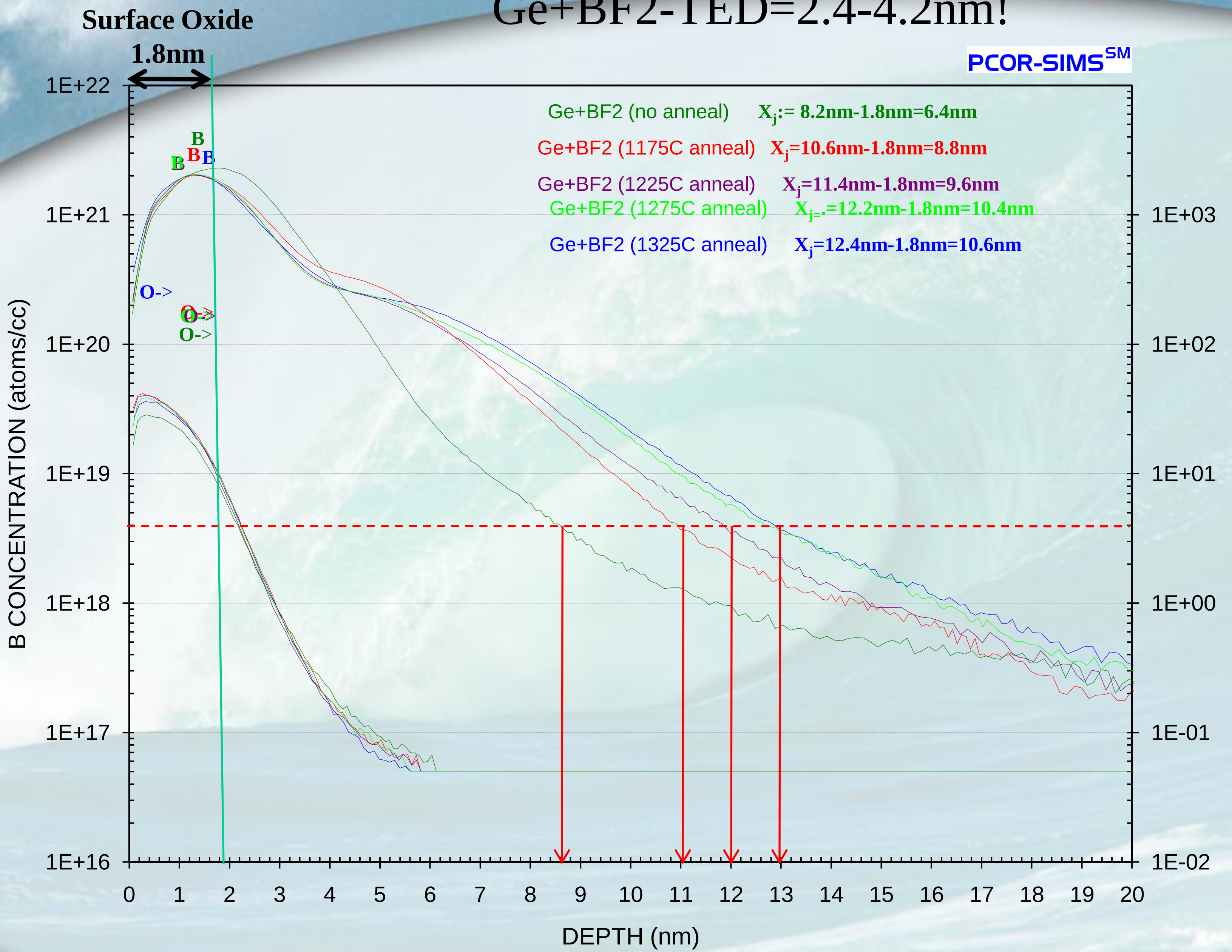


PCOR-SIMS



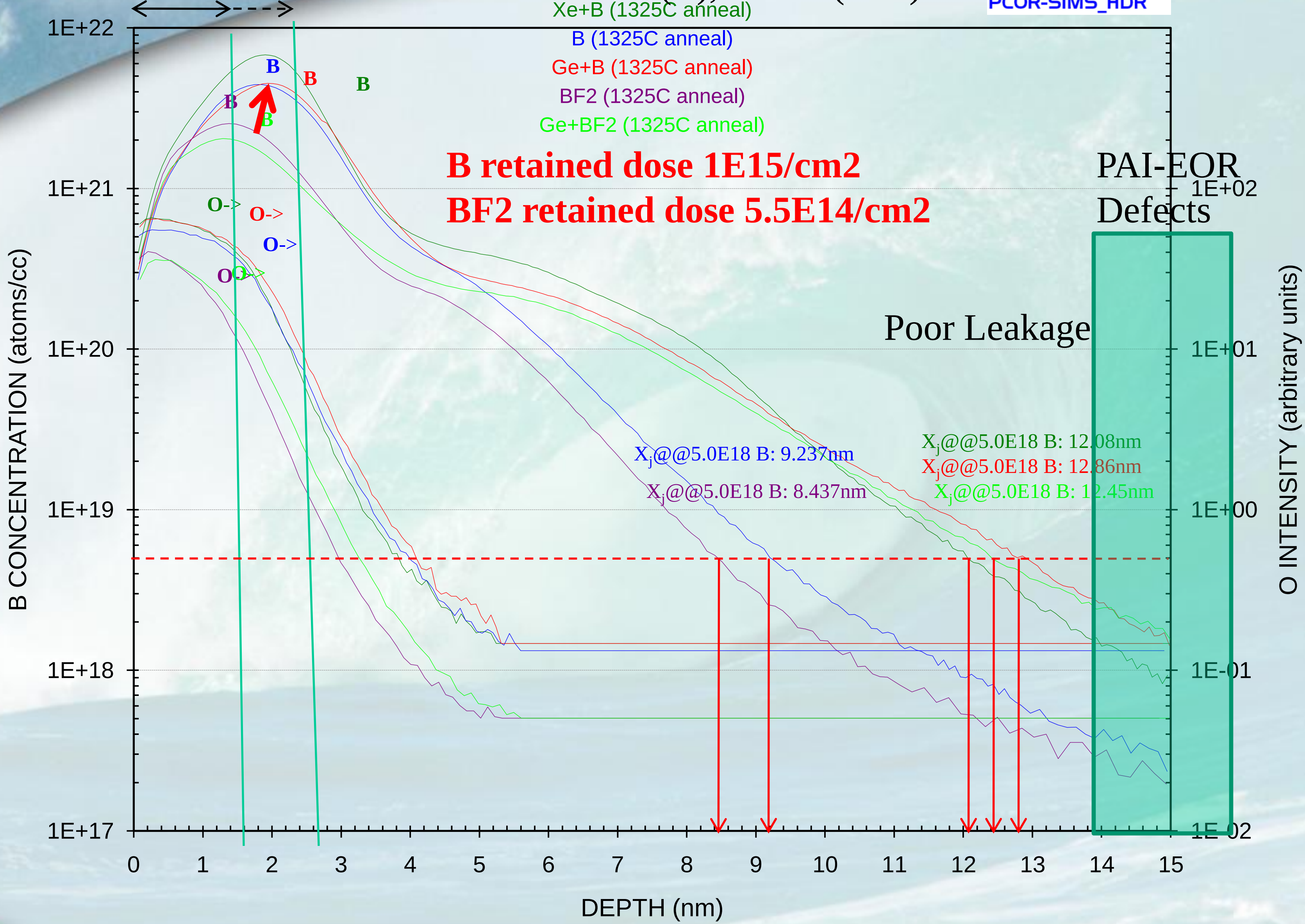
Ge+B TED=3.4nm!
Xe+B TED=2.7nm!
PAI
EOR Defects
Xe+B (1325°C anneal)
Ge+B (1325°C anneal)
B (1325°C anneal)
B ~ 4E20/cm3
B ~ 2.5E20/cm3
B ~ 2.5E20/cm³
O→
2.3 nm
Oxide
Xj=7.2nm
Xj=9.9nm
Xj=10.6m
Boron CONCENTRATION (atoms/cc)
Oxygen INTENSITY (arbitrary units)
DEPTH (nm)
0
2
4
6
8
10
12
14
10^22
10^21
10^20
10^19
10^18
10^3
100
10
1
0.1

Ge+BF2-TED=2.4-4.2nm!

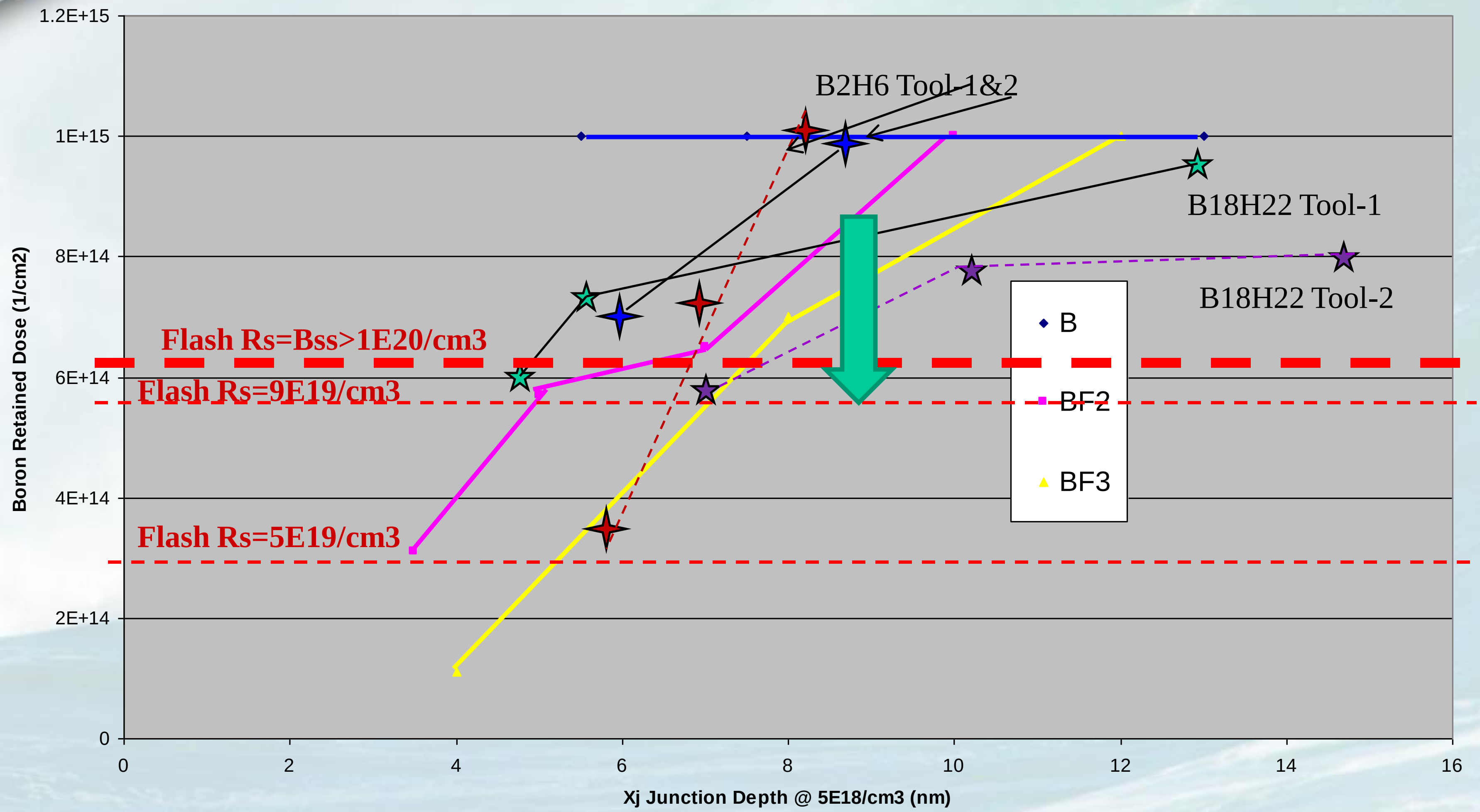


BF2+Ge-PAI Sample21 PCOR_HDR

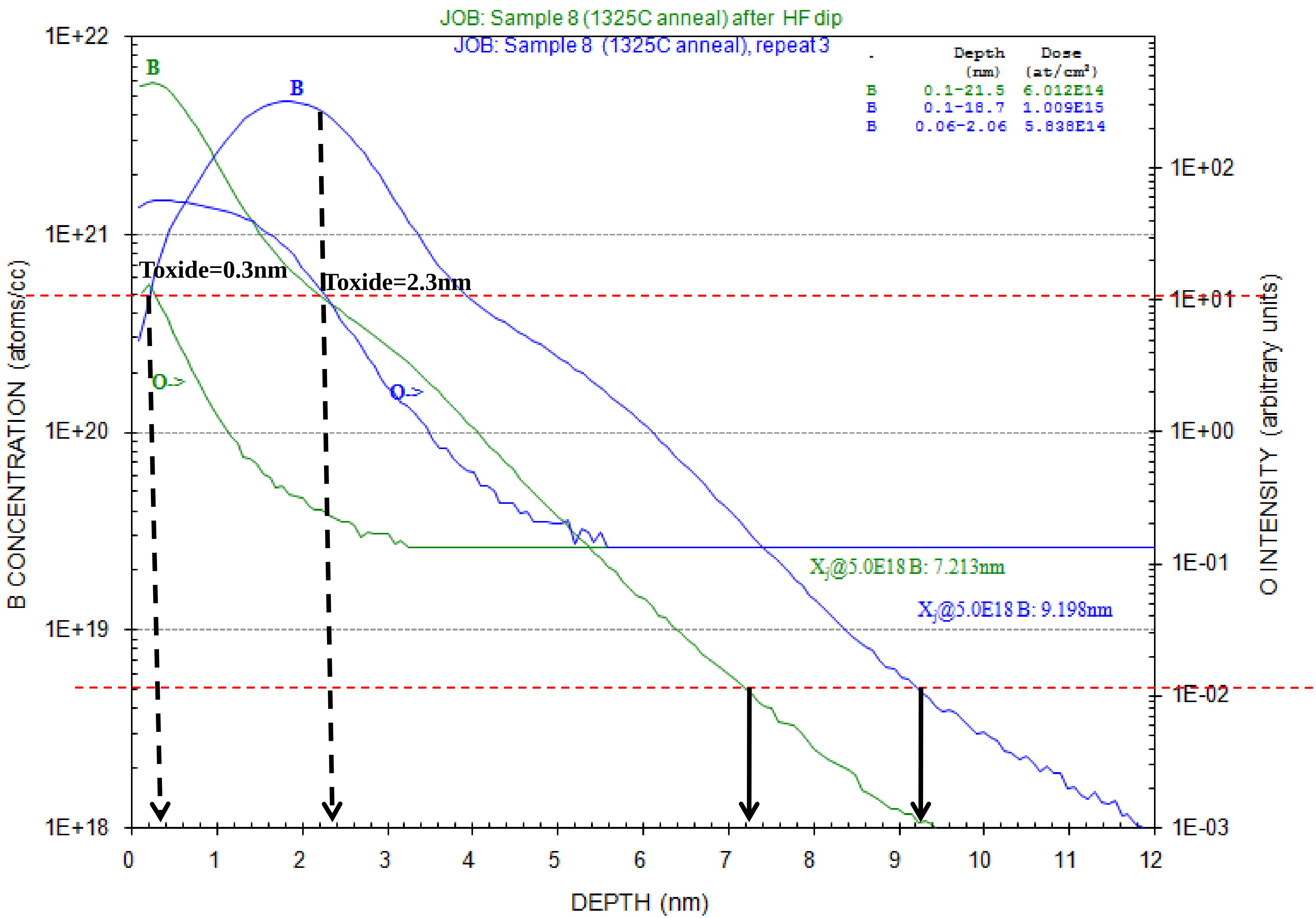
Xe TED=2.5nm (B)
Ge TED=3.5nm (B), 4.2nm (BF2)



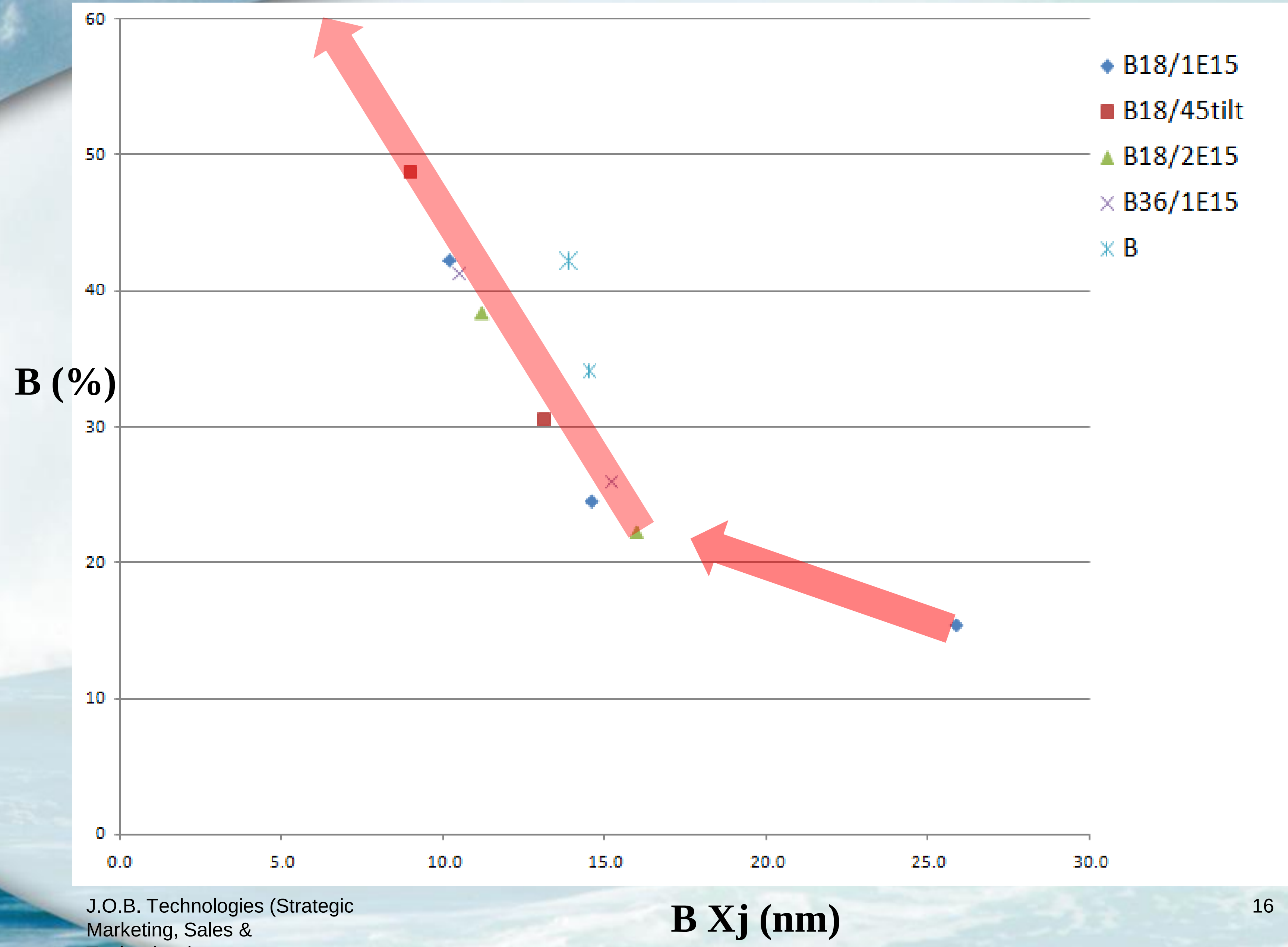
Retained Dose <6E14/cm2 Limits MSA Dopant Activation Level To <Bss (<1.2E20/cm3)!



Borland, Semiconductor International, Dec. 2006, p.49


JOB: Sample 8 (1325C anneal) after HF dip
JOB: Sample 8 (1325C anneal), repeat 3
Depth (nm)
Dose (at/cm²)
B 0.1-21.5 6.012E14
B 0.1-18.7 1.009E15
B 0.06-2.06 5.838E14
B
B
Toxide=0.3nm
Toxide=2.3nm
O->
O->
Xj@5.0E18 B: 7.213nm
Xj@5.0E18 B: 9.198nm
1E+22
1E+21
1E+20
1E+19
1E+18
1E+02
1E+01
1E+00
1E-01
1E-02
1E-03
0
1
2
3
4
5
6
7
8
9
10
11
12
B CONCENTRATION (atoms/cc)
O INTENSITY (arbitrary units)
DEPTH (nm)

% B Dose In 2.0nm Surface Oxide



22nm Node p+ Junction Scaling Using B36H44 And Laser Annealing

J. Borland, J.O.B. Technologies

M. Tanjyo, Nissin Ion Equipment

J. Zelenko, Applied Materials

I. Mirshad & W. Johnson, KLA-Tencor

T. Buyuklimanli, EAG

IEEE/RTP-2009

Oct. 1, 2009

B

Kawasaki et al., Renesas, IWJT-2009, paper S2-4

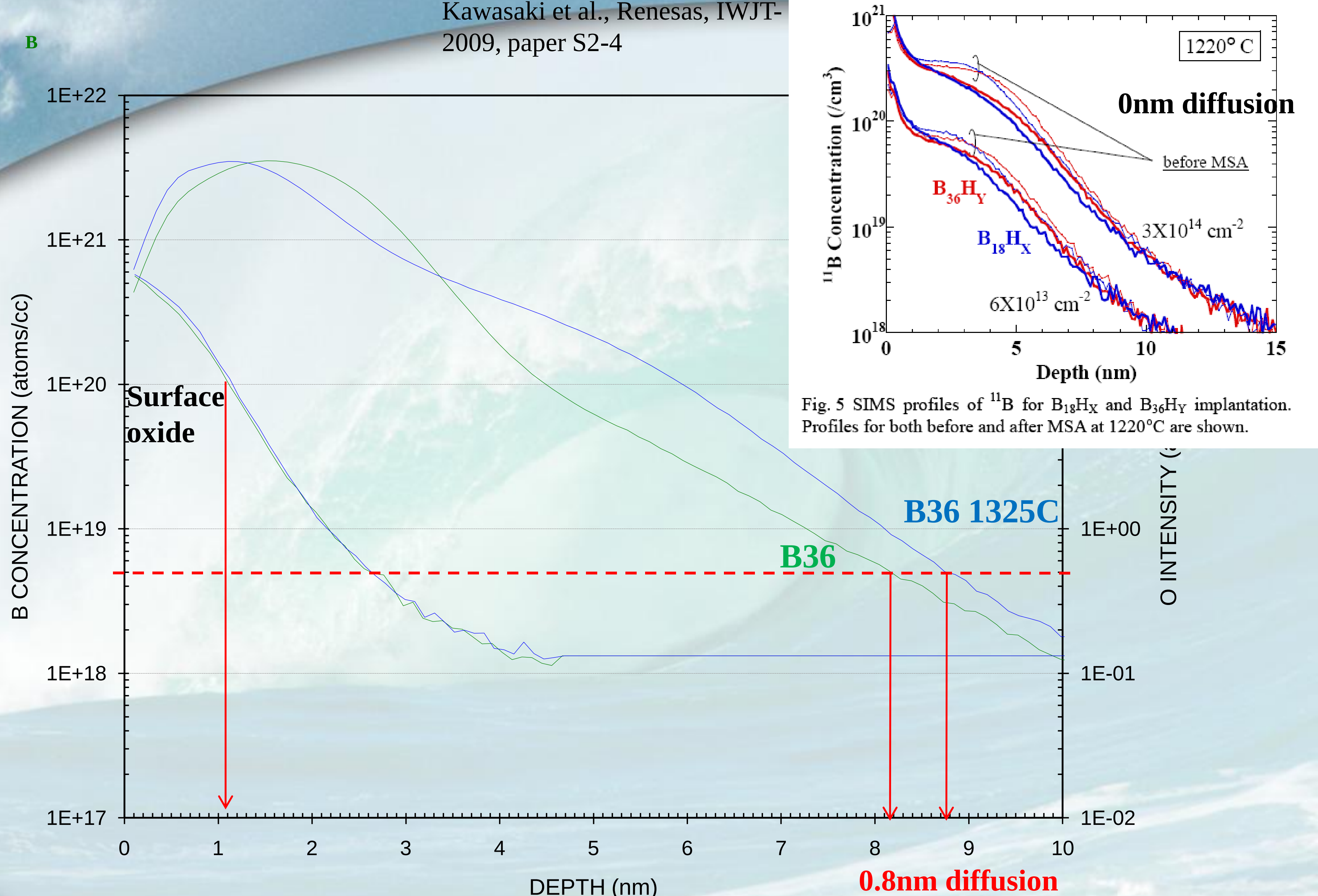
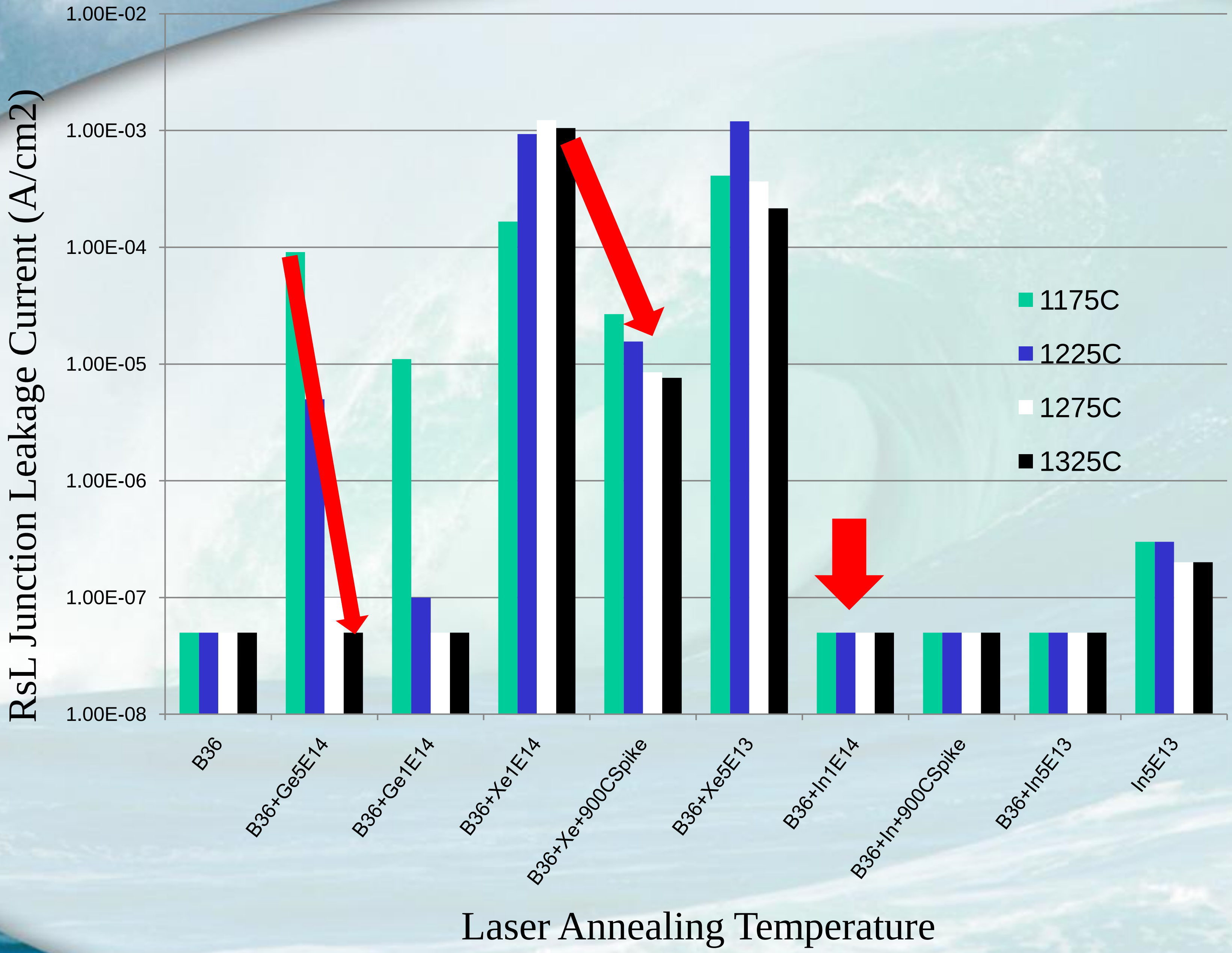
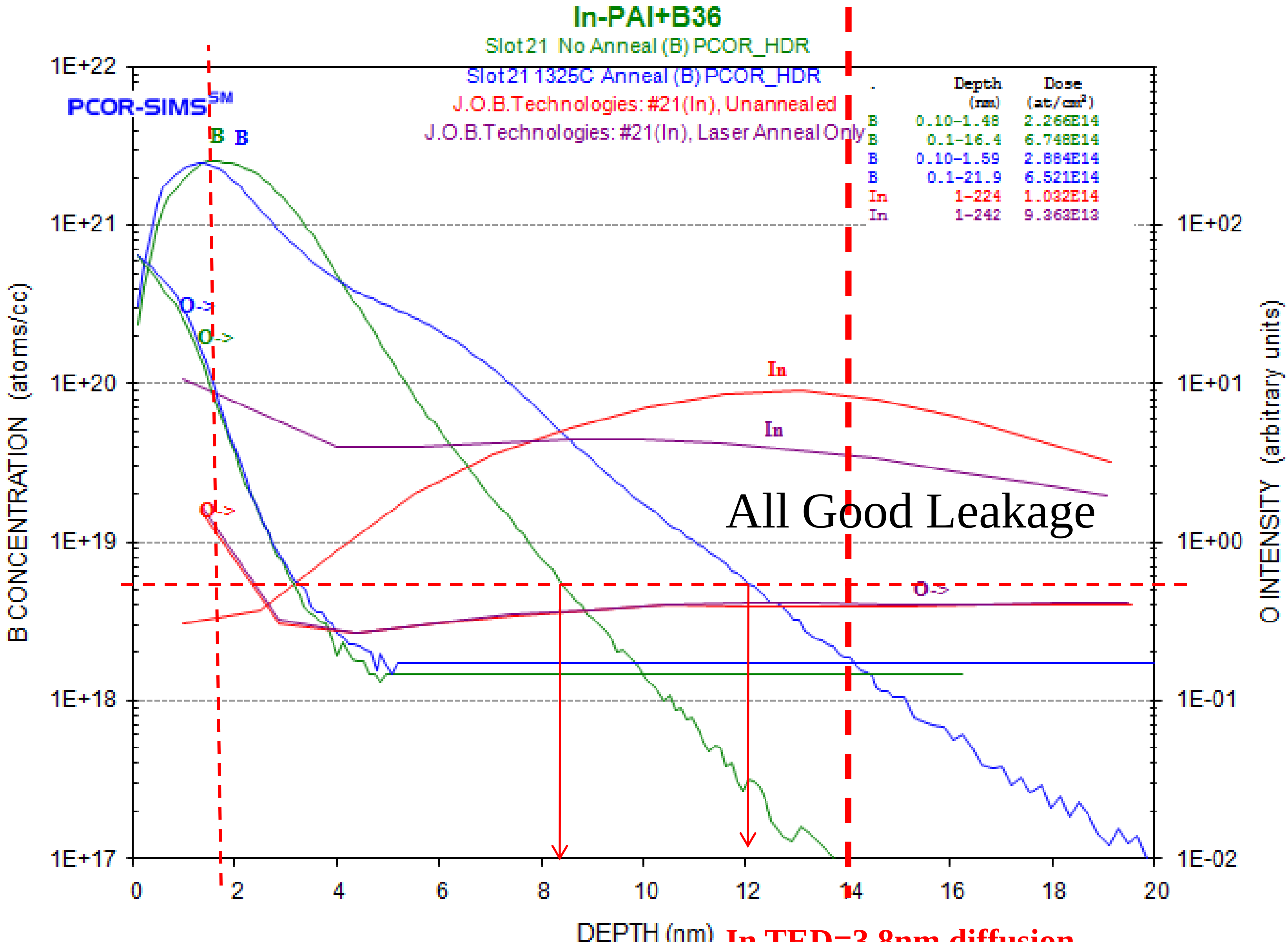


Fig. 5 SIMS profiles of ^{11}B for $B_{18}H_X$ and $B_{36}H_Y$ implantation. Profiles for both before and after MSA at 1220°C are shown.



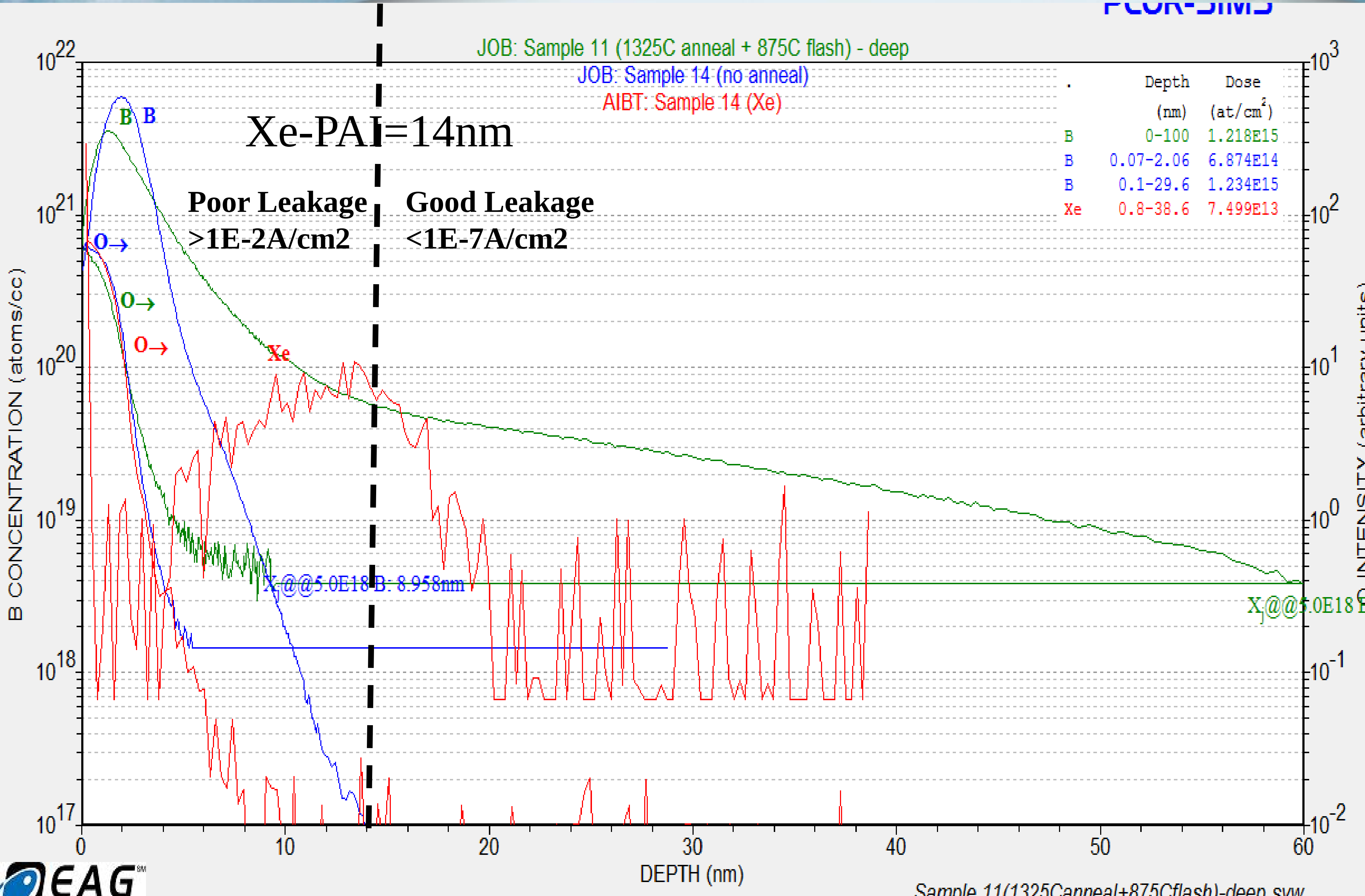
RsL Junction Leakage Current (A/cm2)
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1175C
1225C
1275C
1325C
B36
B36+Ge5E14
B36+Ge1E14
B36+Xe1E14
B36+Xe+900CSpike
B36+Xe5E13
B36+In1E14
B36+In+900CSpike
B36+In5E13
In5E13
Laser Annealing Temperature



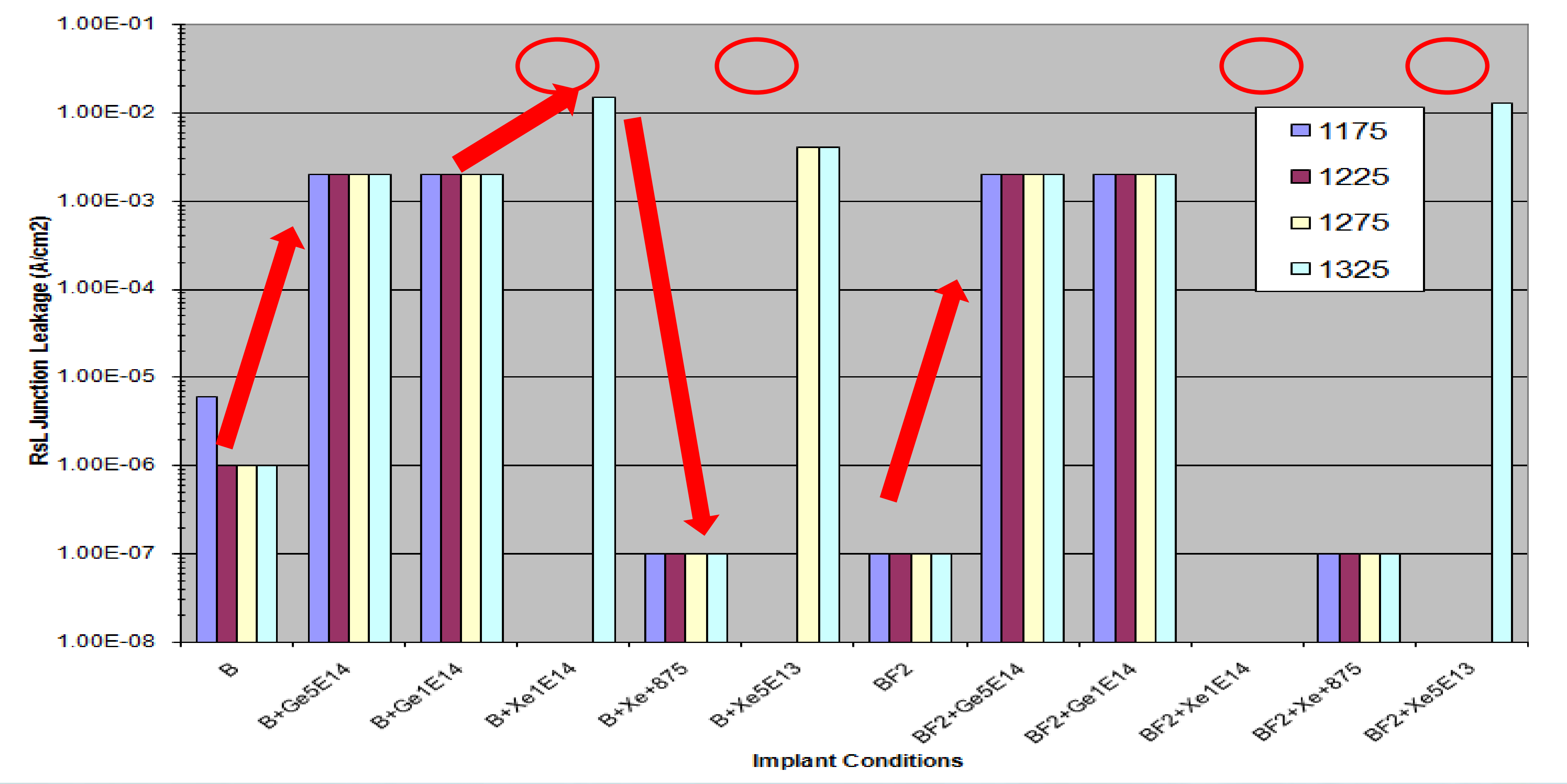
In TED=3.8nm diffusion

Ge TED=5.2nm

Xe TED=3.6nm

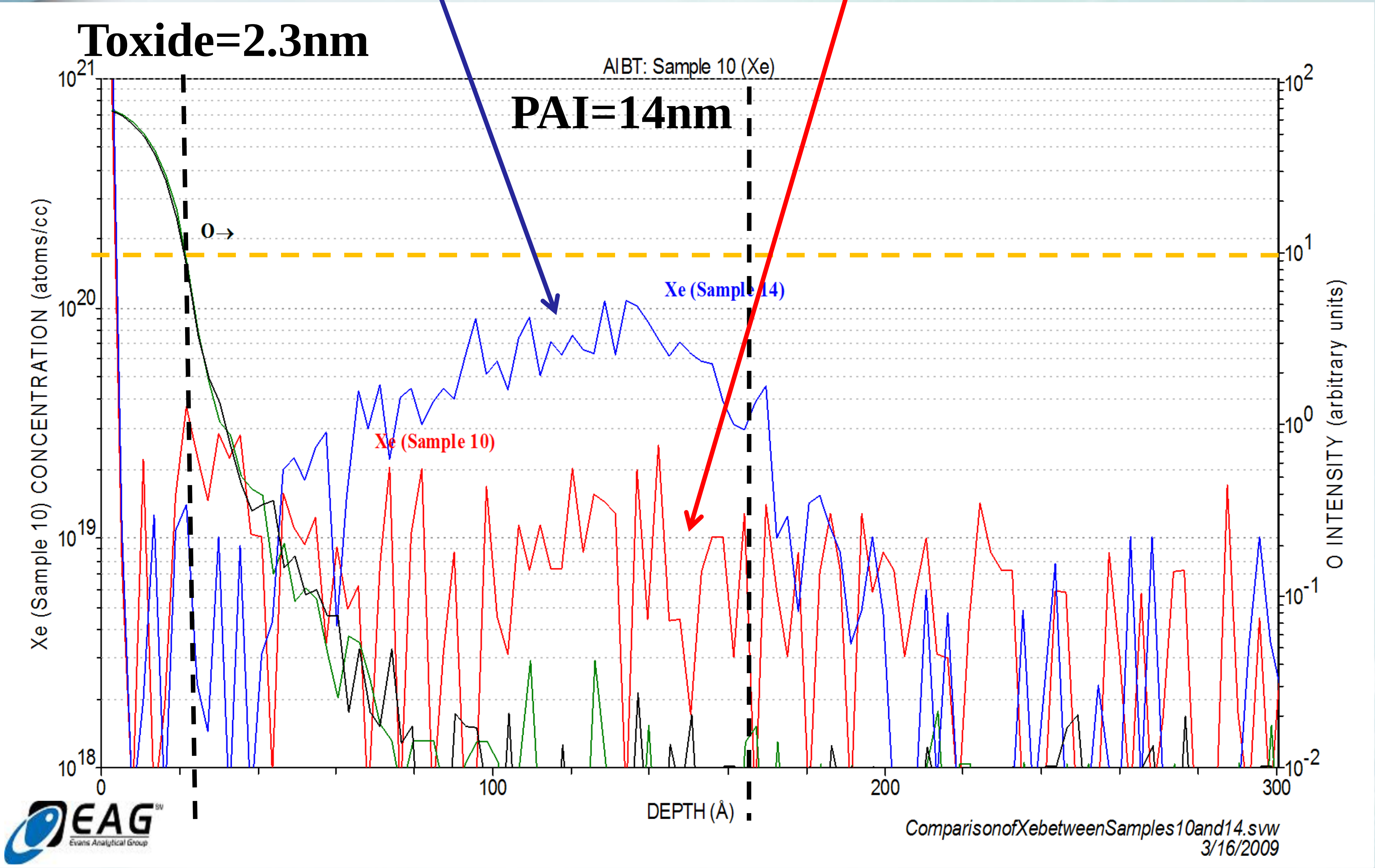


JOB: Sample 11 (1325C anneal + 875C flash) - deep
JOB: Sample 14 (no anneal)
AIBT: Sample 14 (Xe)
Xe-PAI=14nm
Poor Leakage
>1E-2A/cm2
Good Leakage
<1E-7A/cm2
Depth (nm)
Dose (at/cm²)
B 0-100 1.218E15
B 0.07-2.06 6.874E14
B 0.1-29.6 1.234E15
Xe 0.8-38.6 7.499E13
B CONCENTRATION (atoms/cc)
DEPTH (nm)
Xj@@5.0E18 B: 8.958nm
Xe
Sample 11(1325Canneal+875Cflash)-deep.svw

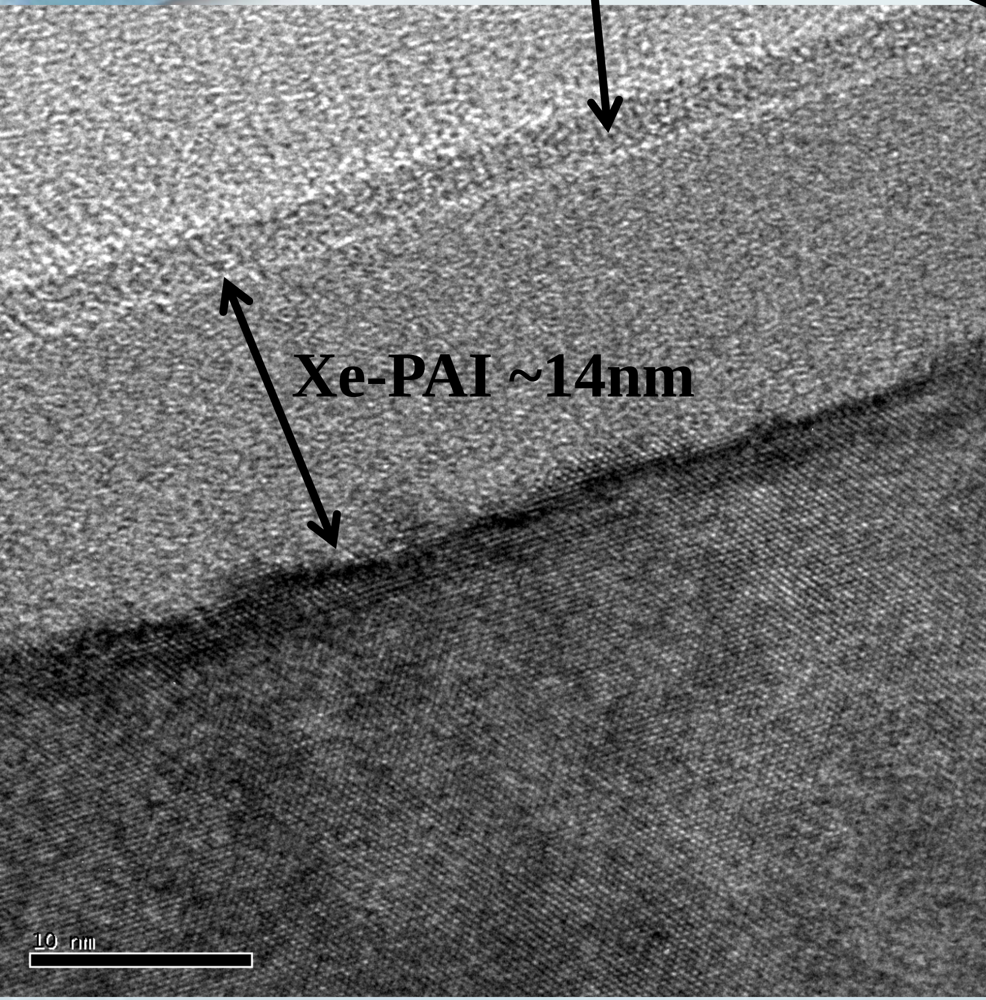


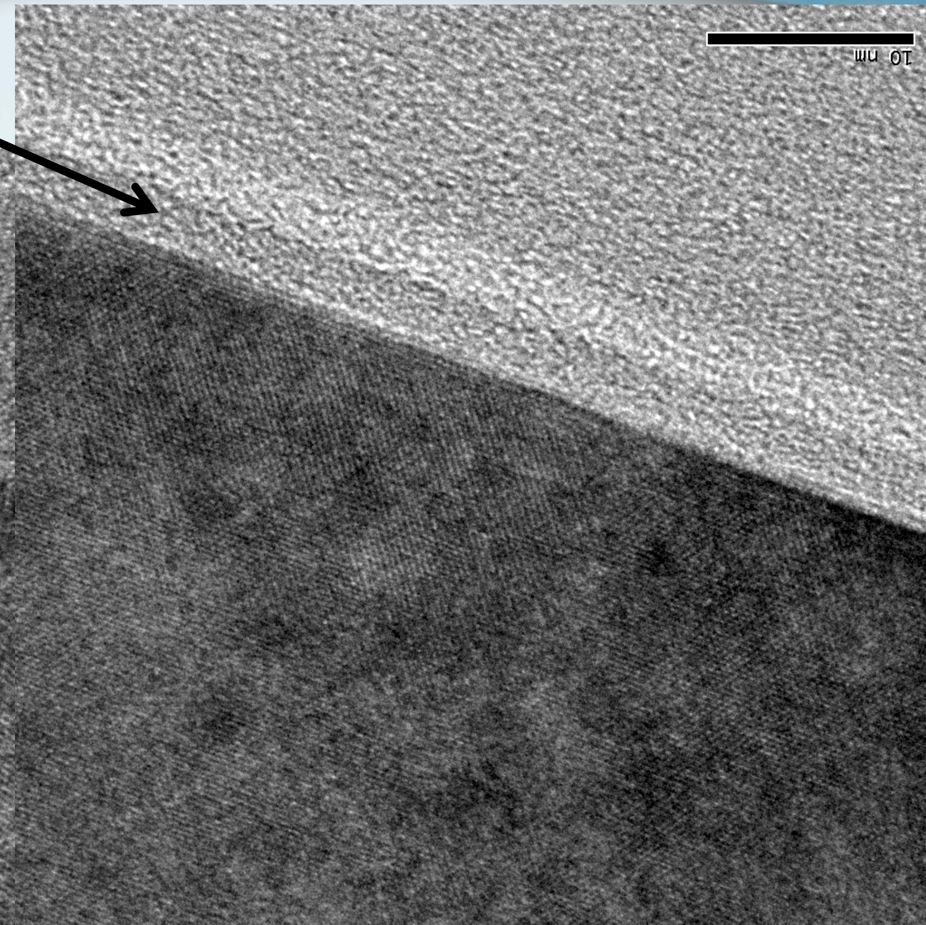
Xj-EOR= -7nm for Xe-PAI & -9nm for Ge-PAI

Xe-PAI No Anneal & 1325C Anneal



Technology)

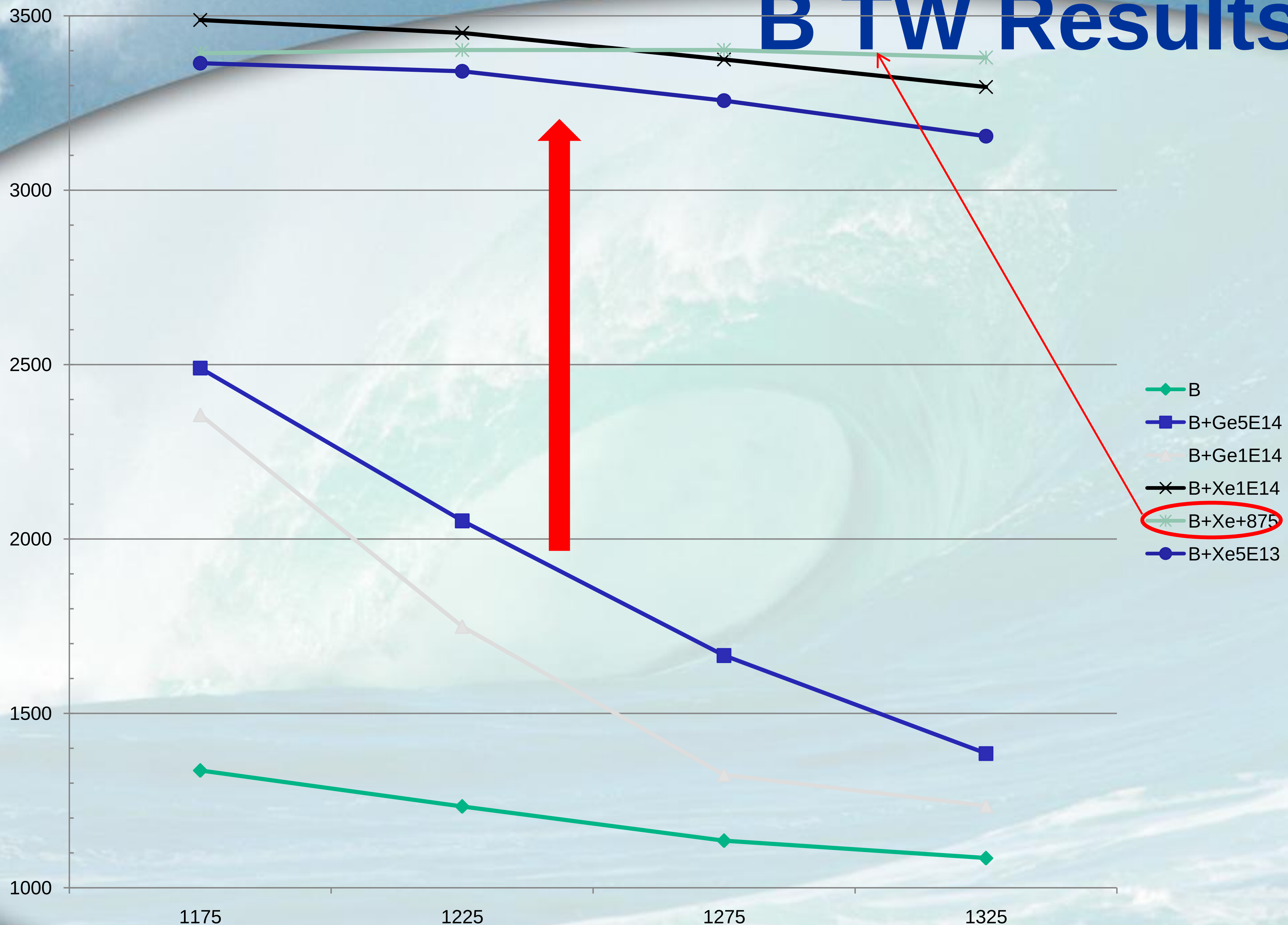




Xe+B 1325C Laser Anneal

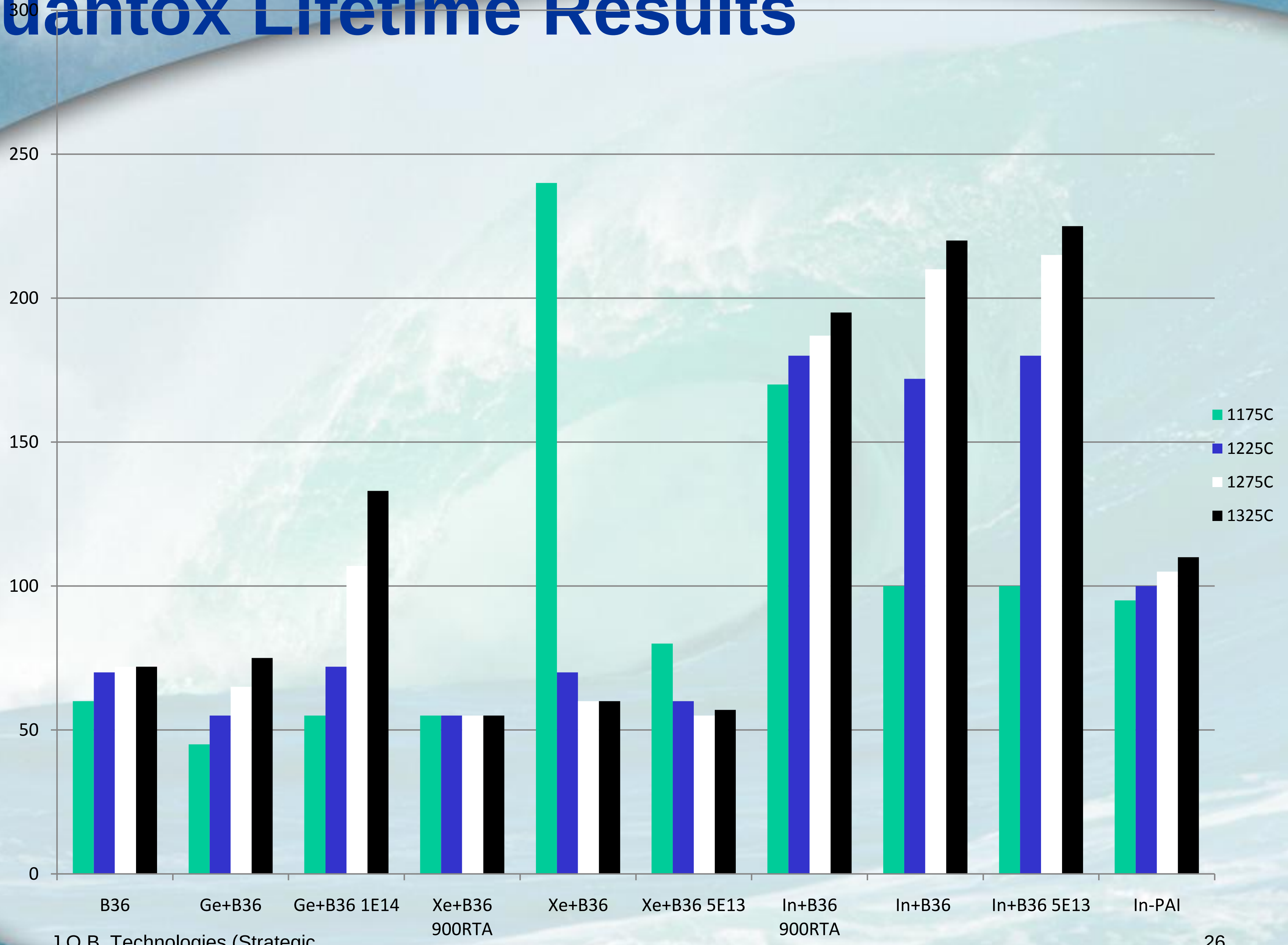
Xe+B No Anneal

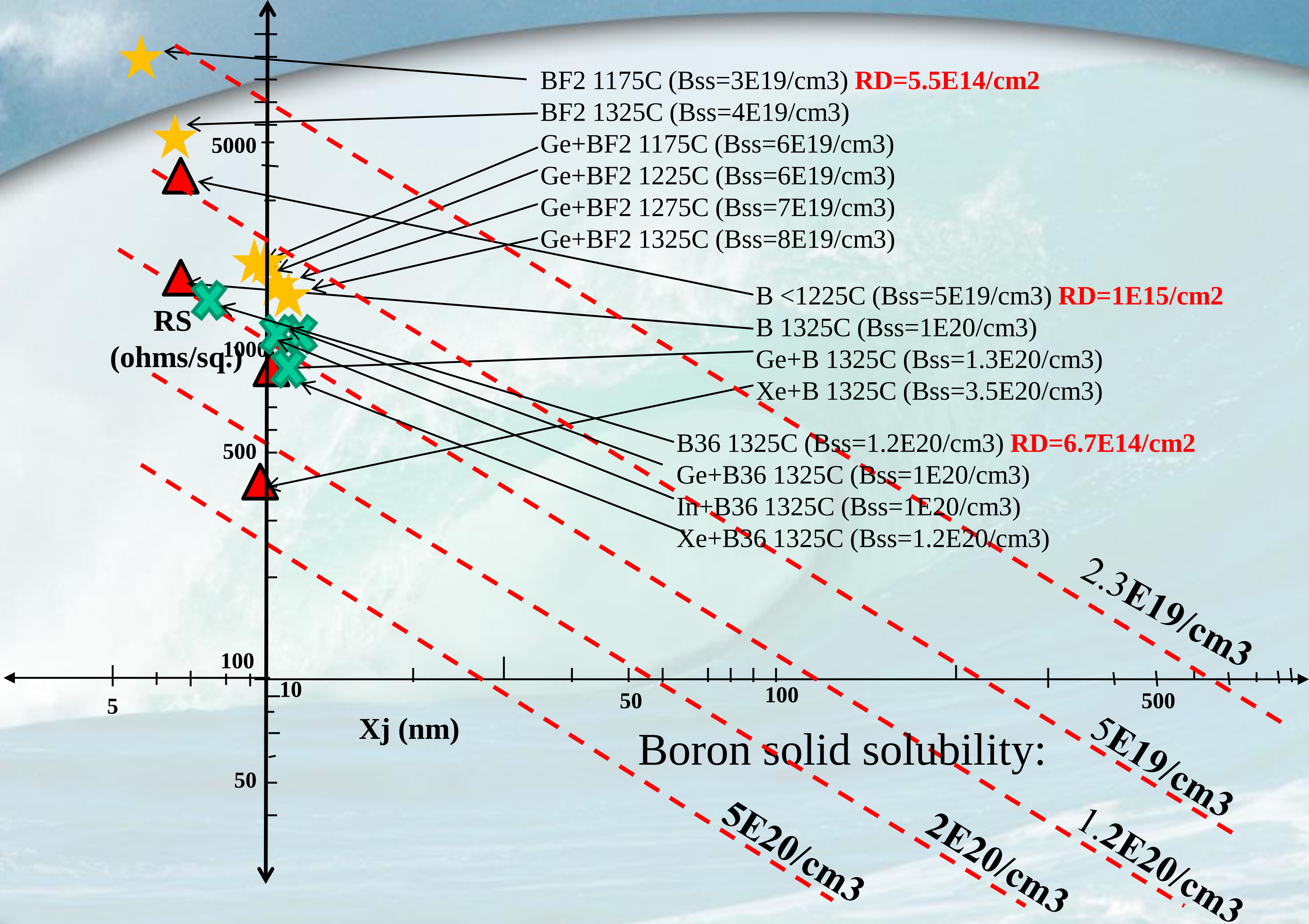
B TW Results



3500
3000
2500
2000
1500
1000
1175
1225
1275
1325
B
B+Ge5E14
B+Ge1E14
B+Xe1E14
B+Xe+875
B+Xe5E13

Quantox Lifetime Results



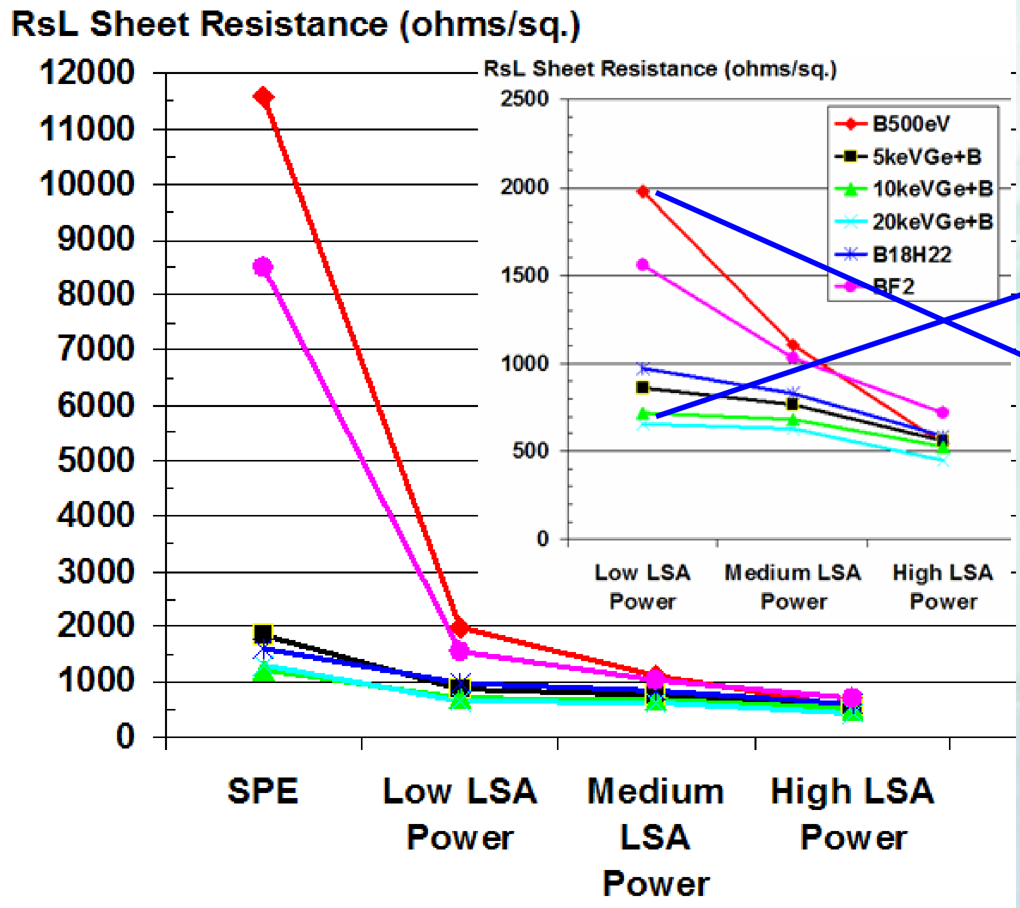


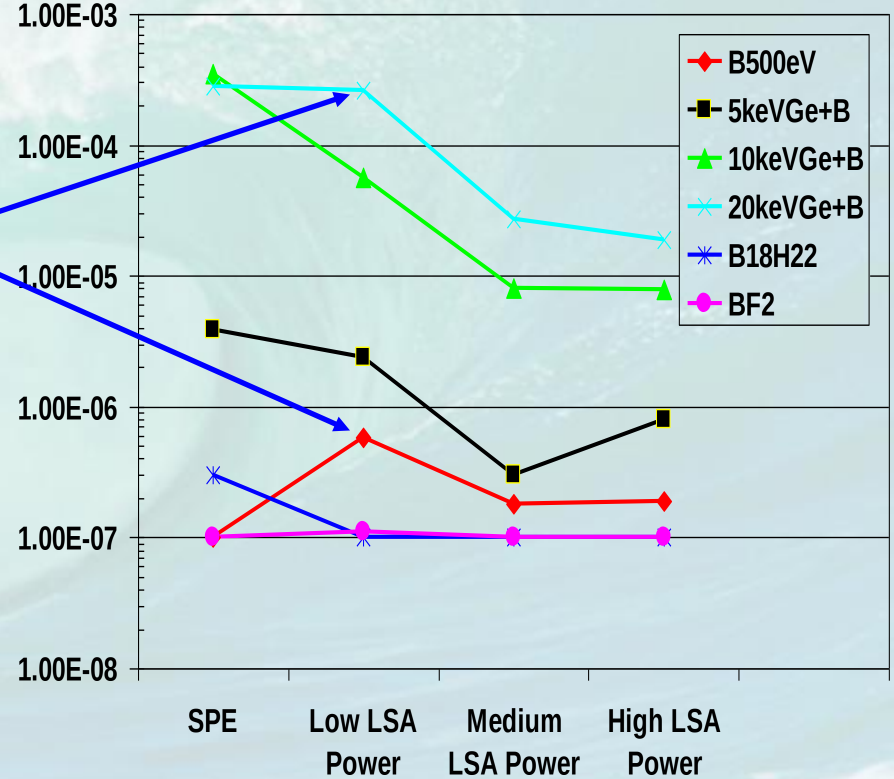
BF2 1175C (Bss=3E19/cm3) RD=5.5E14/cm2
BF2 1325C (Bss=4E19/cm3)
Ge+BF2 1175C (Bss=6E19/cm3)
Ge+BF2 1225C (Bss=6E19/cm3)
Ge+BF2 1275C (Bss=7E19/cm3)
Ge+BF2 1325C (Bss=8E19/cm3)
B <1225C (Bss=5E19/cm3) RD=1E15/cm2
B 1325C (Bss=1E20/cm3)
Ge+B 1325C (Bss=1.3E20/cm3)
Xe+B 1325C (Bss=3.5E20/cm3)
B36 1325C (Bss=1.2E20/cm3) RD=6.7E14/cm2
Ge+B36 1325C (Bss=1E20/cm3)
In+B36 1325C (Bss=1E20/cm3)
Xe+B36 1325C (Bss=1.2E20/cm3)
RS (ohms/sq.)
5000
1000
500
100
50
5
10
50
100
500
Xj (nm)
Boron solid solubility:
2.3E19/cm3
5E19/cm3
1.2E20/cm3
2E20/cm3
5E20/cm3

PAI Enhances Dopant Activation (Bss)

B 500eV Xj=15nm

<u>Ge-PAI</u>	Xj-EOR=+15nm (1E-7A/cm2)
5keV=9nm	Xj-EOR=+6nm (4E-6A/cm2)
10keV=16nm	Xj-EOR=-1nm (3E-4A/cm2)
20keV=32nm	Xj-EOR=-17nm (3E-4Acm2)





Borland et al., JOB Tech/Renesas/FSM/KT, Solid State Technology, July 2008

Insight-2009 & IWJT-2009

- IWJT
  - Varian He-PAI excellent junction leakage
  - UJT He-PAI no EOR defects and (low leakage IIT-2004)
- Oleg of IBM
  - Insight invited paper said that series resistance more critical than SCE so this drives to deeper junctions. Higher dopant activation by adding up to 8 laser passes for As n+ USJ. But gate oxide failure at temperature >1300C.
  - IWJT invited paper said because of difficulties with epi or implant for eSiC a HYBRID approach is another option (SEG+implant) .
- AMD/Dresden IWJT
  - With eSiGe BF2 SDE implant leakage is 5x higher than B and amorphization reduces strain.
  - For eSiC by C-implantation no significant nMOS device improvement.

22nm Node n+ SiC Stressor Using Deep PAI+C_7H_7+P4 With Laser Annealing

IEEE/RTP-2009

John Borland[1], Masayasu Tanjyo[2], Nariaki Hamamoto[2], Tsutomu Nagayama[2], Shankar Muthukrishnan[3], Jeremy Zelenko[3], Iad Mirshad[4], Walt Johnson[4], Temel Buyuklimanli[5], Steve Robie[5], Hiroshi Itokawa[6], Ichiro Mizushima[6] and Kyoichi Suguro[6]

1) J.O.B. Technologies, Aiea, HI

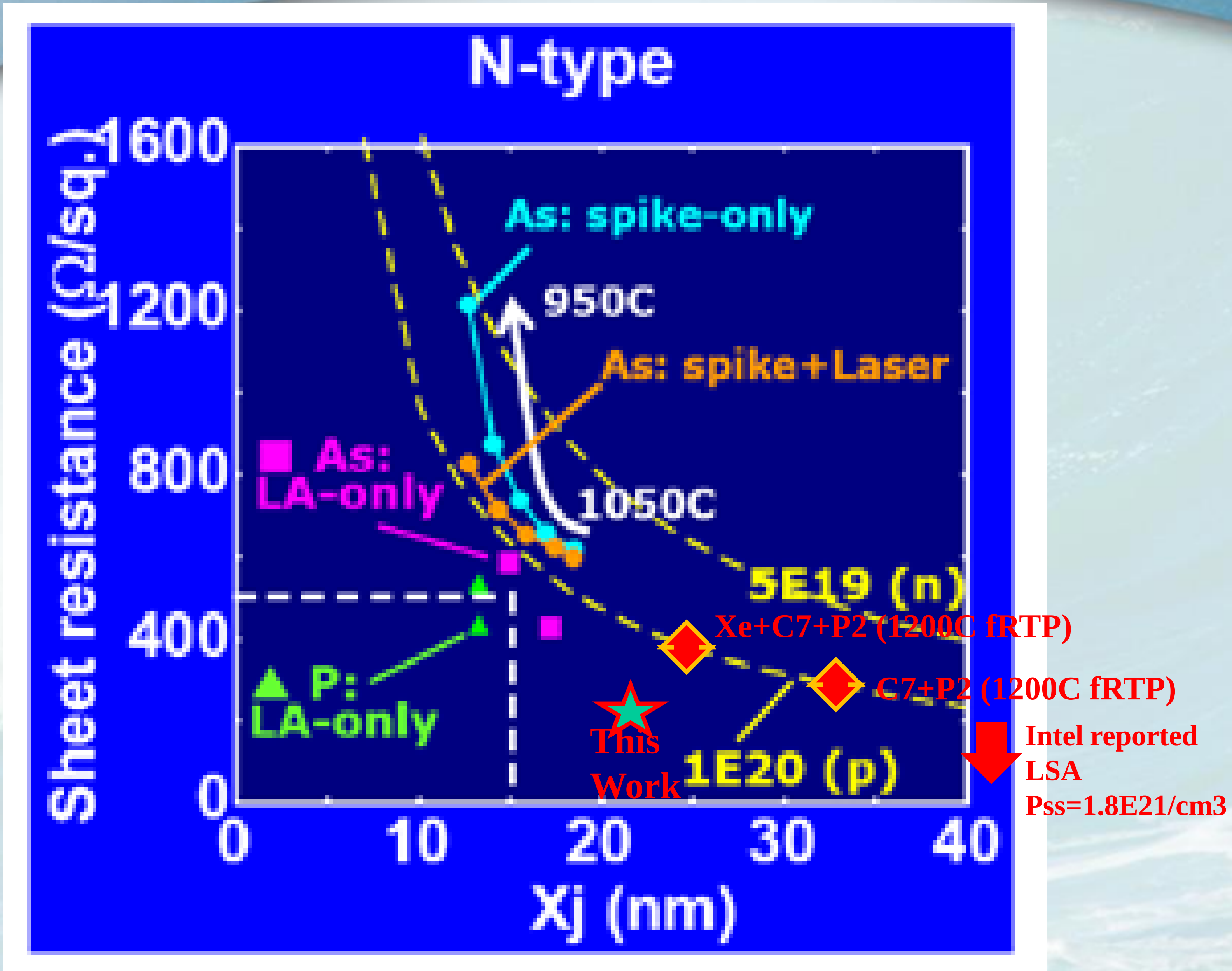
2) Nissin Ion Equipment, Kyoto, Japan

3) Applied Materials, Sunnyvale, CA

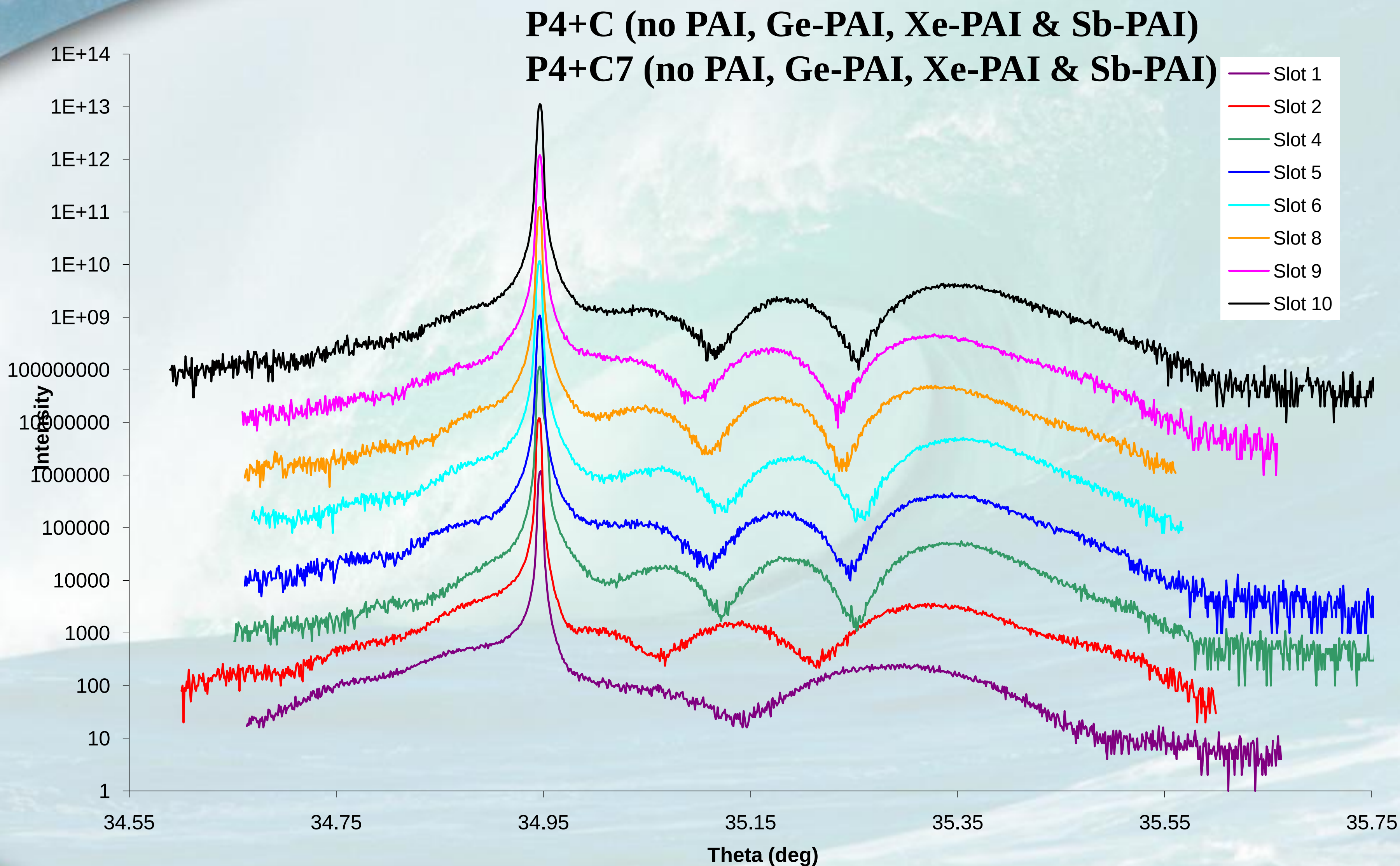
4) KLA-Tencor, San Jose, CA

5) EAG, Sunnyvale, CA

6) Toshiba Corporation, Yokohama, Japan


N-type
Sheet resistance (Ω/sq.)
1600
1200
800
400
0
0
10
20
30
40
Xj (nm)
As: spike-only
950C
As: spike+Laser
As: LA-only
1050C
5E19 (n)
Xe+C7+P2 (1200C fRTP)
C7+P2 (1200C fRTP)
P: LA-only
This Work
1E20 (p)
Intel reported LSA Pss=1.8E21/cm3

C-substituted Si by HRXRD



Outline

- Introduction
- Planar CMOS Doping
- **FinFET CMOS Doping**
  - **16nm Node Bulk or SOI?**
- MSA Process And Equipment Design Issues
- Summary & Next

Summary of FinFET At VLSI Sym-2008 & IEDM-2008

- **VLSI Sym 2008:**
- Planar CMOS to 22nm Node
  - Intel said SRAM needs Bulk FinFET/Trigate at 16nm or Floating Body Cell (Mark Bohr)
    - HK/MG+strain-Si makes pMOS almost equal to nMOS at 45nm node
- **IEDM 2008:**
- ITRS-2008 update (Iwai-san TIT):
  - FD-SOI CMOS delayed until 2013
  - FinFET delayed to 2015 (16nm node)
- Intel:
  - Stated that FinFET not ready for 22nm node manufacturing (K. Kuhn).

IBM Double Gate Fin FET With 30 & 45 Degree High Tilt High Current Implants

SDG (symmetrical double-gate) & ADG (asymmetrical double-gate)

centered for high-performance logic, of <100nA/um at V_{gs}= 0.

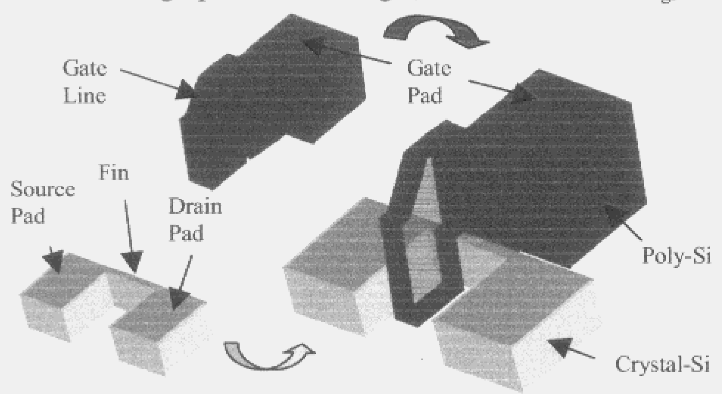
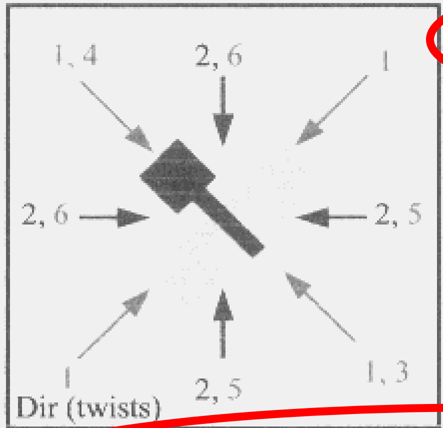


Figure 1: Schematic of the planar FinFET structure. Light(gray) regions indicate the single crystal silicon mesa used for the fin and source/drain pads, dark(red) regions indicate the polysilicon gate line and pad.



SDG extension implants, tilt of 45°, only **one** of following per wafer:

Spec	Dir	Dose /4 (rel)	Ra nm	ΔL nm
As^+	1	1.00	9	18
BF_2^+	1	1.00	9	33
As^+	2	1.00	8	38
BF_2^+	2	1.00	8	50

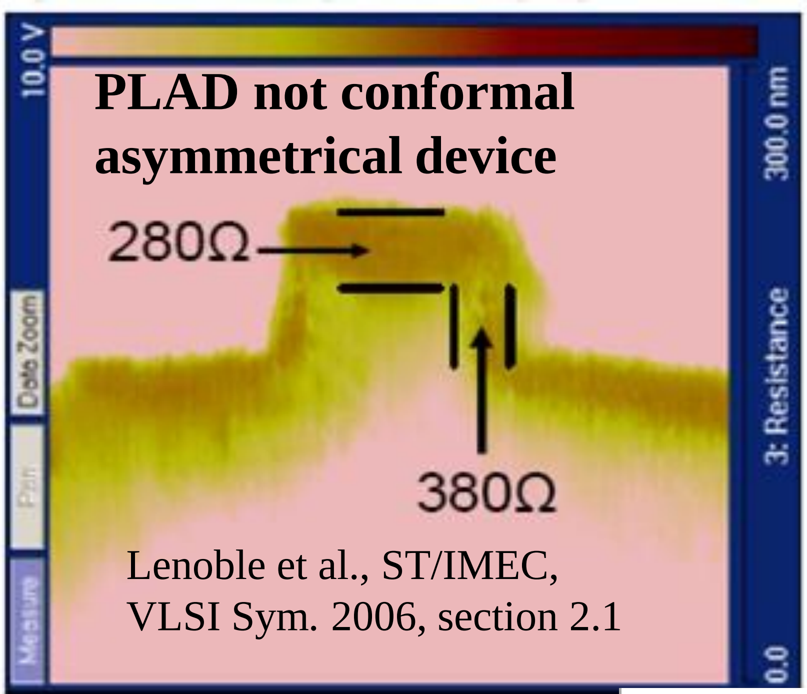
ADG gate and extension implants, tilt of 30°. **Both** of the gate implants were done for each wafer, but only **one** of extension implants per wafer

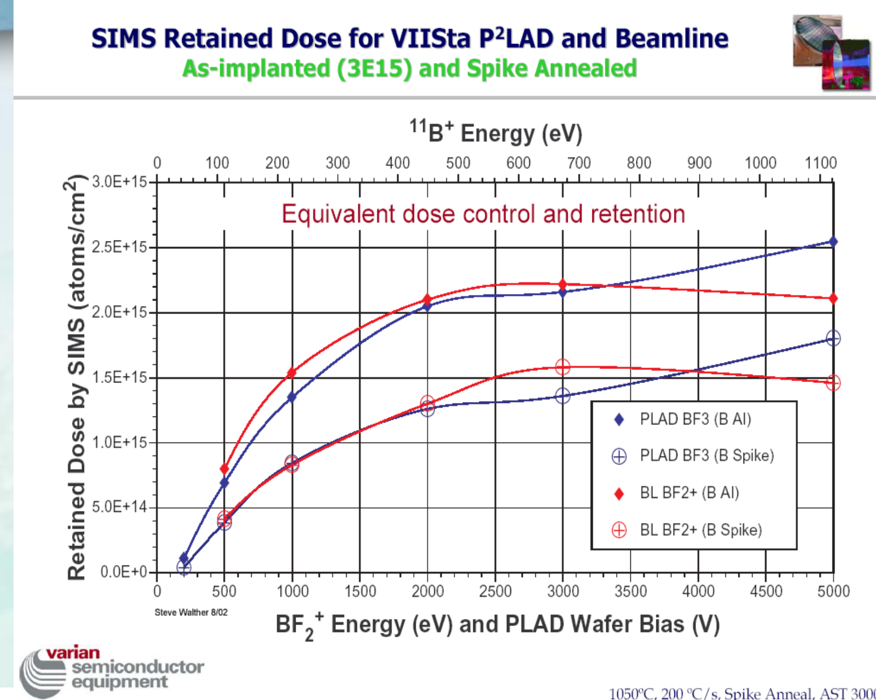
Prior to Gate Etch (both)				**After Gate Etch (only one)**			
Spec	Dir	Dose (rel)	E (rel)	Spec	Dir	Dose /2 (rel)	E (rel)
P	3	0.62	1.00	As	5	1.00	0.50
BF_2	4	0.62	1.00	BF_2	6	1.00	0.25

Table 2: Extension and gate implant conditions. SDG Dose and energy is given in relative units. Ra is the simulated 10% interstitial Si concentration range after implant, measured normal to fin surface.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Kedzierski et al, IEDM-2001





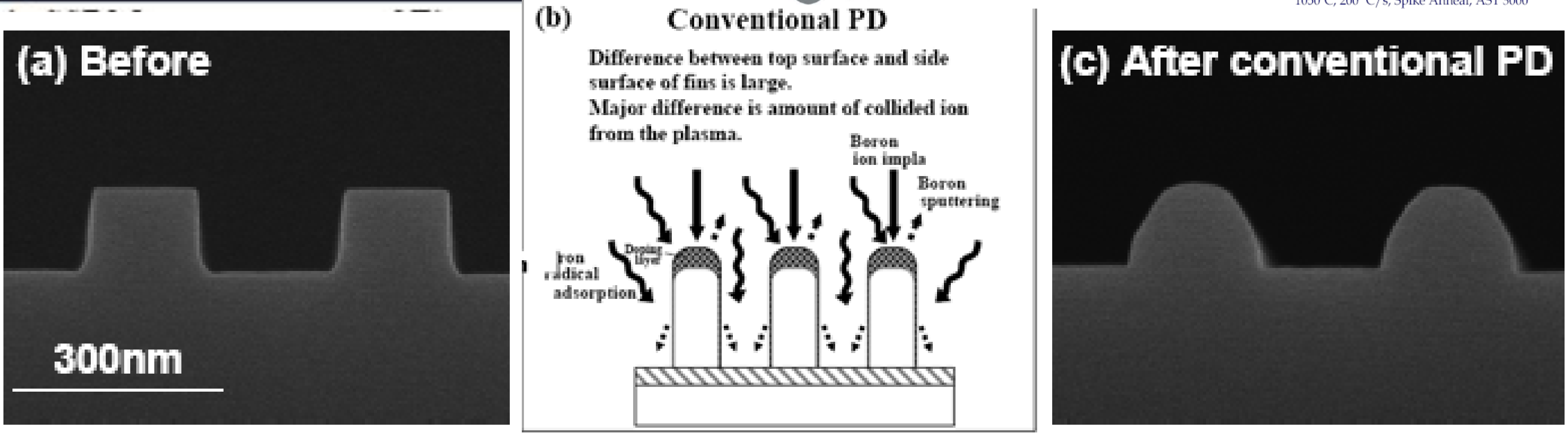


Fig. 4: SEM images; (a) before and (b) after the SRPD process (this work), and (c) after conventional PD.

UJT/Panasonic, IEDM-2008, section 37.3

High Tilt p+ & n+ Molecular Implantation For 3-D Structures: Retained chemical Dose Versus Electrical Activation Limited Conformal Doping

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&

Masayasu Tanjyo, Tsutomu Nagayama and Nariaki Hamamoto

Nissin Ion Equipment, Kyoto, Japan

INSIGHTS 2009

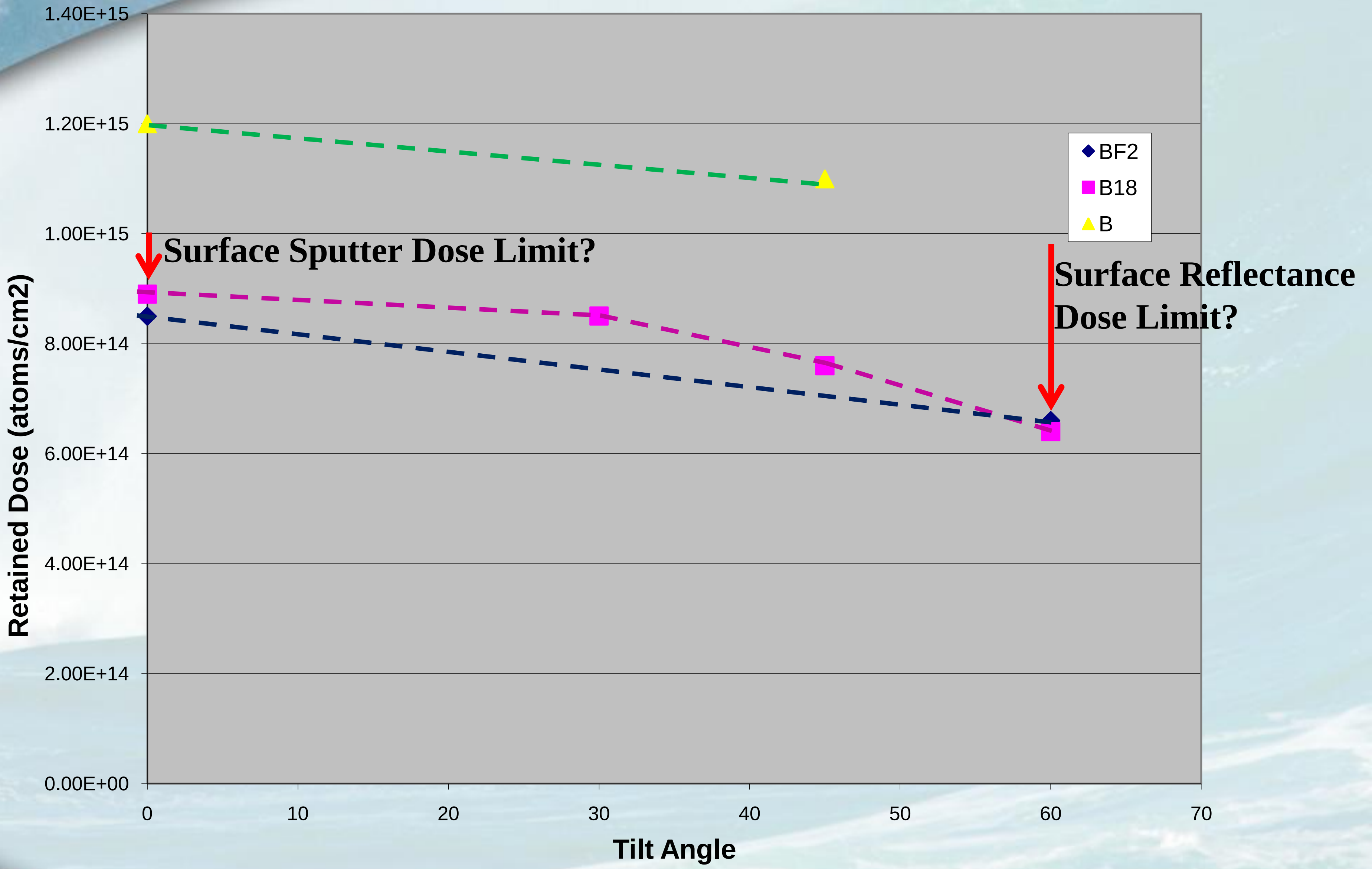
April 28, 2009

P-Type Dopant Implant Matrix

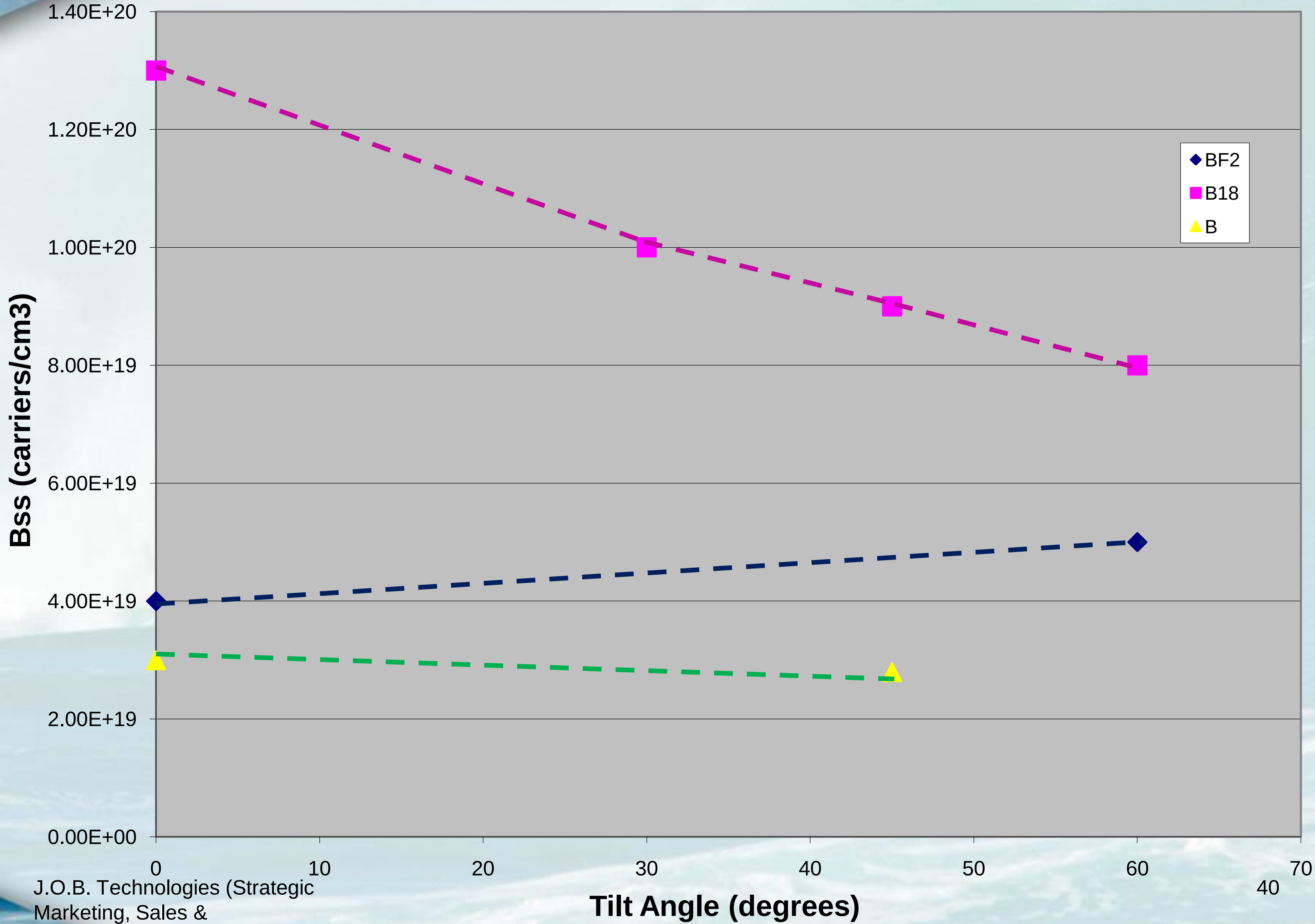
Nissin Claris 0 to 60 Degree Tilt Angle (BF2 & B18H22)
IMEC Quantum-X 0 to 45 Degree Tilt Angle (monomer B)

P-Type	Substrate No.	Ion	Energy [keV]	Dose [/cm2]	Tilt [deg]	Twist [deg]	RS		TW		as I/I SIMS (Xj) A	after anneal SIMS (Xj) A
							(Ω/sq)	%STD	TW units	%STD		
B18-Tilt Depend	slot1	B18	8.0	5.50E+13	0	0	1007.00	2.759	205.23	2.170	110	100
	slot2		8.0		15		1027.40	2.652	203.97	2.210		
	slot3		9.0		30		1014.40	2.739	224.16	2.420		125
	slot4		11.0		45		1026.40	2.816	255.79	2.310		140
	slot5		16.0		60		1038.00	2.873	355.94	2.050	175	165
BF2-Tilt Depend	slot6	BF2	2.00	1.00E+15	0	0	2233.50	1.820	537.41	0.900	130	120
	slot7		2.00		15		2439.20	1.831	532.75	0.970		
	slot8		2.00		30		2535.40	1.719	530.15	1.020		
	slot9		3.00		45		1928.10	1.635	568.92	0.680		
	slot10		4.00		60		1766.80	1.460	581.78	0.480	175	165
(B-Tilt Depend)	slot11	B	0.50	1.00E+15	0	0	2035.00	2.515	597.82	1.200	175	205
	slot12		0.52		15		1983.00	3.104	594.29	1.110		
	slot13		0.58		30		2027.00	2.580	617.06	0.720		
	slot14		0.71		45		2007.00	2.468	629.77	0.420	235	255
	slot15		1.00		60							
B18 Energy Depend	slot16	B18	8.0	5.50E+13	60	0	1688.80	2.693	183.59	1.910		70
	slot17		16.0				1045.00	2.917	353.95	2.050		165
	slot18		32.0				658.33	4.105	582.90	0.390		285
BF2 Energy Depend	slot19	BF2	2.0	1.00E+15	60	0	3995.00	1.409	436.46	2.230		90
	slot20		4.0				1668.90	1.671	579.73	0.490		165
	slot21		8.0				750.80	0.948	582.16	0.410		250

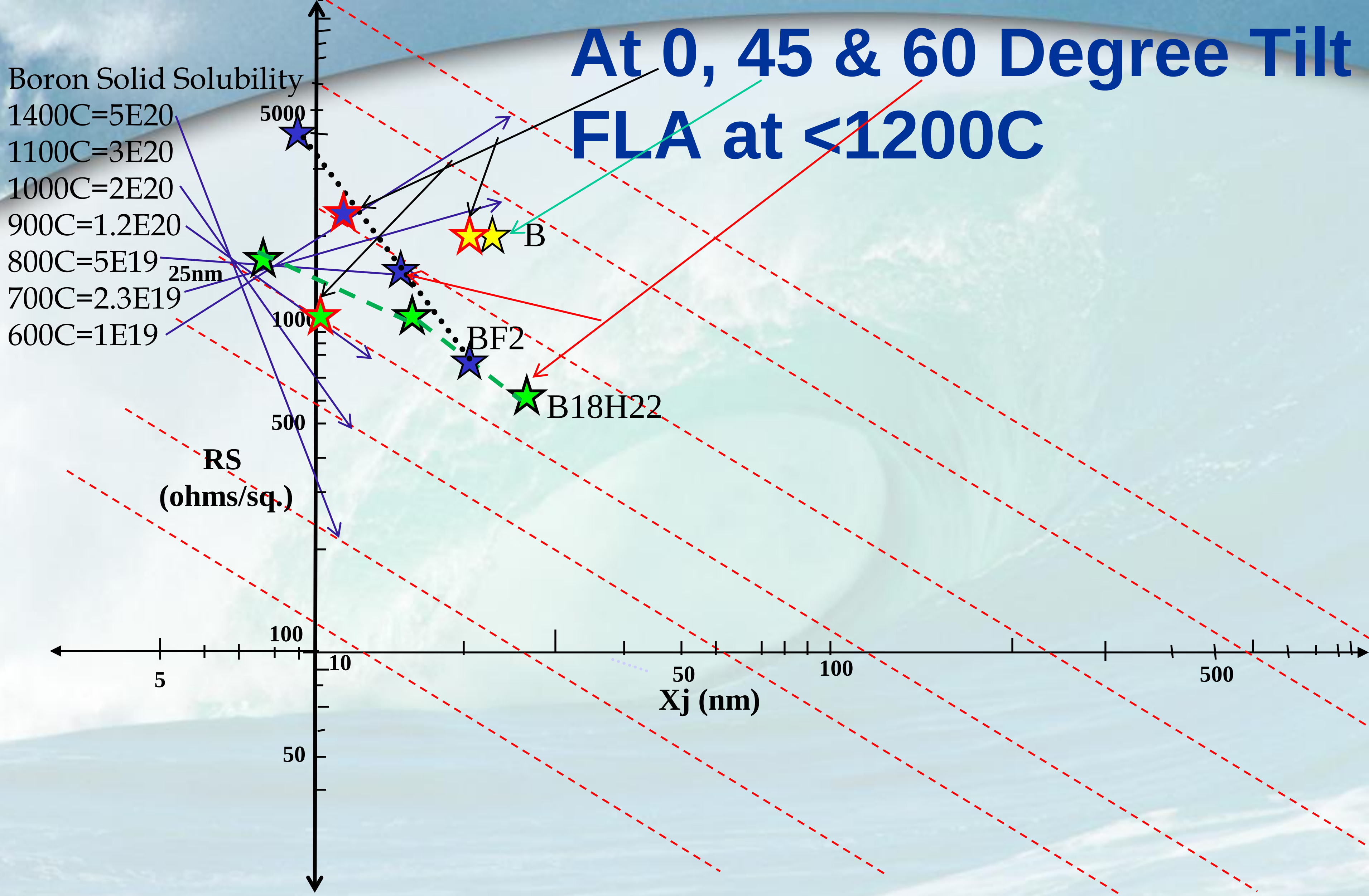
Retained Chemical Dose Versus Tilt Angle



Bss Dopant Electrical Activation Level



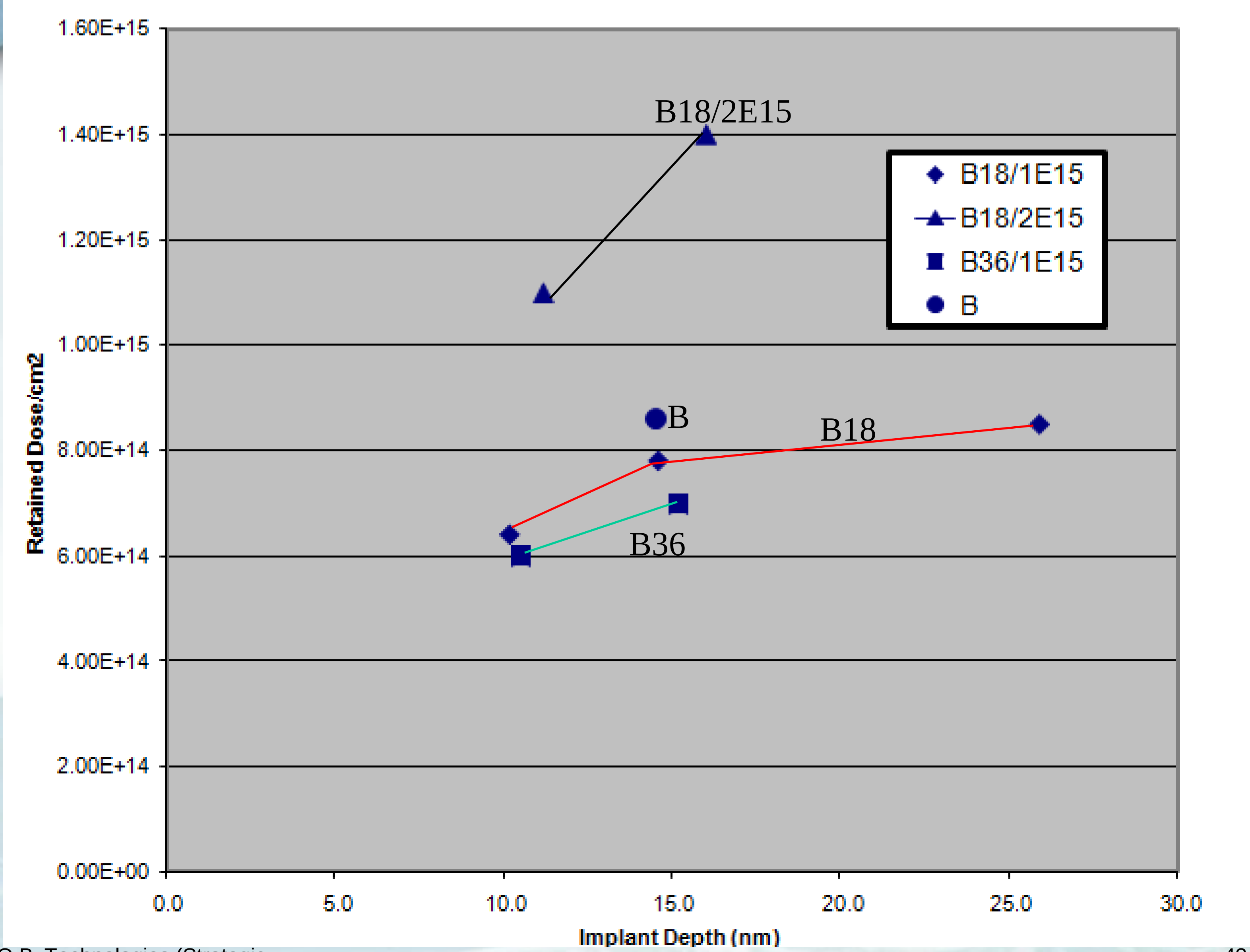
At 0, 45 & 60 Degree Tilt FLA at <1200C



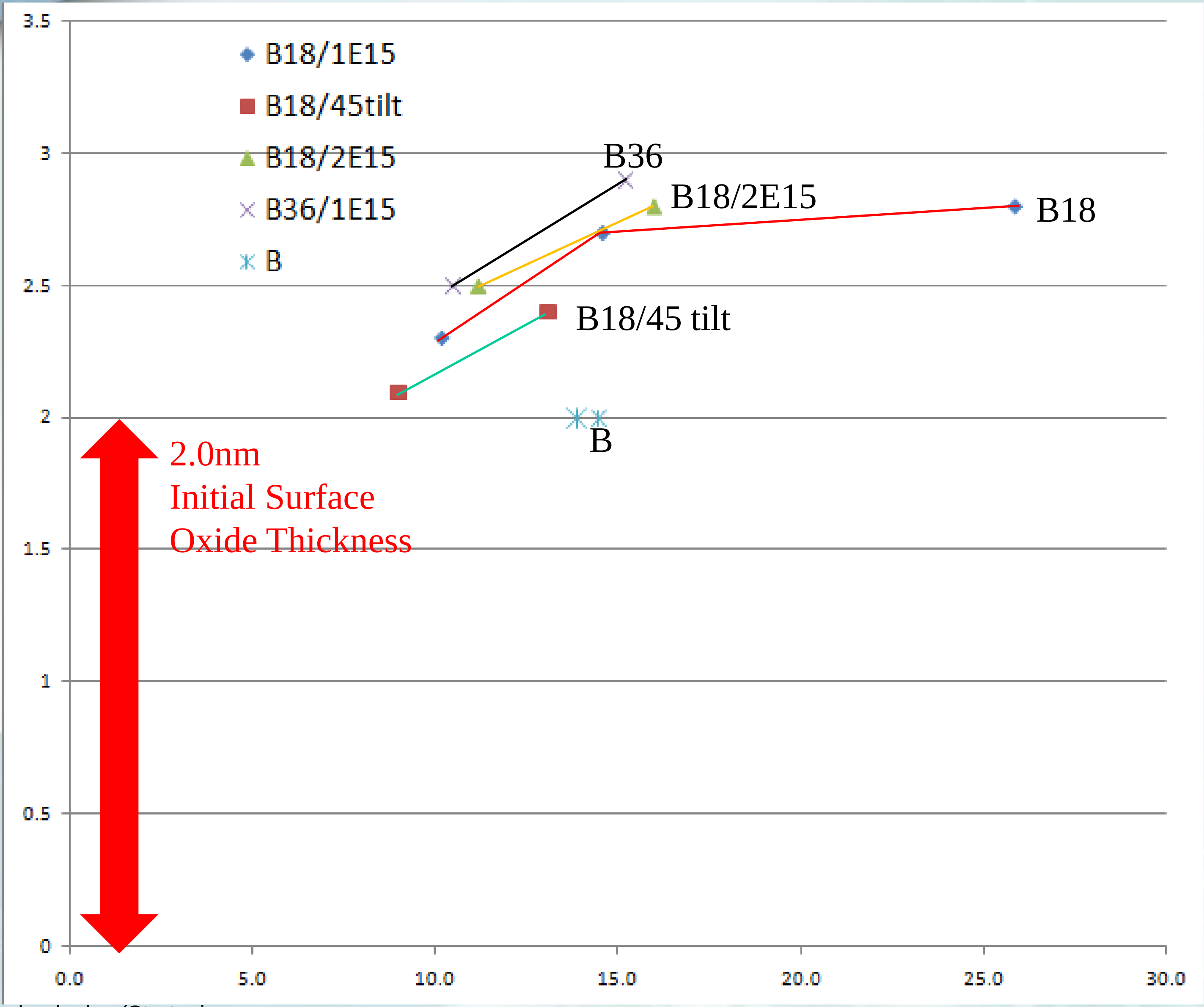
Implant Matrix With 2.0nm Surface Oxide To Determine If Retained Dose Is Sputter Or Surface Reflection Limited

- B18H22:
  - 200eV/1E15, 0 & 45 degree tilt
  - 200eV/2E15, 0 degree tilt
  - 500eV/1E15, 0 & 45 degree tilt
  - 500eV/2E15, 0 degree tilt
  - 1keV/1E15, 0 degree tilt
- B36H44:
  - 200eV/1E15, 0 degree tilt
  - 500eV/1E15, 0 degree tilt
- B:
  - 500eV/1E15, 45 degree tilt

B, B18 & B36 Retained Dose



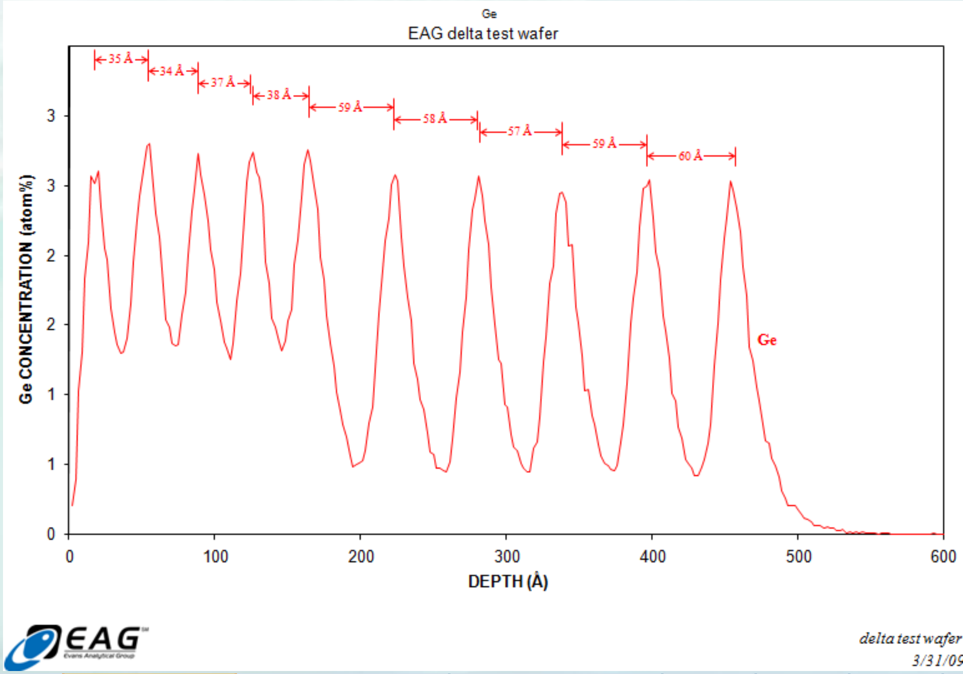
Surface Oxide Effects



B, B18 & B36 Dose Loss Study:

As suggested by EAG repeat test with Si/SiGe Epi marker layer. I suggest we use 2nm oxide/10nm Si/40nm SiGe Epi wafer and also without 2nm oxide but with hydrogen surface termination which will be free of native oxide except oxide grown during implant.

	H2/Si/SiGe	SiO2/Si/SiGe
•Control no implant	X	X
•B (200eV/1E15)	X	X
•B18 (200eV/1E15)	X	X
•B36 (200eV/1E15)	X	X

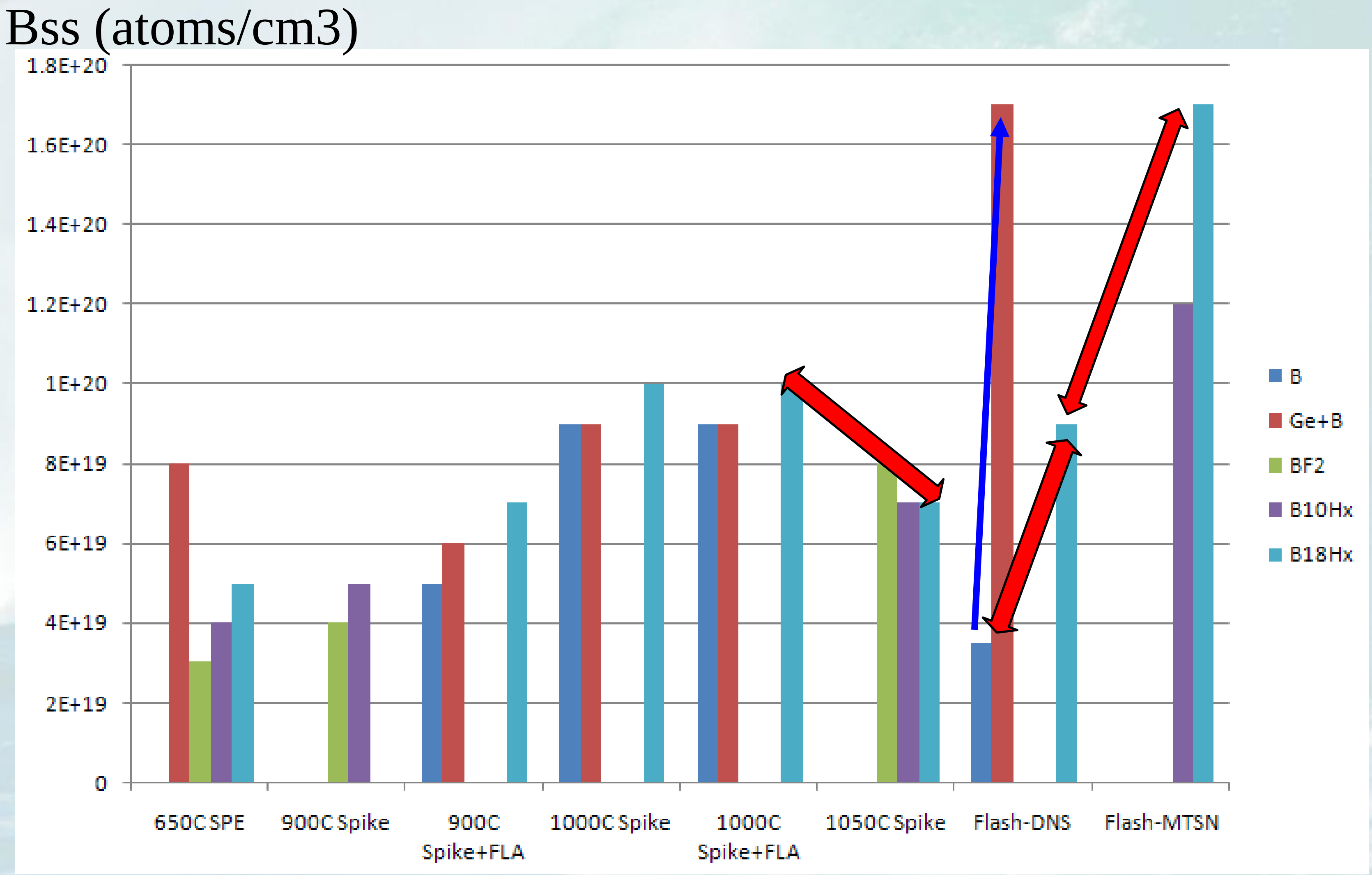


Wafer No.	pre-process			Ellipso Measurement		Implantation						
	SiGe	H2 bake	TEOS	SiO2/c-Si	monitor Si	ion	Energy	Ion Dose	Boron Dose	tilt	twist	step
V092-0003-21	Si(10nm)/SiGe(40nm)/sub.	800C, 30min		3.4A								
V092-0003-22				1.6A		B	00.20 keV	-	1.00E+15 /cm2	0°	0°	1
V092-0003-23				1.4A		B18	04.00 keV	5.56E+13 /cm2	1.00E+15 /cm2	0°	0°	1
V092-0003-24				2.0A		B36	08.00 keV	2.78E+13 /cm2	1.00E+15 /cm2	0°	0°	1
V094-0030-22			2nm	24.0A	20.3A							
V094-0030-23				23.7A		B	00.20 keV	-	1.00E+15 /cm2	0°	0°	1
V094-0030-24				23.6A		B18	04.00 keV	5.56E+13 /cm2	1.00E+15 /cm2	0°	0°	1
V094-0030-25				23.6A		B36	08.00 keV	2.78E+13 /cm2	1.00E+15 /cm2	0°	0°	1

Outline

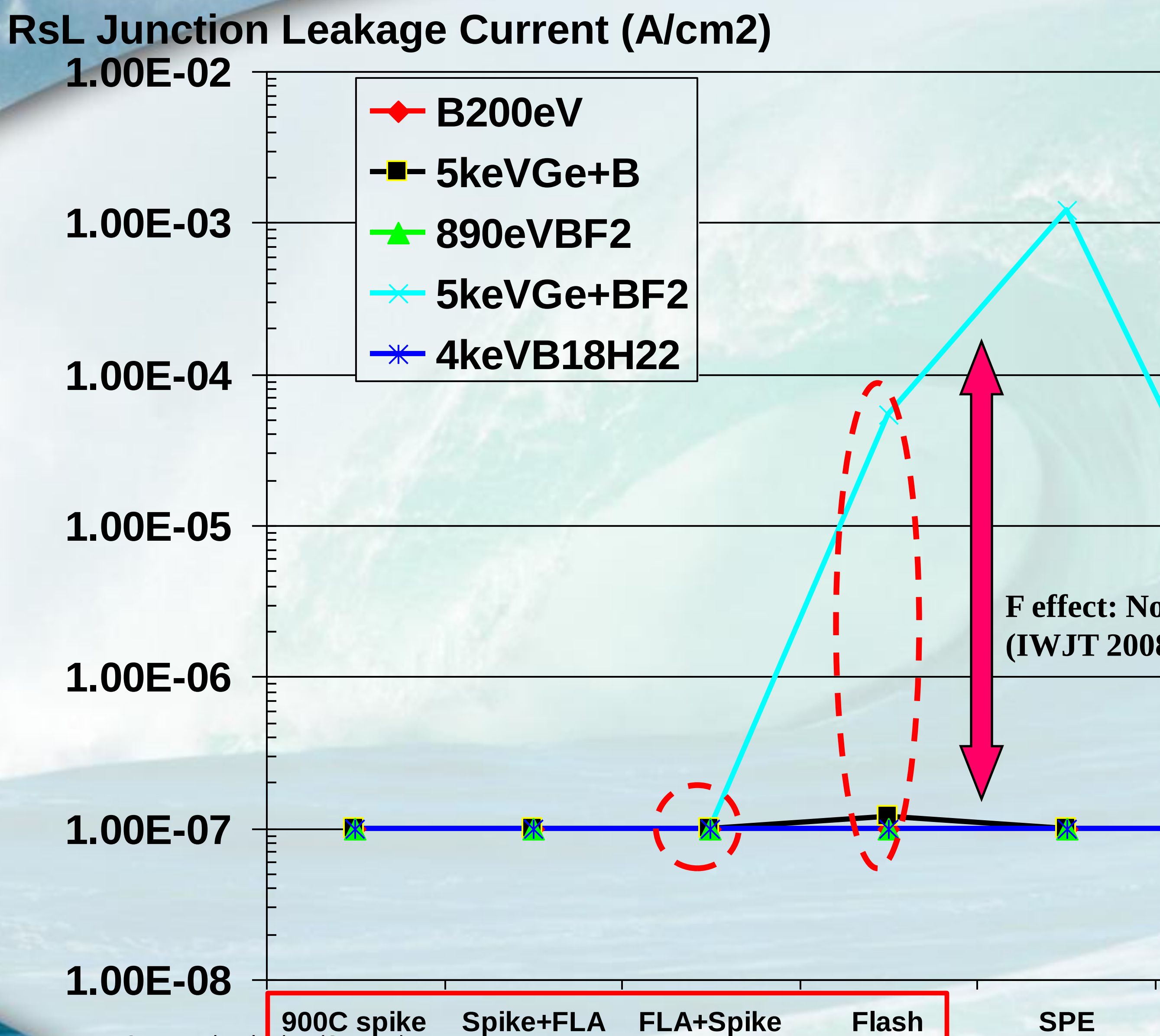
- Introduction
- Planar CMOS Doping
- FinFET CMOS Doping
- **MSA Process And Equipment Design Issues**
- Summary & Next

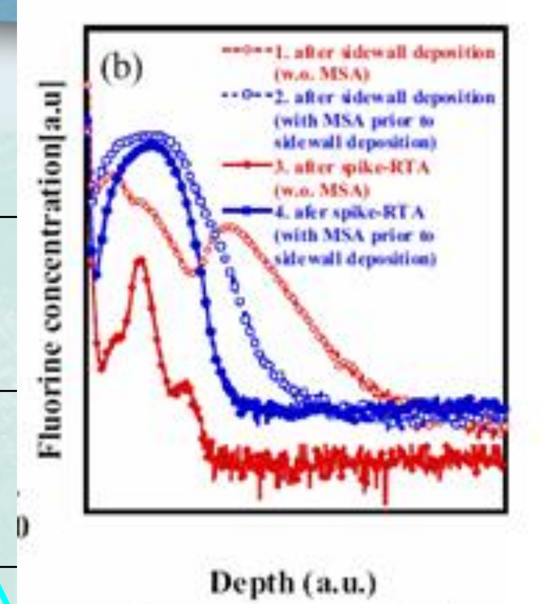
NEC & Selete IWJT 2007:Differences For Flash & Spike Results Temperature?



Borland's IWJT 2007 Joint NEC (S4-8) and Joint Selete (S4-7) papers

Extension Results (Leakage)





Yamamoto et al., IWJT 2008, MSA pins F in substitutional site and degrades leakage!

F effect: Noda (MRS 2008), Yamamoto (IWJT 2008), England (IIT 2008 P41)

>1200C?

Borland & Kiyama, JOB/DNS, IIT-2008

IMEC Now Also Using <900C Spike/RTA For Diffusion-less Pre or Post MSA For Defect Reduction

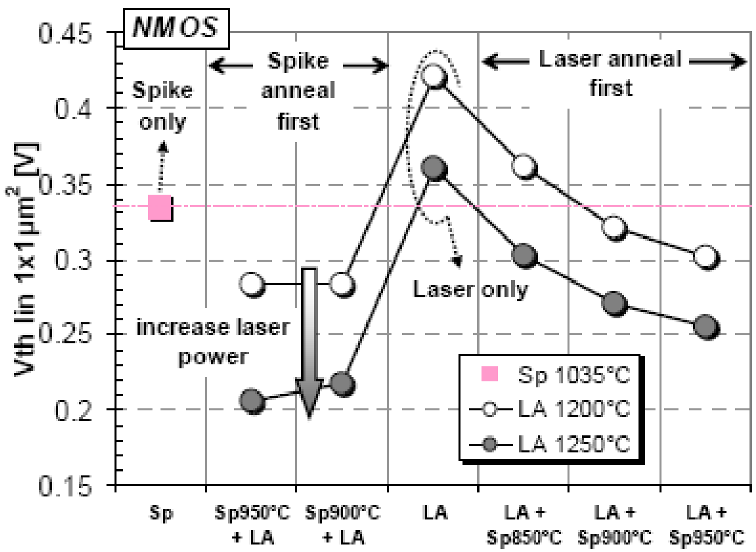


Figure 4: NMOS, with Hk/MG and eWF modulate by La-based capping, long channel Vth as function of different junction anneal conditions.

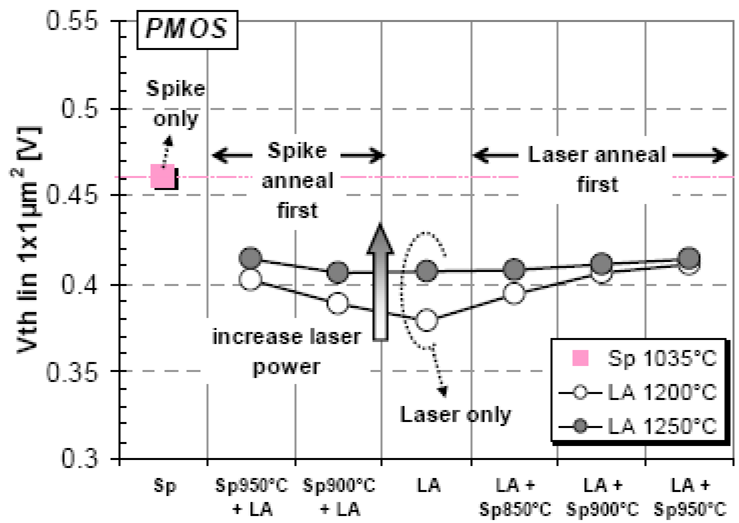


Figure 6: PMOS, with Hk/MG and eWF modulate by Al-based capping, long channel Vth as function of different junction anneal conditions.

C. Ortolland et al., IMEC, IWJT-2009, paper S4-4, p.

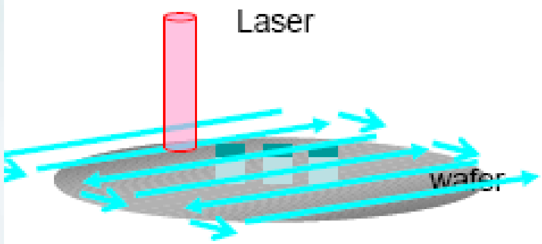
MSA Process & Equipment Design Issues

- Flash
  - Wafer slip, warpage & breakage require special hardware and confidential know-how and wafer edge damage pre-screening.
  - Pre-heat temperature >450C or >750C and limits max peak temperature
  - +/- 60C temperature variation across the wafer.
  - 1-50msec dwell time but if too short surface still amorphous
- Laser
  - Wafer slip, warpage & breakage.
  - Localized hot spots (+50C) causing poly-Si line breakage
  - 100usec to 1msec dwell times
  - Pre-heat temperature >400C
  - Laser stitching pattern and gate stack shadowing requires quad-mode wafer rotation
- Other Integration Issues
  - High-k/metal gate stack failure >1300C
  - eSiGe strain relaxation >1200C, eSiC max Csub>1300C

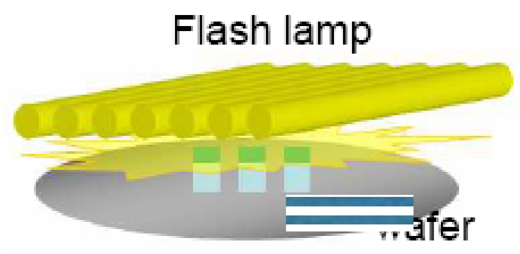
Millisecond annealing

FUJITSU

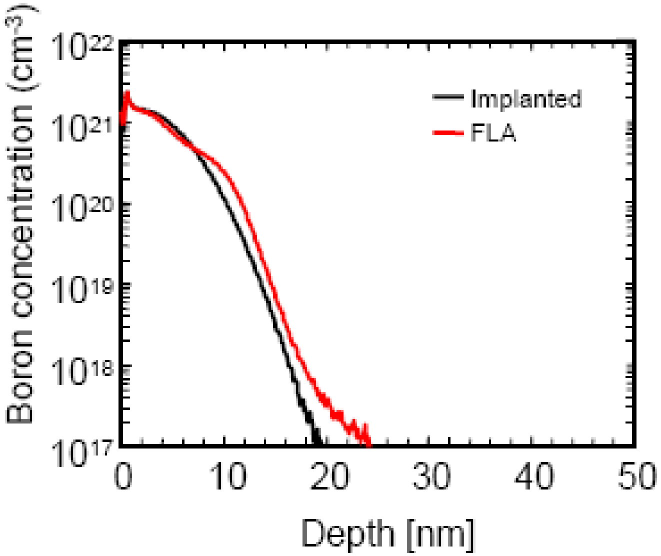
- To minimize dopant diffusion in annealing, the millisecond annealing techniques are applied. It is replaced or combined with spike RTA.
- The technical limitation restricts the annealing time is ranging from sub ms to several ms. The highest temperature is higher than 1350 °C.



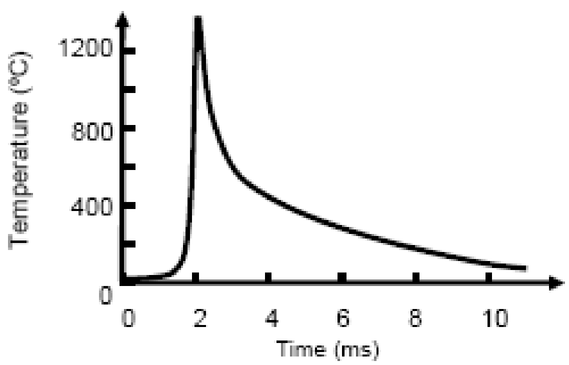
Laser anneal
(~kW/mm^2, CO_2 laser, solid state laser)



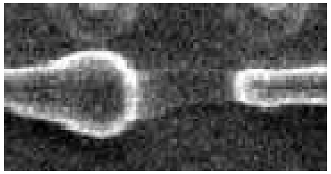
Flash lamp anneal



B SIMS profile after FLA



Thermal distribution of laser anneal



Disconnected poly-Si line due to locally heat condensation

Others also see this LSA effect so keep Temp <1200C

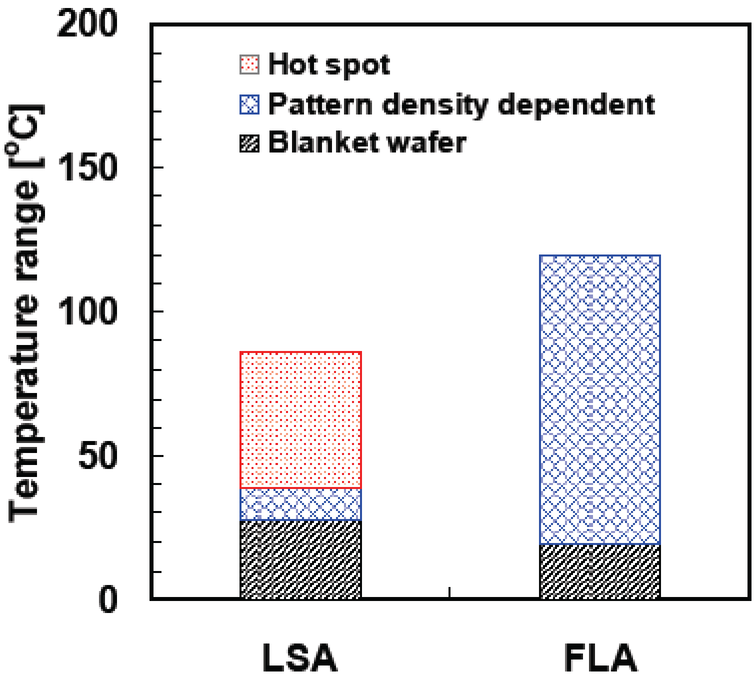
Total temperature fluctuation within patterned wafers

FUJITSU

Total temperature fluctuation of patterned wafers
= Non-uniformity within blanket wafers + Non-uniformity within a chip

Total temperature fluctuation of pattern wafers in LSA and FLA is around 100 ºC. The main part of fluctuation is the variation caused by pattern effect.

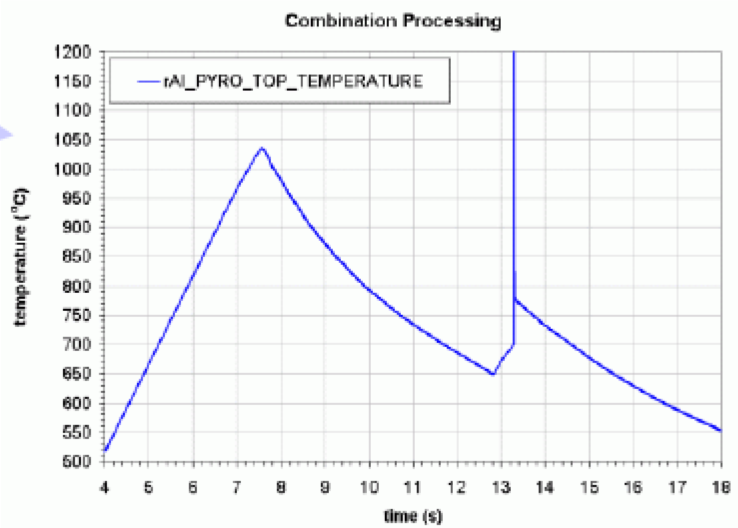
We must devise a countermeasure against deviation of device characteristics caused by pattern effect in LSA and FLA.

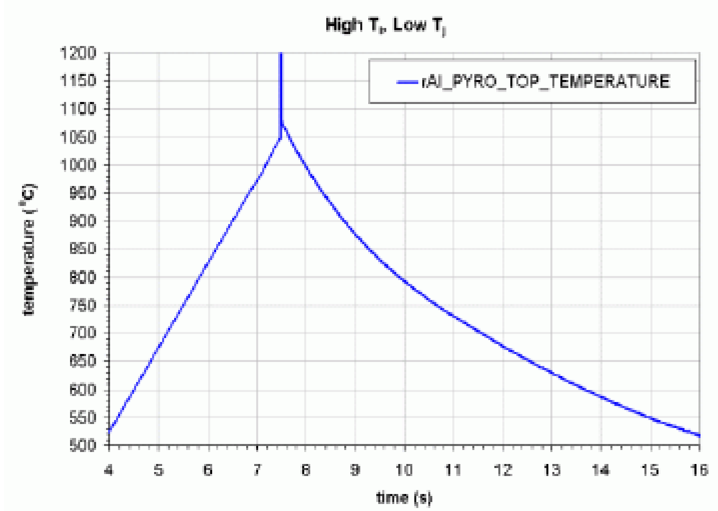


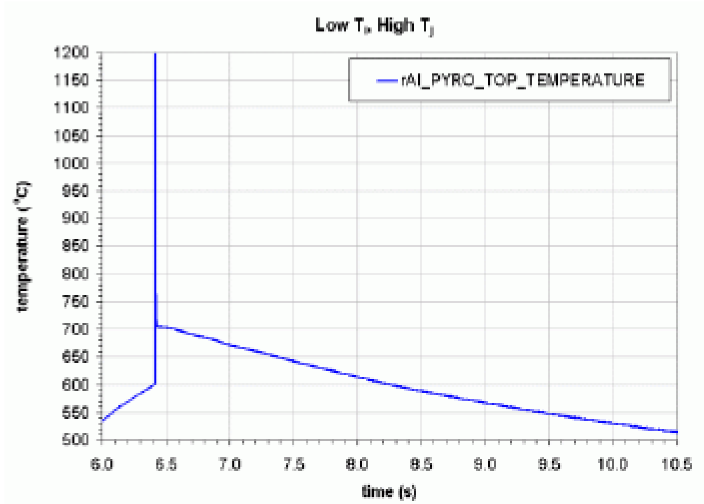
Kubo et al., Fujitsu, IEEE/RTP 2008

Anneal Process Flexibility

Novel combination processes can be run to combine spike + flash







Unmatched process flexibility

A Partner You Trust.
Performance You Value.

mattson

Timans, Mattson, Semicon/West WCJUG July 2008

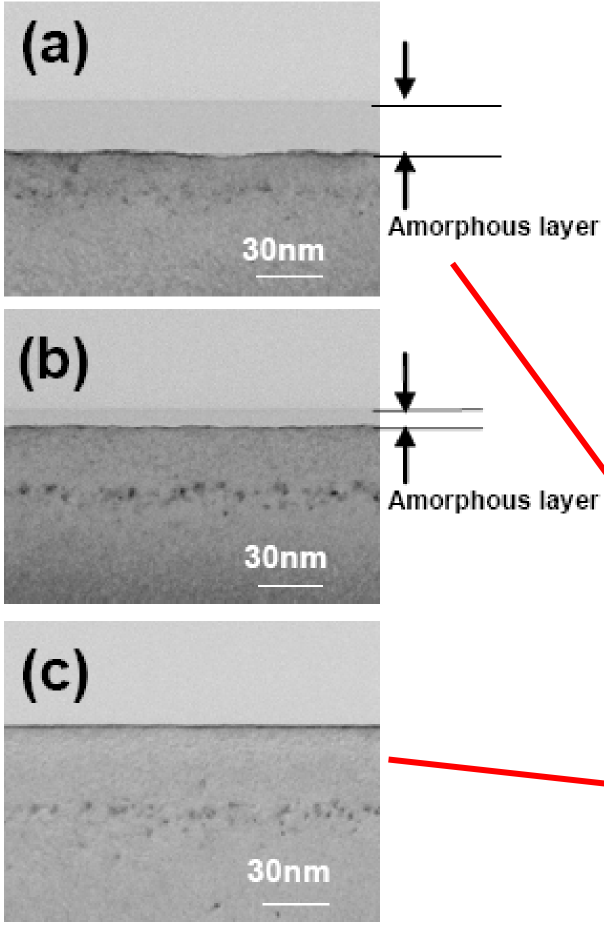


Fig.2 XTEM image of n+/p junction (As: 20keV) after FLA with different discharge voltages.
(a): 3425V, (b): 3525V, (c): 3725V.

Nara et al., Selete, ECS May 2008

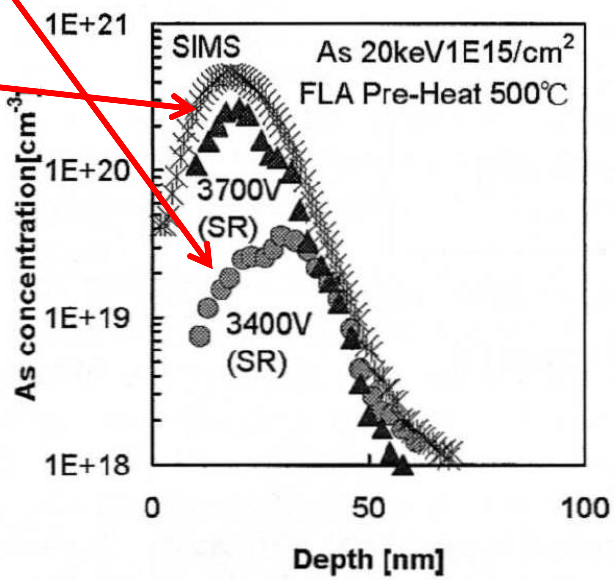


Figure15 SR and SIMS profiles after FLA. The activation phenomena of FLA includes SPER. SR measurement data shows that surface amorphous layer is not activated.

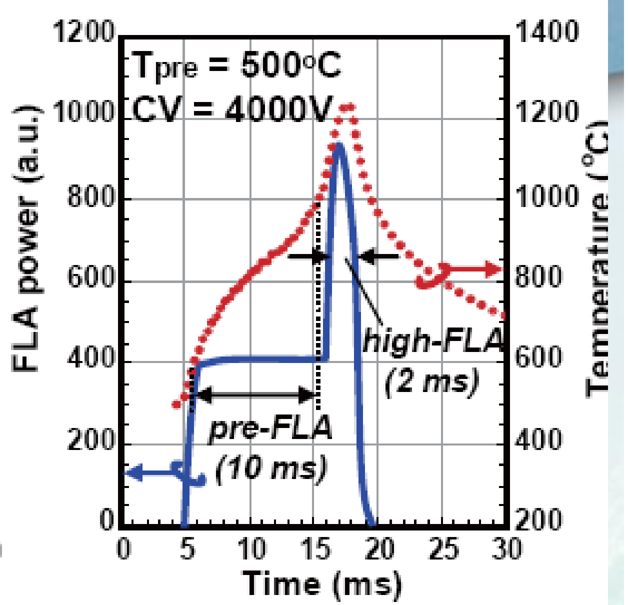


Fig. 4. The FSP-FLA pulse shape used in this work.

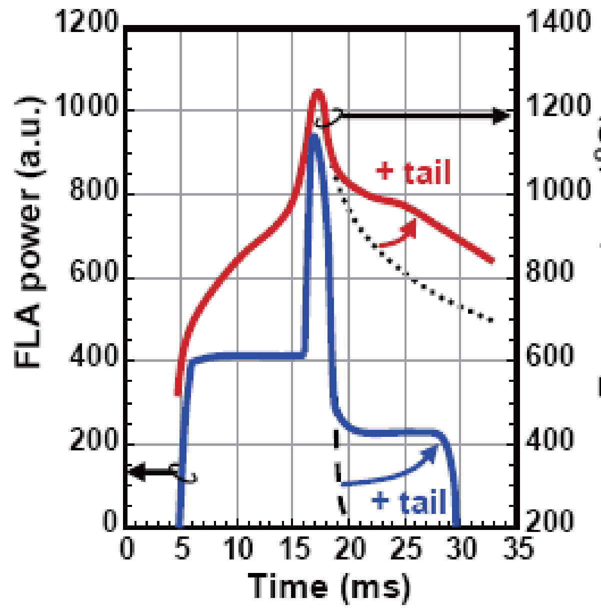


Fig. 12. The pulse shape for tail added FSP-FLA.

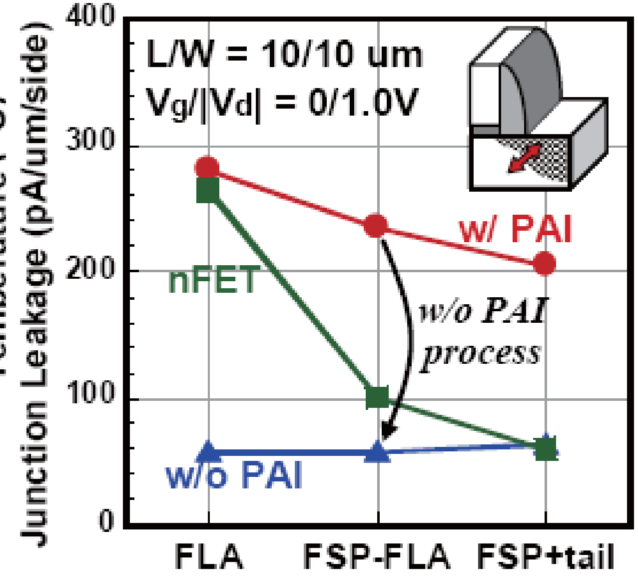


Fig. 11. Junction leakage of p- and n-type FET.

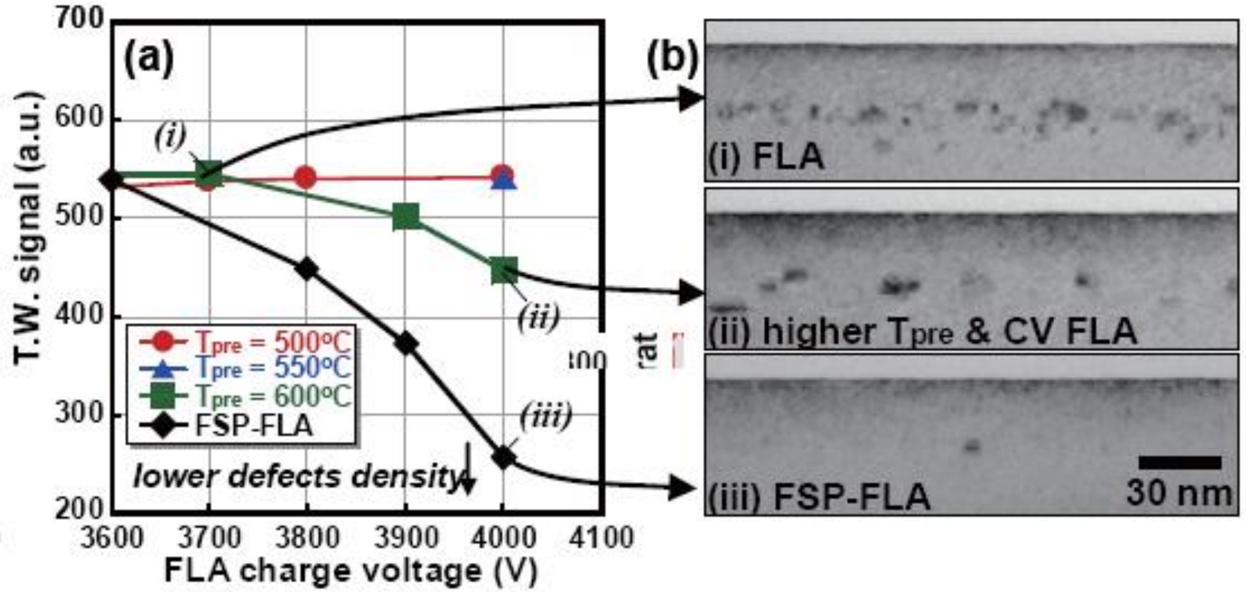


Fig. 7. (a) T.W. signals of FLA and FSP-FLA w/ PAI. (b) TEM images of (i) FLA, (ii) higher FLA, and (iii) FSP-FLA used in this study.

Onizawa et al., Selete, VLSI Sym 2009, paper 8B-4, p. 162

Executive Overview

Junction scaling for 22nm node planar and FinFET CMOS requires low energy implantation but the surface oxide thickness will determine the energy (>83eV) and dose. Engineering the surface amorphous layer maximizes dopant activation, reduces implant damage and junction leakage with sub-melt laser or flash lamp annealing. The annealing process and equipment must be optimized to prevent strain relaxation, high-k/metal gate stack failure and wafer breakage.

JOB Technologies:

- **22nm low defect and leakage p+ USJ**
- **22nm high activation n+ USJ**
- **22nm eSiC strain by implant ation**
- **16nm FinFET high tilt implant retained dose**

Acknowledgements

We are grateful to Jeremy Zelenko of Applied Materials for support with the DSA laser anneals, David Liu and Yuen Lim of Frontier Semiconductor for RsL junction leakage measurements, Walt Johnson & Iad Mirshad of KT for 4PP, Lifetime & TW measurements.