Thermal Processing Issues For 22nm Node Junction Scaling

John Borland, J.O.B. Technologies, Aiea, HI
Susan Felch, Los Alto Hills, CA
Zhimin Wan, AIBT, San Jose, CA
Masuyasu Tanjyo, Nissin, Kyoto, Japan
Temel Buyuklimanli, EAG, Windsor, NJ

Solid State Technology August 2009
Executive Overview

Junction scaling for 22nm node planar and FinFET CMOS requires low energy implantation but the surface oxide thickness will determine the energy (>83eV) and dose. Engineering the surface amorphous layer maximizes dopant activation, reduces implant damage and junction leakage with sub-melt laser or flash lamp annealing. The annealing process and equipment must be optimized to prevent strain relaxation, high-k/metal gate stack failure and wafer breakage.
Outline

• Executive Overview
• Introduction
  – Defect and junction leakage reduction
  – JOB Technologies:
    • 22nm low defect and leakage p+ USJ
    • 22nm high activation n+ USJ
    • 22nm eSiC strain by implantation
    • 16nm FinFET high tilt implant retained dose
• Planar CMOS Doping
• FinFET CMOS Doping
• MSA Process And Equipment Design Issues
• Summary
• Acknowledgements
NEC IEDM-2008: Transistor Leakage (A+B+C+D)

Junction leakage become larger by shallower $SD_{ext}$ with MSA

We want to know “What is the main cause of leak increase”

A=HALO (BTBT)
B=HALO & PAI (EOR damage)
C=Residual implant damage & HALO?
D=STI stress induced leakage
Low Damage Implantation

- Improve self-amorphization, lower critical implant doses for amorphization and smooth amorphous interfaces thereby reducing EOR damage and residual implant damage while enhancing dopant activation with MSA
  - Higher implant beam current or dose rate improves self-amorphization
  - Lower implant wafer temperature (cold or cryo-implantation) 0C to -160C using chilled water of liquid nitrogen wafer cooling
  - Use molecular dopants (B18H22, B36H44, As4 or P4) improves self-amorphization
  - Use heavier ions for PAI (In, Sb or Xe), also He-PAI
- Stable defects and reduction in residual implant damage thereby improving junction leakage
  - Higher MSA peak temperature
  - Pre/post MSA diffusion-less spike/RTA<900C
Outline

• Introduction
• **Planar CMOS Doping**
  – 22nm and 16nm node
• FinFET CMOS Doping
• MSA Process And Equipment Design Issues
• Summary & Next
Low Energy Implant Approach

- Monomer ion beam:
  - Deceleration of higher energy ion beam

- Molecular ion beam:
  - Using $\text{B}_{18}\text{H}_{22}$, $\text{C}_2\text{B}_{10}\text{H}_{12}$ and $\text{B}_{10}\text{H}_{14}$
  - Gas-cluster ion

- Plasma doping
  - High density plasma, $\text{B}_2\text{H}_6$, $\text{BF}_3$
Implant Energy Versus Xj

22nm Node p+ USJ Using Xe-PAI & Laser Annealing

John Ogawa Borland, J.O.B. Technologies, Aiea, Hawaii
Zhimin Wan, AIBT, San Jose, CA
Shankar Muthukrishnan & Jeremy Zelenko, Applied Materials, Sunnyvale, CA
Iad Mirshad & Walt Johnson, KLA-Tencor, San Jose, CA
Temel Buyuklimanli, EAG, East Windsor, NJ

INSIGHTS 2009
April 27, 2009
Experimentation & Results

DSA Laser Annealing 1175C → 1325C & DSA+900C spike anneal

- **B: 100-350eV/1E15**
  - B, Ge-PAI+B or Xe-PAI+B
- **BF2: 500-890eV/1E15**
  - BF2, Ge-PAI+BF2 or Xe-PAI+BF2
PCOR-SIMS

Ge+B TED=3.4nm!
Xe+B TED=2.7nm!
Ge+BF2-TED=2.4-4.2nm!

Surface Oxide
1.8nm

B CONCENTRATION (atoms/cc)

DEPTH (nm)

O INTENSITY (arbitrary units)

BF2+Ge-PAI Sample21 PCOR_HDR
Xe TED=2.5nm (B)
Ge TED=3.5nm (B), 4.2nm (BF2)

B retained dose 1E15/cm²
BF2 retained dose 5.5E14/cm²

Sample 10 (1325C anneal)
2/19/2009

Surface Oxide
PAI-EOR Defects
Poor Leakage

B CONCENTRATION (atoms/cc)
O INTENSITY (arbitrary units)

Xe+B (1325C anneal)
B (1325C anneal)
Ge+B (1325C anneal)
BF2 (1325C anneal)
Ge+BF2 (1325C anneal)
Retained Dose <6E14/cm² Limits MSA Dopant Activation Level To <Bss (<1.2E20/cm³)!

Toxide=0.3nm
Toxide=2.3nm

X_i@5.0E18 B: 7.213nm
X_i@5.0E18 B: 9.198nm
% B Dose In 2.0nm Surface Oxide

B Xj (nm)

B (%)
22nm Node p+ Junction Scaling Using B36H44 And Laser Annealing

J. Borland, J.O.B. Technologies
M. Tanjyo, Nissin Ion Equipment
J. Zelenko, Applied Materials
I. Mirshad & W. Johnson, KLA-Tencor
T. Buyuklimanli, EAG

IEEE/RTP-2009
Oct. 1, 2009
Kawasaki et al., Renesas, IWJT-2009, paper S2-4

Fig. 5 SIMS profiles of $^{11}$B for $\text{B}_{18}\text{H}_6$ and $\text{B}_{36}\text{H}_2$ implantation. Profiles for both before and after MSA at $1220^\circ\text{C}$ are shown.
In TED=3.8nm diffusion
Ge TED=5.2nm
Xe TED=3.6nm
Xe-PAI = 14nm

- Poor Leakage: >1E-2A/cm²
- Good Leakage: <1E-7A/cm²
Xj-EOR= -7nm for Xe-PAI & -9nm for Ge-PAI
Xe-PAI No Anneal & 1325C Anneal

Toxide=2.3nm

PAI=14nm
Boron solid solubility:

- $B < 1225^\circ C$ (Bss=5E19/cm³) $RD=1E15/cm^2$
- $B 1325^\circ C$ (Bss=1E20/cm³)
- $Ge+B 1325^\circ C$ (Bss=1.3E20/cm³)
- $Xe+B 1325^\circ C$ (Bss=3.5E20/cm³)
- $BF_2 1175^\circ C$ (Bss=3E19/cm³) $RD=5.5E14/cm^2$
- $BF_2 1325^\circ C$ (Bss=4E19/cm³)
- $Ge+BF_2 1175^\circ C$ (Bss=6E19/cm³)
- $Ge+BF_2 1225^\circ C$ (Bss=6E19/cm³)
- $Ge+BF_2 1275^\circ C$ (Bss=7E19/cm³)
- $Ge+BF_2 1325^\circ C$ (Bss=8E19/cm³)
- $BF_2 1325^\circ C$ (Bss=4E19/cm³)
- $Ge+BF_2 1225^\circ C$ (Bss=6E19/cm³)
- $Ge+BF_2 1275^\circ C$ (Bss=7E19/cm³)
- $Ge+BF_2 1325^\circ C$ (Bss=8E19/cm³)
- $B_{36} 1325^\circ C$ (Bss=1.2E20/cm³) $RD=6.7E14/cm^2$
- $Ge+B_{36} 1325^\circ C$ (Bss=1E20/cm³)
- $In+B_{36} 1325^\circ C$ (Bss=1E20/cm³)
- $Xe+B_{36} 1325^\circ C$ (Bss=1.2E20/cm³)
PAI Enhances Dopant Activation (Bss)

B 500eV Xj=15nm
Ge-PAI Xj-EOR=+15nm (1E-7A/cm²)
5keV=9nm Xj-EOR=+6nm (4E-6A/cm²)
10keV=16nm Xj-EOR=-1nm (3E-4A/cm²)
20keV=32nm Xj-EOR=-17nm (3E-4A/cm²)

RsL Junction Leakage Current (A/cm²)

Insight-2009 & IWJT-2009

• IWJT
  – Varian He-PAI excellent junction leakage
  – UJT He-PAI no EOR defects and (low leakage IIT-2004)

• Oleg of IBM
  – Insight invited paper said that series resistance more critical than SCE so this drives to deeper junctions. Higher dopant activation by adding up to 8 laser passes for As n+ USJ. But gate oxide failure at temperature >1300C.
  – IWJT invited paper said because of difficulties with epi or implant for eSiC a HYBRID approach is another option (SEG+implant).

• AMD/Dresden IWJT
  – With eSiGe BF2 SDE implant leakage is 5x higher than B and amorphization reduces strain.
  – For eSiC by C-implantation no significant nMOS device improvement.
22nm Node n+ SiC Stressor Using Deep PAI+C\textsubscript{7}H\textsubscript{7}+P4 With Laser Annealing

IEEE/RTP-2009

John Borland\textsuperscript{1}, Masayasu Tanjyo\textsuperscript{2}, Nariaki Hamamoto\textsuperscript{2}, Tsutomu Nagayama\textsuperscript{2}, Shankar Muthukrishnan\textsuperscript{3}, Jeremy Zelenko\textsuperscript{3}, Iad Mirshad\textsuperscript{4}, Walt Johnson\textsuperscript{4}, Temel Buyukimanli\textsuperscript{5}, Steve Robie\textsuperscript{5}, Hiroshi Itokawa\textsuperscript{6}, Ichiro Mizushima\textsuperscript{6} and Kyoichi Suguro\textsuperscript{6}

1) J.O.B. Technologies, Aiea, HI
2) Nissin Ion Equipment, Kyoto, Japan
3) Applied Materials, Sunnyvale, CA
4) KLA-Tencor, San Jose, CA
5) EAG, Sunnyvale, CA
6) Toshiba Corporation, Yokohama, Japan
Intel reported LSA 
Pss=1.8E21/cm³

This Work

Xe+C7+P2 (1200°C fRTP)

C7+P2 (1200°C fRTP)
C-substituted Si by HRXRD

P4+C (no PAI, Ge-PAI, Xe-PAI & Sb-PAI)
P4+C7 (no PAI, Ge-PAI, Xe-PAI & Sb-PAI)
Outline

• Introduction
• Planar CMOS Doping
• FinFET CMOS Doping
  – 16nm Node Bulk or SOI?
• MSA Process And Equipment Design Issues
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Summary of FinFET At VLSI Sym-2008 & IEDM-2008

- **VLSI Sym 2008:**
  - Planar CMOS to 22nm Node
    - Intel said SRAM needs Bulk FinFET/Trigate at 16nm or Floating Body Cell (Mark Bohr)
      - HK/MG+strain-Si makes pMOS almost equal to nMOS at 45nm node

- **IEDM 2008:**
  - ITRS-2008 update (Iwai-san TIT):
    - FD-SOI CMOS delayed until 2013
    - FinFET delayed to 2015 (16nm node)

- **Intel:**
  - Stated that FinFET not ready for 22nm node manufacturing (K. Kuhn).
IBM Double Gate Fin FET With 30 & 45 Degree High Tilt High Current Implants

SDG (symmetrical double-gate) & ADG (asymmetrical double-gate)

Figure 1: Schematic of the planar FinFET structure. Light(gray) regions indicate the single crystal silicon mesa used for the fin and source/drain pads, dark(red) regions indicate the polysilicon gate line and pad.

ADG gate and extension implants, tilt of 30°. Both of the gate implants were done for each wafer, but only one of extension implants per wafer.

Table 2: Extension and gate implant conditions. SDG Dose and energy is given in relative units. Ra is the simulated 10% interstitial Si concentration range after implant, measured normal to fin surface.
PLAD not conformal asymmetrical device

Lenoble et al., ST/IMEC, VLSI Sym. 2006, section 2.1
High Tilt p+ & n+ Molecular Implantation For 3-D Structures: Retained chemical Dose Versus Electrical Activation Limited Conformal Doping

John Ogawa Borland
J.O.B. Technologies, Aiea, Hawaii
&
Masayasu Tanjyo, Tsutomu Nagayama and Nariaki Hamamoto
Nissin Ion Equipment, Kyoto, Japan
INSIGHTS 2009
April 28, 2009
# P-Type Dopant Implant Matrix

**Nissin** Claris 0 to 60 Degree Tilt Angle (BF2 & B18H22)

**IMEC** Quantum-X 0 to 45 Degree Tilt Angle (monomer B)

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Bss Dopant Electrical Activation Level

![Graph showing Bss dopant electrical activation level with tilt angle (degrees) on the x-axis and Bss (carriers/cm³) on the y-axis. Different dopants are represented by different markers: BF2, B18, and B.](image_url)
Boron Solid Solubility

- $1400^\circ C = 5 \times 10^{20}$
- $1100^\circ C = 3 \times 10^{20}$
- $1000^\circ C = 2 \times 10^{20}$
- $900^\circ C = 1.2 \times 10^{20}$
- $800^\circ C = 5 \times 10^{19}$
- $700^\circ C = 2.3 \times 10^{19}$
- $600^\circ C = 1 \times 10^{19}$

**RS (ohms/sq.)**

- B
- BF$_2$
- B$_{18}$H$_{22}$

**At 0, 45 & 60 Degree Tilt**

**FLA at <1200^\circ C**
Implant Matrix With 2.0nm Surface Oxide To Determine If Retained Dose Is Sputter Or Surface Reflection Limited

- **B18H22:**
  - 200eV/1E15, 0 & 45 degree tilt
  - 200eV/2E15, 0 degree tilt
  - 500eV/1E15, 0 & 45 degree tilt
  - 500eV/2E15, 0 degree tilt
  - 1keV/1E15, 0 degree tilt

- **B36H44:**
  - 200eV/1E15, 0 degree tilt
  - 500eV/1E15, 0 degree tilt

- **B:**
  - 500eV/1E15, 45 degree tilt
B, B18 & B36 Retained Dose
Surface Oxide Effects

2.0nm Initial Surface Oxide Thickness
B, B18 & B36 Dose Loss Study:

As suggested by EAG repeat test with Si/SiGe Epi marker layer. I suggest we use 2nm oxide/10nm Si/40nm SiGe Epi wafer and also without 2nm oxide but with hydrogen surface termination which will be free of native oxide except oxide grown during implant.

- Control no implant: X
- B (200eV/1E15): X
- B18 (200eV/1E15): X
- B36 (200eV/1E15): X
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• FinFET CMOS Doping
• **MSA Process And Equipment Design Issues**
• Summary & Next
NEC & Selete IWJT 2007: Differences For Flash & Spike Results Temperature?

Bss (atoms/cm³)
Extension Results (Leakage)

RsL Junction Leakage Current (A/cm²)

- B200eV
- 5keVGe+B
- 890eVBF2
- 5keVGe+BF2
- 4keVB18H22

Yamamoto et al., IWJT 2008, MSA pins F in substitutional site and degrades leakage!

F effect: Noda (MRS 2008), Yamamoto (IWJT 2008), England (IIT 2008 P41)

Borland & Kiyama, JOB/DNS, IIT-2008
IMEC Now Also Using <900°C Spike/RTA For Diffusion-less Pre or Post MSA For Defect Reduction

**Figure 4:** NMOS, with Hk/MG and eWF modulate by La-based capping, long channel $V_{th}$ as function of different junction anneal conditions.

**Figure 6:** PMOS, with Hk/MG and eWF modulate by Al-based capping, long channel $V_{th}$ as function of different junction anneal conditions.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

C. Ortolland et al., IMEC, IWJT-2009, paper S4-4, p. 49
MSA Process & Equipment Design Issues

• Flash
  – Wafer slip, warpage & breakage require special hardware and confidential know-how and wafer edge damage pre-screening.
  – Pre-heat temperature >450C or >750C and limits max peak temperature
  – +/- 60C temperature variation across the wafer.
  – 1-50msec dwell time but if too short surface still amorphous

• Laser
  – Wafer slip, warpage & breakage.
  – Localized hot spots (+50C) causing poly-Si line breakage
  – 100usec to 1msec dwell times
  – Pre-heat temperature >400C
  – Laser stitching pattern and gate stack shadowing requires quad-mode wafer rotation

• Other Integration Issues
  – High-k/metal gate stack failure >1300C
  – eSiGe strain relaxation >1200C, eSiC max Csub>1300C
Millisecond annealing

- To minimize dopant diffusion in annealing, the millisecond annealing techniques are applied. It is replaced or combined with spike RTA.
- The technical limitation restricts the annealing time is ranging from sub ms to several ms. The highest temperature is higher than 1350 °C.

Others also see this LSA effect so keep Temp <1200°C
Total temperature fluctuation within patterned wafers

Total temperature fluctuation of patterned wafers
= Non-uniformity within blanket wafers + Non-uniformity within a chip

Total temperature fluctuation of pattern wafers in LSA and FLA is around 100 °C. The main part of fluctuation is the variation caused by pattern effect.

We must devise a countermeasure against deviation of device characteristics caused by pattern effect in LSA and FLA.
Anneal Process Flexibility

Novel combination processes can be run to combine spike + flash

Unmatched process flexibility
Fig. 2 XTEM image of n+/p junction (As: 20keV) after FLA with different discharge voltages. 
(a): 3425V, (b): 3525V, (c): 3725V.

Figure 15 SR and SIMS profiles after FLA. The activation phenomena of FLA includes SPER. SR measurement data shows that surface amorphous layer is not activated.
Fig. 4. The FSP-FLA pulse shape used in this work.

Fig. 12. The pulse shape for tail added FSP-FLA.

Fig. 11. Junction leakage of p- and n-type FET.

Fig. 7. (a) T.W. signals of FLA and FSP-FLA w/ PAI. (b) TEM images of (i) FLA, (ii) higher FLA, and (iii) FSP-FLA used in this study.
Junction scaling for 22nm node planar and FinFET CMOS requires low energy implantation but the surface oxide thickness will determine the energy (>83eV) and dose. Engineering the surface amorphous layer maximizes dopant activation, reduces implant damage and junction leakage with sub-melt laser or flash lamp annealing. The annealing process and equipment must be optimized to prevent strain relaxation, high-k/metal gate stack failure and wafer breakage.

**JOB Technologies:**
- 22nm low defect and leakage p+ USJ
- 22nm high activation n+ USJ
- 22nm eSiC strain by implantation
- 16nm FinFET high tilt implant retained dose
We are grateful to Jeremy Zelenko of Applied Materials for support with the DSA laser anneals, David Liu and Yuen Lim of Frontier Semiconductor for RsL junction leakage measurements, Walt Johnson & Iad Mirshad of KT for 4PP, Lifetime & TW measurements.