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Modeling Stress, Defect Evolution, and Junction Leakage

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October 8th, 2008

NCCAVS
JUNCTION TECHNOLOGY GROUP

Outline

- Stress trends
- Peak stress vs residual stress
- How much stress is too much?
- Bandgap impact on junction leakage
- Stress and SiGe impact on bandgap
- Layout impact on stress
- Non-silicon materials

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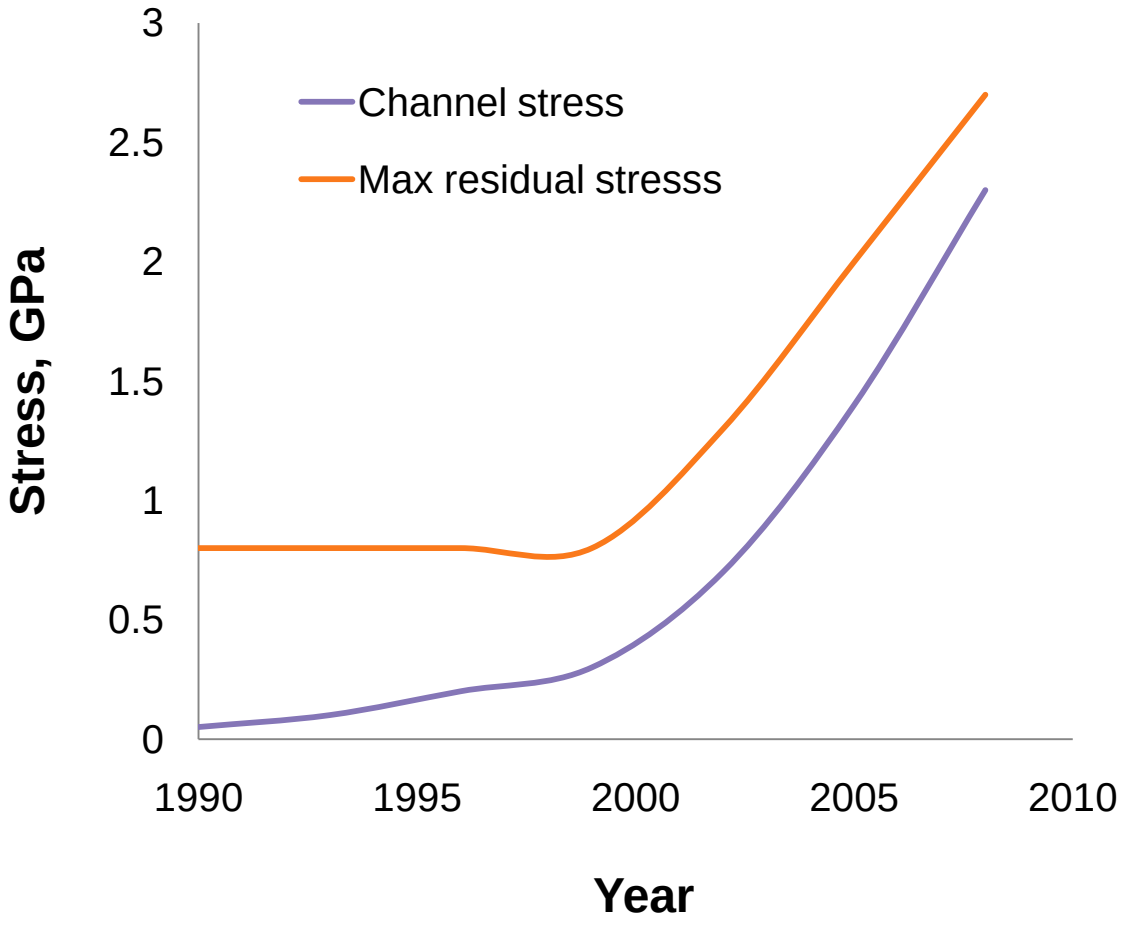
Stress in Transistors in Production



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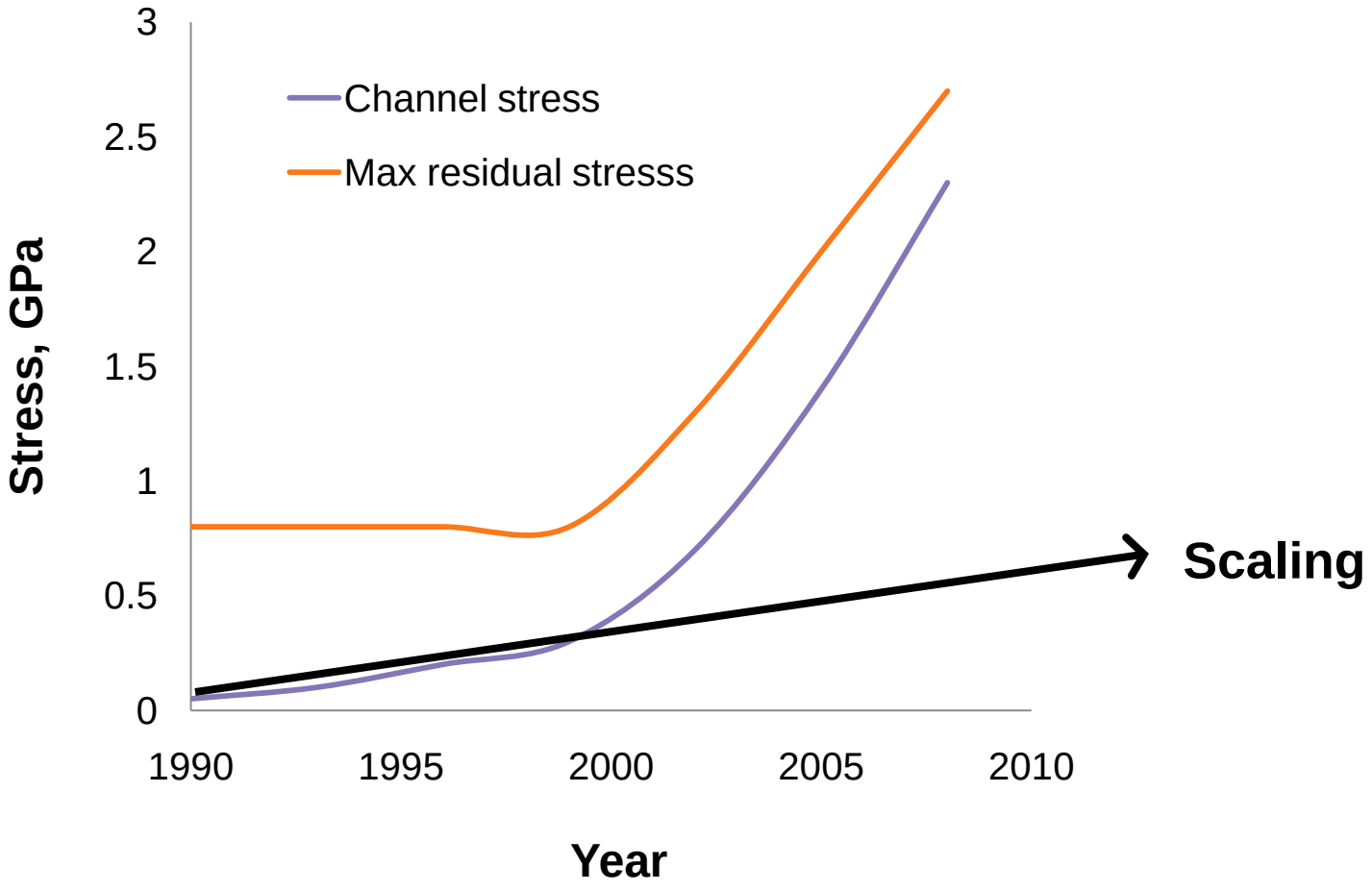

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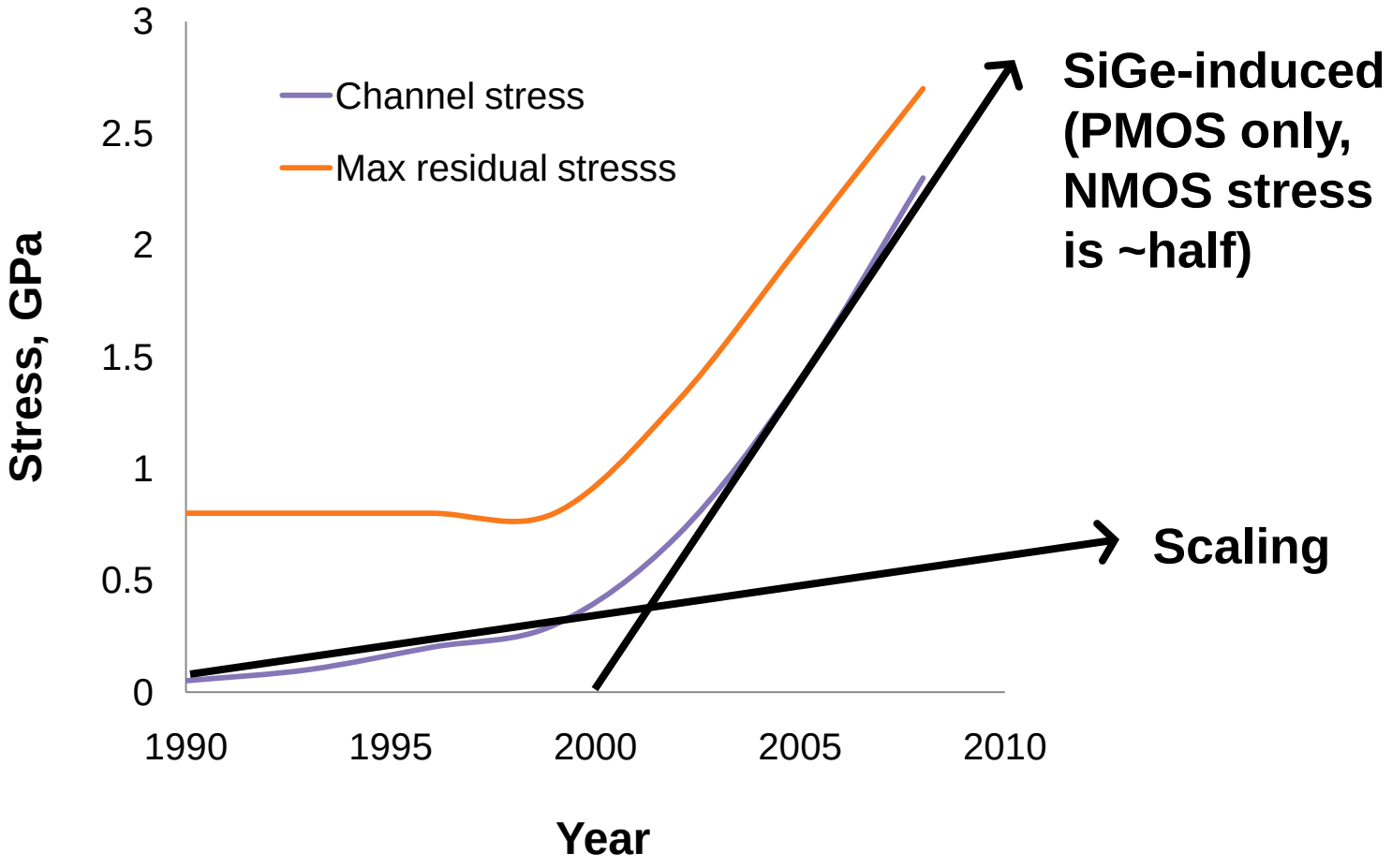

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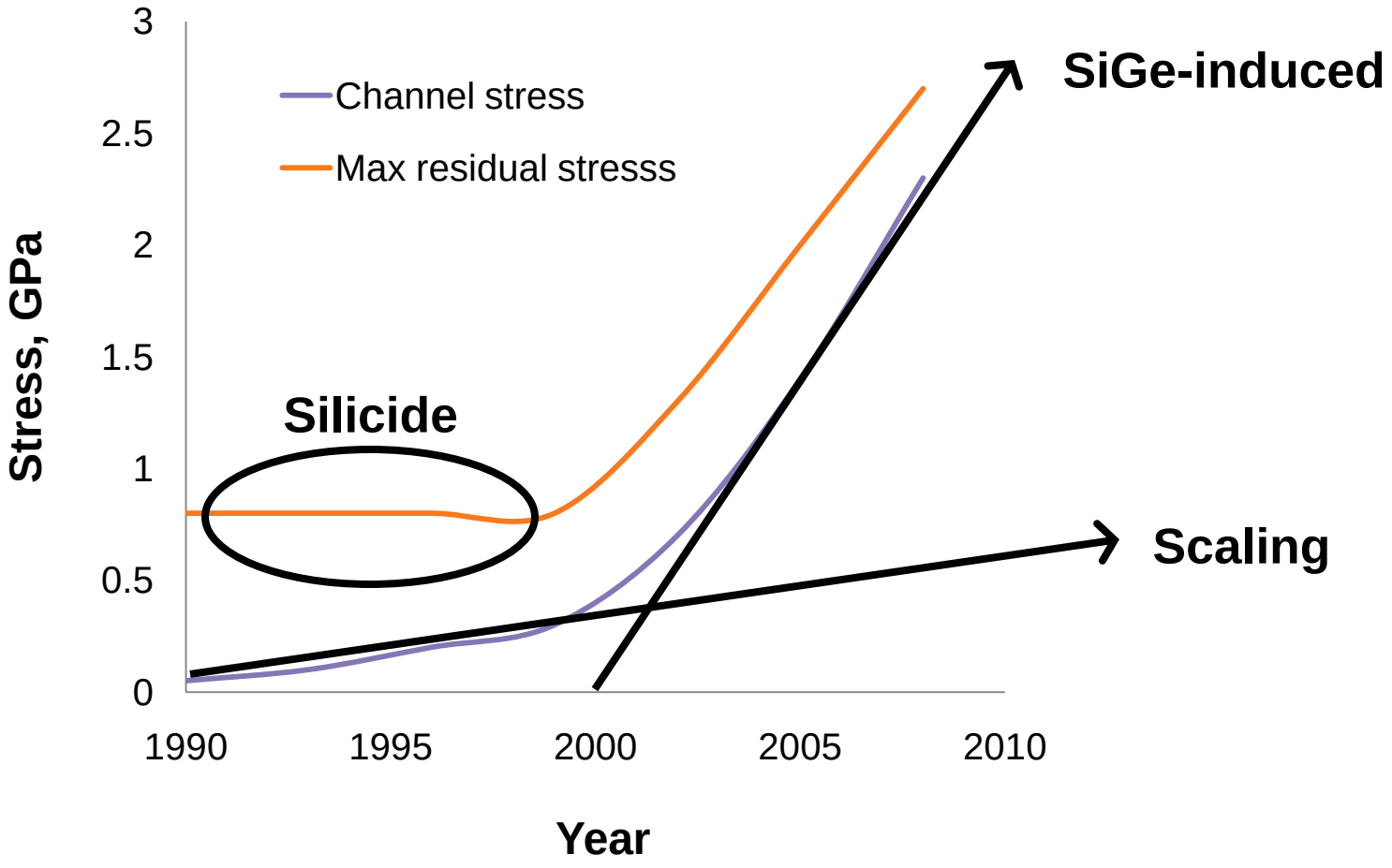

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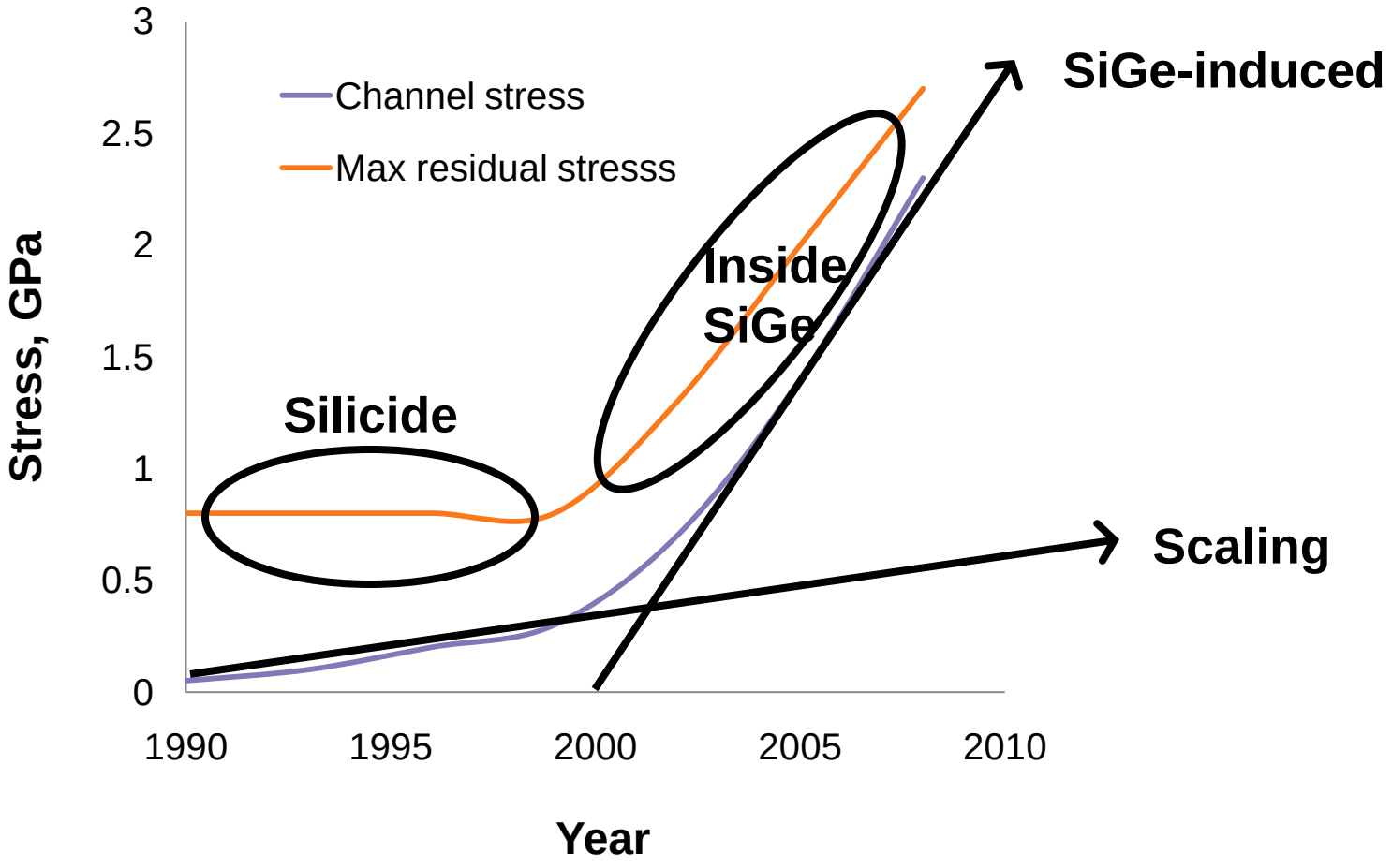

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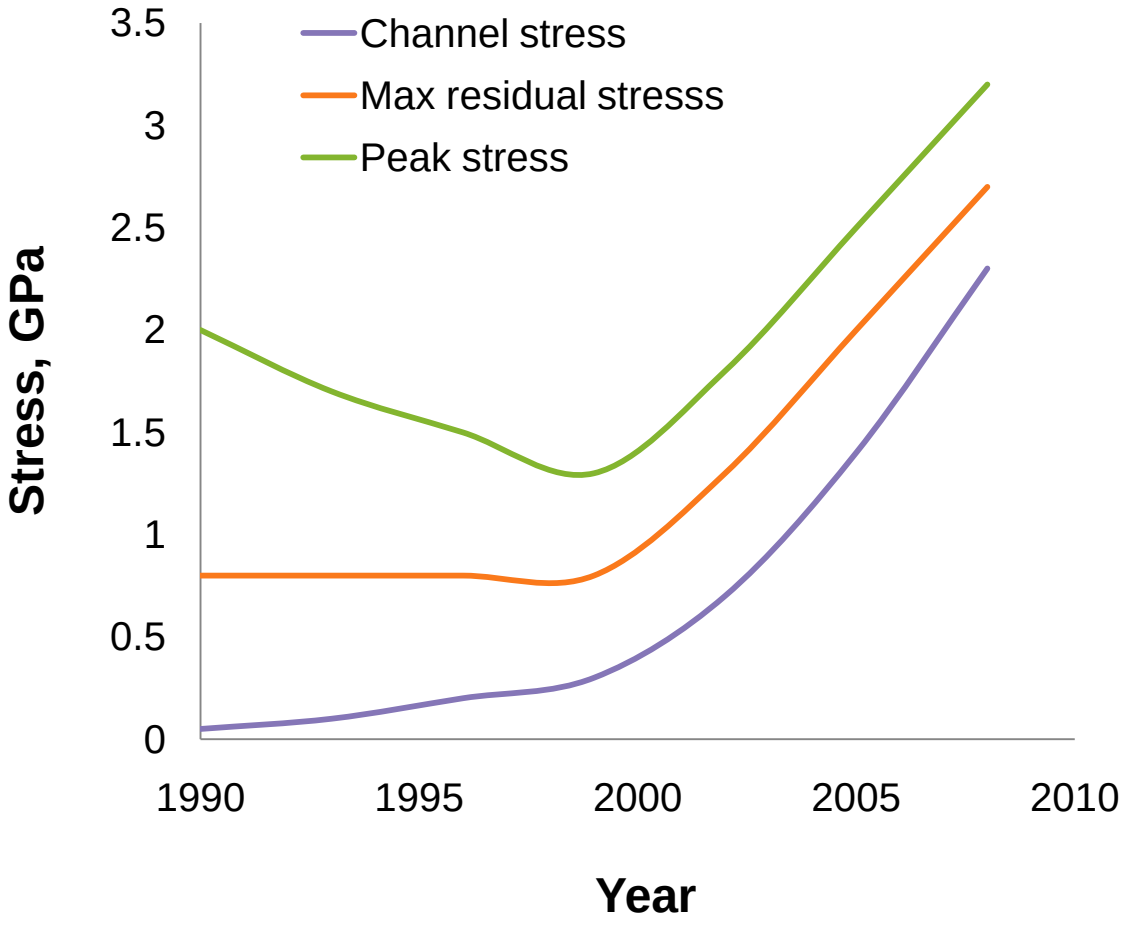

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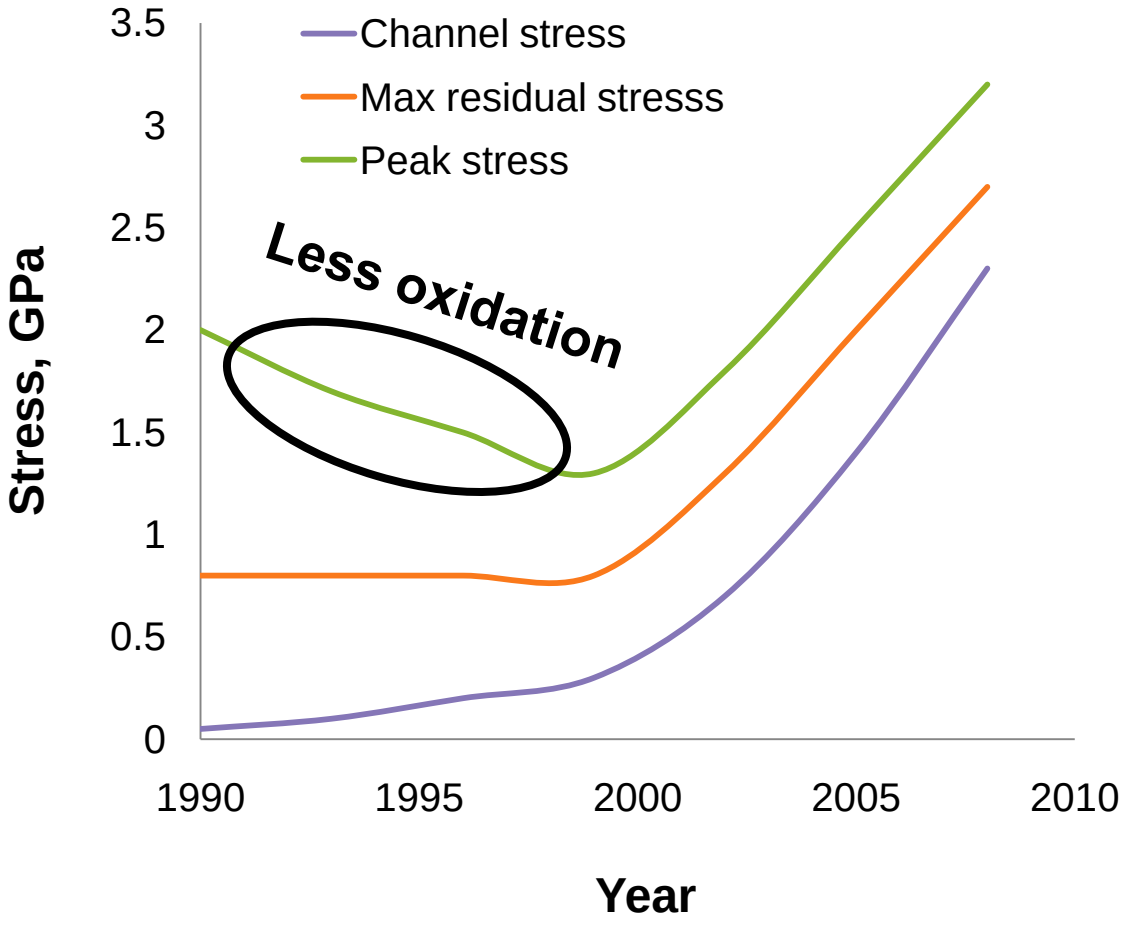

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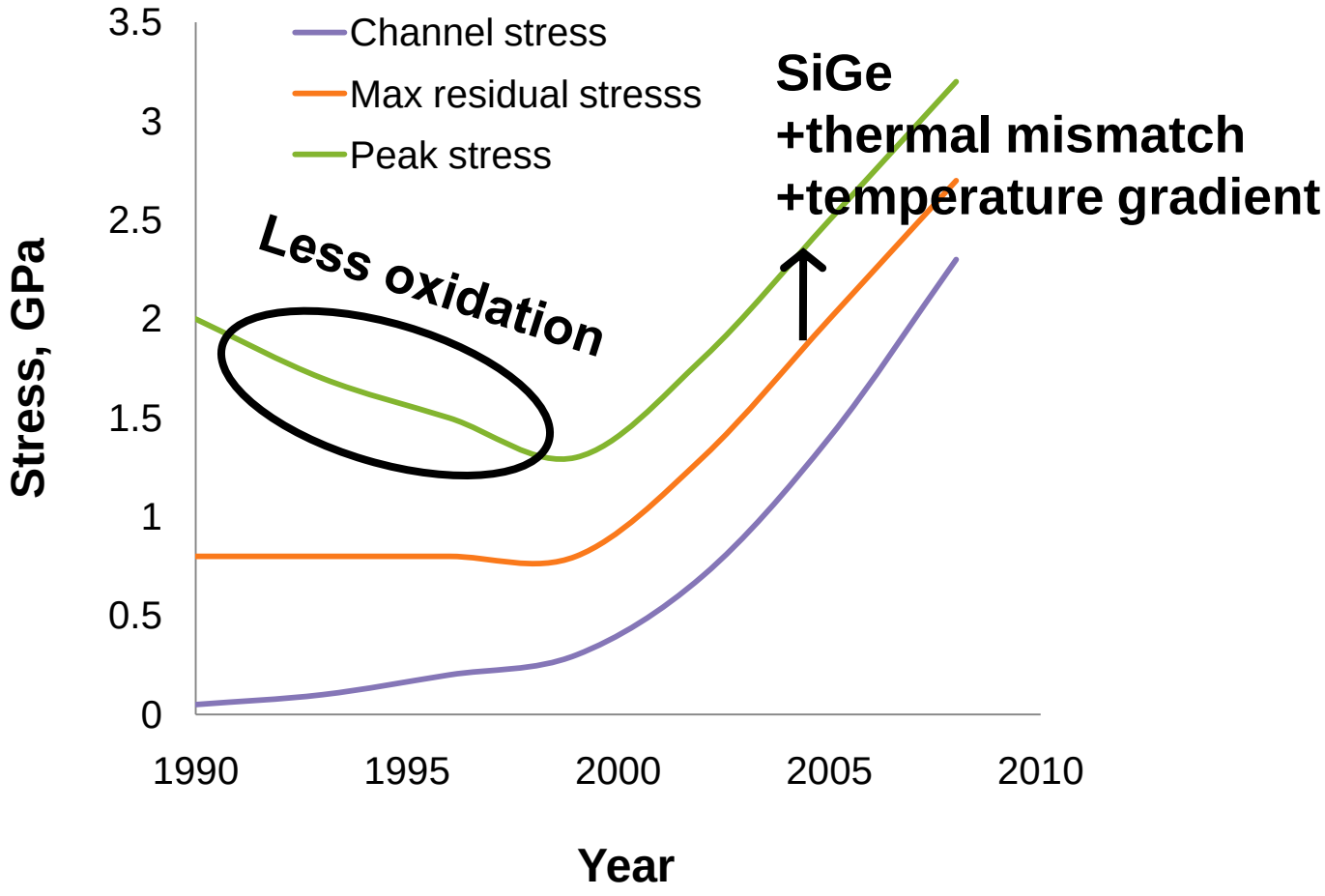

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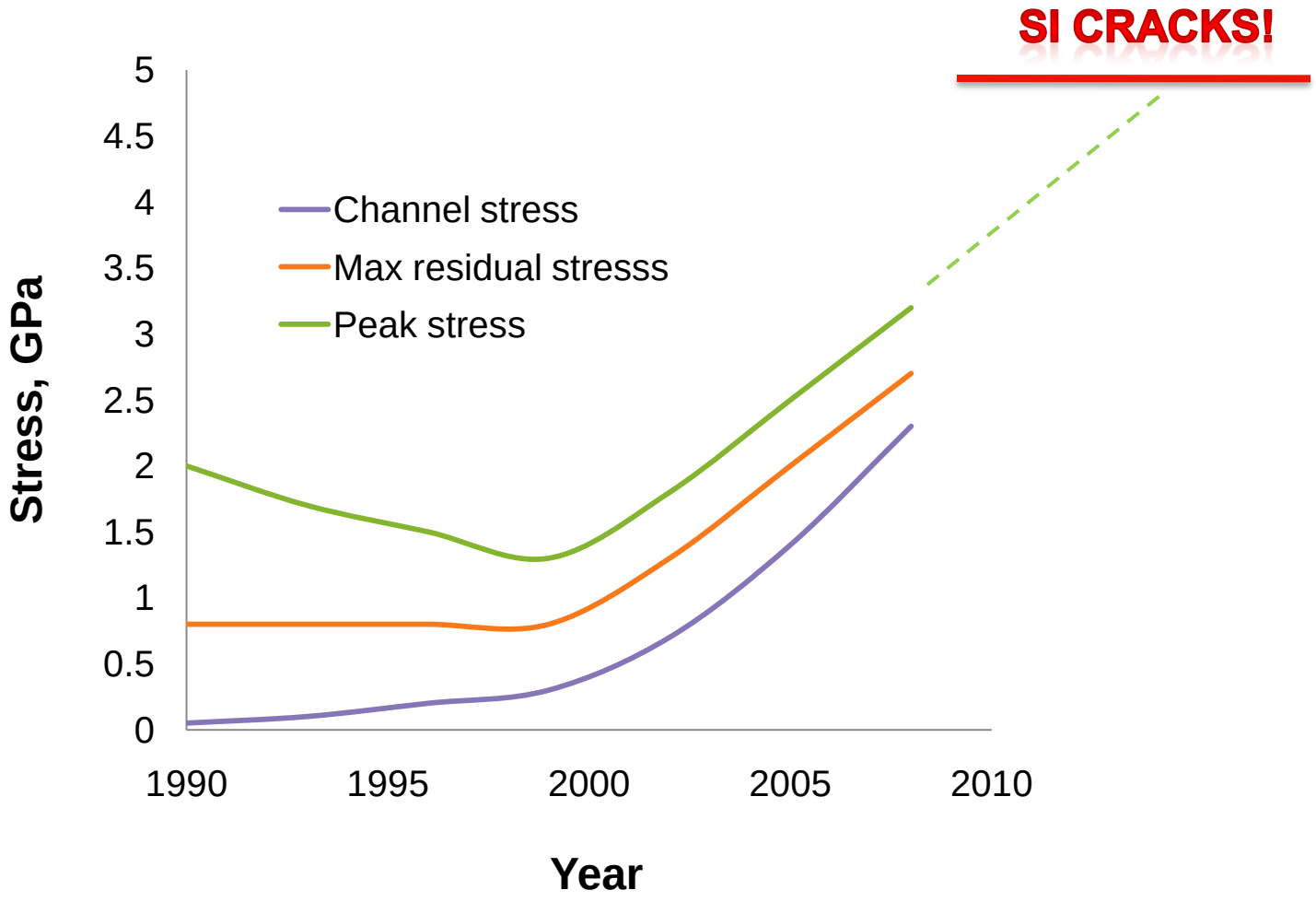
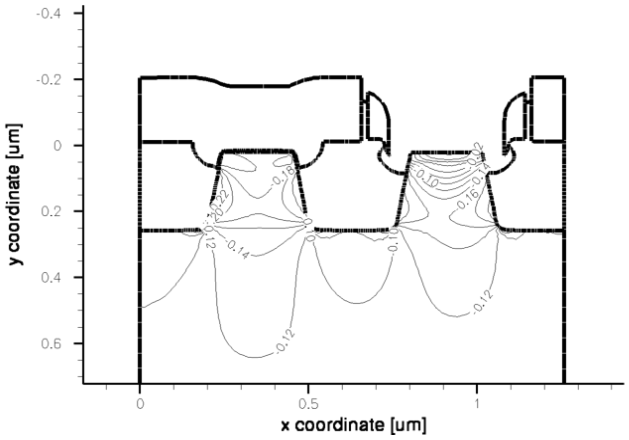
How Much Stress Is Too Much?

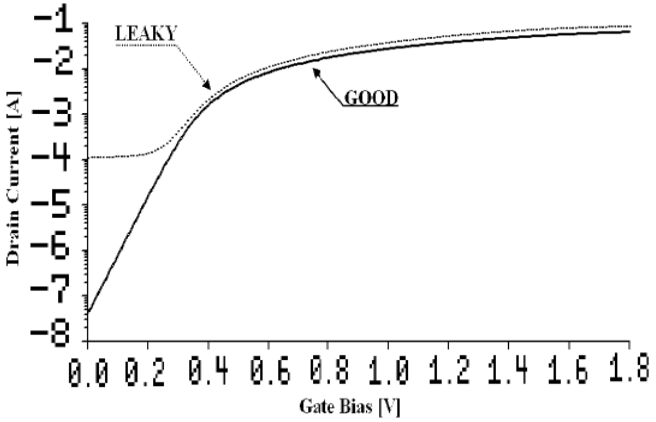
- Mechanical strength of Si is ~5 GPa
- Defect formation happens much earlier
  - Depends on impurities like oxygen
  - Depends on thermal history
- Some stresses are more damaging than others, like shear stress in a dislocation slip plane
- Tensile stress is worse than compressive

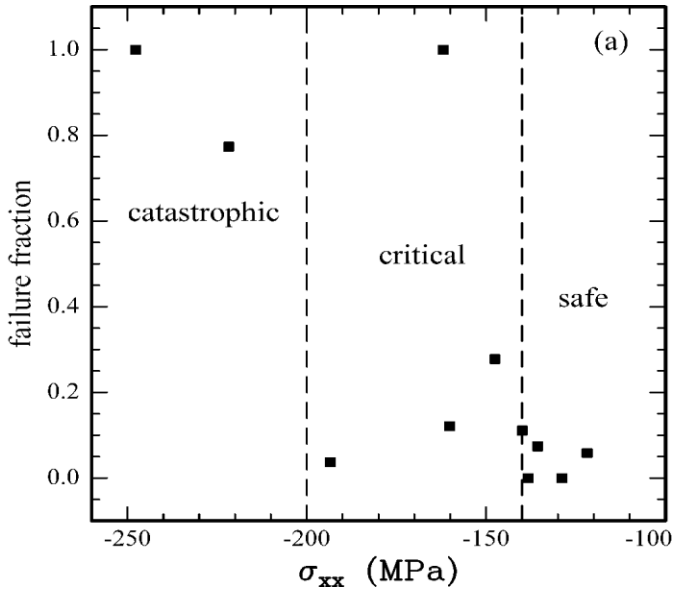
Stress in Transistors in Production

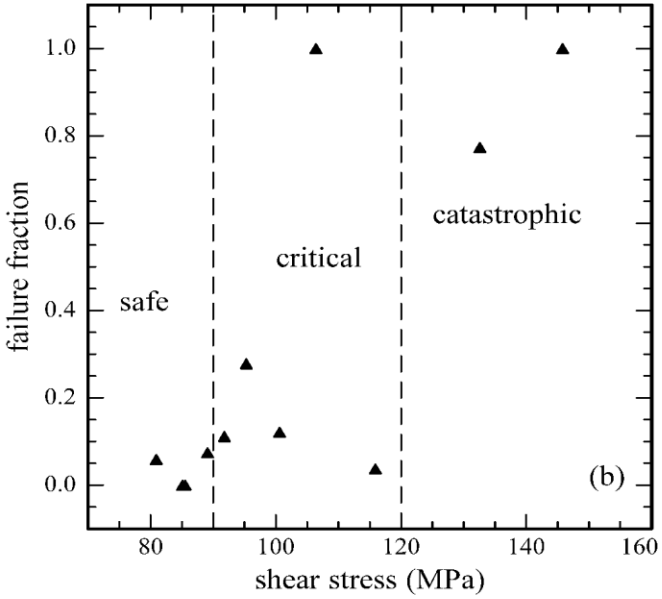


Numonyx: STI-Induced Dislocations



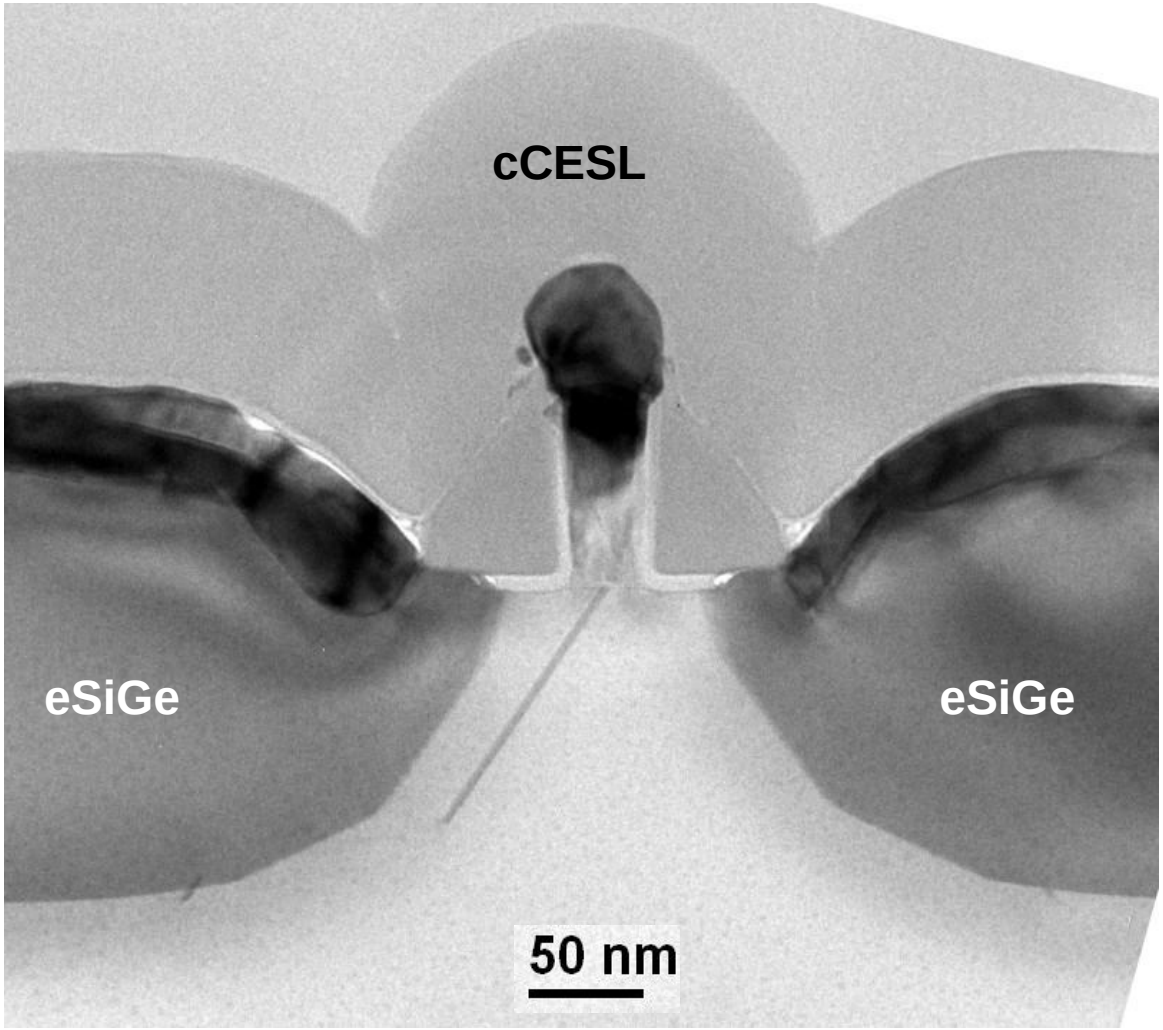






Polignano et al, TED'07

Stress-Induced Dislocations



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Junction Leakage vs Bandgap

Thermal generation-recombination current exponentially decreases with band gap increase:

$$J/J_{ref} = \exp(\Delta Eg/2kT)$$

The band gap in turn depends on stress and impurities like Ge

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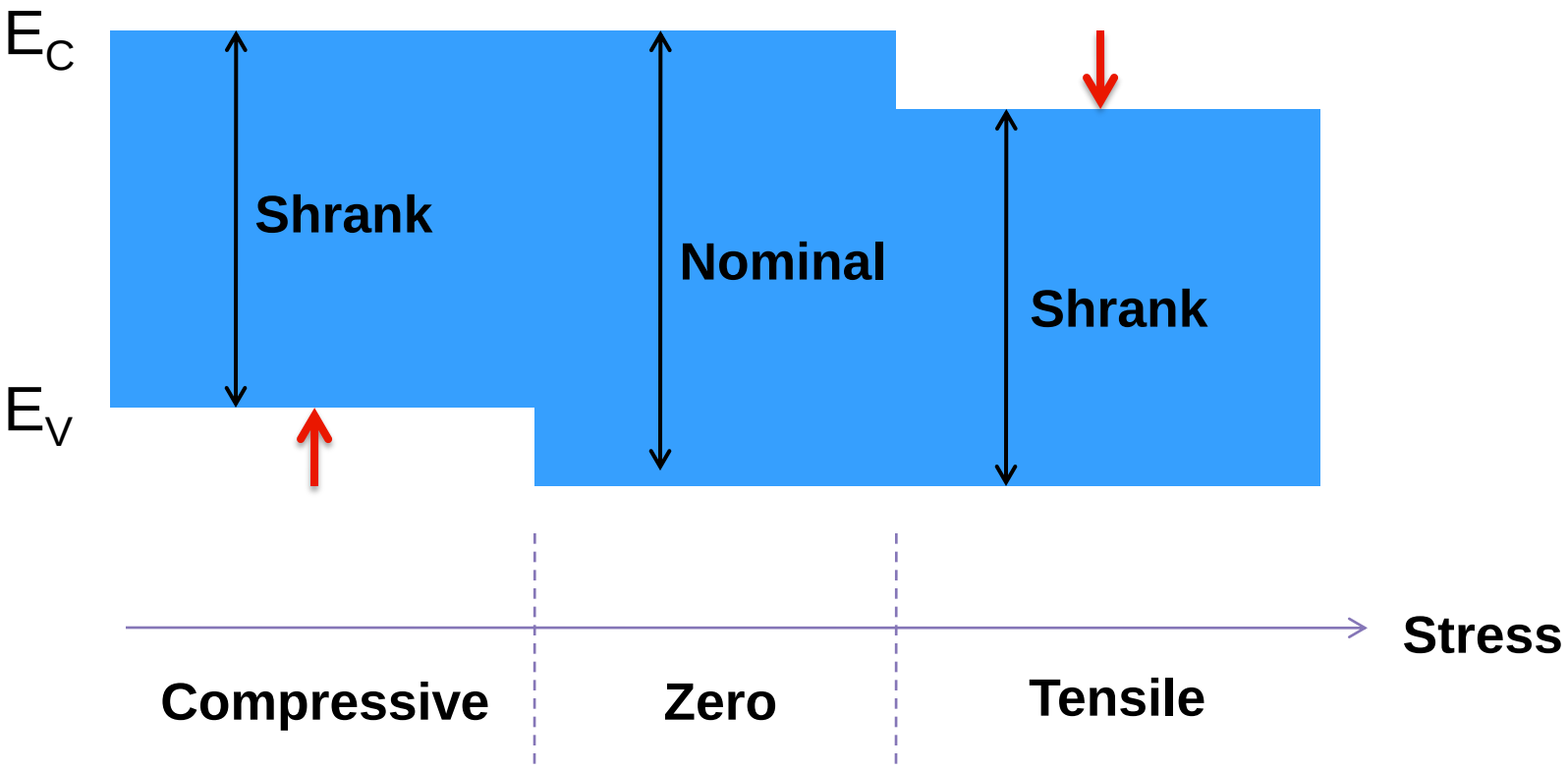
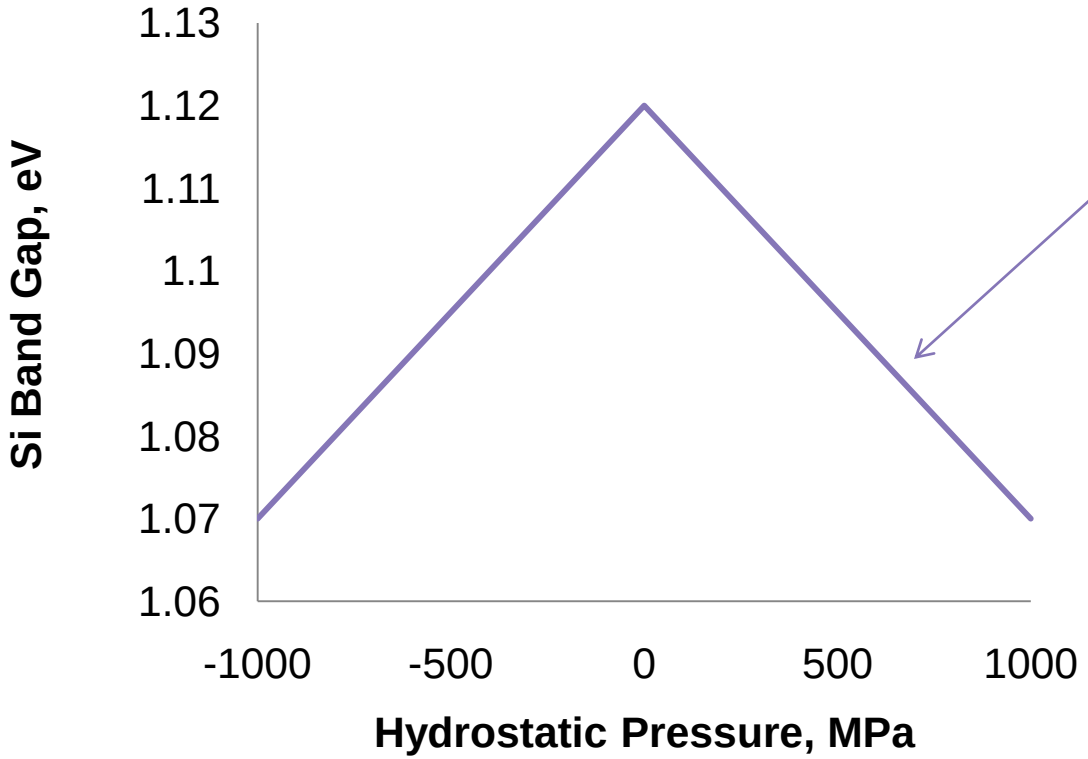
Band Structure vs Stress (Simplified)



Bandgap vs Stress

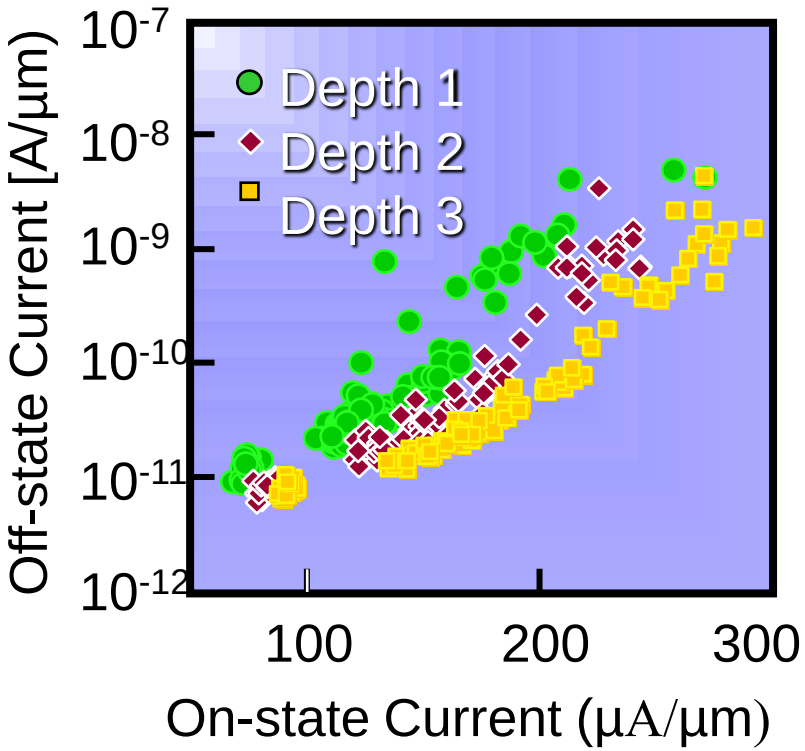


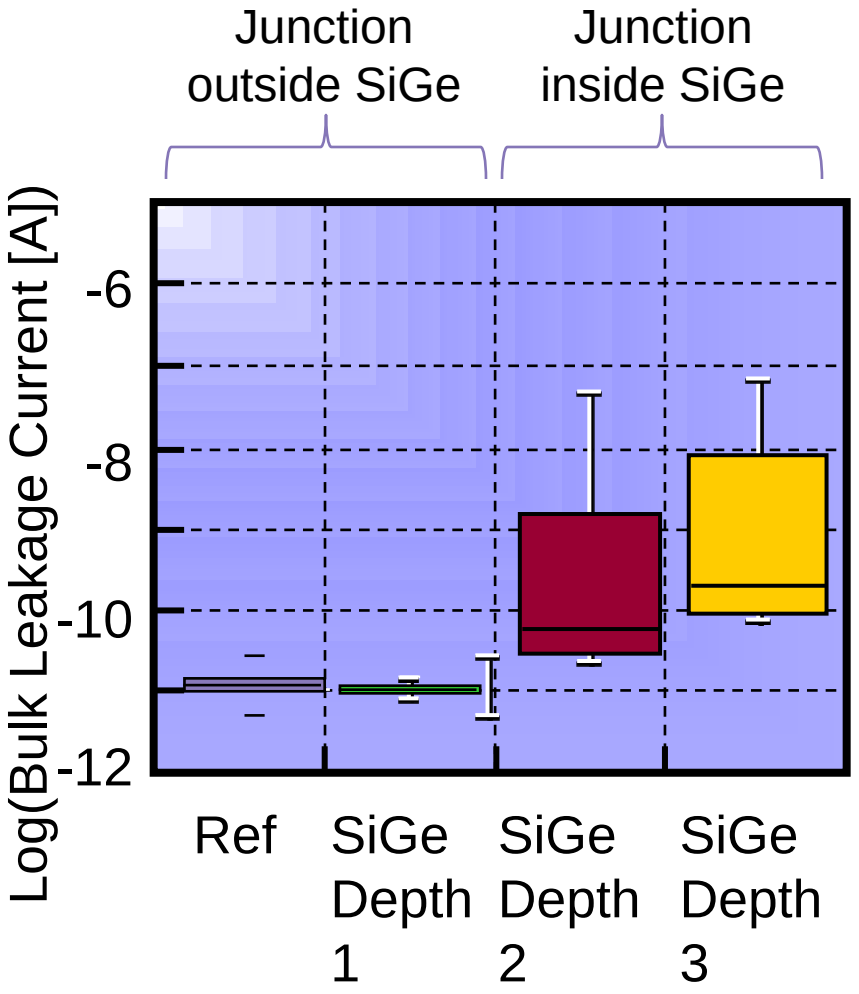
Close to symmetric,
~50 mV/GPa

Example: S/D Junction Inside 20% SiGe

- Compressive stress shrinks Eg by 90mV
- 20% germanium adds another 80mV
- Total band gap narrowing is 80mV + 90mV = 170mV
- This increases junction leakage by ~30x

Stress Impact on Junction Leakage

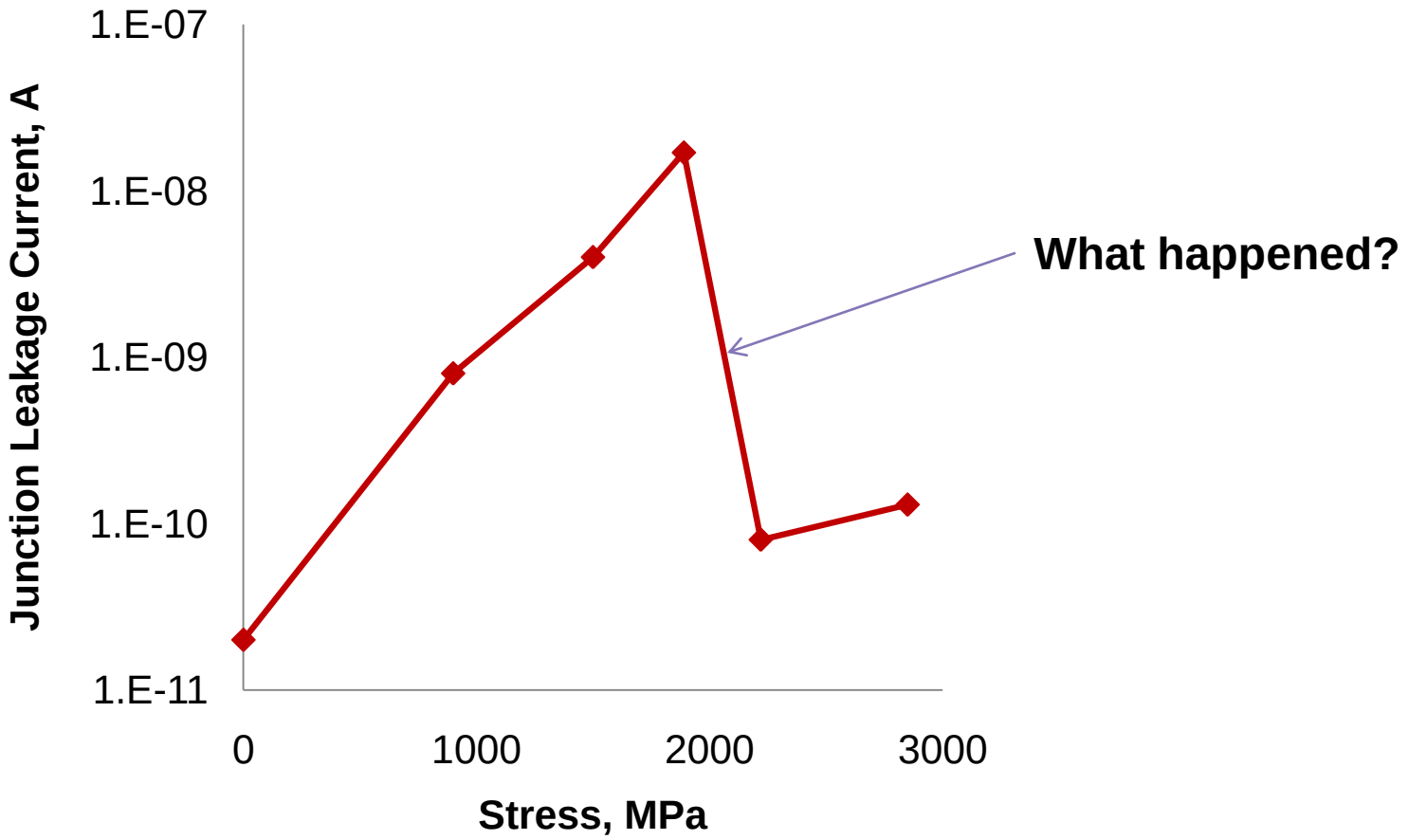




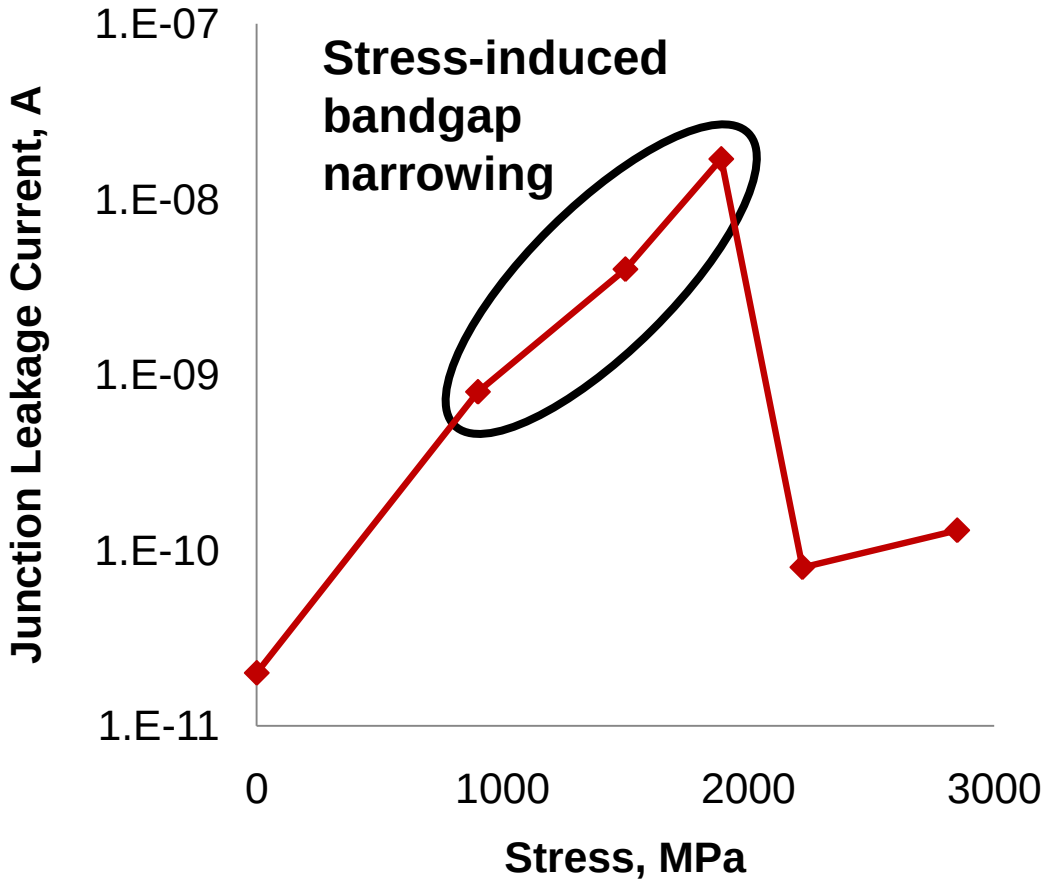
Depth 1 < Depth 2 < Depth 3

Nouri et al, IEDM'04

Junction Leakage: Typical Observation



Junction Leakage: Typical Observation



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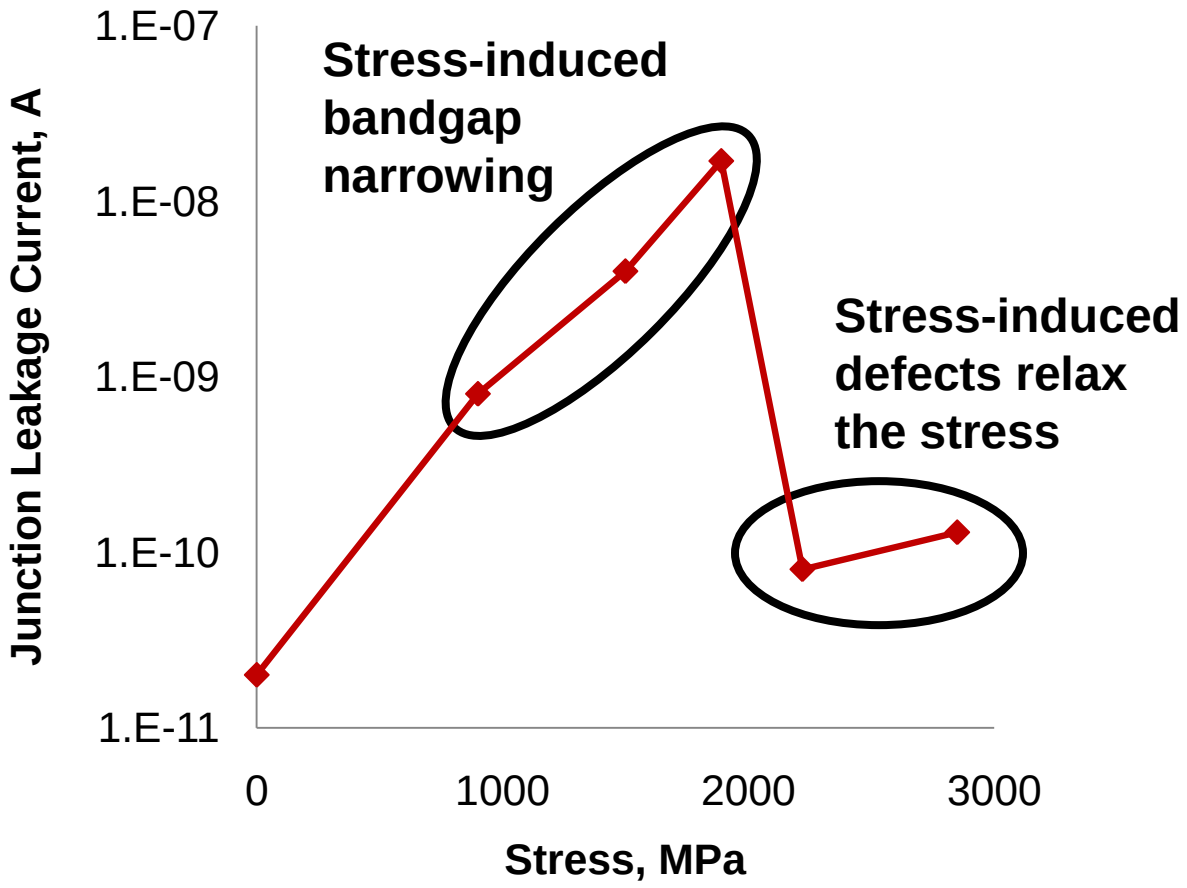
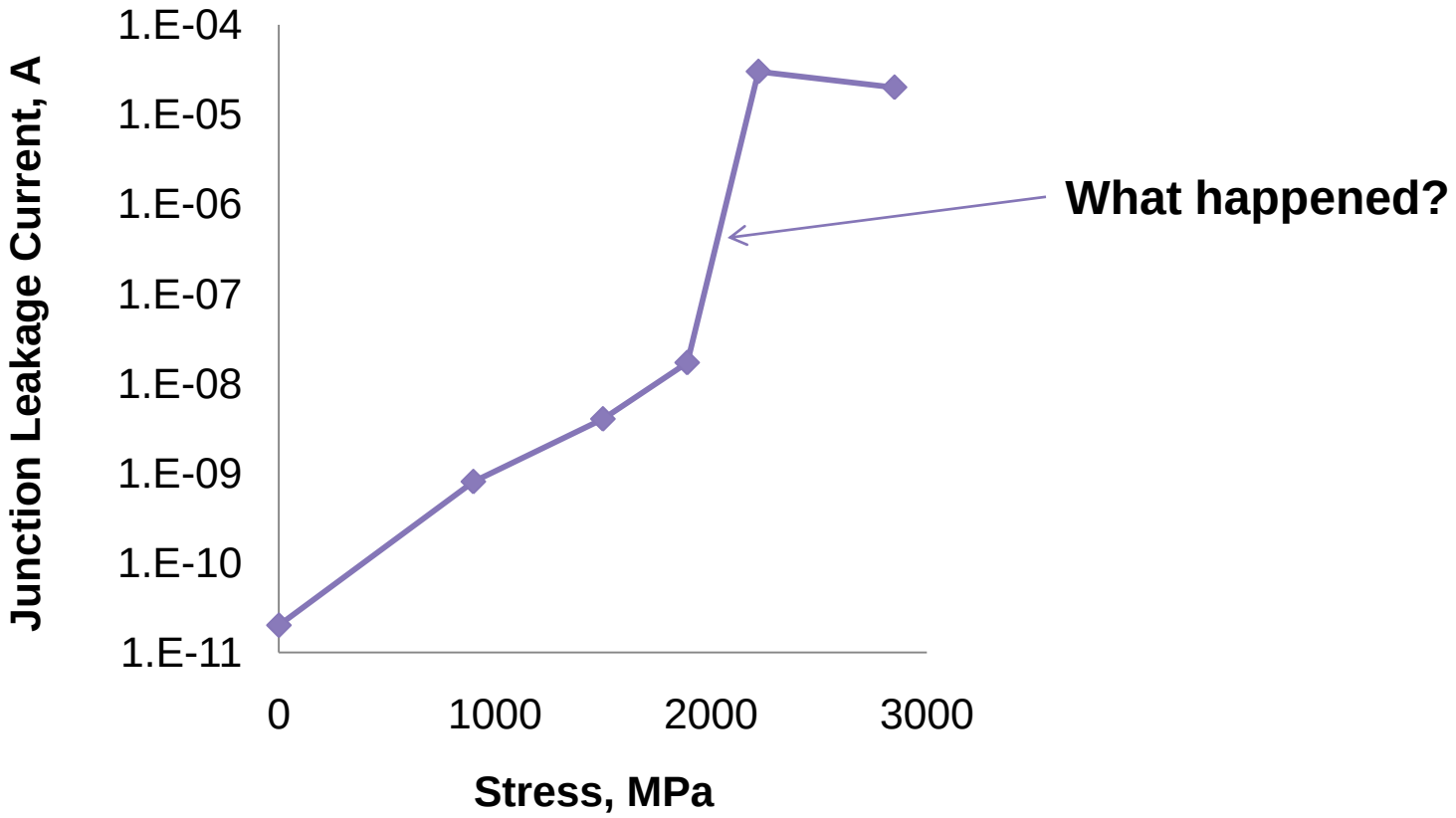


Junction Leakage: Alternative Behavior



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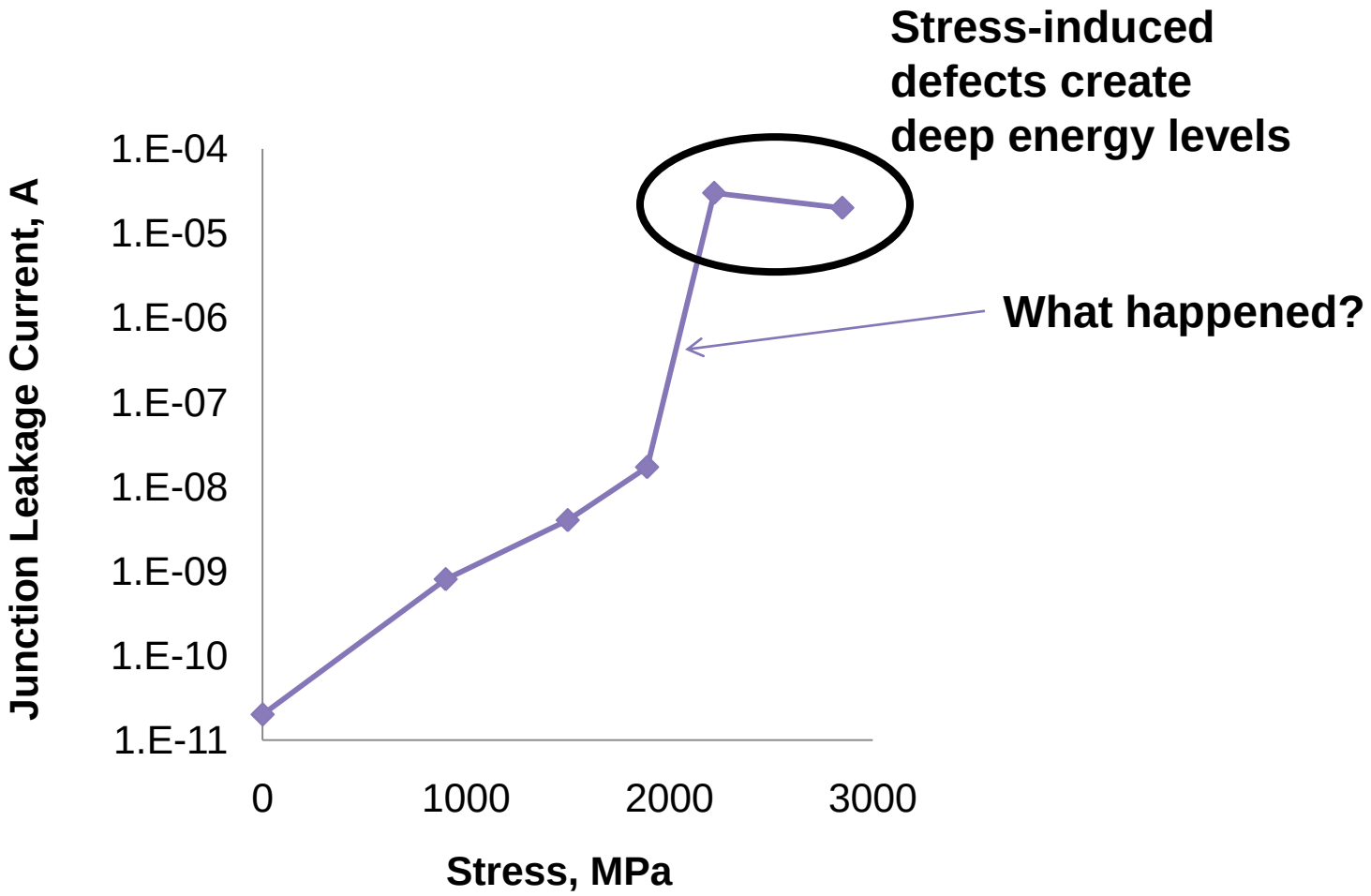
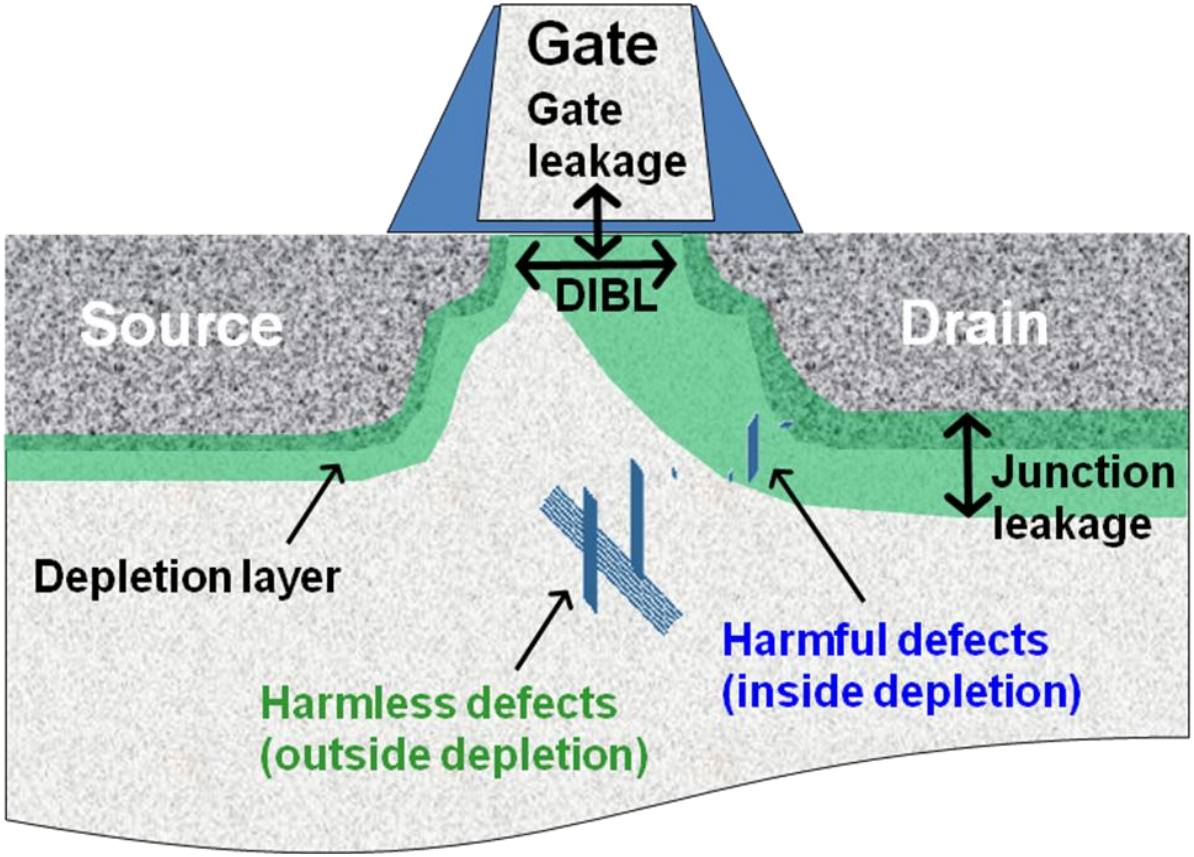
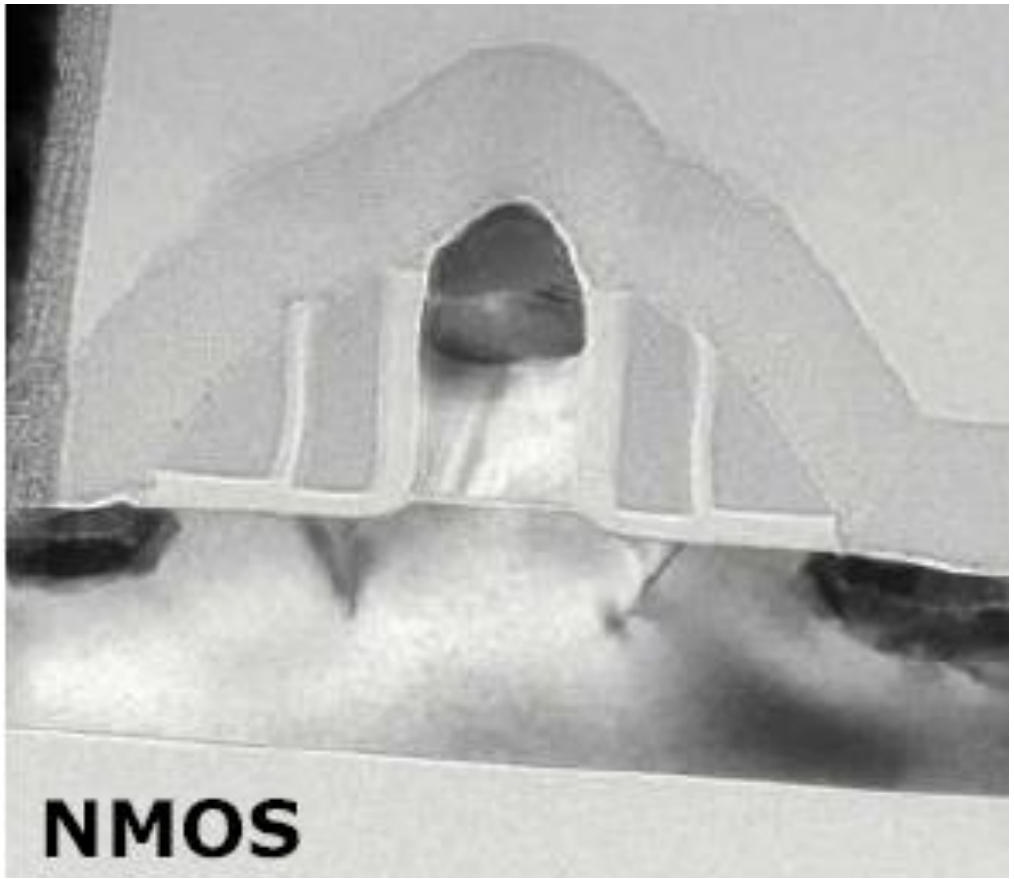


Harmful Stress and Defects



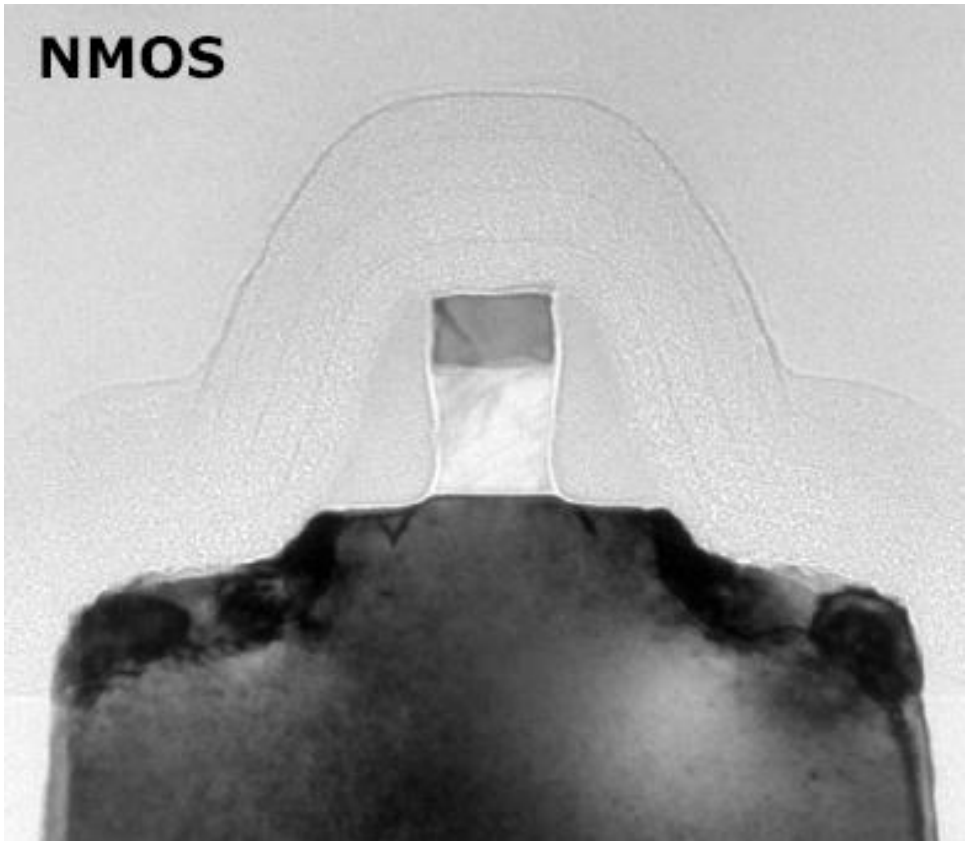
Safe Dislocations



TEM image of a 50nm SOI transistor from AMD Athlon 64 2700 chip, showing harmless dislocations under the spacers

Source: Chipworks

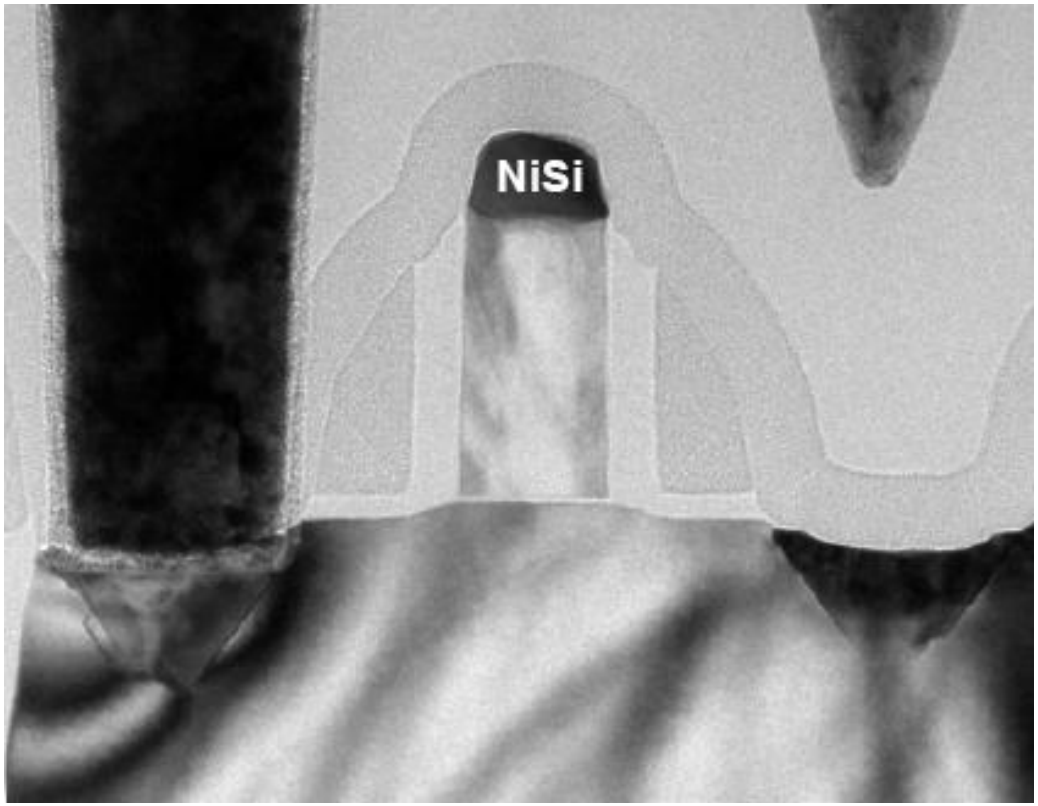
Safe Dislocations



TEM image of a 42nm transistor from Intel's Presler chip, showing harmless dislocations under the spacers

Source: Chipworks

Safe Dislocations



TEM image of a 55nm transistor from Matsushita's DVD SOC chip, showing dislocations under the silicide that are apparently harmless

Source: Chipworks

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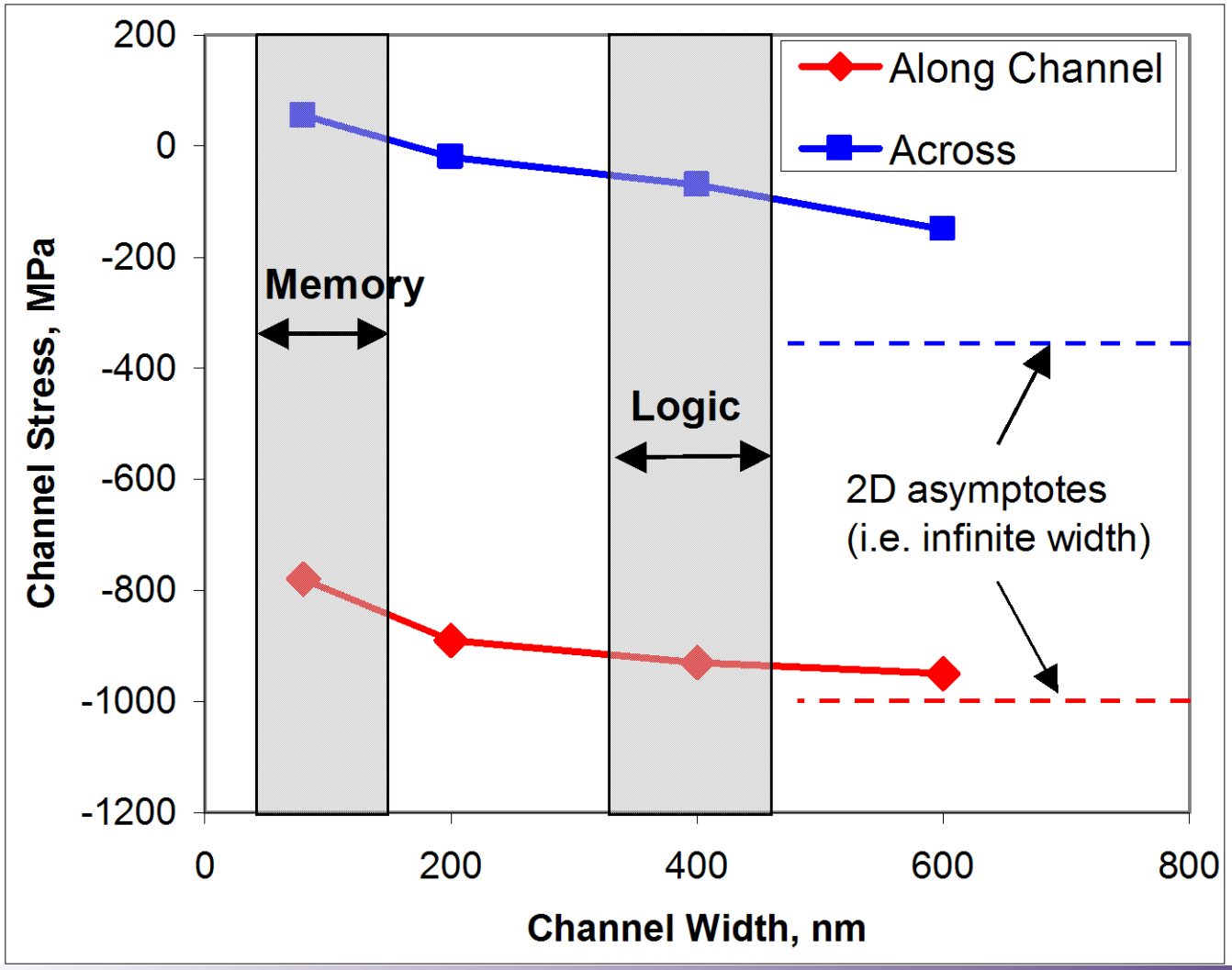
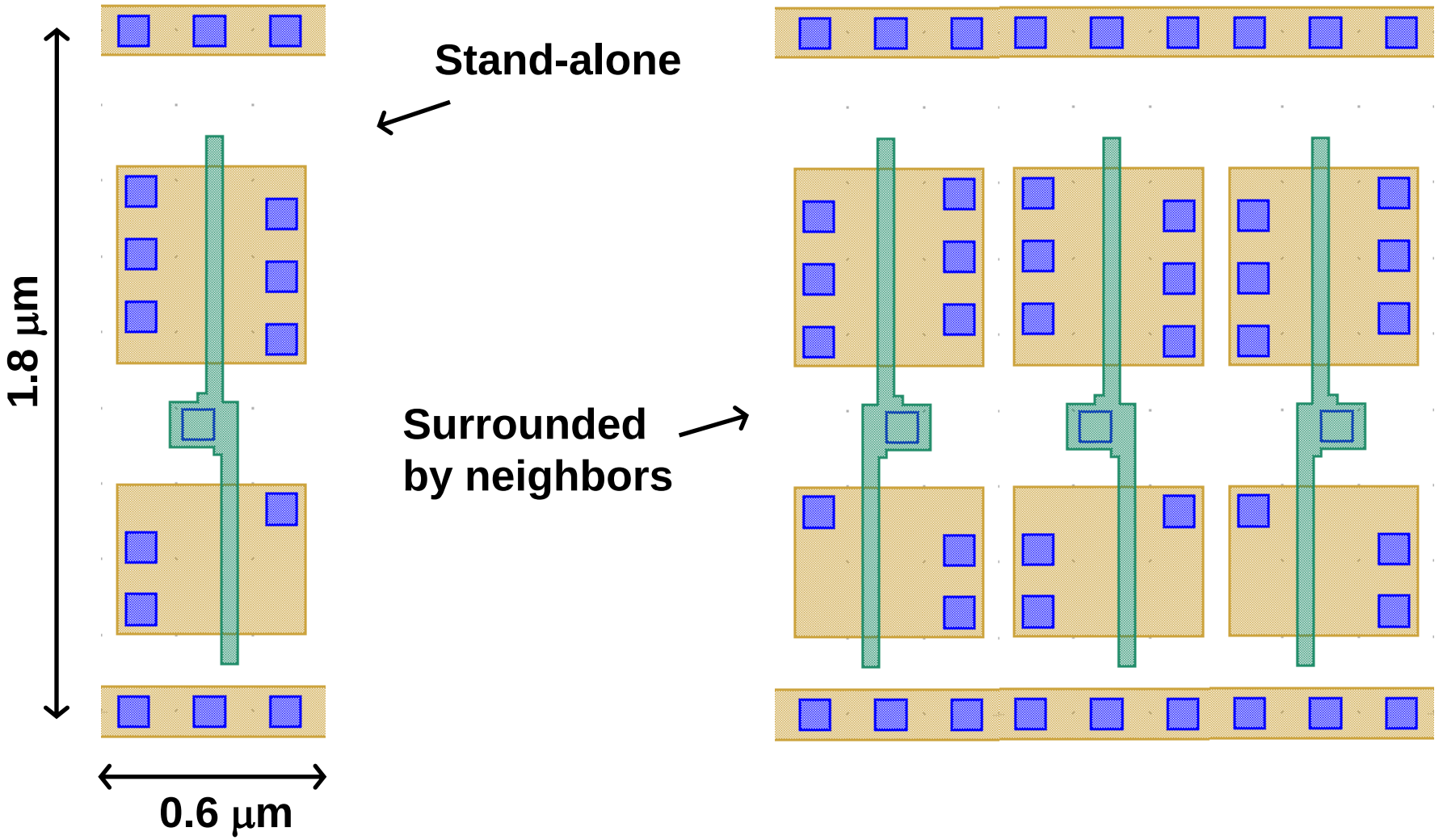
3D Stress Modeling for Typical W's



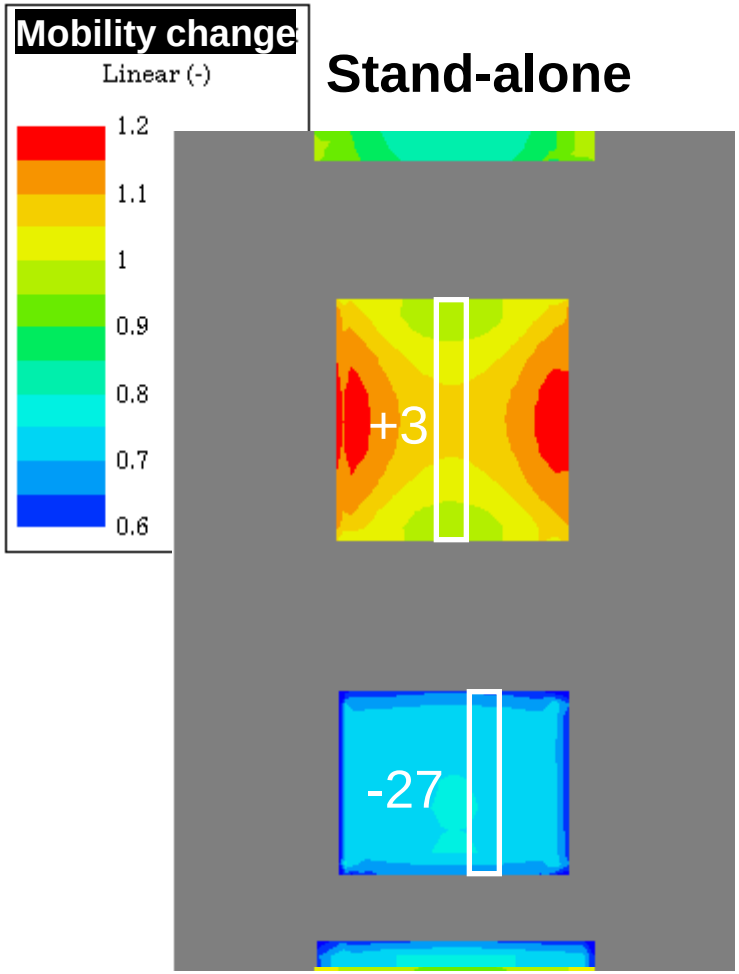
2D is not enough. All typical Xtors require 3D

Moroz et al, Solid State Technology'04

2 Inverters in Different Neighborhoods

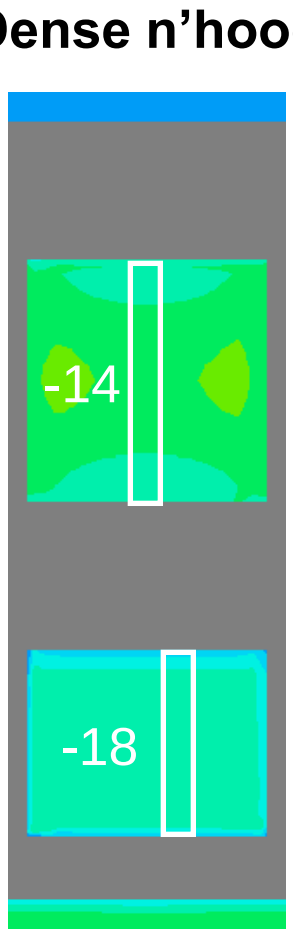


Stress-Induced Mobility Variation (%)

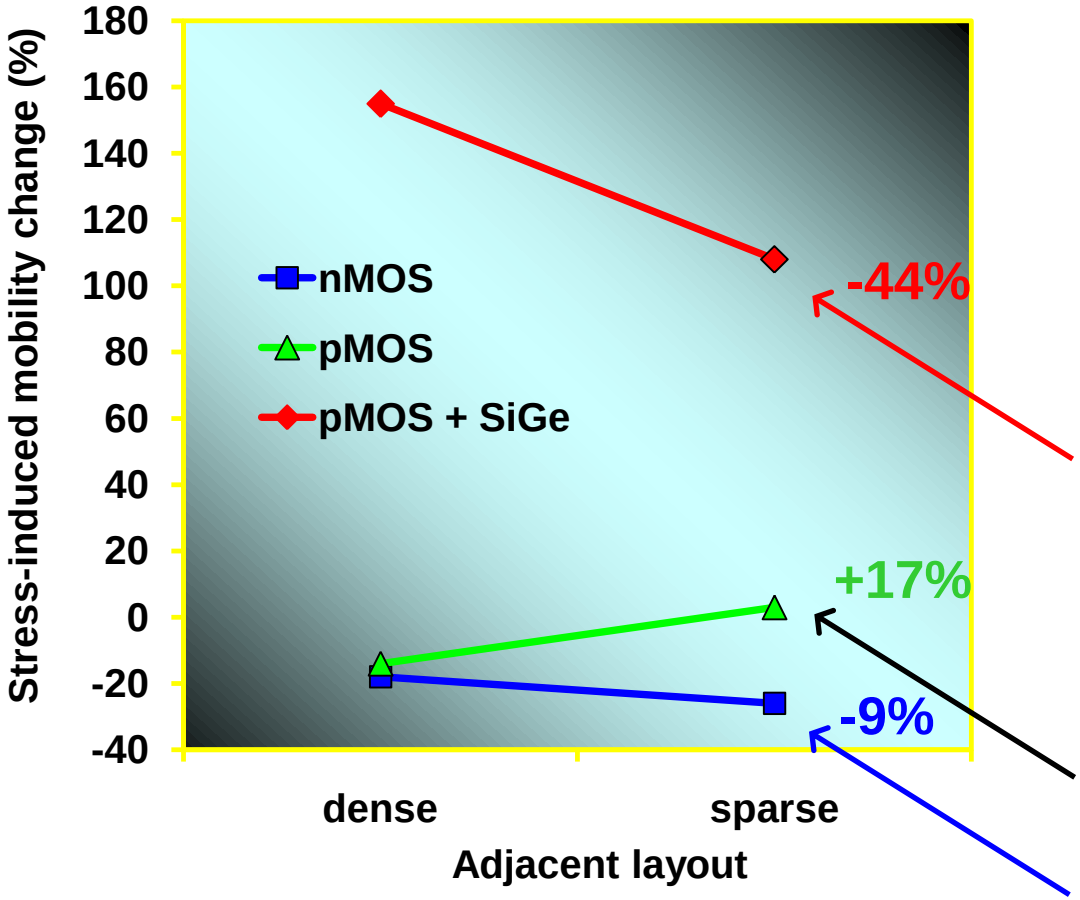


Things to notice:

- **pMOS difference 17%**
- **nMOS difference 9%**
- **nMOS/pMOS ratio difference 26%**



The Importance of Neighborhood



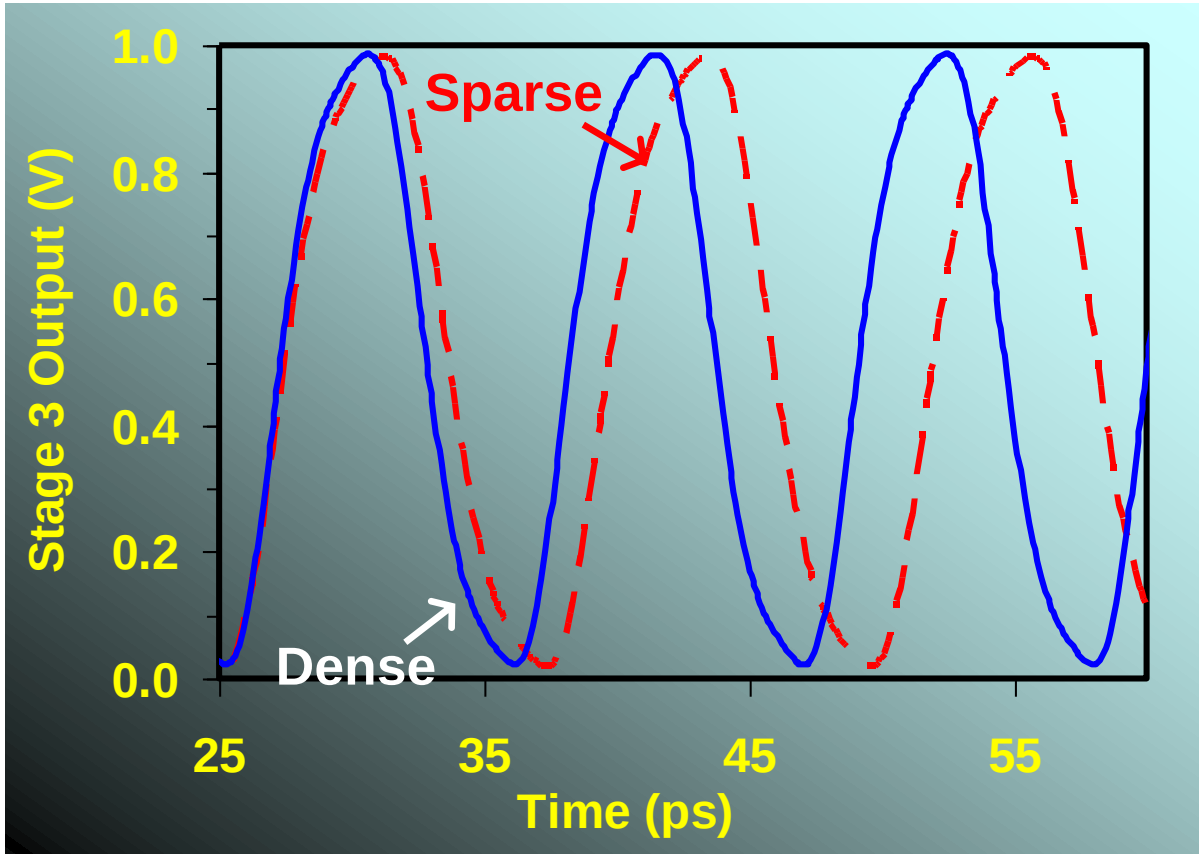
Introduction of eSiGe S/D:
- **Improves hole mobility**
- **Reverses the trend**
- **Still exhibits layout sensitivity**

Beneficial strong compressive SiGe stress is partially relaxed by relatively soft STI

Increased beneficial compressive STI stress

Increased harmful compressive STI stress

Competition of Two Ring Oscillators



The ring oscillator in dense layout neighborhood outruns the one in sparse layout by >10%

Moroz et al, ISQED'06

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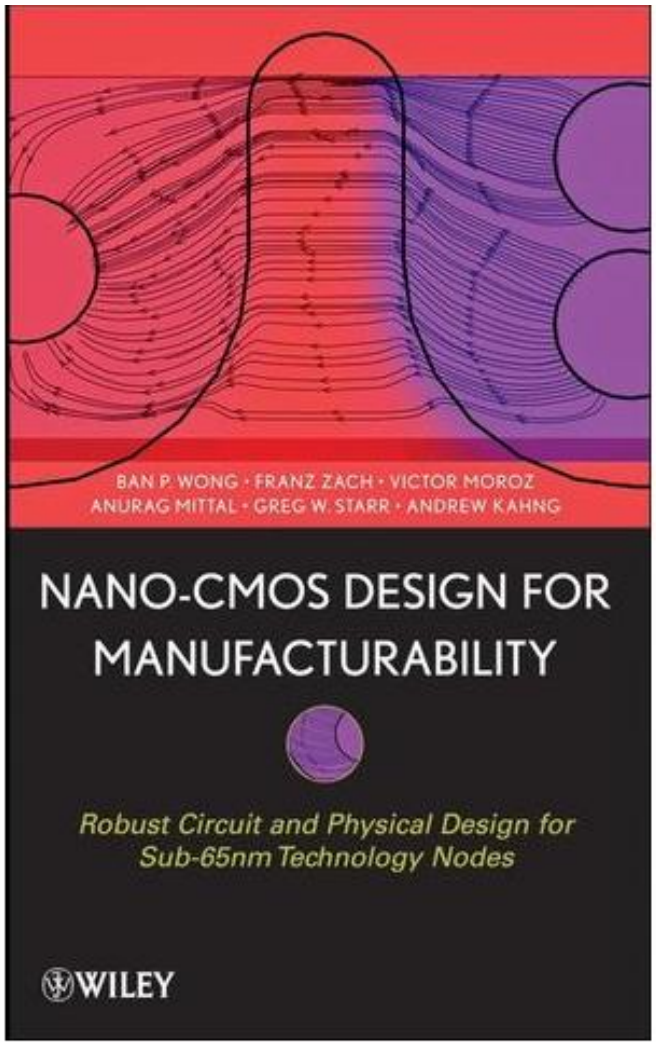
Non-Si Materials

- Qualitatively, the impact of stress on non-silicon semiconductors is similar to silicon.
- One important difference is that silicon is the most rigid of semiconductors of interest. That means that the same applied force leads to the larger strain in non-silicon semiconductors compared to silicon. For example, silicon has Youngs modulus of 165 GPa, whereas GaAs has Youngs modulus of only 85 GPa. The same stress corresponds to twice as big of a strain in GaAs compared to Si.
- The reason this is important is that it is strain that determines the band structure of a semiconductor.
- The flip side of the lower Youngs modulus is that the material is not as strong and suffers from defects and cracks at a lower stress level.

Conclusions

- Can not increase stress much higher than current leading edge
- Stress and Ge induced band gap narrowing can be simulated
- Bandgap narrowing degrades junction leakage
- Stress-induced defects can be beneficial
- Stress is a strong function of layout
- Stress will be used beyond silicon

The Upcoming Book



These and other related effects are described in the book coming out on October 17, 2008