Carrier Recombination, Leakage Current and all that…..

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Junction Leakage Current Mechanisms: Defects & Doping

Carrier Recombination-based Metrologies

- **Photoluminescence, MOR (TW)**
- **Surface charge, JPV leakage (RsL)**

Machine and Process Effects

- **ms-Anneals, Support pins, Halo damage & doping**

Guidelines for low-leakage process

- **Scan rates, Beam current, Molecular ions, Cryo-implants**

Leakage Current

Leakage current limits planar CMOS scaling.

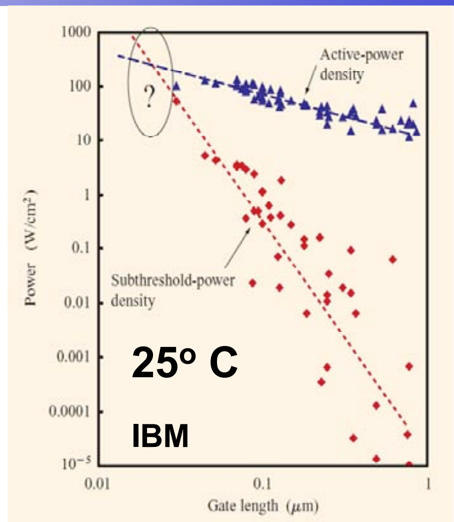
* Carrier recombination/generation (SRH)
* Band-to-band tunneling (BTBT)
* Sub-threshold leakage (DIBL, etc.)
* Gate oxide leakage (high-k)

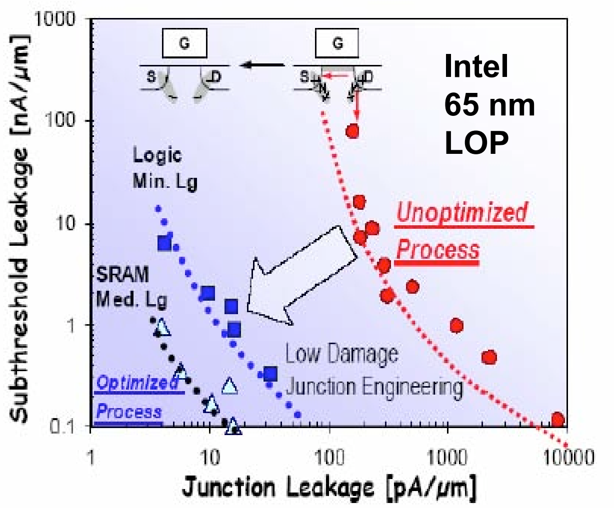
Diffusing junctions to be deeper than damage works for >65 nm CMOS.

For 45 nm CMOS, junctions are “diffusion-less”. As-implanted damage is the key factor.

Other tradeoffs:

* L_{gate}, t_{ox}, V_{th}, layout rules, etc.





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Nowak/IBM 02, Jan/Intel 05

Leakage Current: Defects

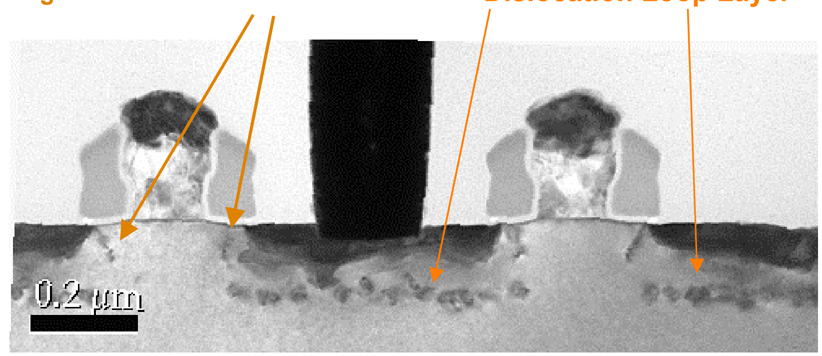
Defects in junction depletion zone drive process-related leakage.

Damage Leakage Mechanisms:

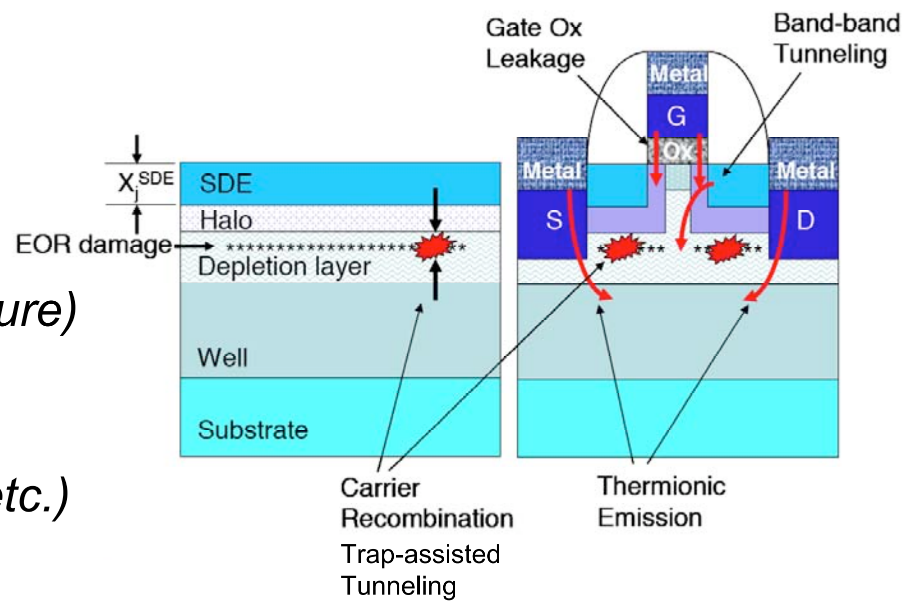
* Carrier recombination/generation *(Shockley-Read-Hall)*
* Trap-assisted tunneling *(TAT).*

Process Options:

* **Implant damage & sequences**
  (ion type/energy/dose, beam current/scan rate/wafer temperature)
* **Anneal conditions**
  (peak temperature, time, ambient, temperature ramp rate, base temperature, etc.)



XTEM Pentium Transistors (Courtesy of Intel)



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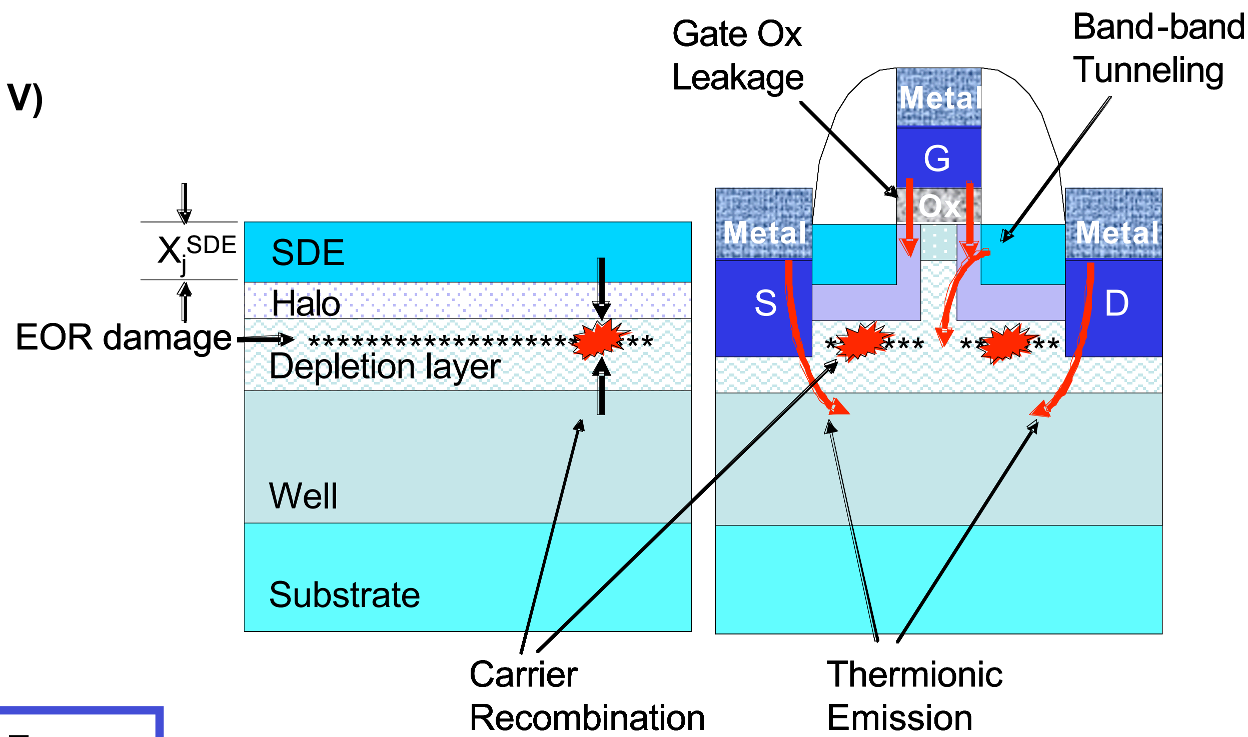
Leakage Current: Test wafers & Transistors

Light illumination (forward bias ~25 mV)
Carrier recombination
Trap assisted tunneling

Transistors (reverse bias ~ -1 V)
Carrier Generation
Trap assisted tunneling
Band-to-band tunneling
Contact emission
Gate leakage
Sub-threshold current



$$J_{gen} = \mathbf{I_o(A/cm^2)} * (e^{qV/kT} - 1)$$

Leakage Current: Defects & Doping

$$\mathbf{J_{leakage} = \{J_{diffusion} + J_{surface}\} + J_{SCR} + J_{band\text{-}to\text{-}band}}$$

$$= \{[(q^*n_i^2/N_D)(D_n/\tau_n)^{1/2} + (qs^*n_i^2/N_A)](e^{qV/kT} + 1)\} \sim \mathit{10^{-10}\ A/cm^2\ for\ p^+/n(halo)}$$

$$+ q \int_{Xj}^{Xj+W} [(1+\Gamma_{TAT})[v_{th}\, \sigma_n \sigma_p\, N_{trap}(z)\, (pn-n_i^2)/(\sigma_n(n+n_1) + \sigma_p(p+p_1))]\, dz$$

$$+ qc\, V\, E_{max}^{3/2}\, (e^{-Eo/Emax})$$

$N_{trap}(z)$ = carrier trap density, σ_n, σ_p = carrier recombination cross-sections

For *forward bias* (light-generated carriers, V~+25 mV):

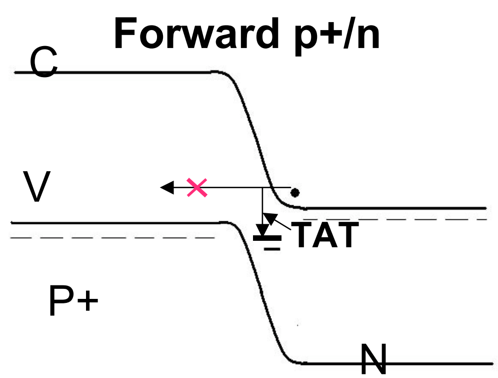
$J_{leakage}(+kT/q) \sim J_{SCR} = J_{SRH} + J_{TAT}$

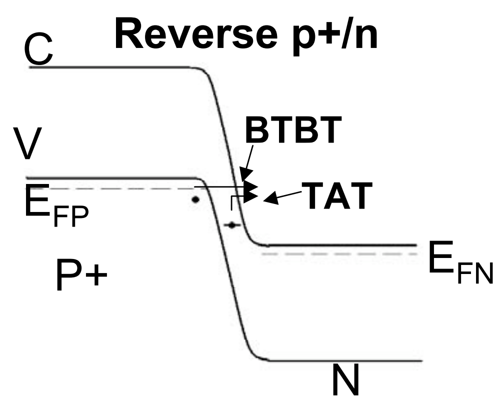
$= qn_i\, W\, (1+\Gamma_{TAT}) / \tau_{SRH}$

$= I_o(RsL)(e^{qV/kt} - 1)$

For *reverse bias*: (SRH +TAT +BTBT)

$J_{leakage}(-1V) \sim J_{SCR} + J_{BTBT}$





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Carrier Recombination-based Metrologies

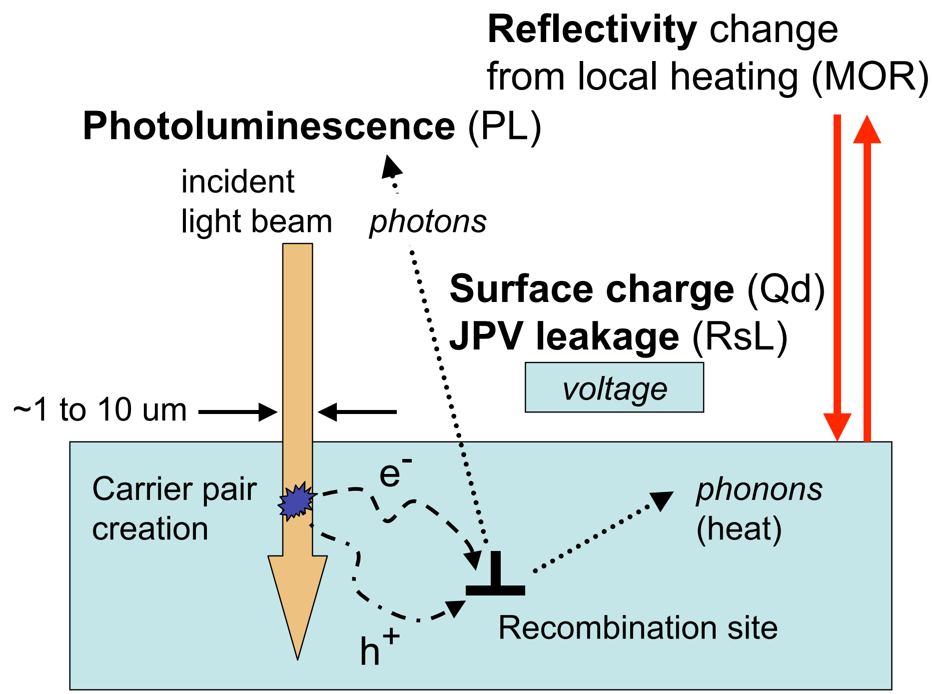
Carrier recombination drives the "process dependent" (damage & doping) aspects of junction leakage current.

Recombination effects are measured by photo-generated carriers:

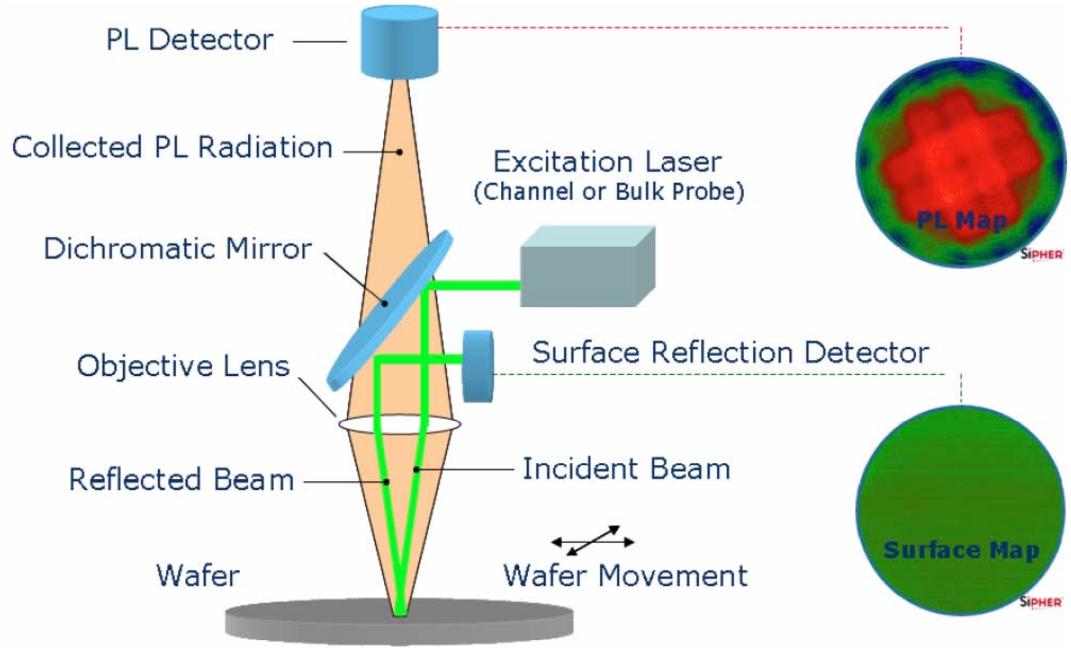
Carrier charge loss: Qd, RsL

Photon emission: PL

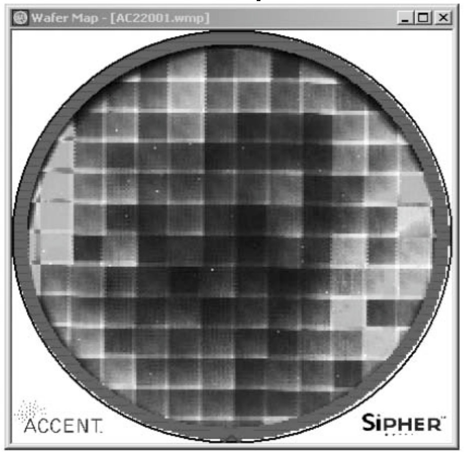
Phonon-driven reflectivity: MOR (TW)



Photoluminescence: PL



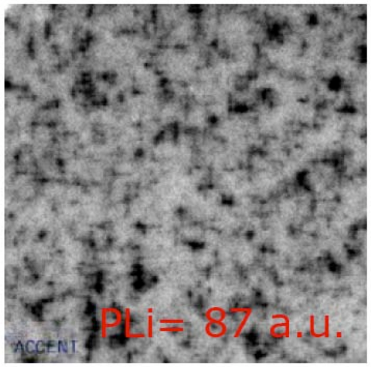
Step-pulse laser anneal
0.5 keV B implant



$$PLD_{internal} = (1/N_{photon})*[p / \tau_{rad}]$$

$$1/\tau = 1/\tau_{rad} + 1/\tau_{Auger} + 1/\tau_{SRH}$$

Flash annealed Ge PAI + B
500 um scan, 1 um step



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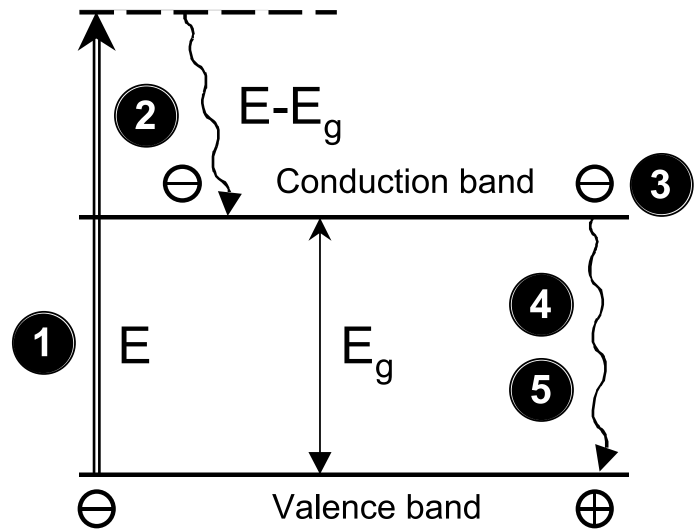
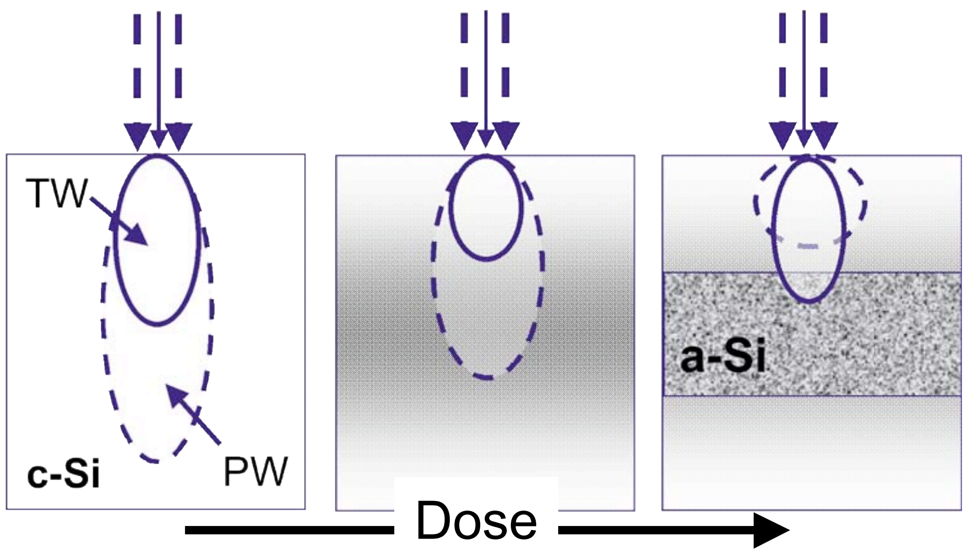
Modulated Optical Reflectance: Thermal Wave

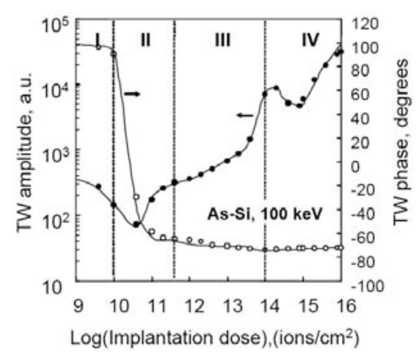
Modulated (~MHz) light beam:

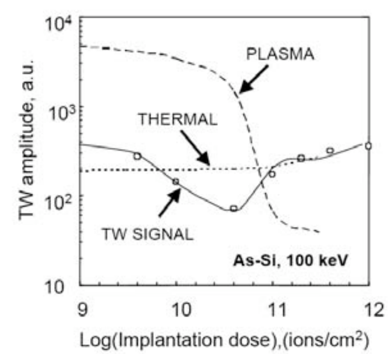
1. photons create carriers
2. electrons decay to conduction band
   (releases phonons = "thermal" wave)
3. carrier pairs diffuse ("plasma" wave)
4. carriers recombine at defects (4) or surface (5)
   (releasing more phonons).

DC light beam measures reflectivity changes.
(TW unit = 10 ppm change in reflectivity).









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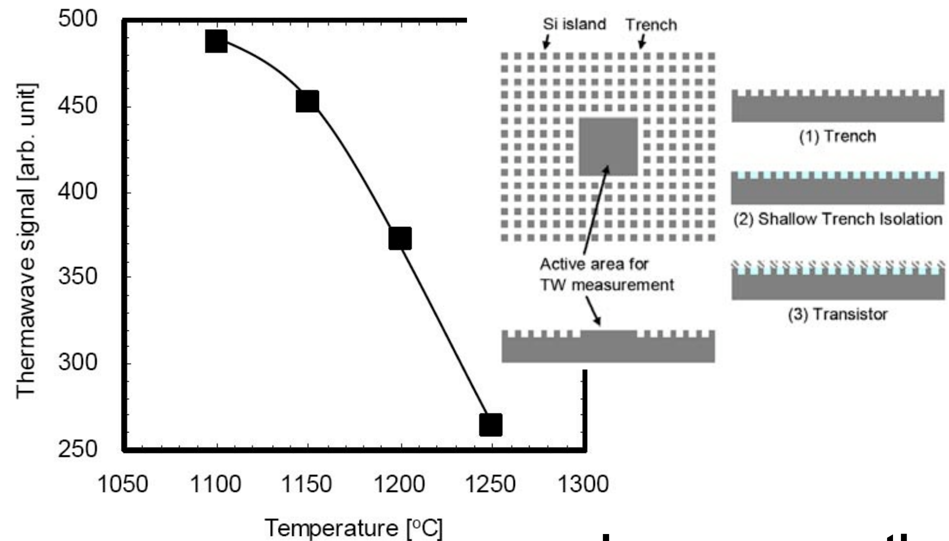
MOR/TW Tracking Laser Anneal Temperature

TW signals from 10x10 um test areas imbedded in model structure types (STI, trench, gates) show effects of patterns with ms-anneals.

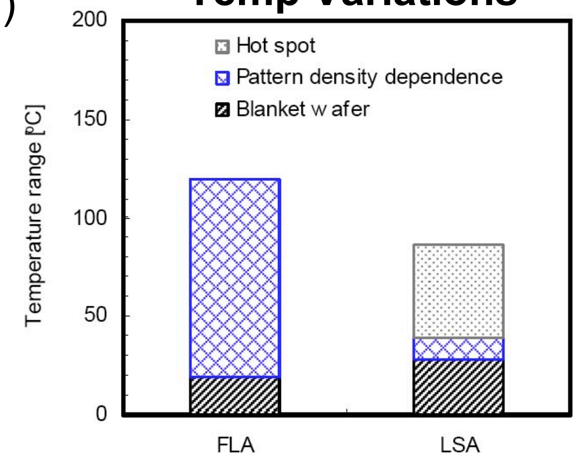
Implants "optimized" to give monotonic TW trends with peak temperature.

Many local effects recognized, including local melting ("hot spot") near large area (100x100 um) open areas with laser scans.

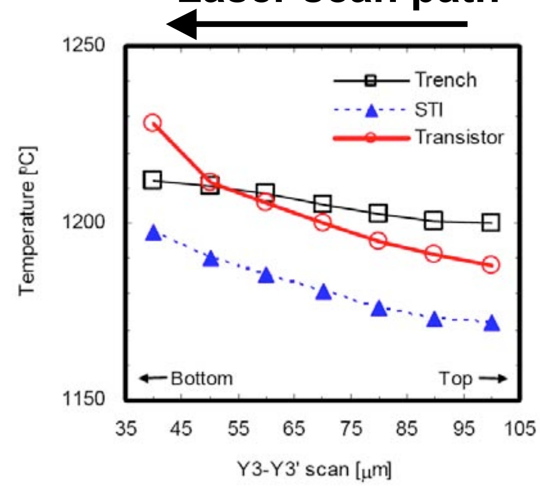
Typical temperature range for various patterns is
~ 75 to 120 C.



Temp Variations



Laser scan path



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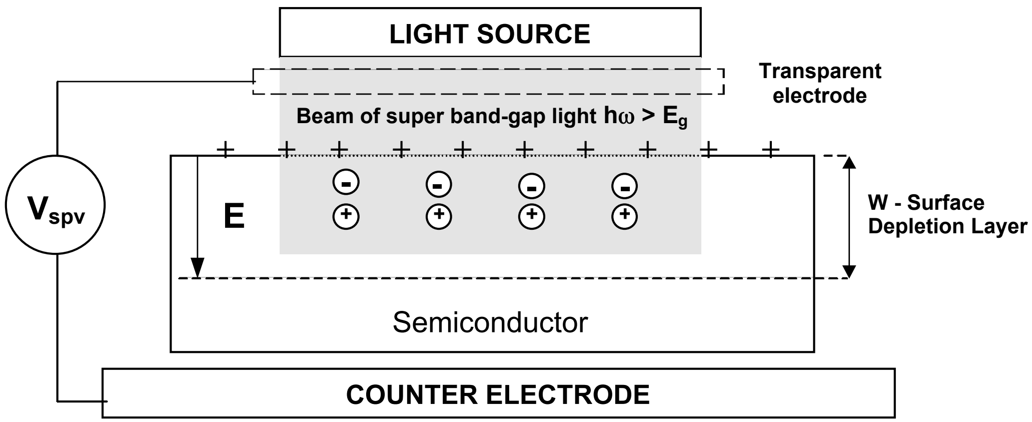
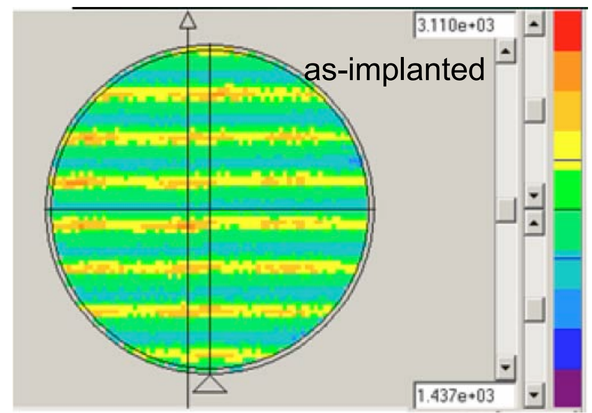
Surface Photo-Voltage: Surface Charge





Surface photo-voltage:

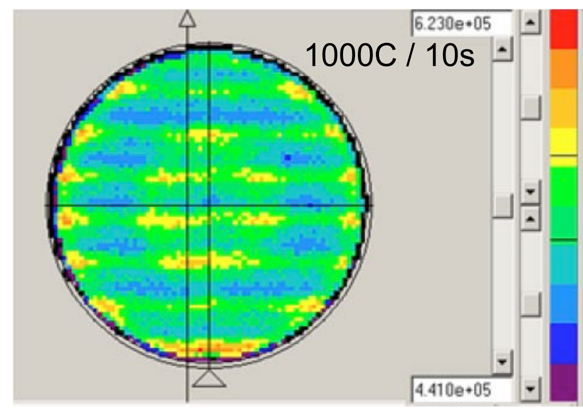
$$V_{spv}(\omega) = \frac{q\Phi W\tau_0}{\varepsilon(1+i\omega\tau)}$$

Surface charge:

$$Q_d \approx qn_i\left(\frac{q^2 n_i}{\varepsilon m\omega^2}\right)N_{eff}^2$$

$N_{eff} = \sigma^*(\Delta R)^*N_{trap}$

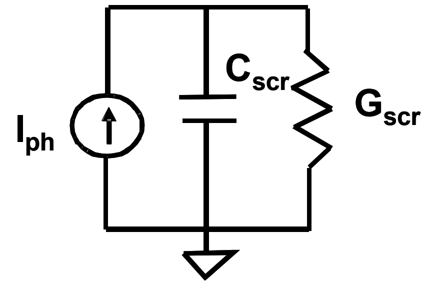
σ= capture cross-sec.
(ΔR) = damage width
N_{trap} = trap density

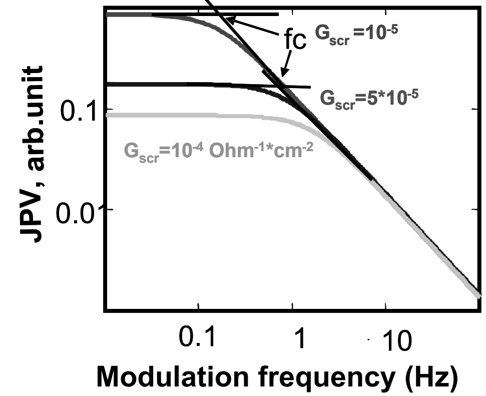


Junction Photo-voltage: Leakage (RsL)

JPV frequency response depends on:

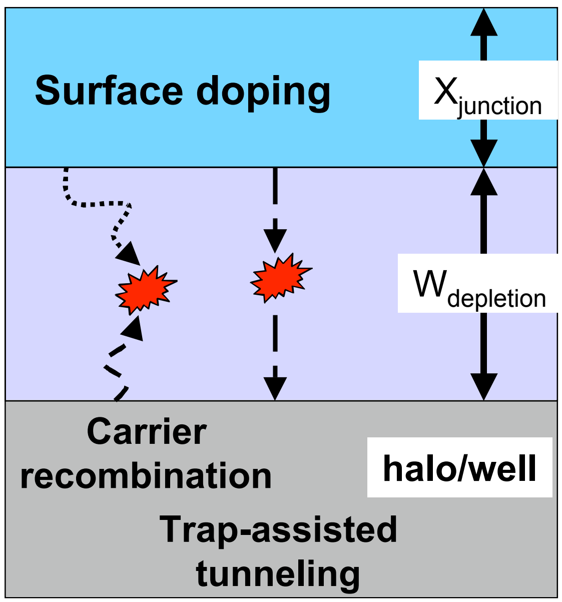
- **Halo doping (C_{SCR})**
- **Carrier recombination & tunneling**

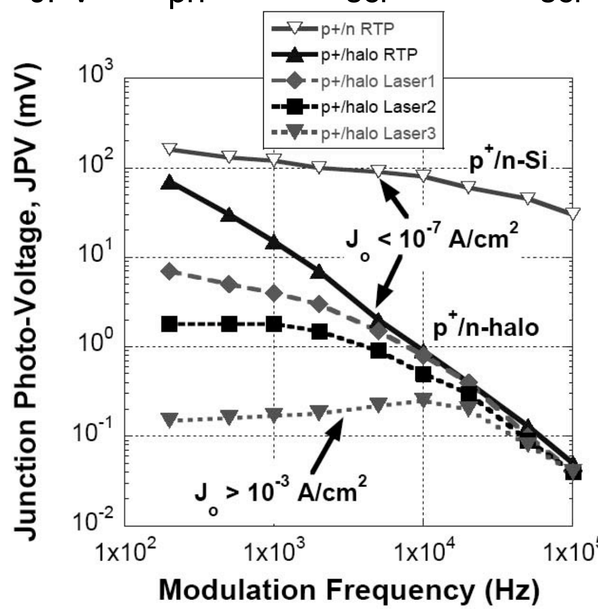




$$J_{RsL}=(kT/q)G_{scr}=I_o\ (A/cm^2)$$

$$V_{JPV} = I_{ph}*[1/(G_{scr} + i\omega C_{scr})]$$



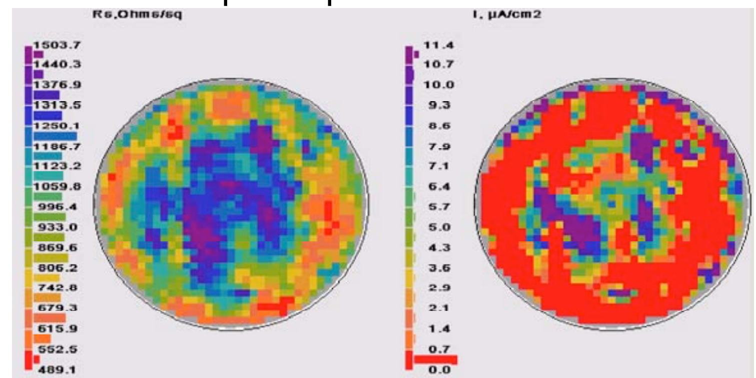


RsL: Sheet Resistance & Leakage
Laser Anneals

* Carrier spreading gives R_{sheet} & $C_{substrate}$.
* New RsL probe operates with sub-mm pixel size for R_{sheet}.

* Jo (leakage) maps often correlate to Rs maps , showing delivered power variations for ms-anneals.
* Jo maps have lower spatial resolution due to use of lower modulation frequency for leakage analysis.

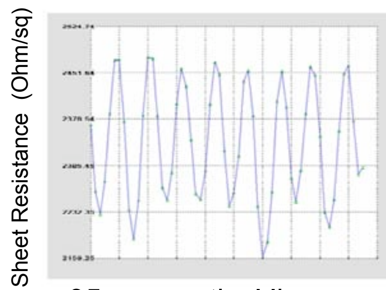
0.5 keV B, 10^{15} B/cm^2,
step-and-pulse laser anneal



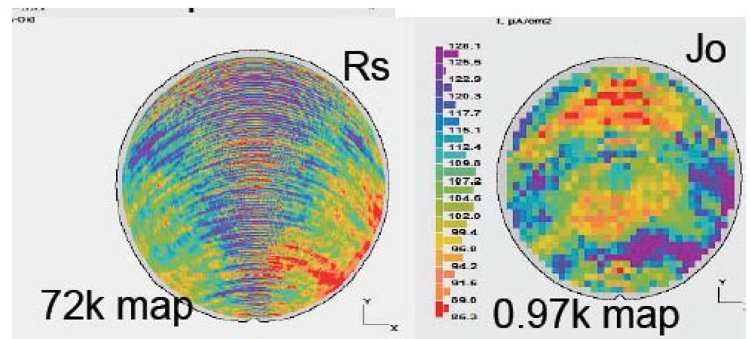
Sheet resistance
sigma = 25%

Leakage current
10^{-7} to 2×10^{-5} A/cm^2

Scanned laser



35 mm vertical line scan



Sheet resistance
sigma = 2.8%

Leakage current
8.4×10^{-5} to 1.5×10^{-4} A/cm^2

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Machine Effects: Laser Scans

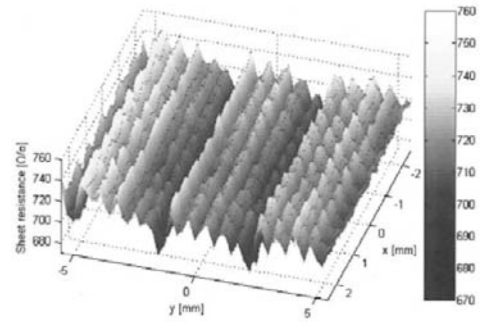
Annealing variations show up as non-uniformities in dopant activation (R_{sheet}) and carrier recombination (MOR, leakage with RsL).

Laser scanning shows effects of:

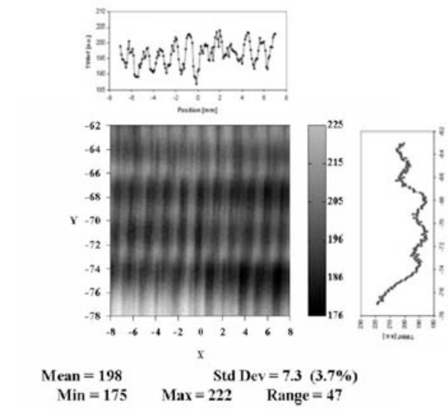
* Laser path overlaps (stitching)
* Optical interference ("ripples").

Local mapping enables rapid prototyping measurements and process calibrations.

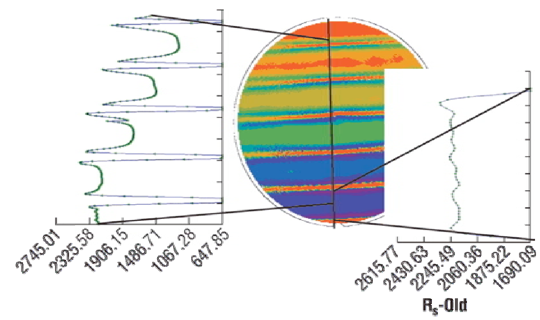
U-4PP



MOR



RsL



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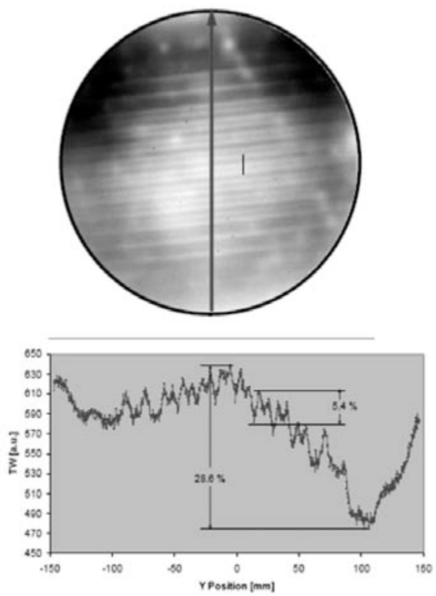
Machine Effects: Flash Lamps

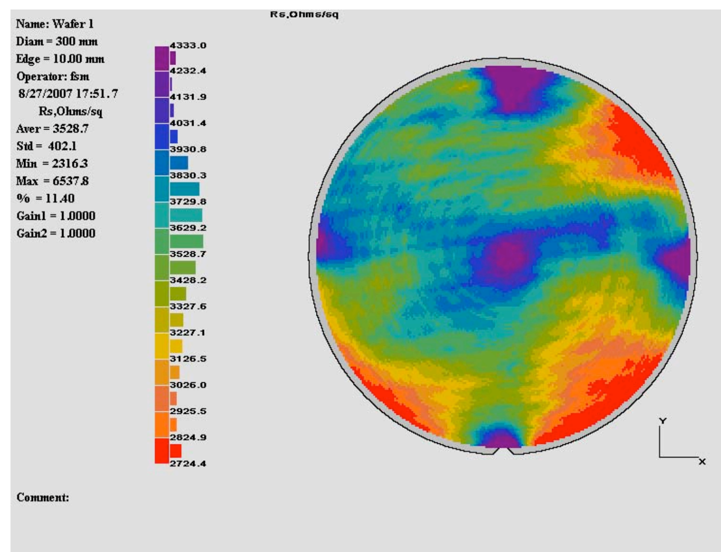
Incident power variations from multi-lamp arrays
in ms-pulses give variations in:

 * dopant activation: Rsheet (~11 % overall)
 * local recombination rates: MOR (~29 % overall, ~5 % local)

MOR (TW) map



Sheet Resistance (RsL) map

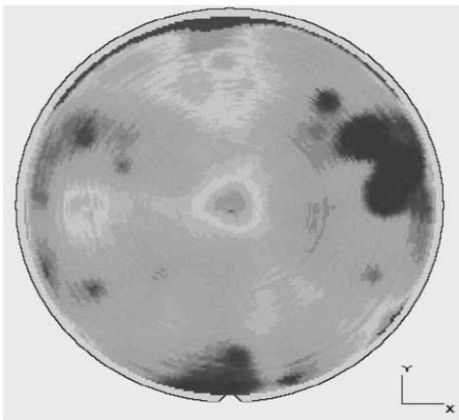


Machine Effects: Support pins

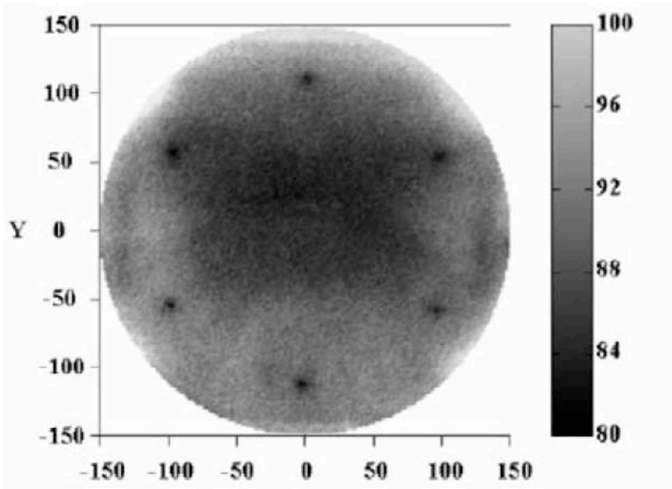
Wafer support pins in ms-flash annealers result in local temperature variations (some hotter, some cooler) which are visible in both activation (R_{sheet}) and recombination effects.

PL map

R_{sheet} (RsL) map



MOR (TW) map

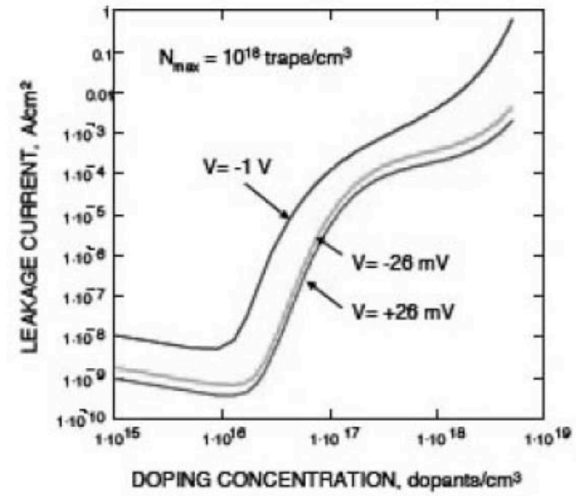


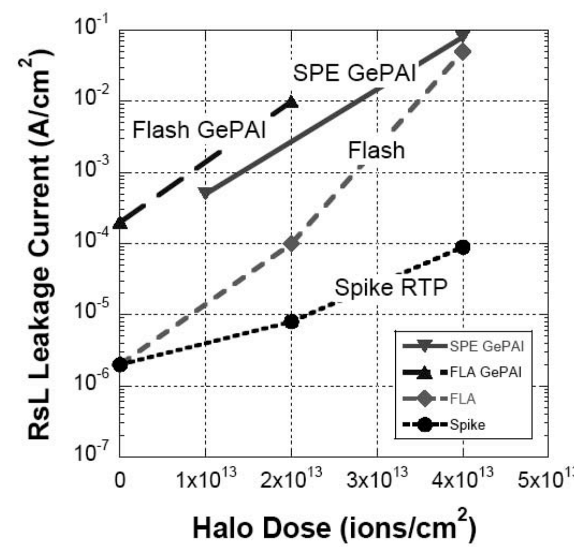
Process Effects: Halo damage & doping

Halo doping and damage levels are major factors in junction leakage.

Increased halo implant dose:
* Decreases junction depletion layer thickness (*Increases leakage current* through shorter carrier diffusion paths before recombination and higher tunneling rates).
* Increases EOR damage levels (*Increases leakage* by adding more SCR defects).
* *Increases band-to-band tunneling leakage*.

Effects strongly influenced by process conditions:
* PAI & SDE ion, dose & energy, beam current & wafer temperature.
* Halo implant beam current, scan rate & wafer temperature, halo-specific anneals.
* Annealing conditions.





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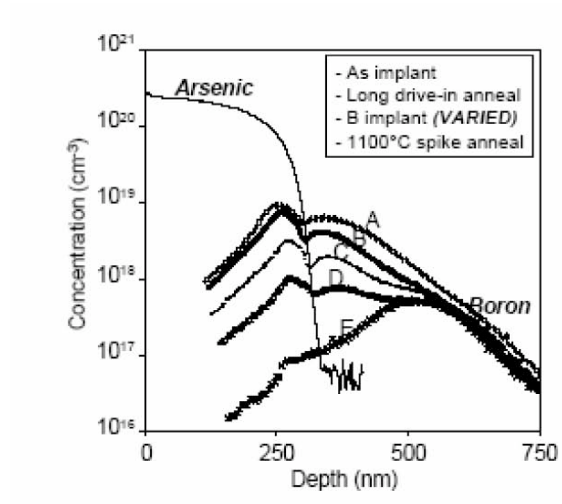
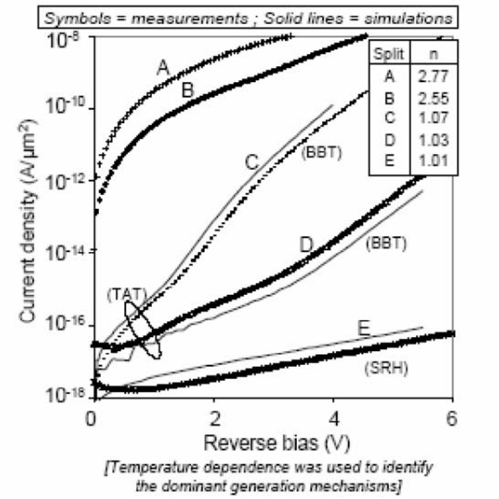
Leakage Current: Substrate ("Halo") Doping

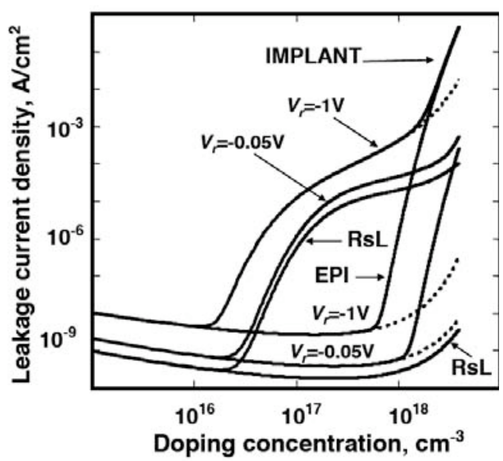
Halo doping controls short channel effects:
* V_{th} roll-off
* Reduces SDE Xj
* Lateral punchthru

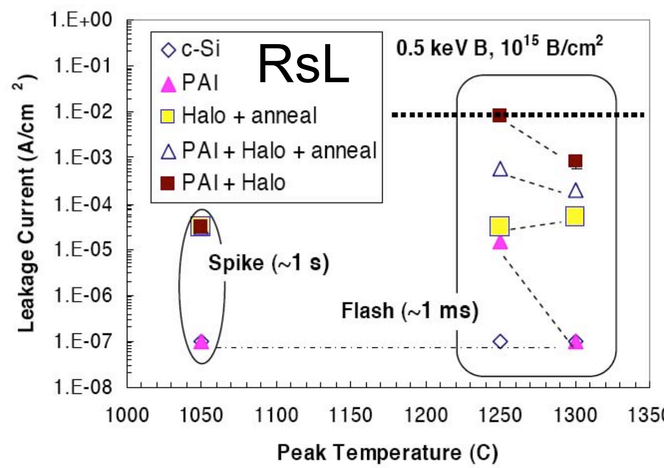




BUT!! halo doping also:

* Reduces depletion layer thickness
* Increases leakage current from SRH, TAT & BTBT.





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R. Duffy/PHX 06, M. Current/FSM 07

Guidelines for low leakage process

1. **Adjust relative location of damage and Xj.**
   Drive diffusion of Xj beyond damage.
   "Diffusion-less" is not always the best choice.

2. **Minimize halo dose and damage (if possible).**
   Halo-specific anneals (if possible).

3. **Create full-depth amorp layers (damage accumulation)**
   High beam currents, Controlled scan rates, Molecular ions,
   Lower wafer temperature.

4. **Measure everything…all the time**; MOR, RsL, etc.

Leakage Current: Damage Location

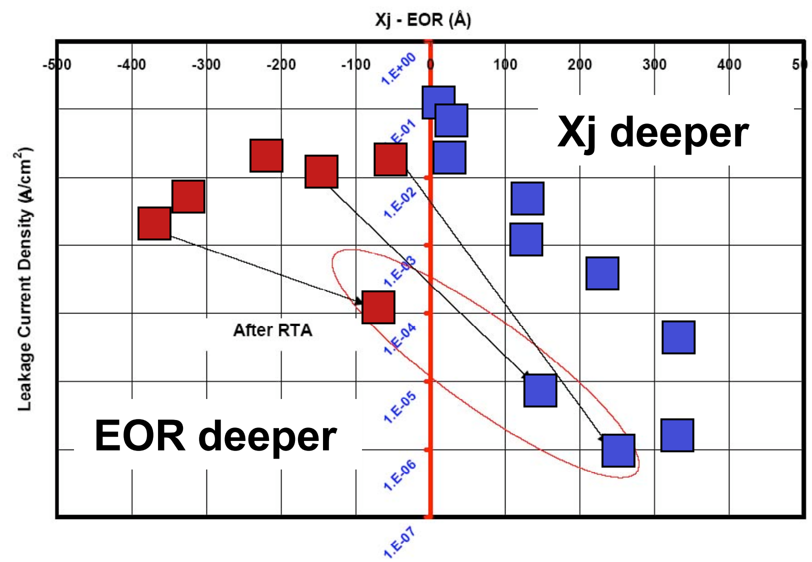
SHR & TAT depend on “traps” (defects) in the junction depletion zone.

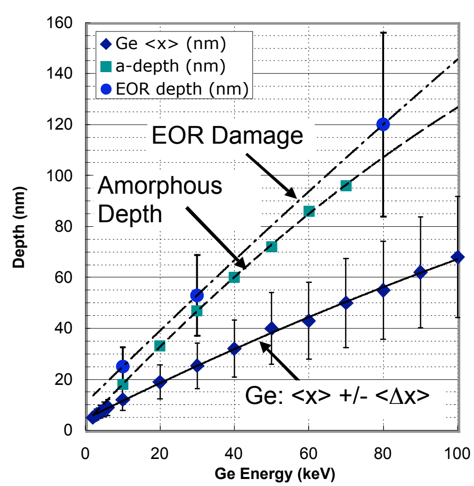
Magnitude of leakage depends on trap “strength” (shape, strain field, chemistry).

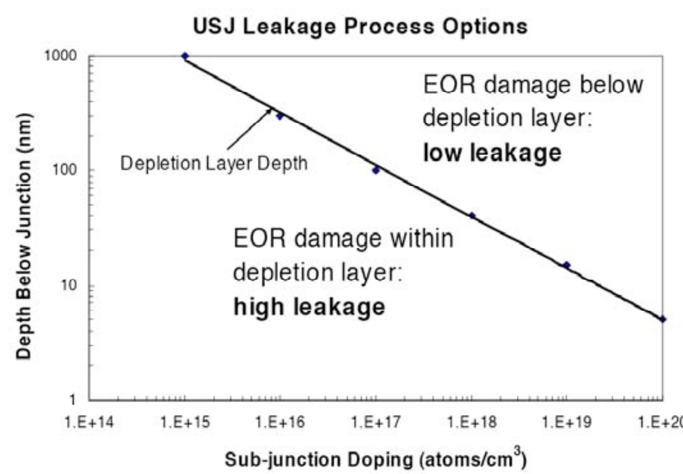
End-of-range (EOR damage) determined by implant ion & energy.

Xj location depends on diffusion.

Keep defects out of the depletion layer.







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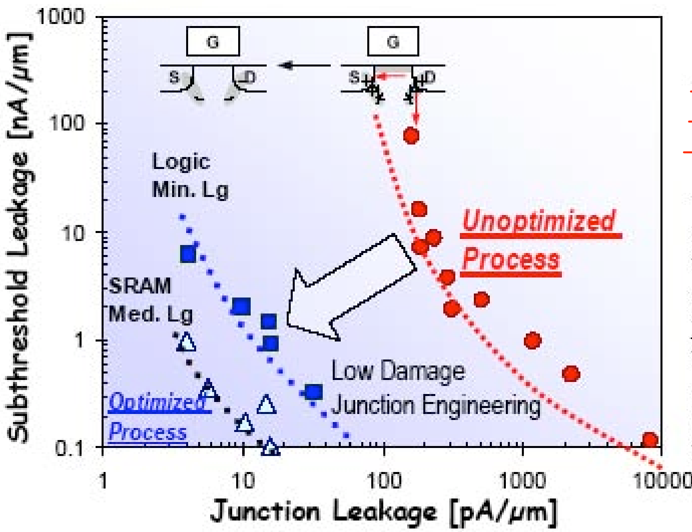
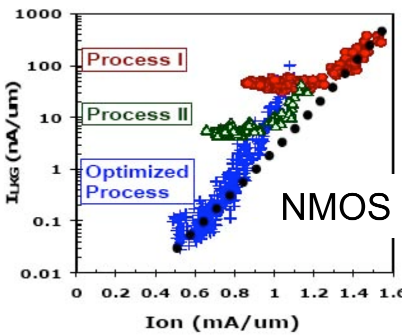
S. Felch/Varian 02, M. Current/FSM 07

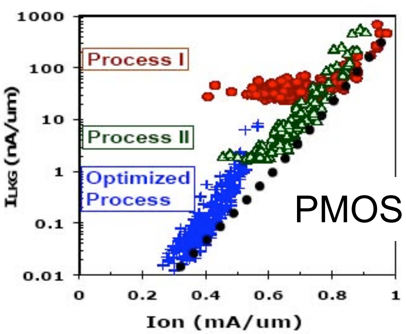
Leakage Optimization: Intel IEDM05



There are 2 main sources of junction leakage for sub-100nm CMOS transistors: trap-assisted leakage due to damage from the high dose source/drain extension implants and band-to-band tunneling leakage due to the very steep and highly doped source/drain extension-well junctions that are required for low R_{EXT} and good control of short channel effects. Reduction of implantation damage can be achieved by optimization of dopant species and implant conditions, such that any residual implantation damage is fully contained inside the source/drain diffusions and thus kept away from the junction depletion regions. By grading the source/drain extension and well junctions the band-to-band tunneling leakage can be reduced, but at the expense of higher R_{EXT}. This loss in transistor performance can, however, be mitigated by the performance benefits of strained silicon.



Intel 65 nm process solution:
Diffuse dopants so that....
Damage is shallower than Xj.



A 65nm Ultra Low Power Logic Platform Technology using Uni-axial Strained Silicon Transistors

C.-H. Jan, P. Bai, J. Choi, G. Curello, S. Jacobs, J. Jeong, K. Johnson, D. Jones, S. Klopcic, J. Lin, N. Lindert, A. Lio, S. Natarajan, J. Neirynck, P. Packan, J. Park, I. Post, M. Patel, S. Ramey, P. Reese, L. Rockford, A. Roskowski, G. Sacks, B. Turkot, Y. Wang, L. Wei, J. Yip, I. Young, K. Zhang, Y. Zhang, M. Bohr and B. Holt

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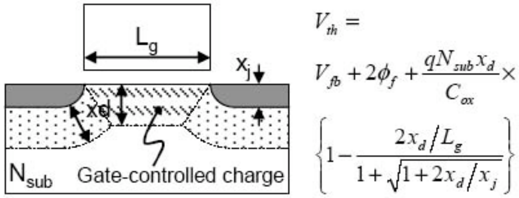
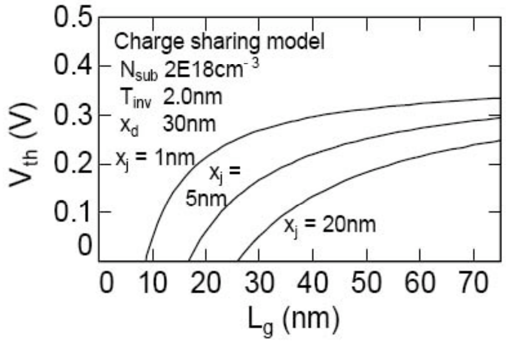
Junction Shape Tuning

For SDE Xj = 5nm, Vth roll-off can be controlled for L_{gate} = 20 nm.



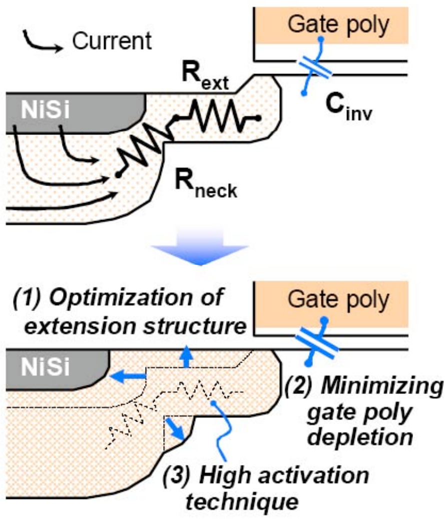


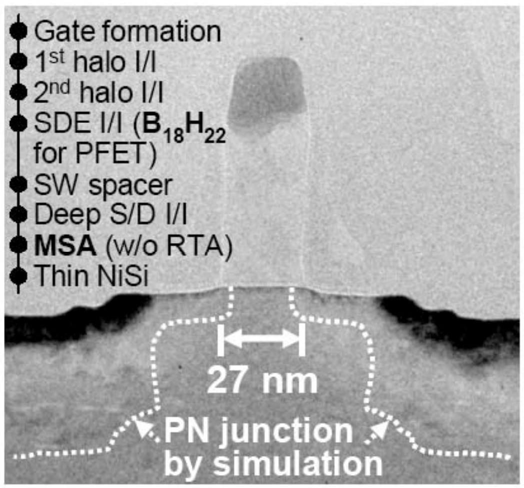
BUT!!!! Shallow SDE X_J is not good enough.
Need also:

* Low SD series resistance (no thin paths).
* Proper SDE/gate overlap.
* No SDC current crowding or leakage.

Use process & layout tricks:

* B_{18}^+ & ms-anneal (shallow Xj, high activation).
* Reduce SDE etching step.
* Extra high-tilt SDE doping.
* High poly-gate activation.
* Shifted metal contact.





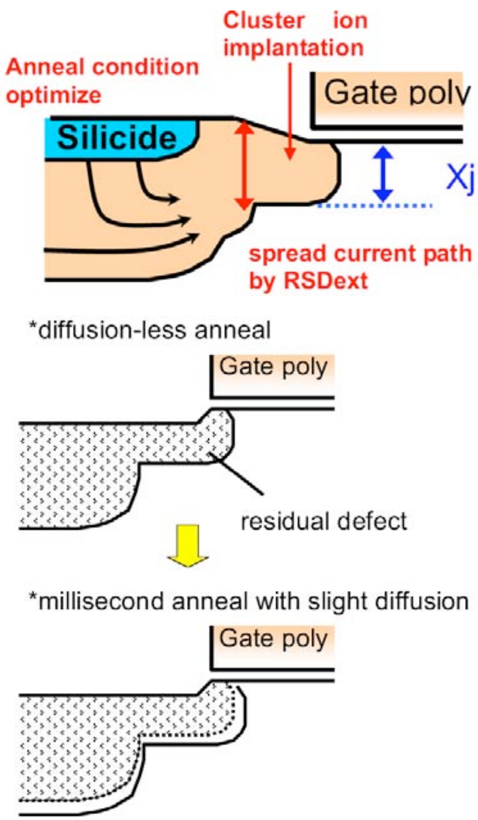
Current Scientific

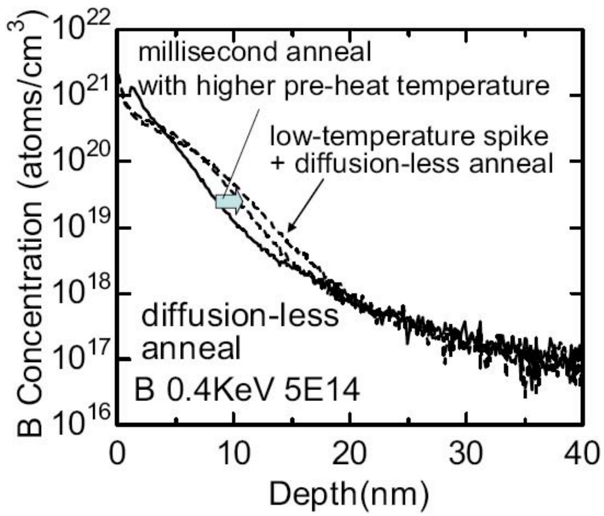
Uejima/NEC 07

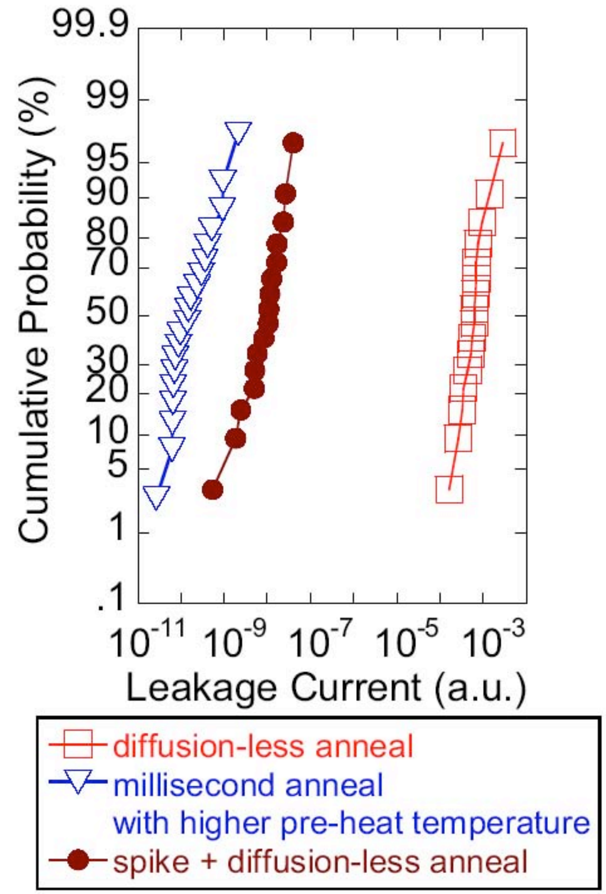
Defect/Junction Adjustments: ms-Anneals

Allow for "some" diffusion to drive Xj deeper than EOR damage.

Minimize EOR damage with B_{18} doping.



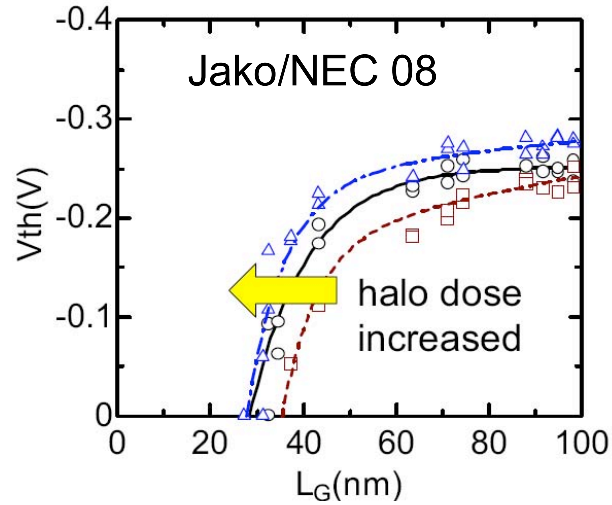




Current Scientific

Yako/NEC RTP08

Halo Dose Choices

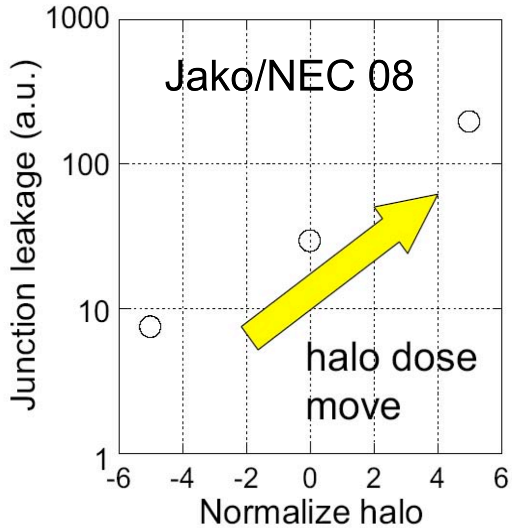


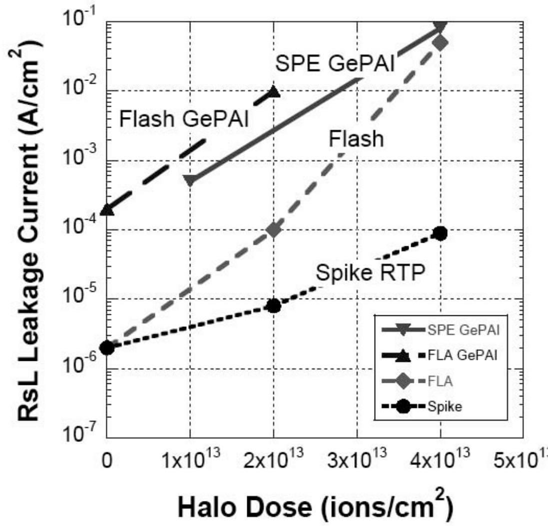
Halo doping is good:

Less Vth roll-off (SCE).

Halo doping is bad:

Higher leakage current.





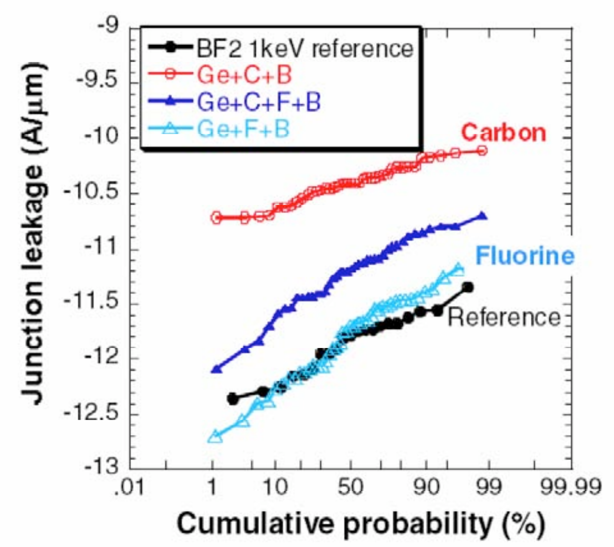
Upshot: Minimize halo dose and damage (use B_{10} or B_{18}).

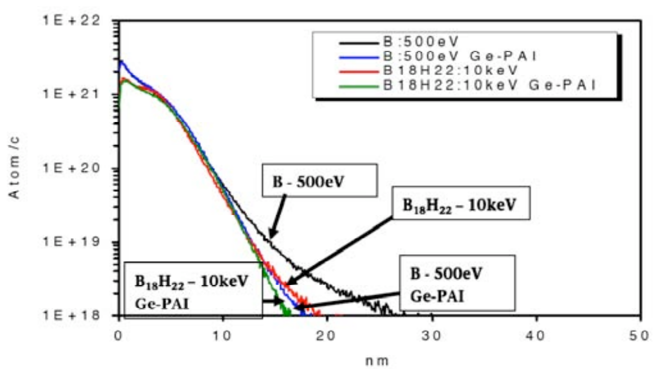
Leakage Current: Implant Ions

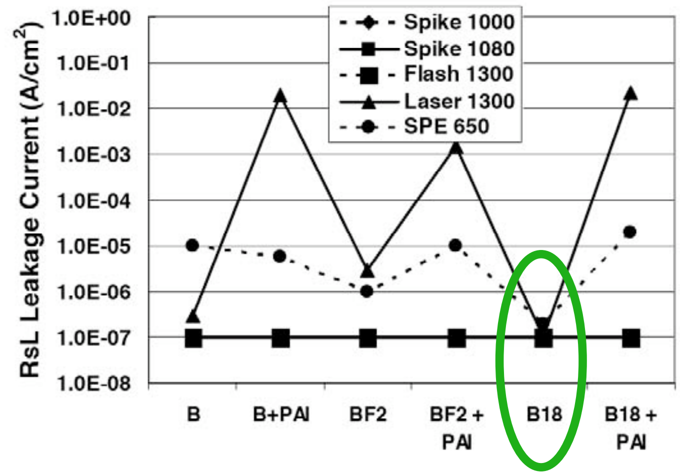
Specifics matter:
* Cocktail atoms at Xj (high leakage).
* C-defects have higher leakage than F.
* PAI leaves deep defects (high leakage).

Diffusion-less anneals (laser, flash, SPE) have higher risk of leakage than RTA/spike.

Molecular ions (B_{10}, B_{18}), with no PAI, give low process-related leakage (shallow damage).







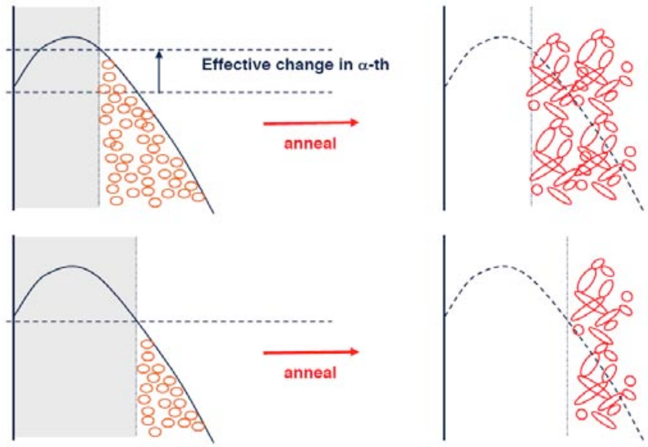
Current Scientific

B. Pawlak 06, Borland 06

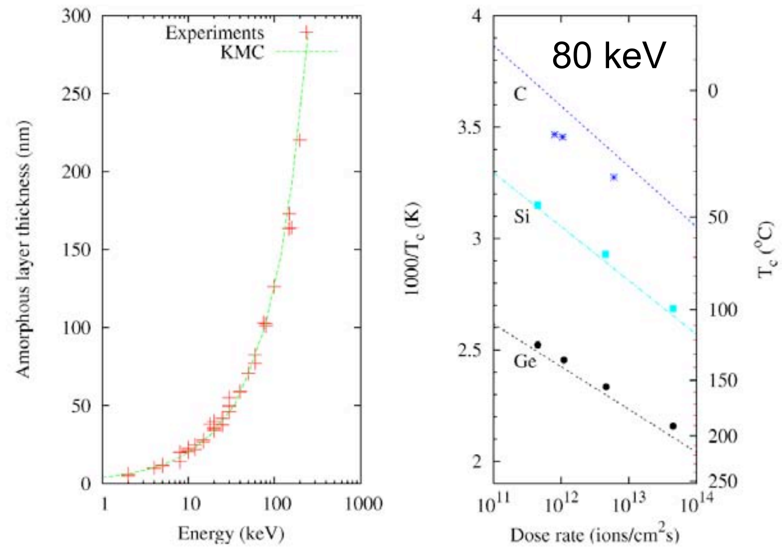
A Case for Cryo-implants for Low Leakage

Low damage accumulation
Low ion mass, low current
High temperature
Shallow a/c, rough a/c interface
Dense EOR damage, high leakage

High damage accumulation
High ion mass, high current
Low temperature
Deep a/c, smooth a/sc interface
Sparse EOR damage, low leakage



Good match: Data to KMC models



Implant conditions:

Ion (Ge+B, BF_2, B_{10}, B_{18}, GCIB, P_2, etc.)

Beam current, beam size, scan rate, etc.

Wafer temperature

Anneal conditions:

Peak temperature, time at peak

Base temp, ramp rate to/from peak, etc.

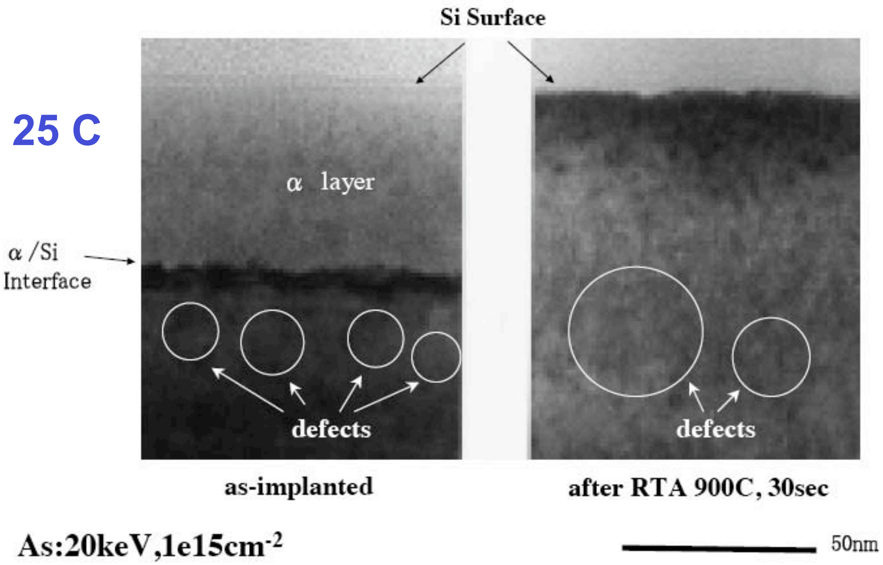
Current Scientific

Harris/ACLS IIT08, Zographos/Synopsys 08

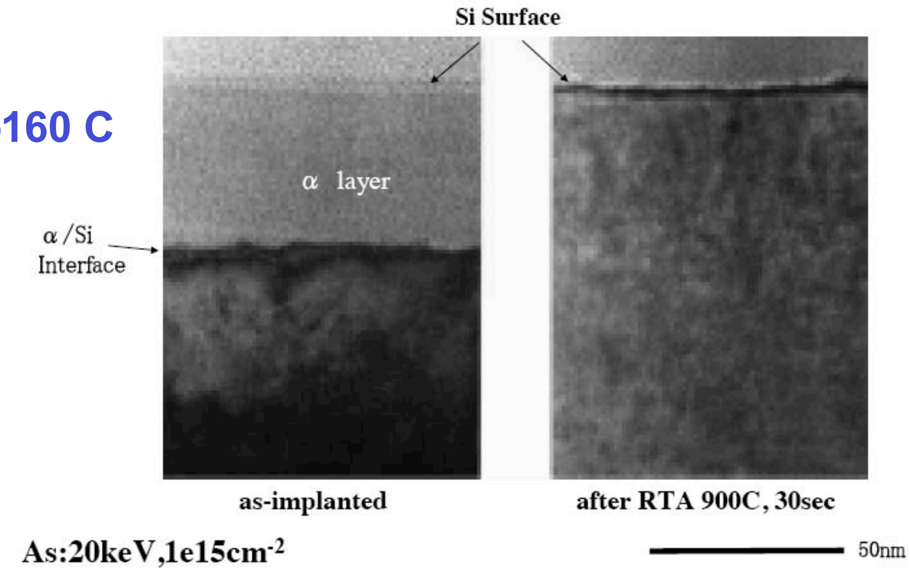
Cryo-implants: Damage & leakage

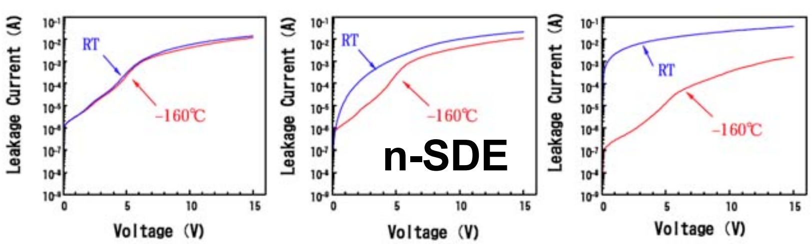
Heavy-ion (As^+) defect level and leakage much improved by cryo-implant.
Cryo-implant gives more planar a/c interface (better crystal regrowth plane).
Less effect for 10 keV B^+ implants.

25 C

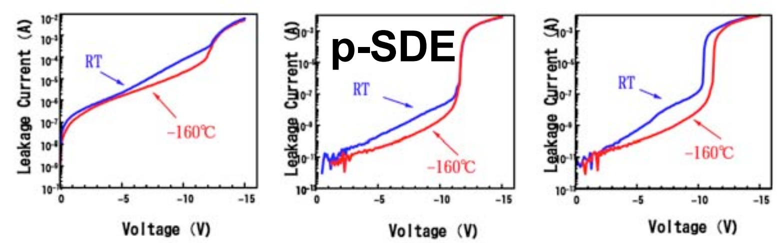


-160 C





(a) As dose:1E13cm-2 (b) As dose:1E14cm-2 (c) As dose:1E15cm-2



(a) B dose:1E13cm-2 (b) B dose:1E14cm-2 (c) B dose:1E15cm-2

Current Scientific

Suguro/Toshiba 02

A/C Depth: Beam Current & Scan Rates

SIMS "markers" (B & F peaks at EOR damage) show effects of:

*** Beam current**

*** Scan rate (batch vs serial)**

α-thickness

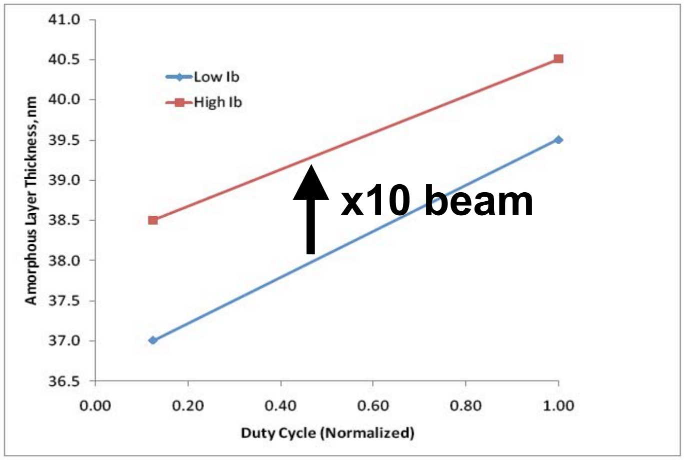


Figure 3. Amorphous layer formation as measured by TEM. The implant was a 20 keV BF_2, 2E15 ions/cm^2 on a single-wafer spot beam system. High I_b is 10X low I_b in this case.

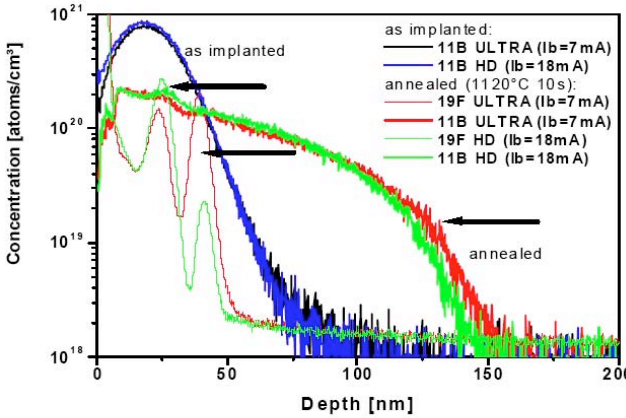


Fig. 1. SIMS profile of B and F for 20keV BF_2 3E15cm^{-2} on Optima HD (HD) and ULTRA as implanted (B only) and after anneal.

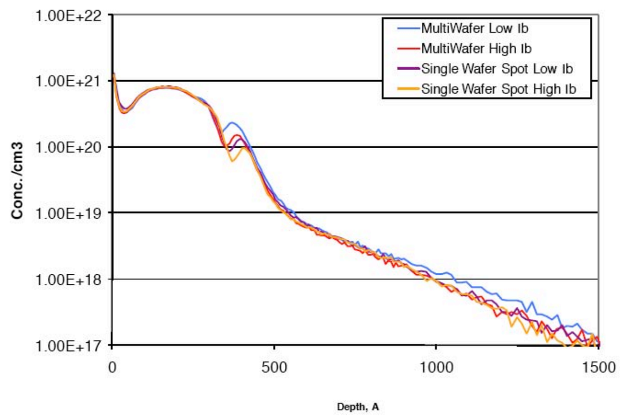
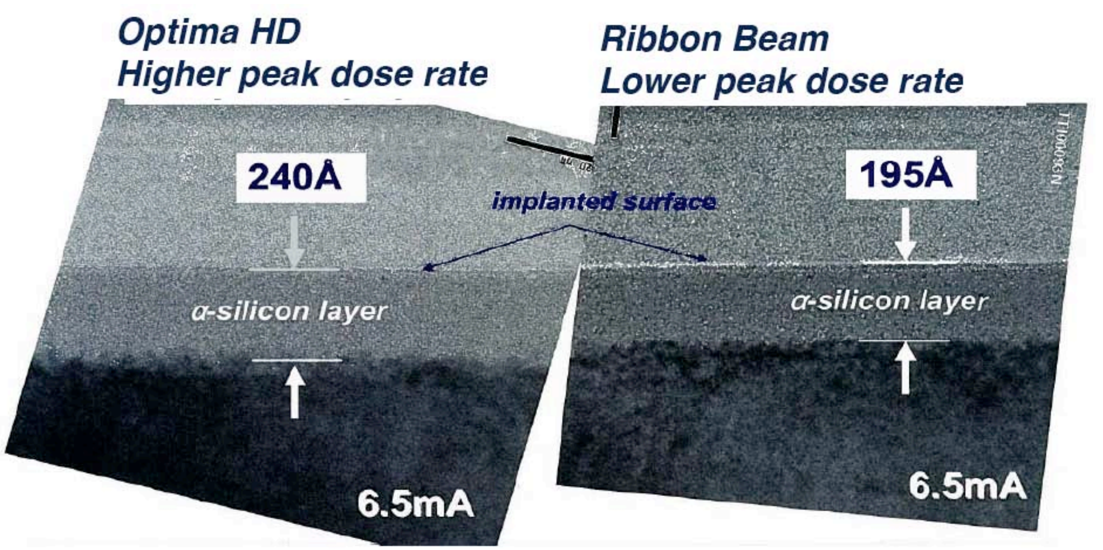


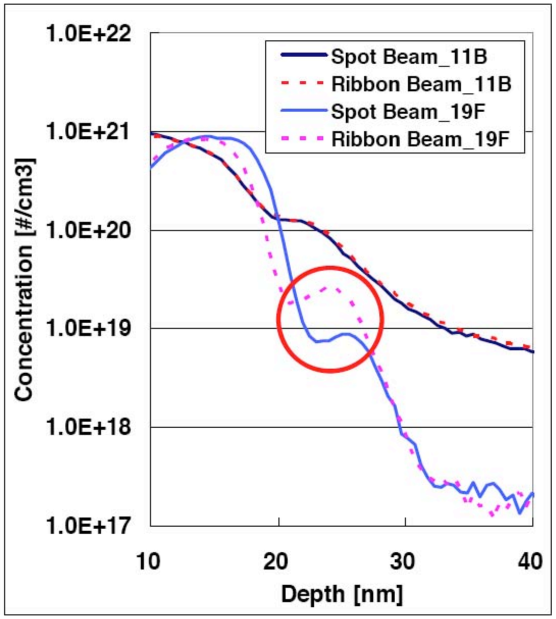
Figure 4. Post-anneal comparison of Boron accumulation in the EOR damaged region of a BF_2 high-dose implant for a stationary (spot) beam on multi-wafer and single-wafer platforms.

Scan rates & Peak Currents: Spot vs Ribbon

* Peak current and scan rate differences give different device results for batch & serial (spot and ribbon beams) implanters.
* F peak (from BF_2) marker can track EOR damage and density.
* Vary beam current, scan rate and wafer temp. to match machine results.
* Could also use carrier recombination metrologies for faster-turn tuning.

10 keV BF_2,





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B_{18} vs Ge PAI+B: Dopant profiles & Damage

- Molecular ions make more planar a/c interface than B^+.
- B_{18} channeling much less than B^+ (close to PAI + B).
- B_{18} shows no residual damage in TEM for "diffusion-less" anneals.

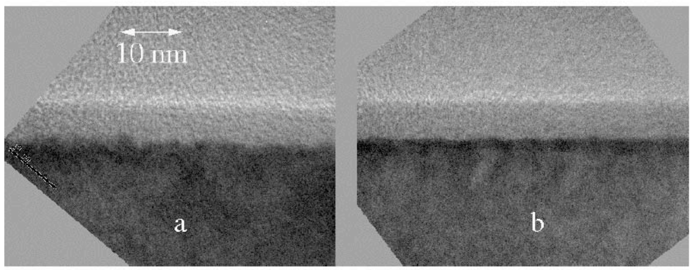
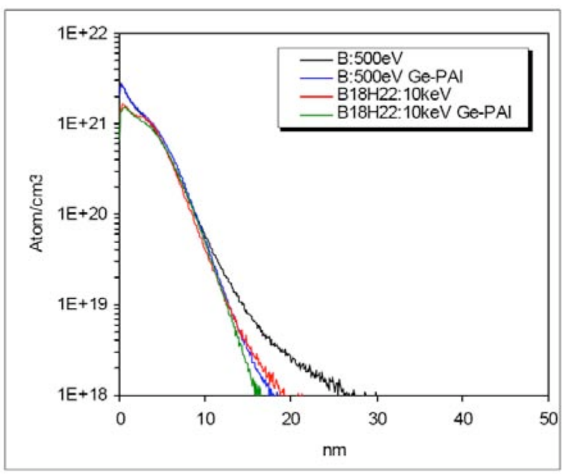
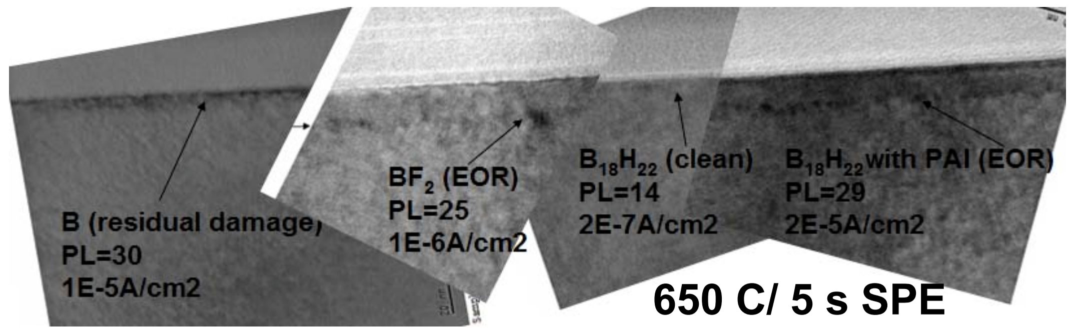
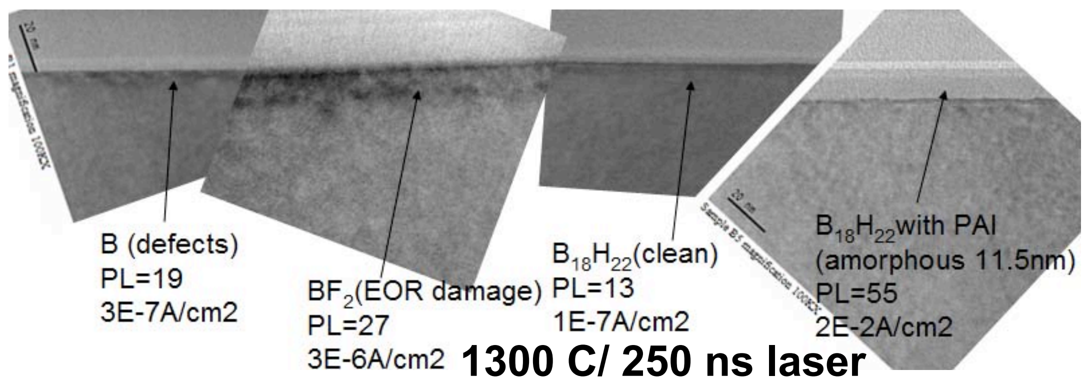


Fig. 1: X-TEM comparison for a) B_{11} to b) $B_{18}H_{22}$ with 6.2nm of self-amorphization.

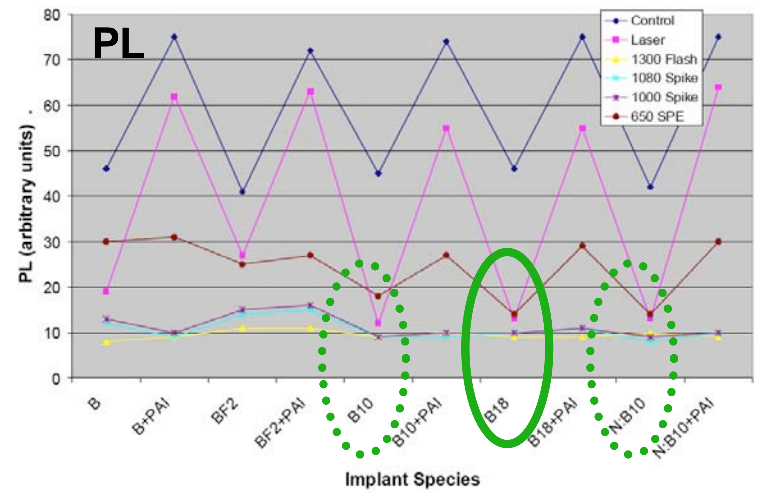


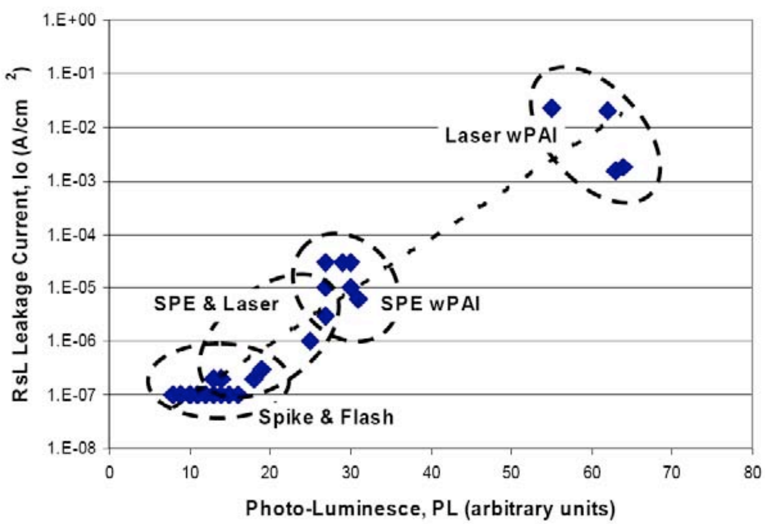


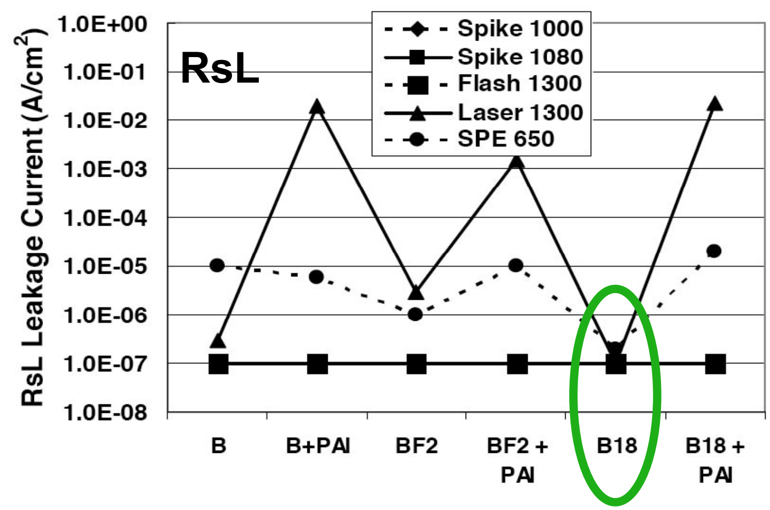


B_{18} vs Ge PAI+B: Recombination rates

- Carrier recombination probes (PL, RsL, MOR) show low leakage for B_{18} (and B_{10}) for SPE and laser anneals .
- Low leakage device results also seen for B_{18}.
- B_{18} damage accumulation still to be understood in detail.







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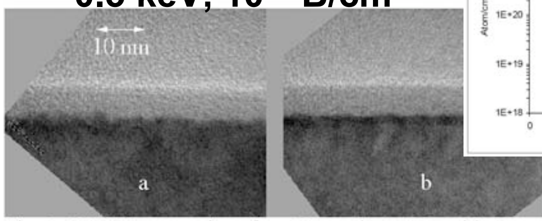
Cryo-B_{18} Implants:
How low can junction leakage go?

1. 0.5 keV, 10^{15} B/cm^2



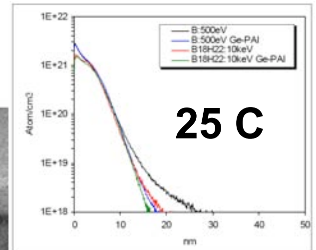


Fig. 1: X-TEM comparison for a) B_{11} to b) $B_{18}H_{22}$ with 6.2nm of self-amorphization.

What do these look like for <0 C implants?

Thicker, more planar a-layer?

Less B channeling for B_{18}?

2. What are the dopant activation levels, Xj and leakage after anneal of cryo-B_{18}-doping?

Then:

Next step: CGIB = *no* damage at all = no SRH +TAT leakage

Still need to deal with BTBT for SDE/halo CMOS.

Carrier Recombination, Leakage Current and all that…..

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Junction Leakage Current Mechanisms: Defects & Doping

Carrier Recombination-based Metrologies

- **Photoluminescence, MOR (TW)**
- **Surface charge, JPV leakage (RsL)**

Machine and Process Effects

- **ms-Anneals, Support pins, Halo damage & doping**

Guidelines for low-leakage process

- **Scan rates, Beam current, Molecular ions, Cryo-implants**

But, getting ideas is the easy part.....

"*Getting the ideas is easy . . . the hard part is hitting one key at a time.*"

currentsci@aol.com

Current Scientific

Ion Implantation Process Engineering:

a practical textbook by M.I. Current

Preface: book scope, level, plan, commercial history of ion implant tool sales 1970 to 2007.

1. IC transistor doping basics:

Implant profile characteristics: depth, dose, profile shape, stopping (SRIM, TRIM-BASIC).
Damage accumulation, sputtering, sputter-limited dose, channeling
Masking basics: PR "economics", thickness, outgassing & carbonization, mask-edge effects
Principal doped regions for Bipolar-CMOS transistors
Roadmap trends for gate size, junction depth, channel doping, transistor speed, leakage
ULSI issues: channel doping and gate length fluctuations, poly-gate depletion,
"Ultimate" CMOS devices: FD-SOI, FinFET doping.

2. Ion implantation technology:

Evolution of basic system architecture
Ion sources (Freeman, Bernas, Button, RF/micro-wave)
Mass analysis, bend angles, resolution, source noise effects
Beam transport: emittance, perveance
Accelerator column design, beam scanning, decelerator electrodes
Wafer scanning geometries, beam incidence angle variations
Scanned area fraction vs beam size for x-y scan, spinning wheel, pendulum, ribbon beams
Faraday designs, single and multiple loop, noise & sampling ranges
Charge control systems: electron, ion & plasma flows
Throughput calculations; beam current, scanned area, wafer loading, beam tuning
Plasma immersion: sources, throughput, energy control, non-planar targets

3. Annealing:

Annealing effects: Damage annealing, electrical activation, diffusion
Furnace operations: push/pull, ambients, wafer strain effects/slip
RTP operations: temperature profiles, lamp pattern effects
ms-anneals: radiant energy coupling, surface temperature transients, stress/slip, laser scanning

4. Process characterization techniques
5. Dosimetry
6. Ultra-pure processing
7. Channeling
8. Charging
9. Damage accumulation and annealing
10. Operational efficiencies
11. Safety and environmental issues
12. Advanced topics: PIII, SOI, etc.

CD-ROM materials (options)

1. Safety: toxic, electrical, radiation, mechanical hazards
2. Ion source materials: ionization characteristics, etc.
3. Ion profile codes: guide to TRIM, TRIM-Dyn, SRIM, PRAL, UT-MARLOWE,
4. Short-course foils for major topics
5. Full-text and figures in pdf; text searchable.

Draft edition due mid-2009.

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