Predictable Success

Modeling Evolution of Temperature, Stress, Defects, and Dopant Activation in Silicon During Spike and Millisecond Annealing for 32 nm node

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Synopsys, Mountain View, California

Semicon West 2008, San Francisco

Outline

- Millisecond annealing
  - Optical effects
  - Heat transfer
  - Stress induced by thermal gradients
  - Stability of source/drain resistance
  - Defect annealing for S/D and halo implants

- Layout-induced V_T and L_{eff} variations
  - Threshold and L_{eff} shifts are driven by TED
  - Non-trivial shape of diffusion mask
  - Compact model for fast analysis

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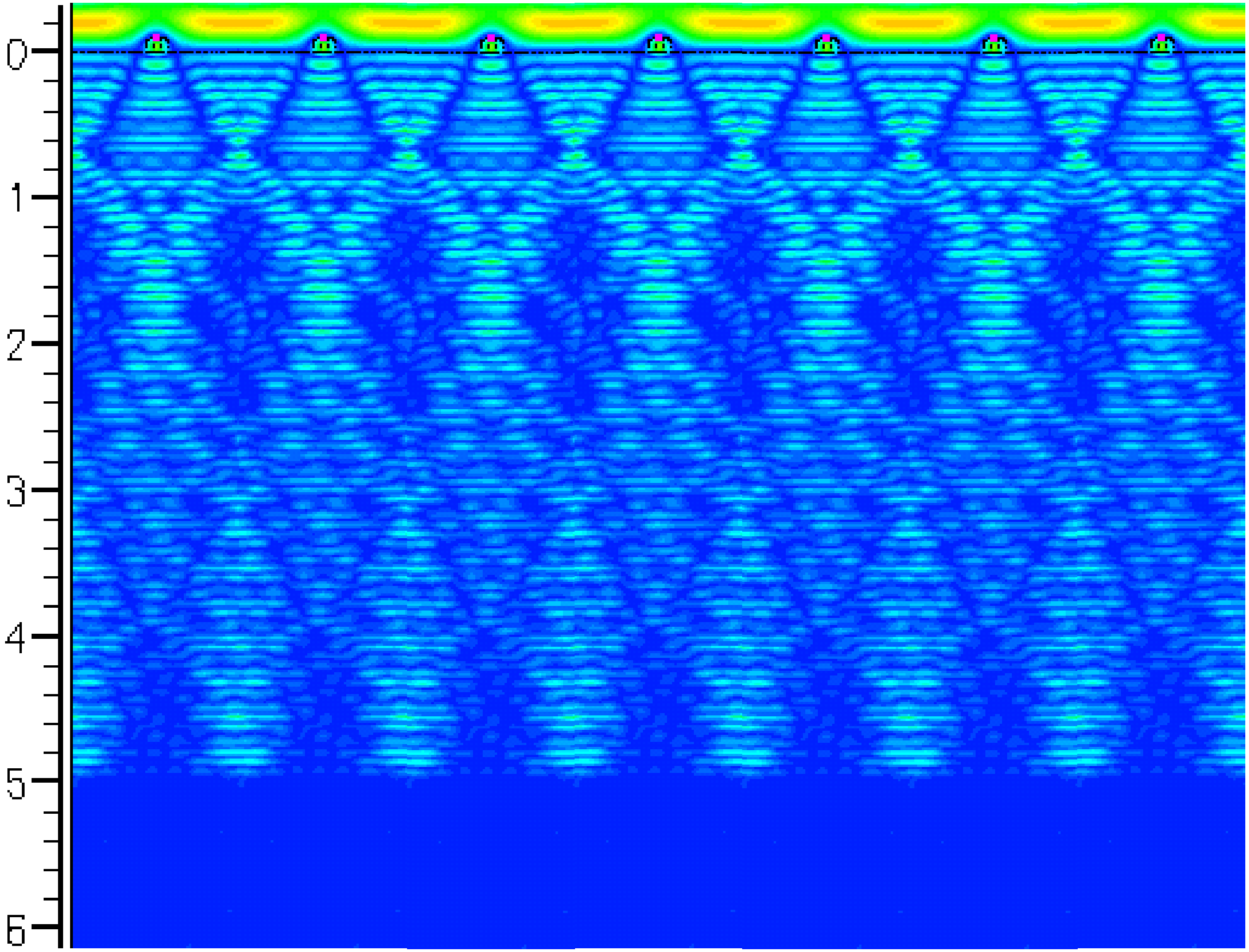
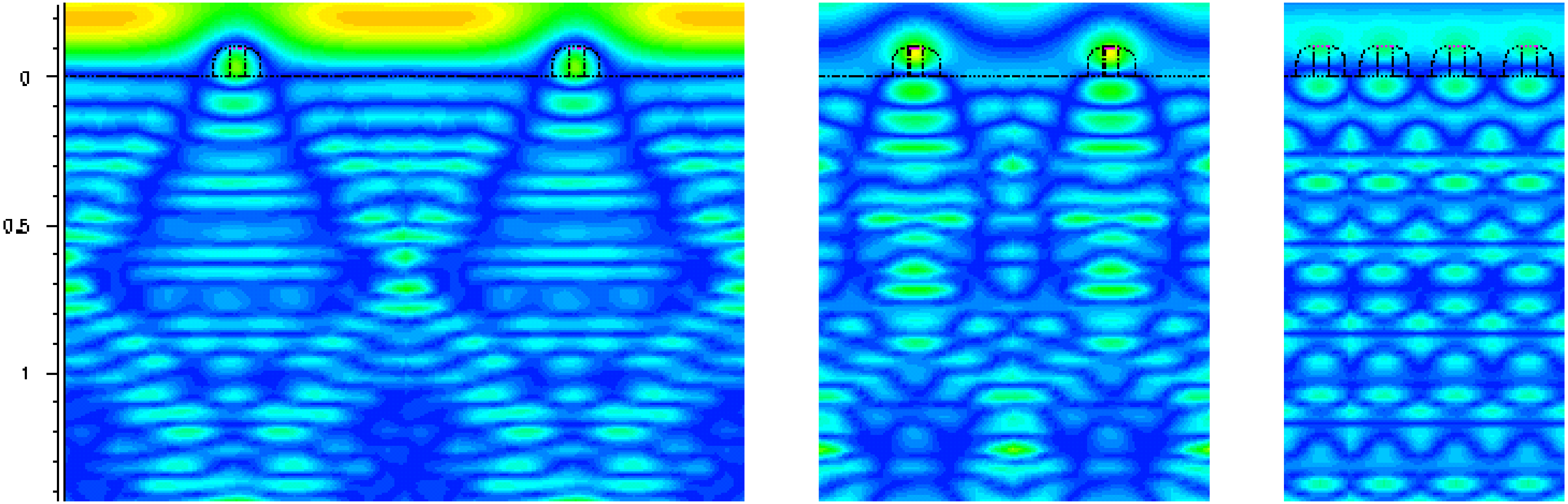
Optical Generation Pattern @L=32nm



Sub-wavelength features create light patterns in Si wafers with 32nm transistors

Optical Generation vs Poly Pitch @32nm



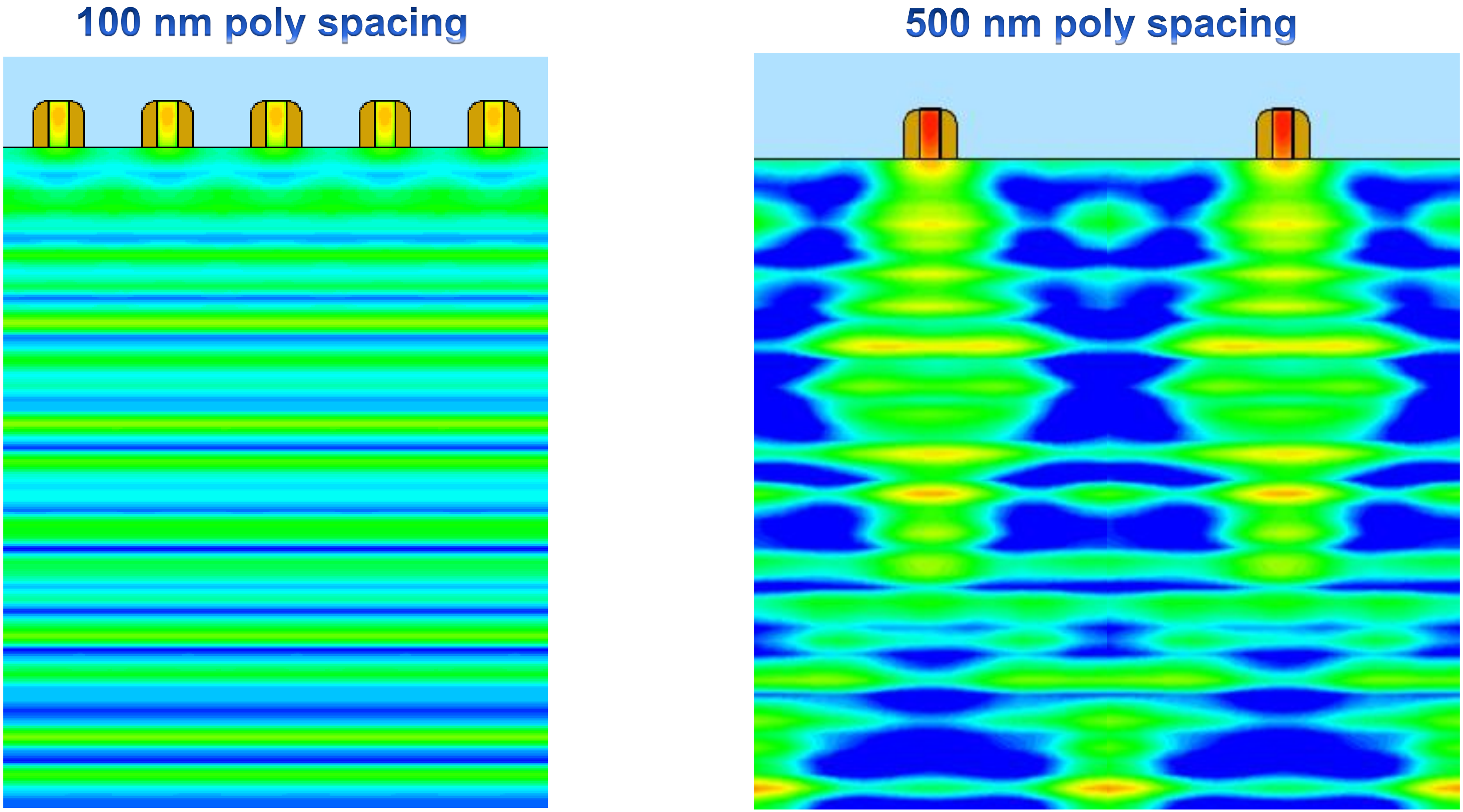
1 µm poly spacing

500 nm poly spacing

100 nm

Poly gates act as lenses, with the light pattern determined by transistor placement

Time Averaged Heat Generation @32nm


100 nm poly spacing

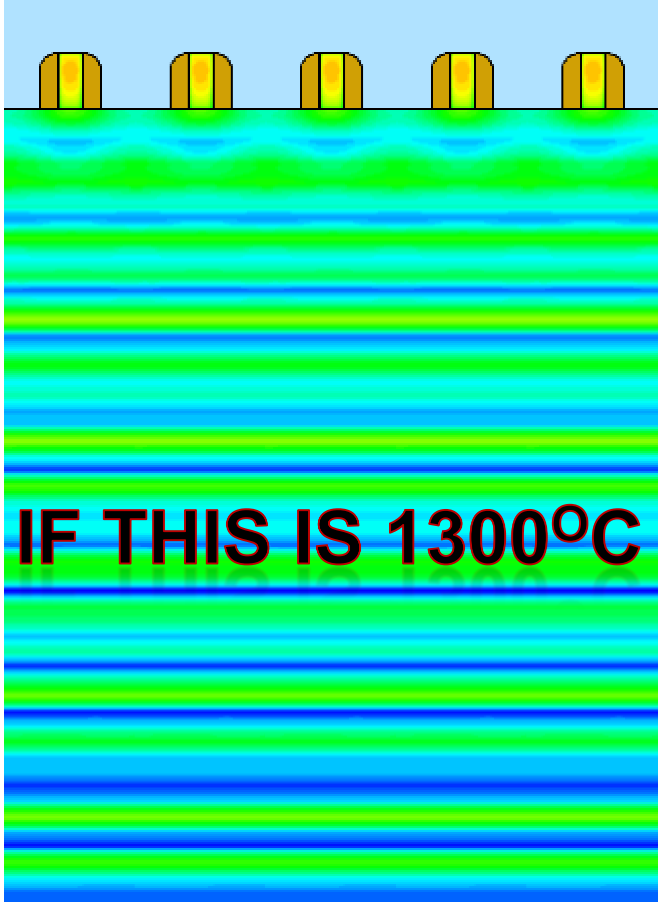
500 nm poly spacing

87% heat absorption

84% heat absorption

Time Averaged Heat Generation @32nm

100 nm poly spacing

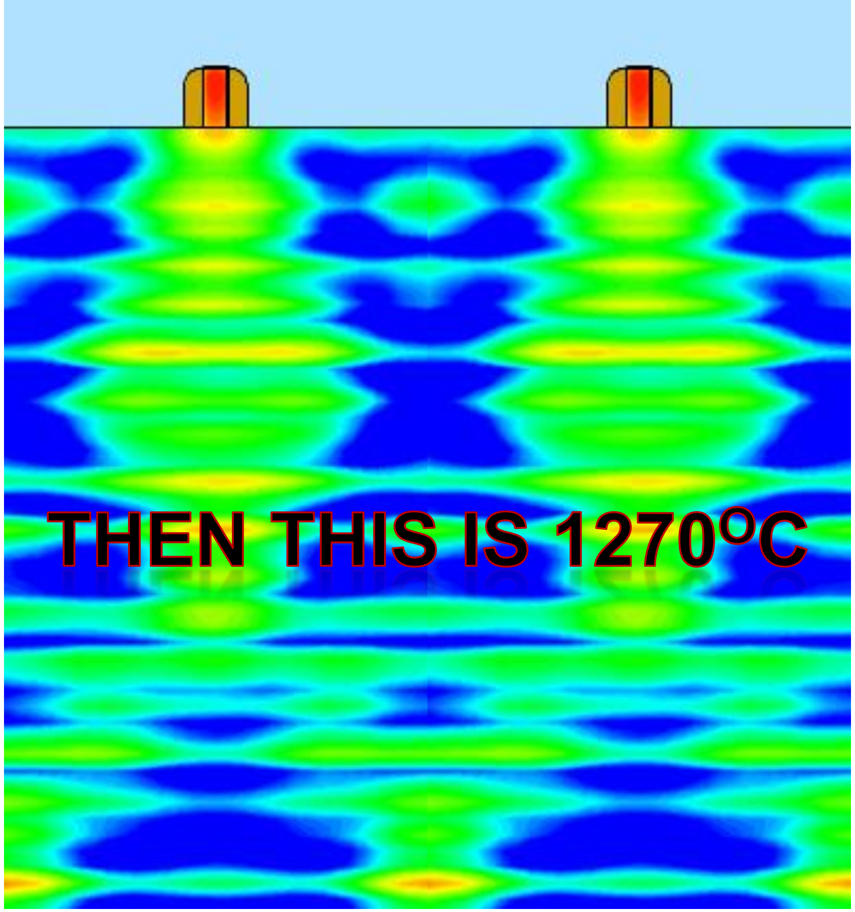


IF THIS IS 1300$^{\mathrm{O}}$C

87% heat absorption

Quite similar integral heat

500 nm poly spacing

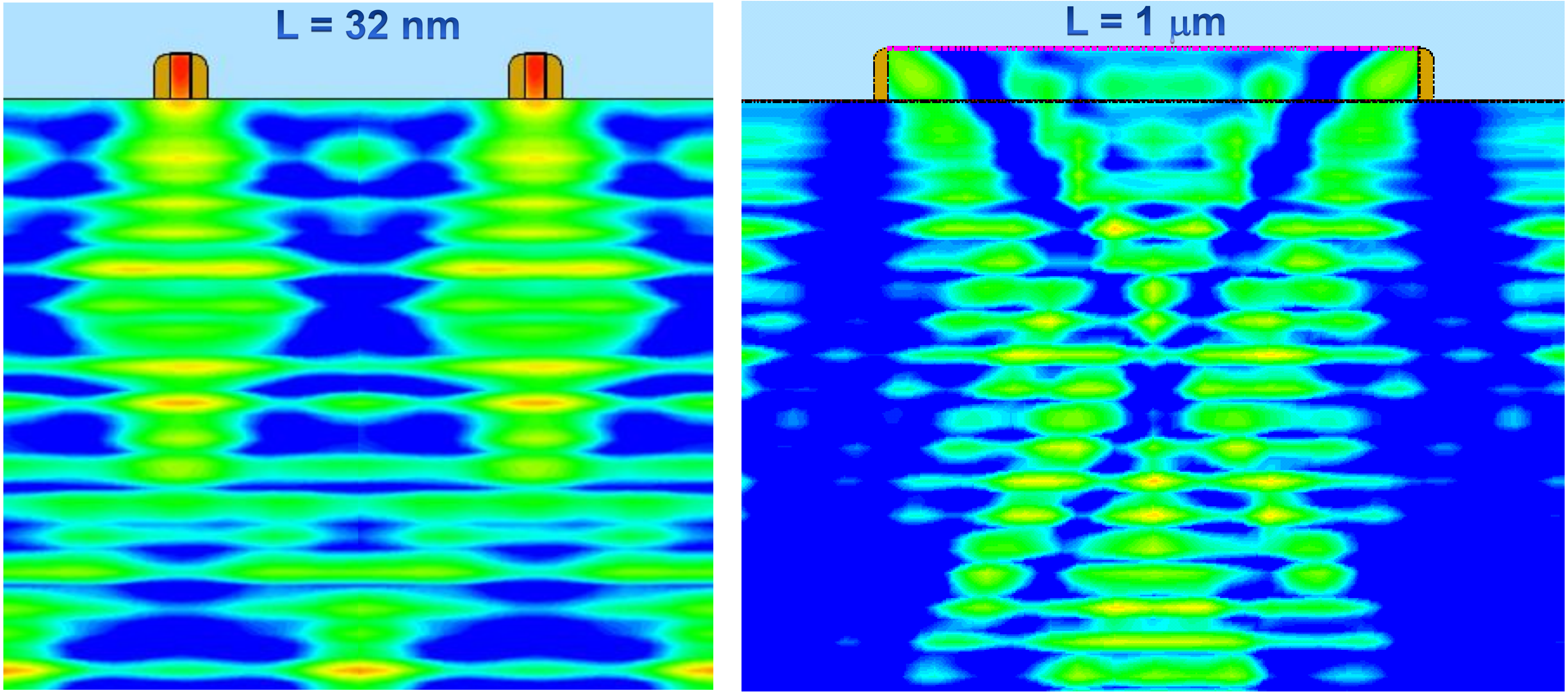


THEN THIS IS 1270$^{\mathrm{O}}$C

84% heat absorption

Heat Generation vs Poly Width

Same 500 nm poly spacing

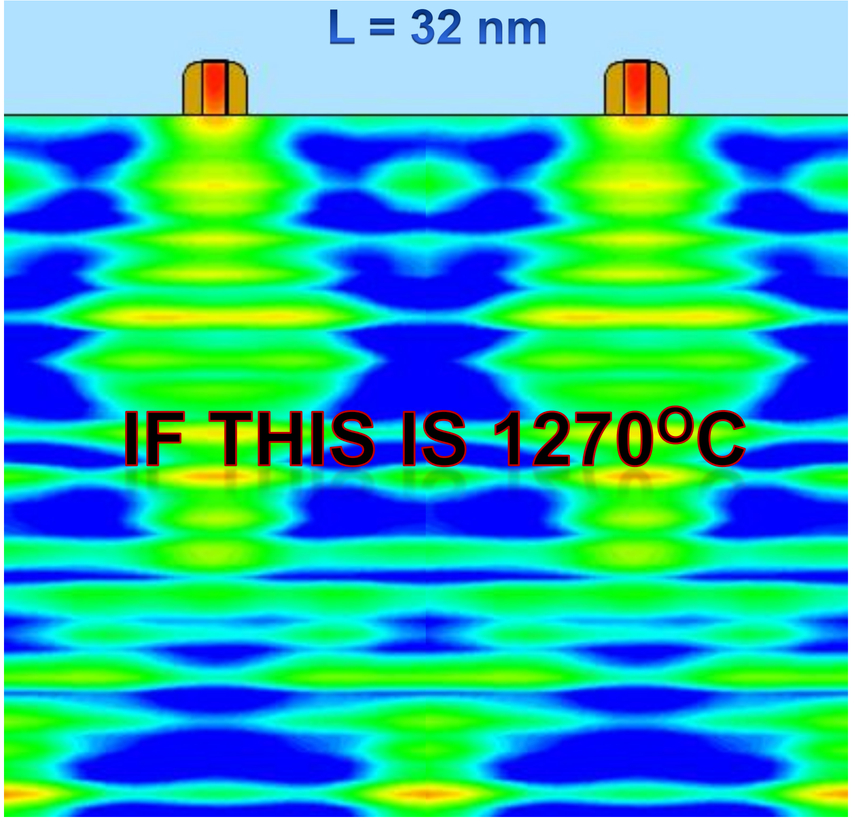


84% heat absorption

63% heat absorption

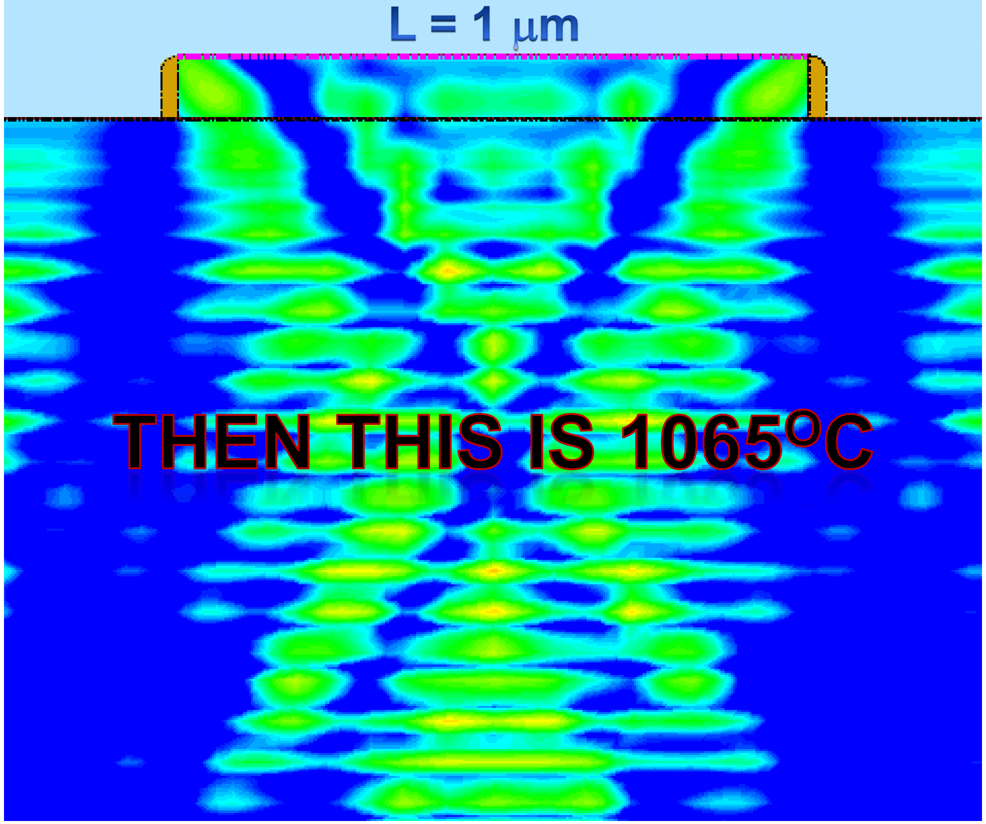
Heat Generation vs Poly Width

Same 500 nm poly spacing



L = 32 nm

IF THIS IS 1270°C



L = 1 μm

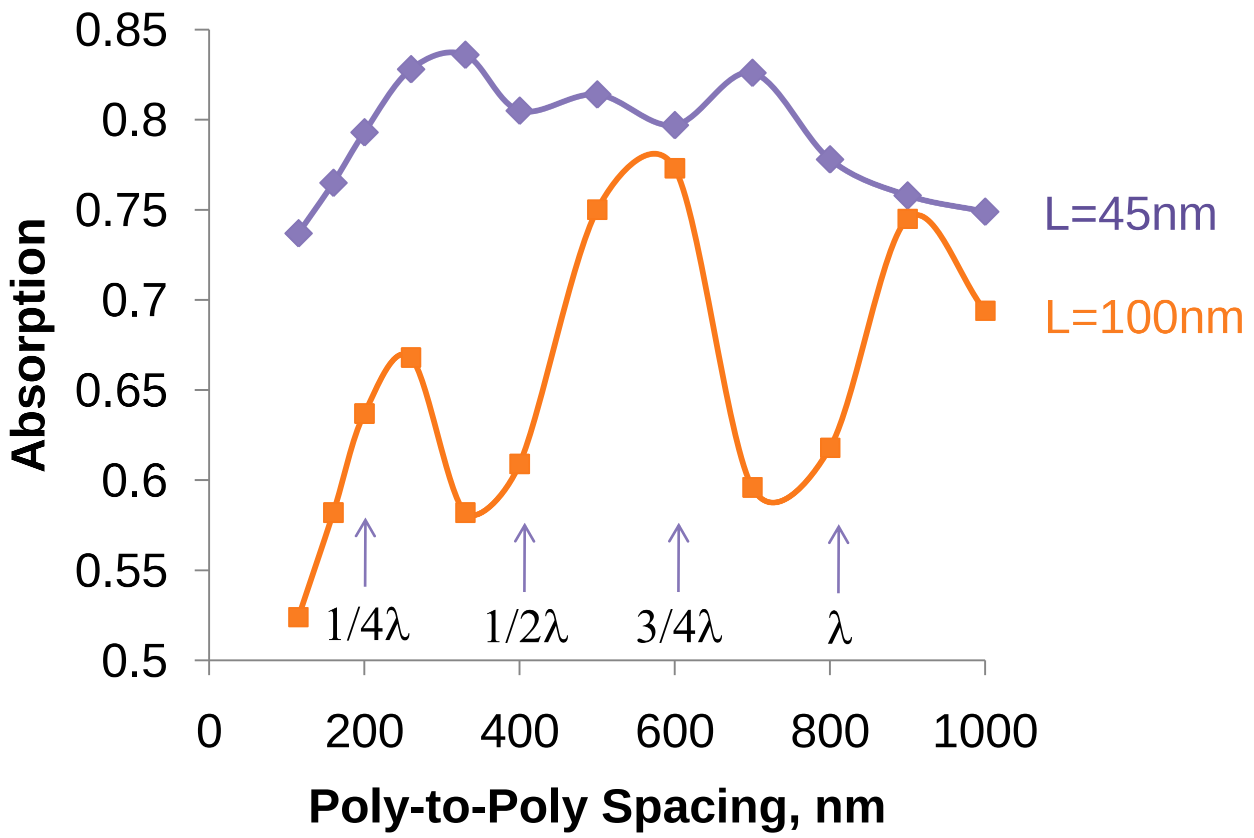
THEN THIS IS 1065°C

84% heat absorption

63% heat absorption

Poly is MUCH hotter and silicon is 25% hotter

Detailed Poly Spacing Trends

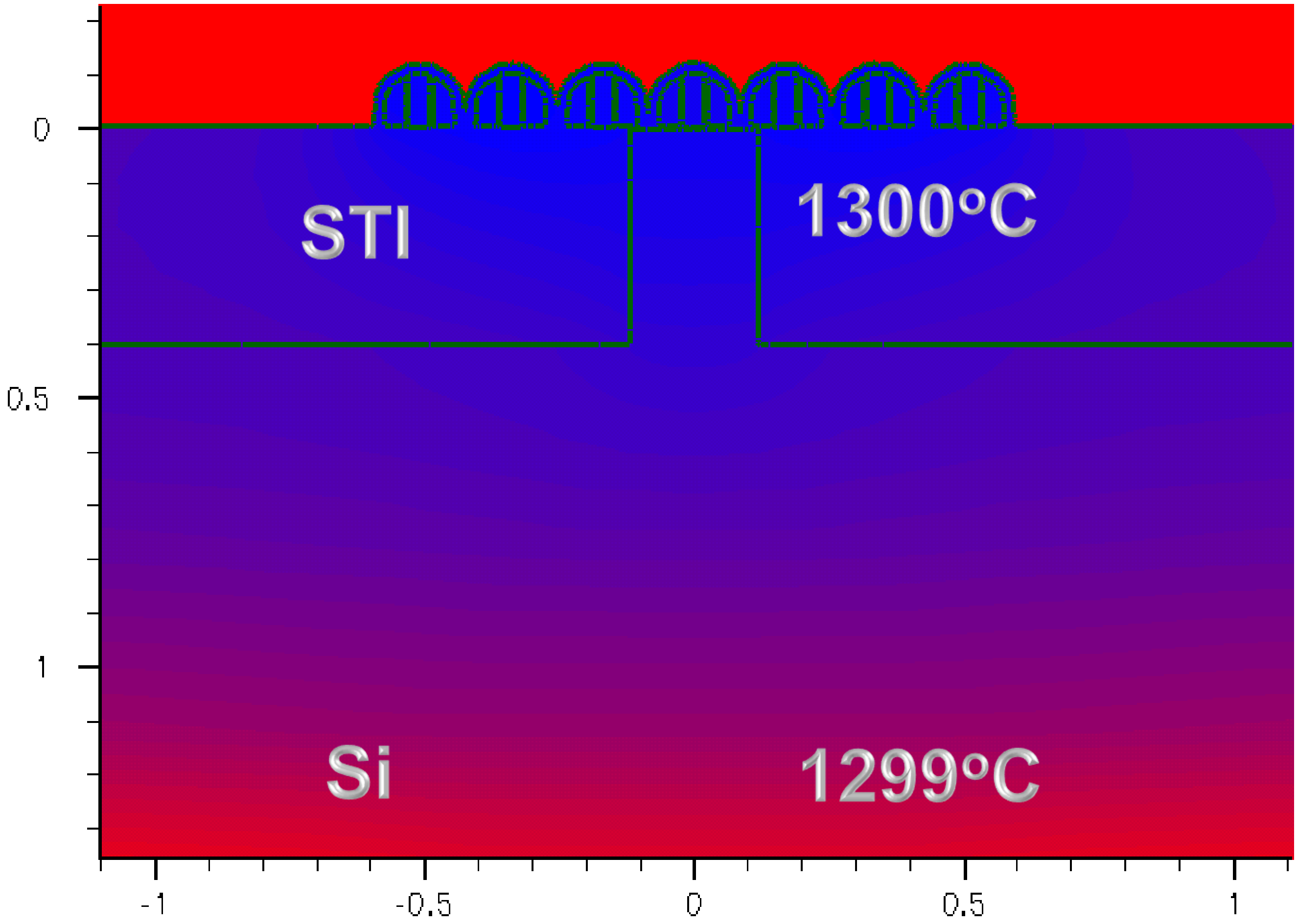


Apparent wave enhancement/ suppression behavior

Heat Transfer Within the Wafer

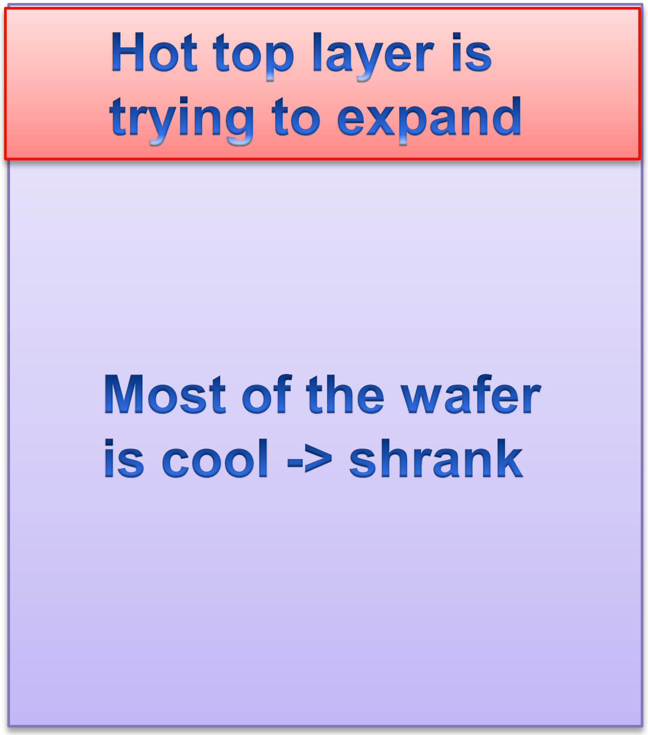
- **Heat transfer within the wafer is very fast, advancing >100 μm/ms**
- **Therefore, layout patterns <100 μm get uniform temperature, with $\Delta T < 1$ °C/μm**
- **The issue can be large areas of layout with significantly different heat absorption**
- **This can be resolved by using a heat absorption layer or appropriate dummy fill**

Typical Temperature Distribution



In ms-timeframe, feature scale T variations are < 1°C

Stress Induced by Temperature Gradient



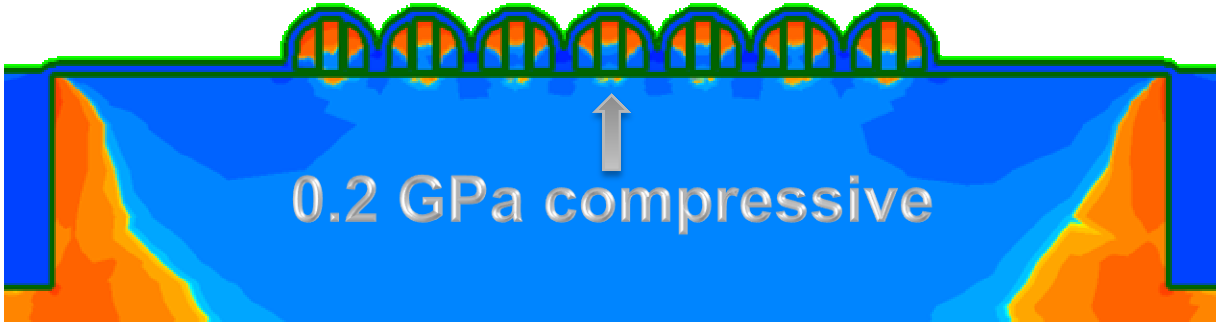
Hot top layer is
trying to expand

Most of the wafer
is cool -> shrank

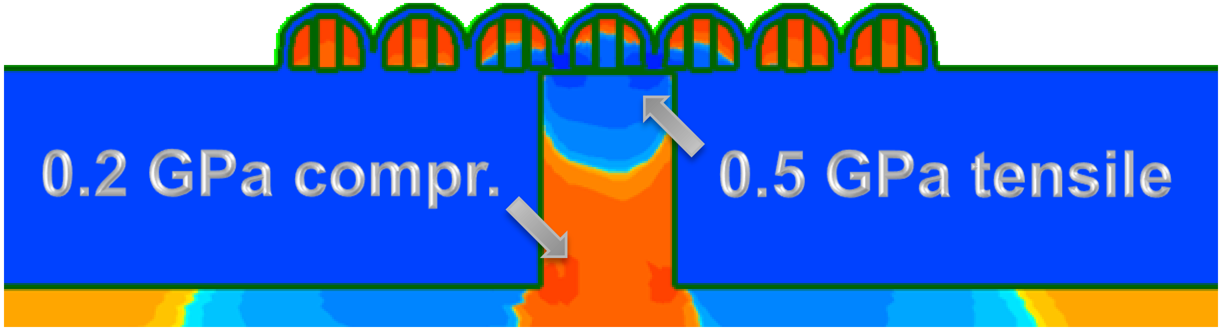
Compressive stress
is expected at the
top of Si wafer

Stress Induced by T Gradient + Pattern

Si-dominant pattern

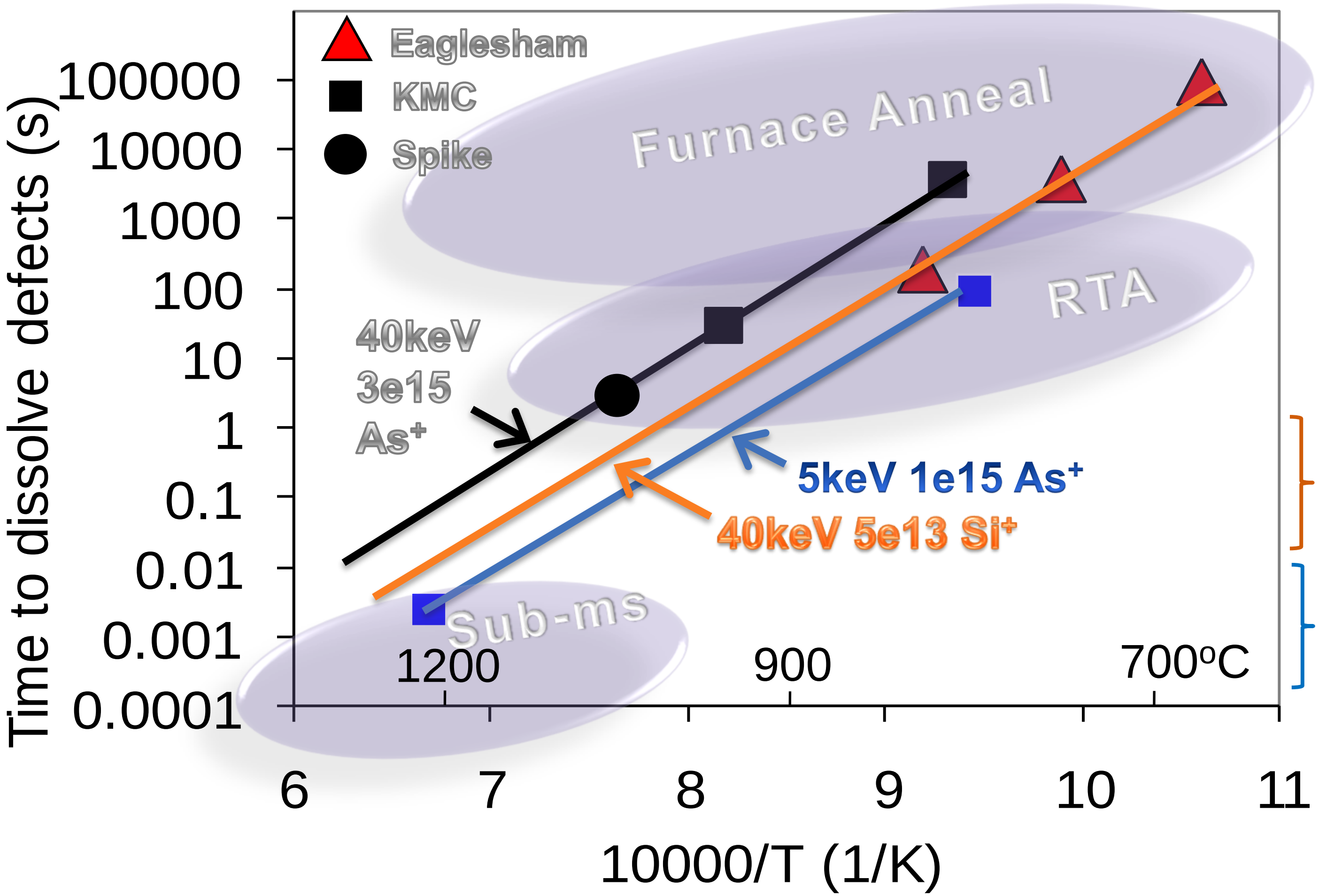


STI-dominant pattern



Depending on local layout, thermal expansion stress changes sign!

Thermal Budget to Dissolve Damage



Can only get here with multiple scans

Hard to anneal defects for >10keV implant using ms-anneal

Annealing Implant Damage

- When ms anneal is used w/o spike or with sub-1000 °C spike, it does not anneal implant damage from higher E implants

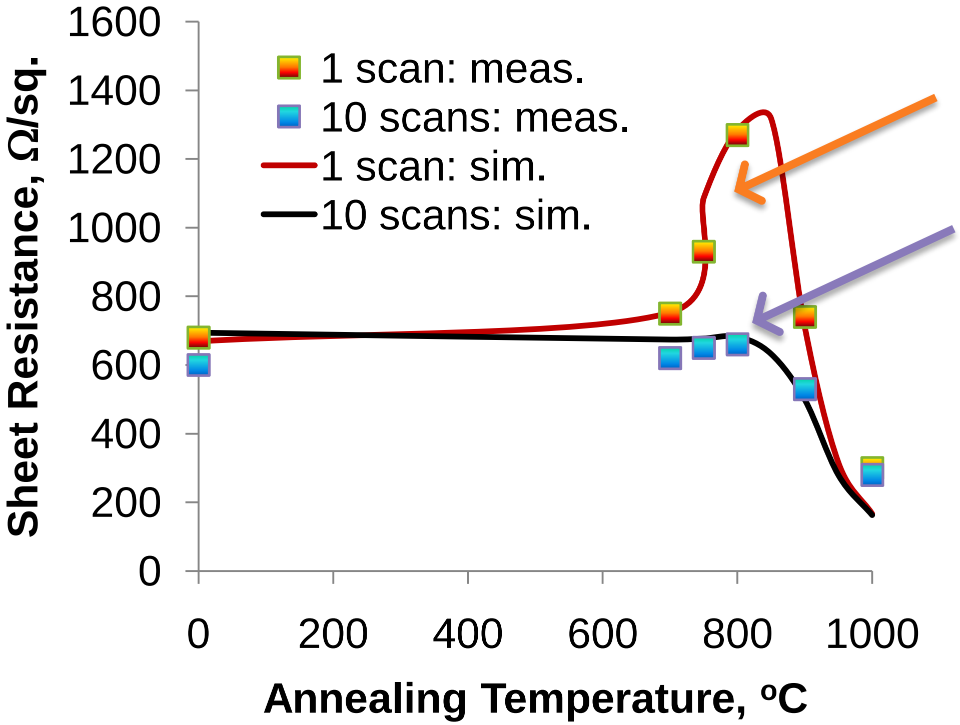
- The residual damage backfires by deactivating S/D dopants or by provoking junction leakage

- One solution is to use multiple ms scans

- Another – to trap I's using C, F, or N

Several Laser Scans Stabilize S/D Rs

- *10^{15} cm^{-2} Ge^{+} @5 keV*
- *10^{15} cm^{-2} B^{+} @500 eV*
- *1150°C laser scan(s)*
- *1 minute anneal*



Residual defects deactivate boron by creating BICs in 700°C to 900°C T range

Ten laser scans completely anneal implant damage and stabilize boron Rs

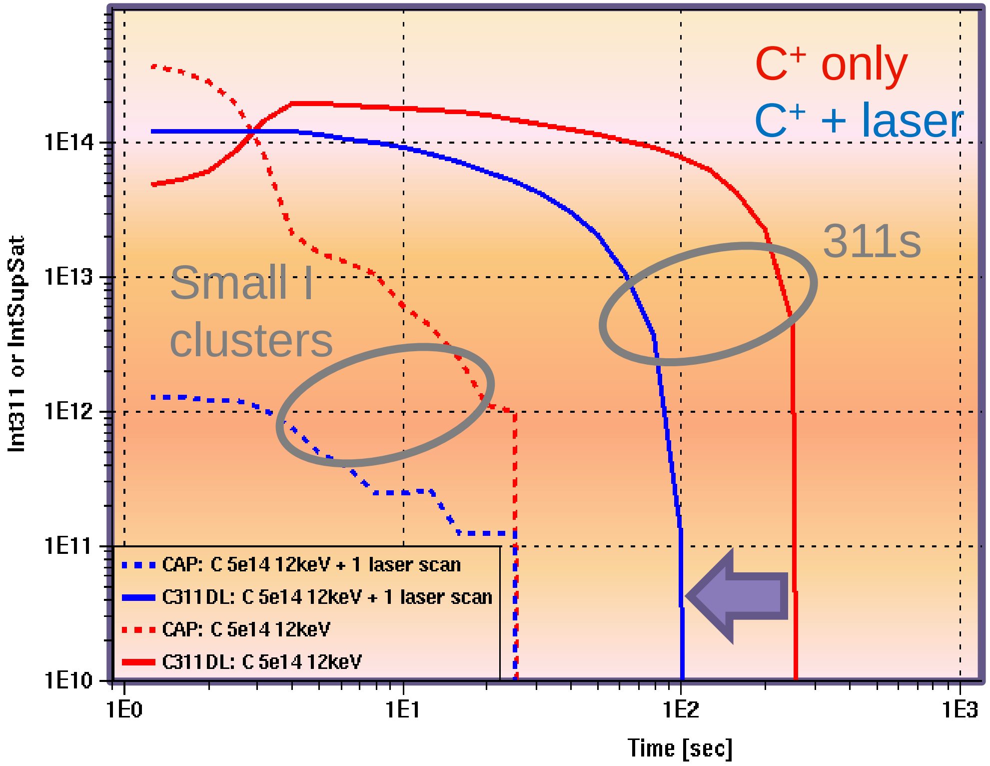
Measured data from
J. Sharp et al, MRS 2006

Simulation performed with
Sentaurus Process KMC

Halo Implant with Millisecond Anneal

- For halo implant, deactivation/clustering is not an issue because of the lower dopant concentration
- What is important are residual extended defects that might survive due to higher implant energy -> deeper
- The residual defects introduce energy levels in the bandgap -> junction leakage

Halo Implant with C⁺ and Laser

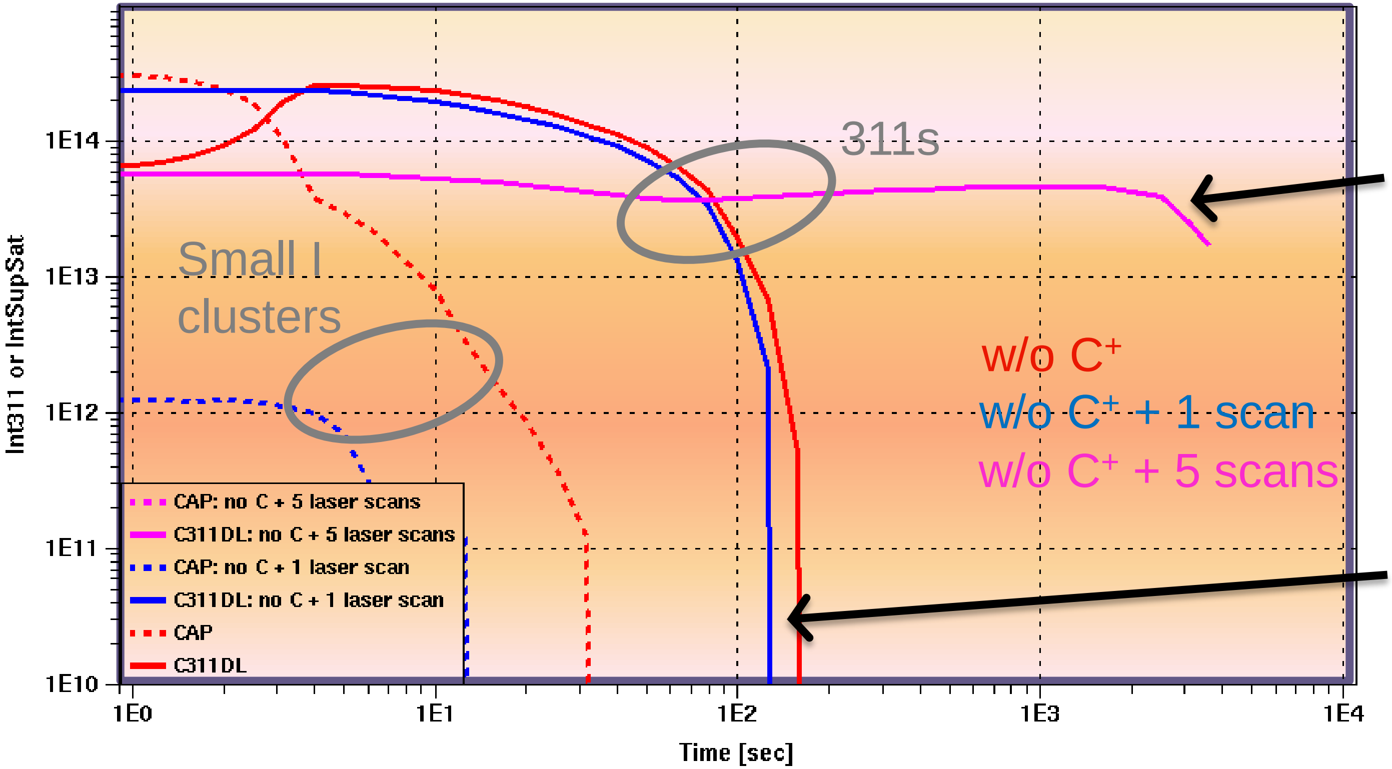


Once C⁺ co-implant is used, a laser scan helps to cut damage annealing time by 2.5x

- **5e14 cm^{-2} C⁺ PAI @12 keV**
- **1e13 cm^{-2} As⁺ halo @20 keV**
- **laser anneal**
- **mid-T anneal**

Simulation performed with Sentaurus Process KMC

Halo Implant w/o C^+ with Laser



5 scans make it ~60x worse, because 311s grow into stable dislocation loops that are harder to dissolve

1 scan does not make an impact

Simulation performed with Sentaurus Process KMC

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Layout Impact on Threshold Voltage

Sony at VLSI 2007:

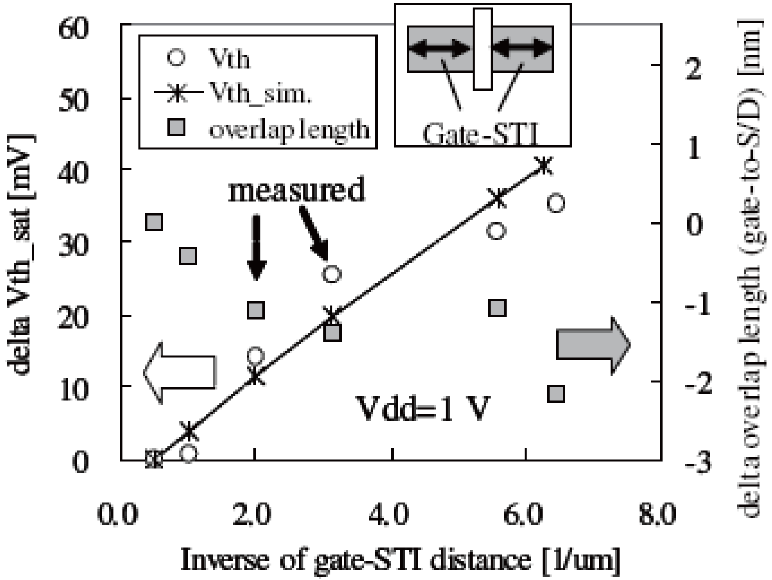


Fig. 5 Dependences of delta Vth_sat and delta overlap length on gate-STI distance for NFET.

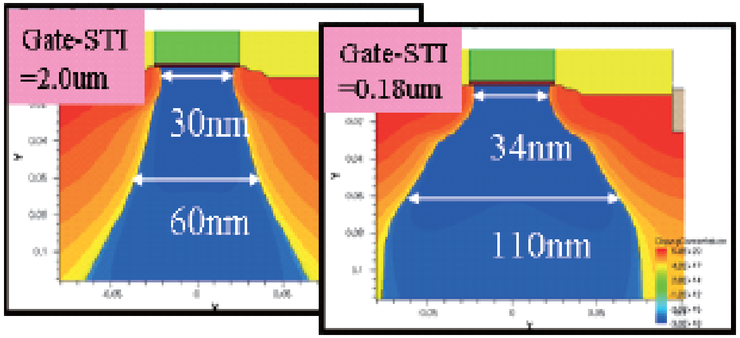
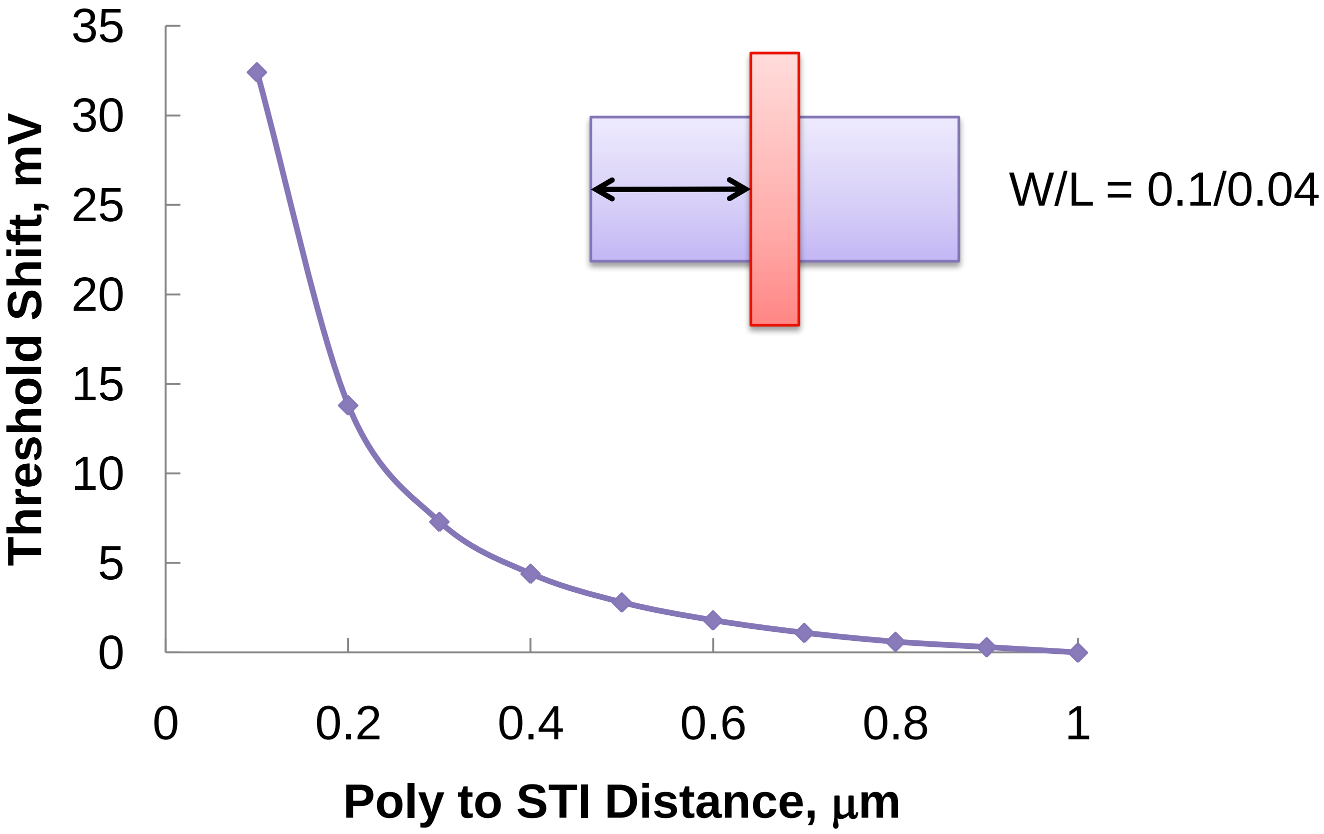


Fig. 4 Simulated difference of dopant distribution profile of an NFET as gate-STI shrinks. Both extension and S/D dopant diffusion are retarded.

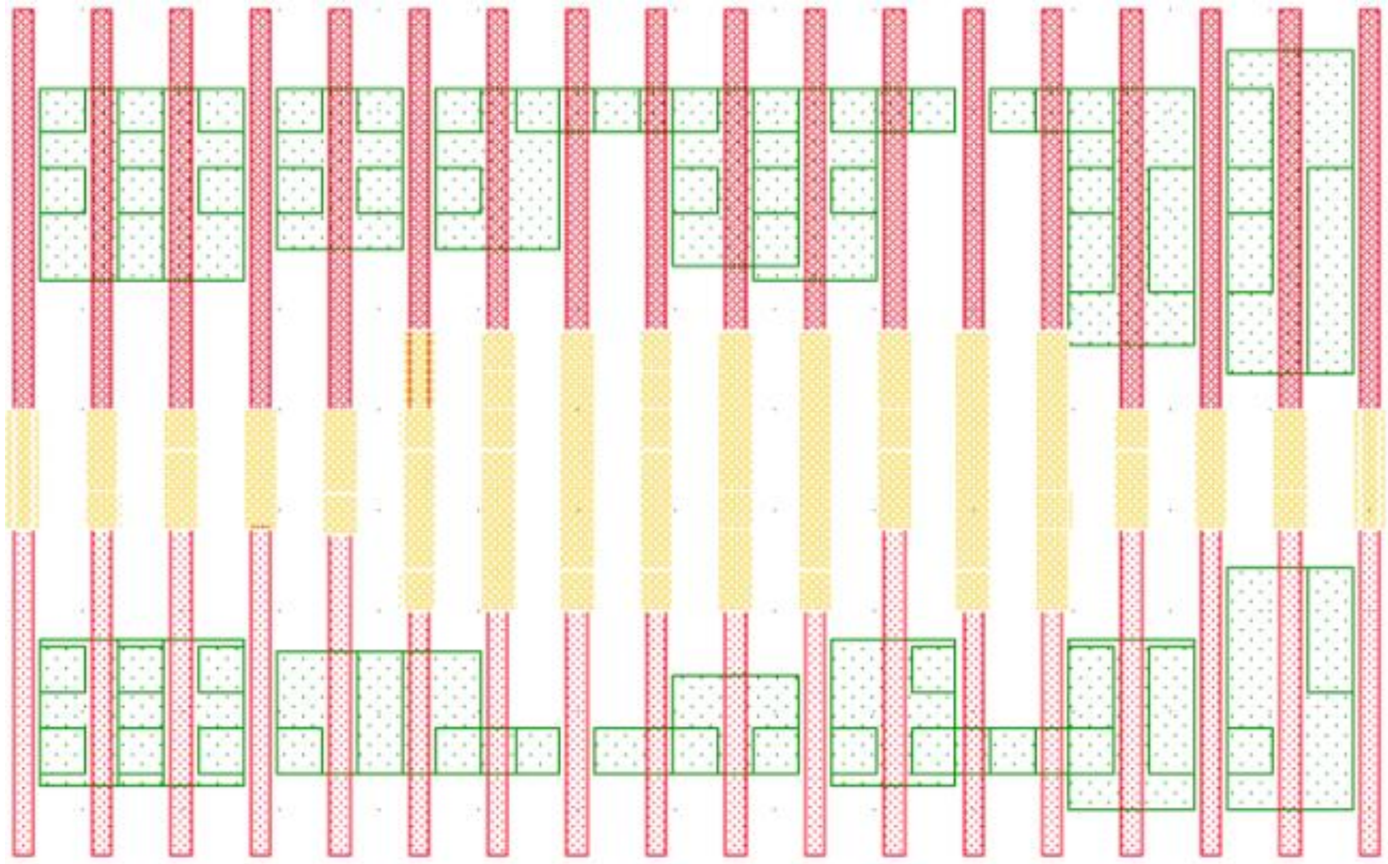
- Threshold changes ~40 mV in response to a simple layout change
- Simultaneously, Leff changes by ~4 nm due to S/D TED

Typical V_T Behavior vs Poly-to-STI Dist.



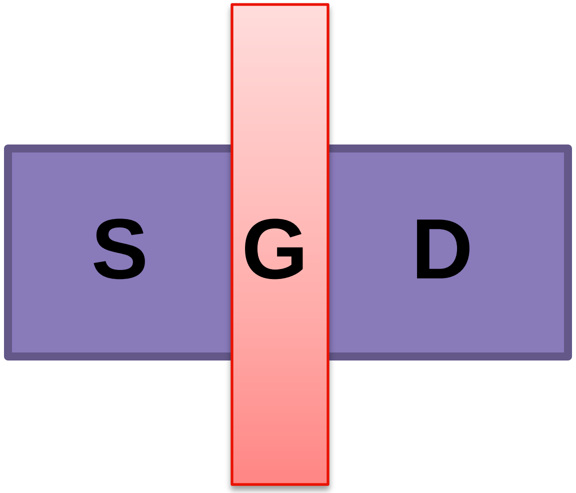
W/L = 0.1/0.04

32nm Libraries: Everybody’s Jogging

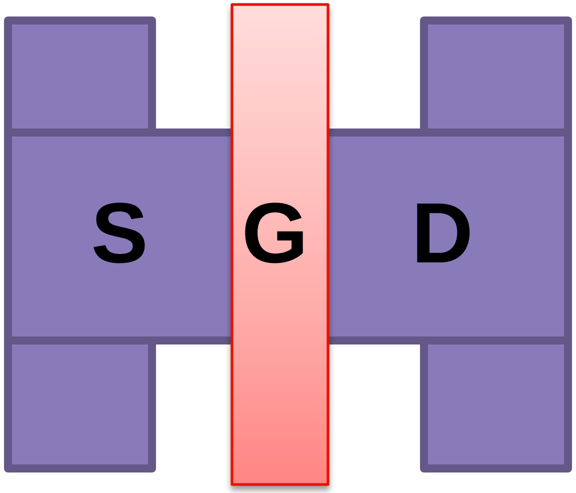


- Despite restricted design rules, lots of active jogs and isolated vs nested gates
- Significant V_T and I_{off} variations persist

Shape of the Source/Drain Layout

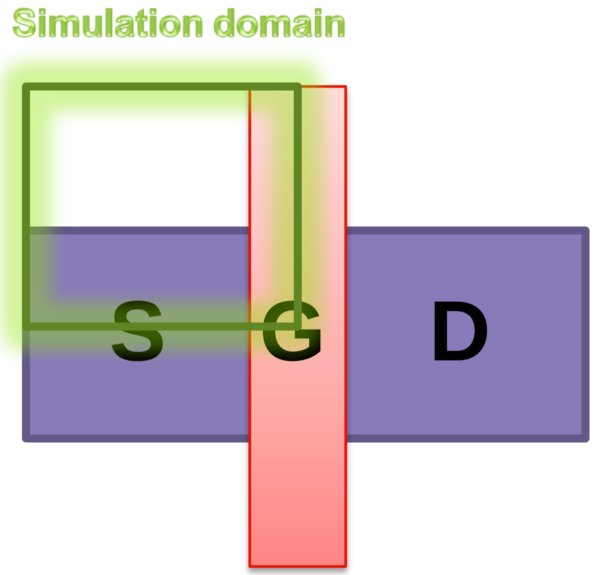


Simple rectangular
“I shape”



Increasingly popular
“H shape”

Exploit Symmetry -> Model ¼ Structure



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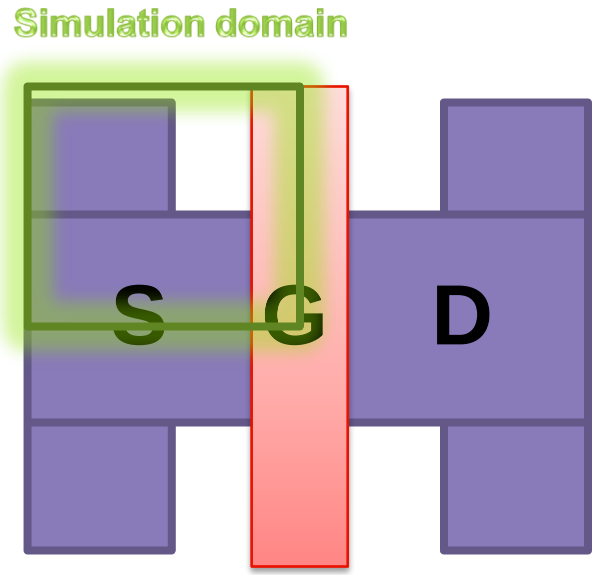

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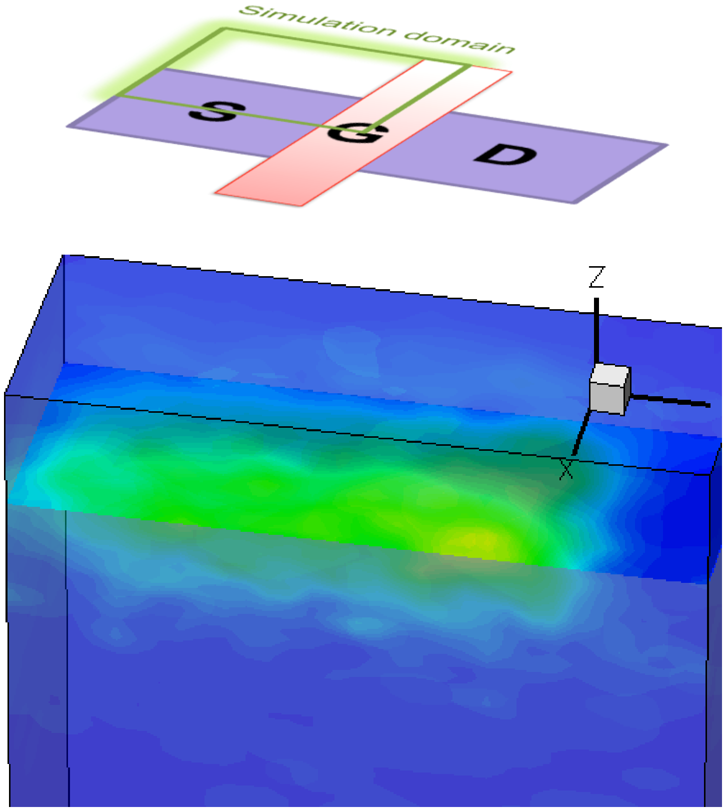
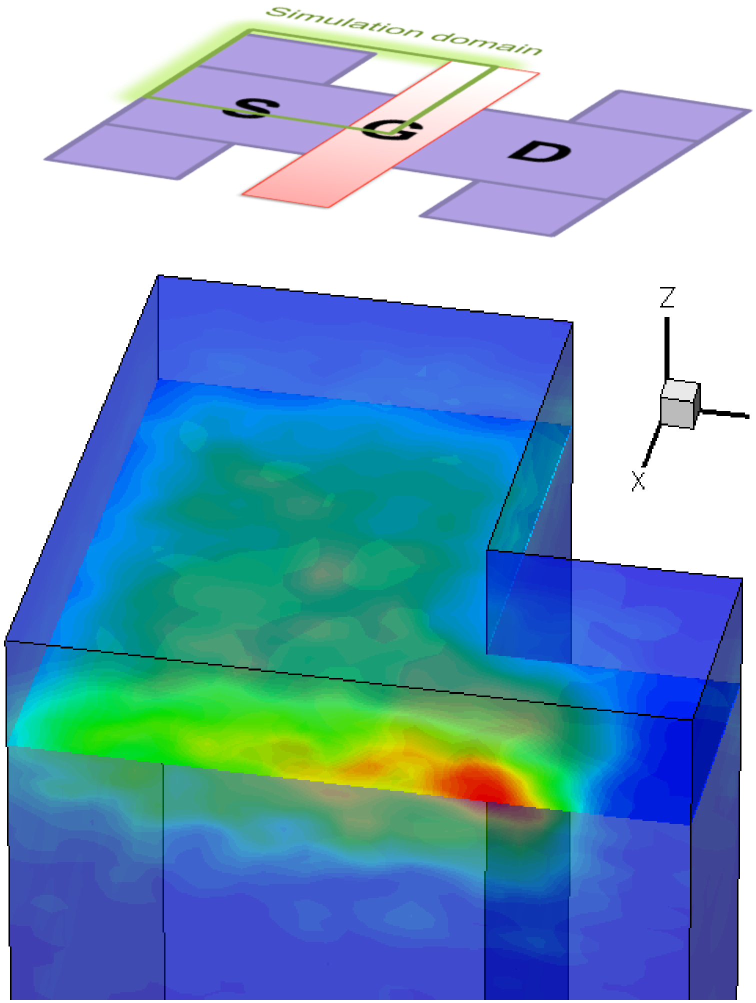
S/D Arsenic TED

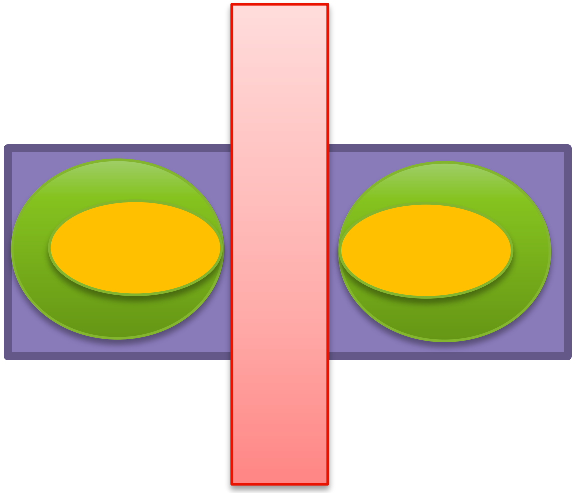


Higher TED in the middle of S/D

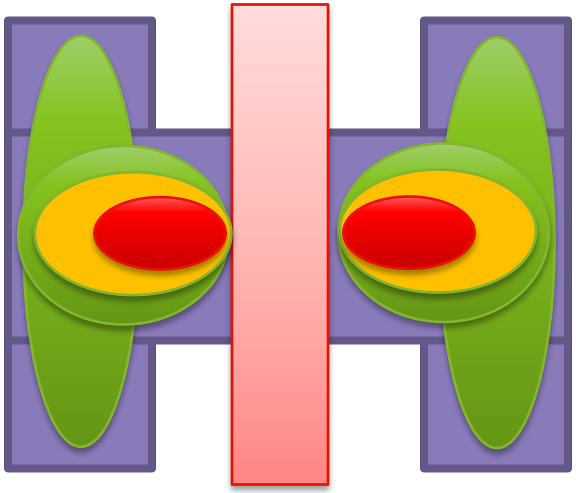


Even higher TED @SDE

Schematic TED Distribution: Top View

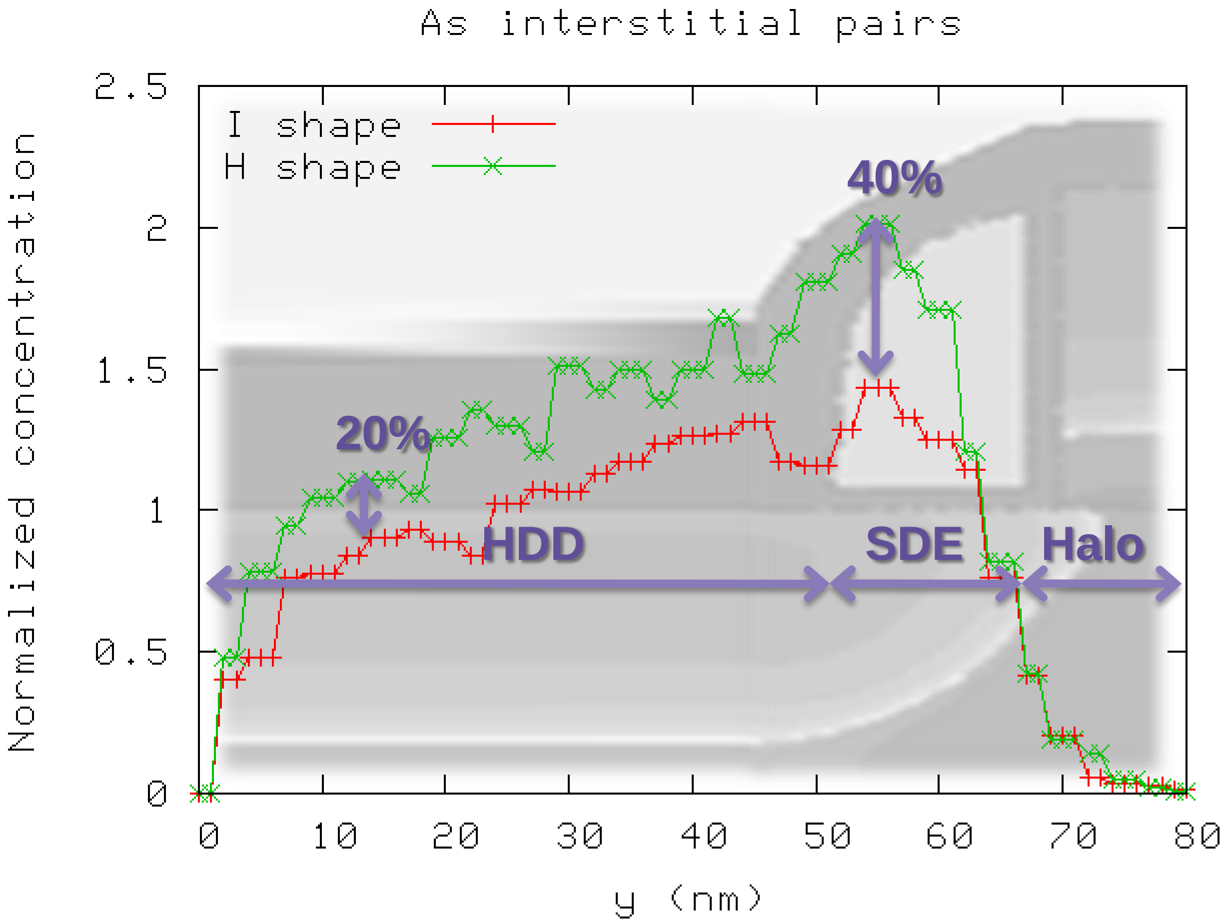


TED peak is away from STI



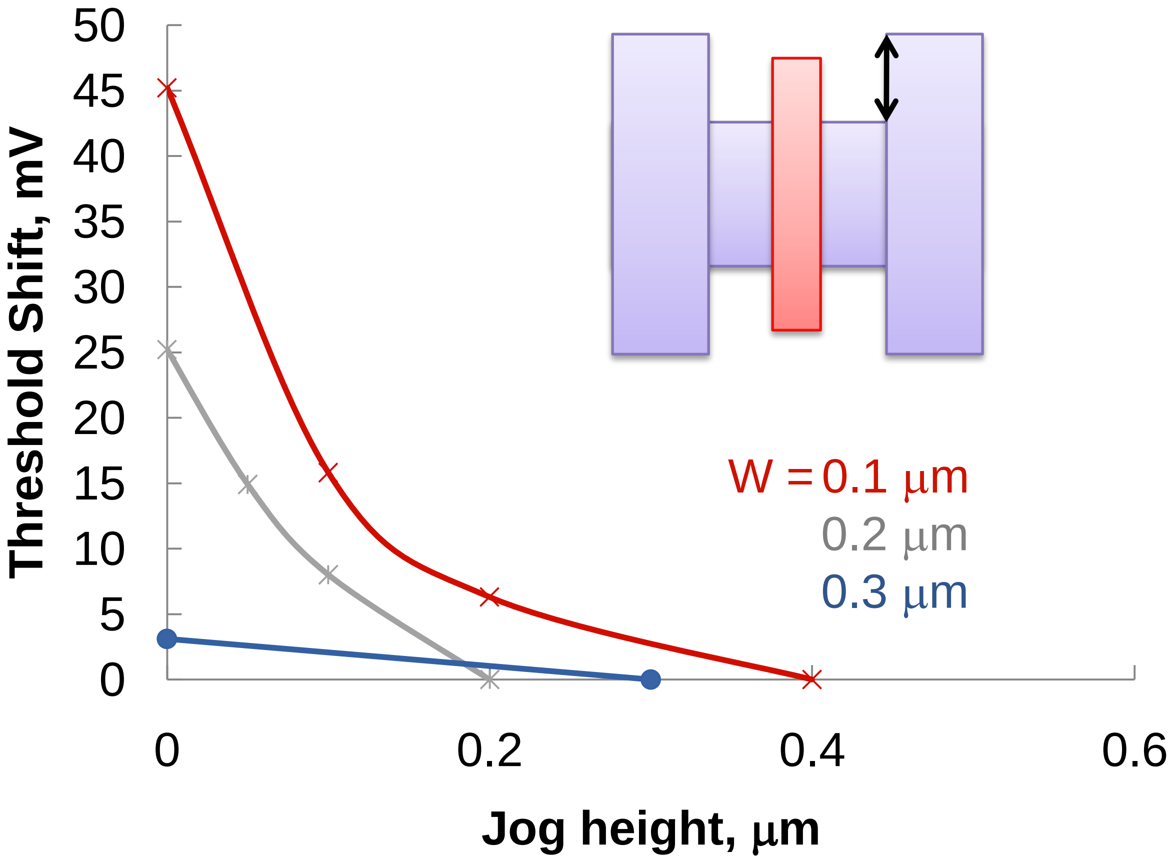
TED peak is higher & close to the channel

Quantitative S/D TED Assessment



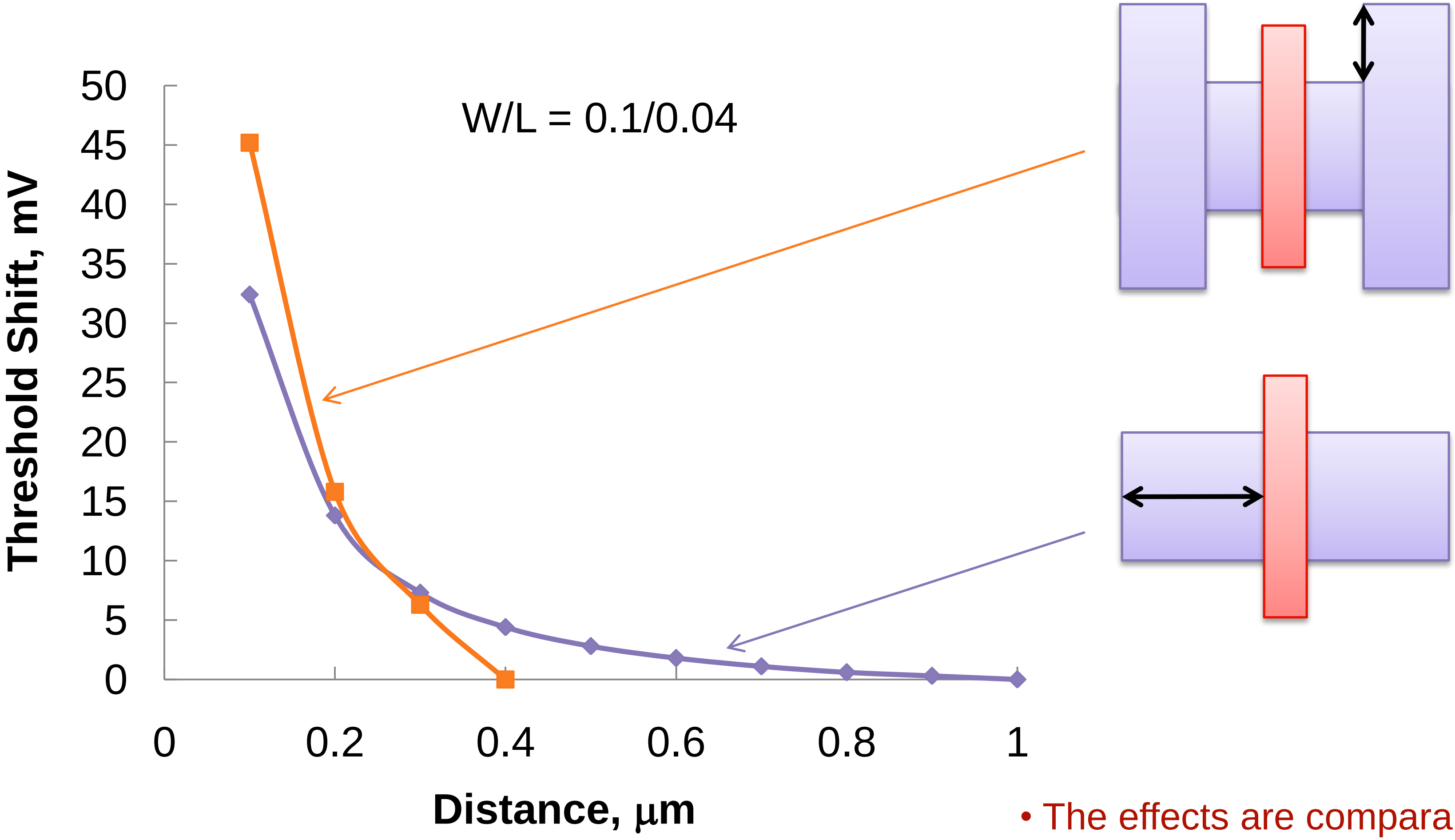
H-shape S/D has 40% more TED @SDE than I-shape, which translates into shorter Leff

The Jog Effect Increases With Scaling



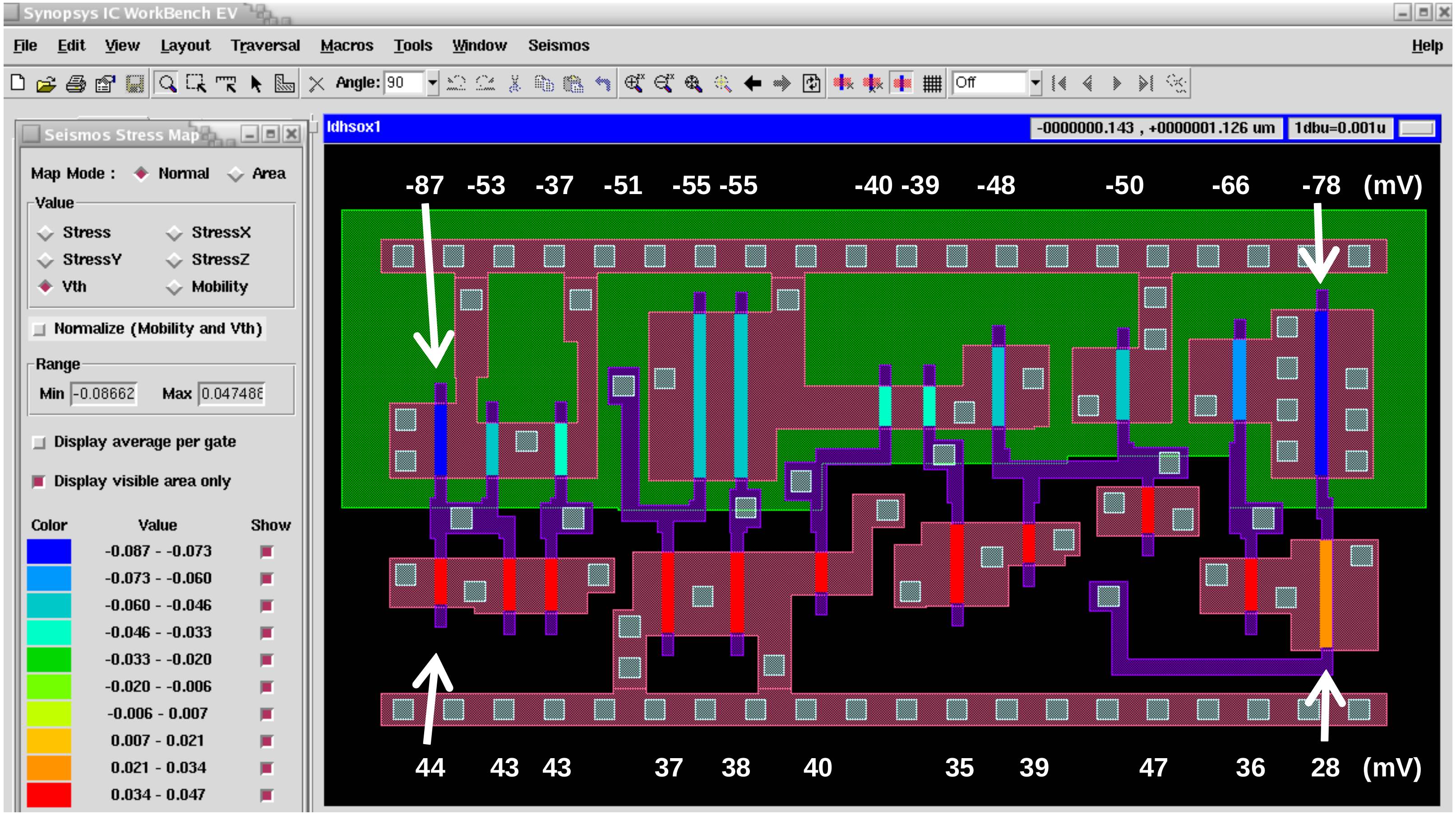
- Negligible effect @0.3µm,
- Becoming major effect @0.1µm

Comparing The Two Effects



- The effects are comparable
- Trends are in the same direction

Compact Model for V_T and L_{eff}



Map Mode : ● Normal ○ Area

Value

○ Stress ○ StressX
○ StressY ○ StressZ
● Vth ○ Mobility

☐ Normalize (Mobility and Vth)

Range

Min -0.08662 Max 0.04748

☐ Display average per gate

☑ Display visible area only

Color	Value	Show
🟦	-0.087 - -0.073	☑
🟦	-0.073 - -0.060	☑
🟦	-0.060 - -0.046	☑
🟩	-0.046 - -0.033	☑
🟩	-0.033 - -0.020	☑
🟩	-0.020 - -0.006	☑
🟩	-0.006 - 0.007	☑
🟨	0.007 - 0.021	☑
🟧	0.021 - 0.034	☑
🟥	0.034 - 0.047	☑

For fast analysis of V_T and L_{eff} variations, a compact model compliments TCAD

Conclusions

- **Optical effects analyzed for laser annealing**
- **Pattern-specific heat transfer and stress evolution are discussed**
- **Approach to improve T uniformity suggested**
- **New V_T and L_{eff} layout-induced variations are shown for the 32nm node**
- **Approach for fast V_T and L_{eff} analysis suggested**
- **Continuum models applied to optical, heat transfer, & stress calculations. Besides, KMC and compact models applied to diffusion, defects, and dopant activation.**