

Flash Lamp Annealing Technology Update for 32nm node

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contents

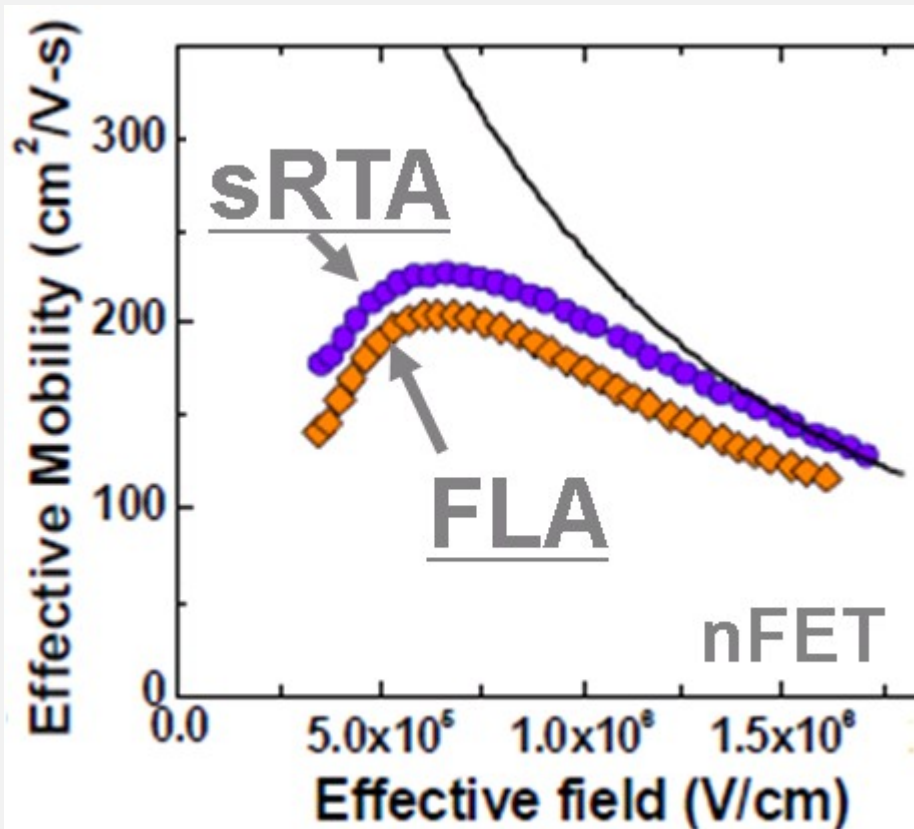
1. Technology requirements for 32nm and beyond
 - High-K/Metal impact
2. FLA improvement
 - Longer time Flash
4. Introduce new device application
FUSI process and FLA
6. summary

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FLA for High-K/Metal

- High-k/Metal gate is a key material for 32nm node device.
- FLA treatment degrades high-k/Metal device performance.



Kalra et al., IEDM 2007

FLA on HfSiO/TiN
increases the trap sites,
and degrade the μ_{eff} & BTI.

FLA for High-K/Metal

- Current process flow can be like next page
- Applying FLA for High-K/Metal gate device (Gate first) , Post-RTA (recovery anneal) is needed
- Spike-RTA is used for Post-RTA . But spike-RTA accelerate dopant diffusion. So it is not a good idea to use spike-RTA.

FLA process flow example

	65nm	45nm and next	45nm and next	45nm and next
gate formation	←	←	←	←
shallow, Halo implantation	←	←	←	←
annealing	not uses		FLA	FLA
spacer formation	←	←	←	←
deep S/D implanta				
annealing	RTP	FLA	RTP low temp.	FLA
	FLA	RTP low temp.	FLA	
silicide	RTP	?	?	?

For 32nm process, we still need sRTA
 But this is not perfect. Spike-RTA creates diffusion.

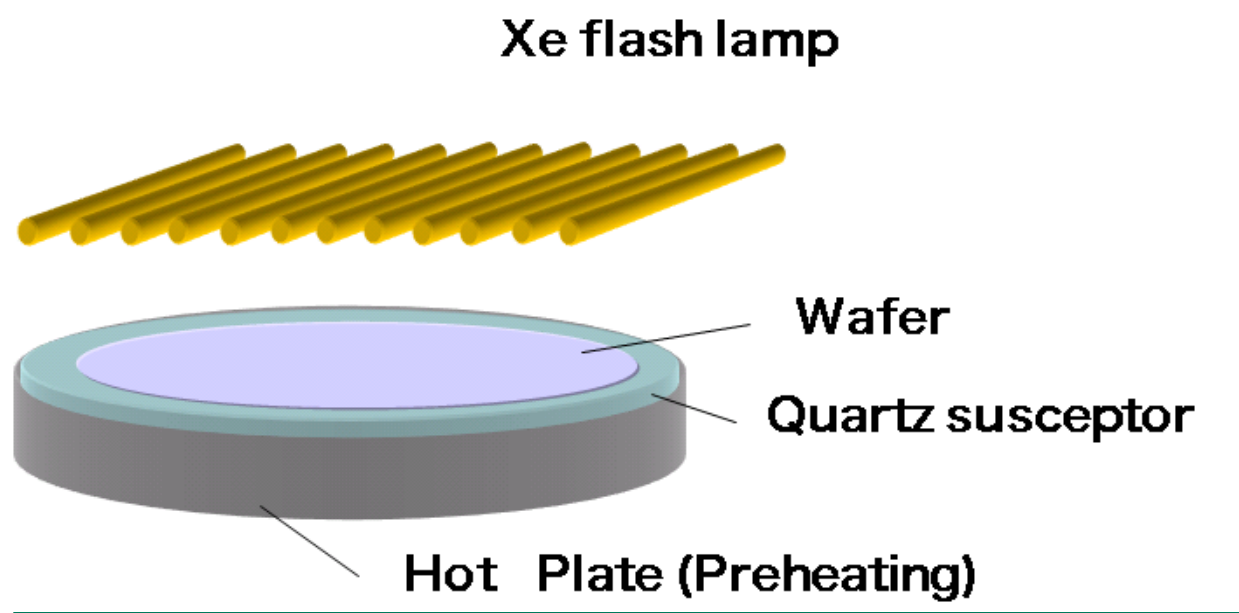
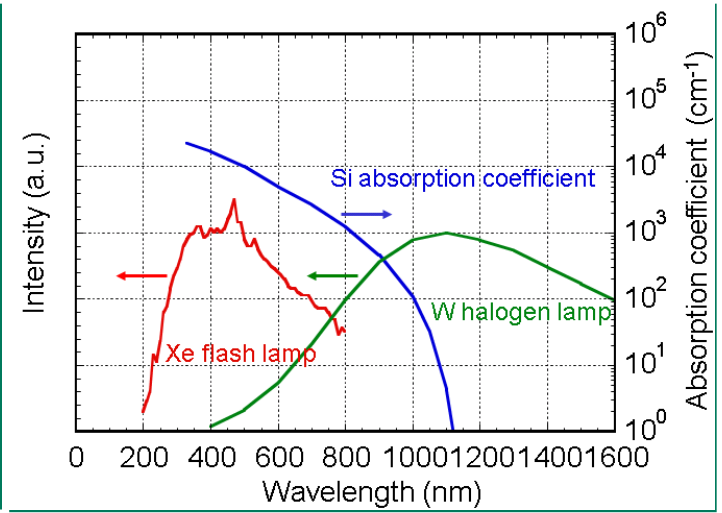
ref : Kiyama , WC JTG 2007

contents

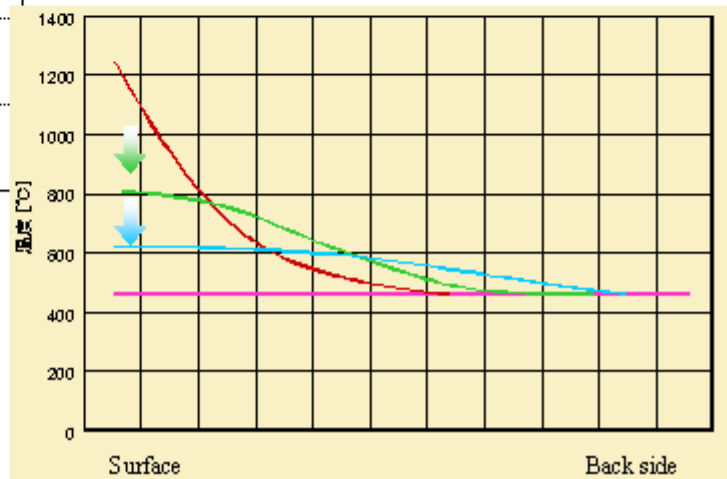
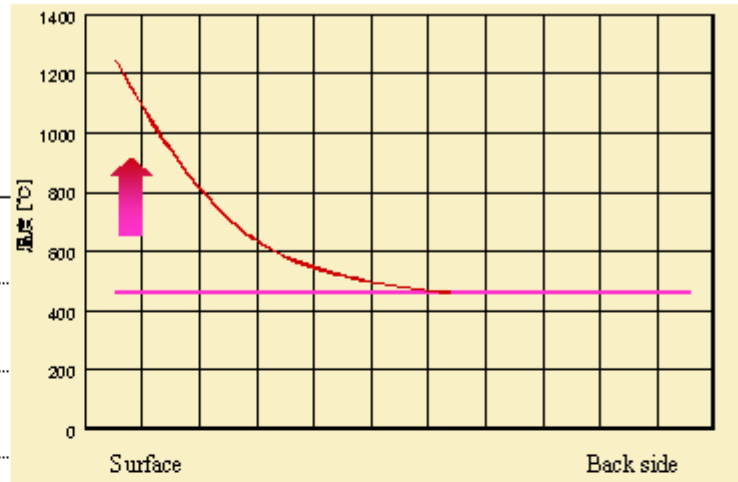
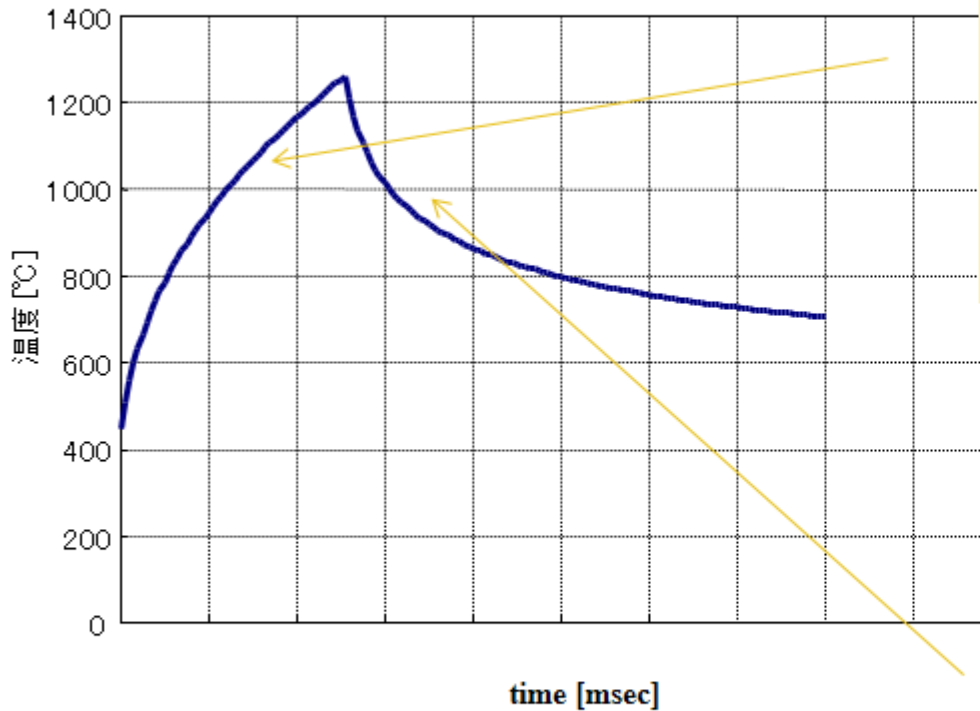
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FLA concept

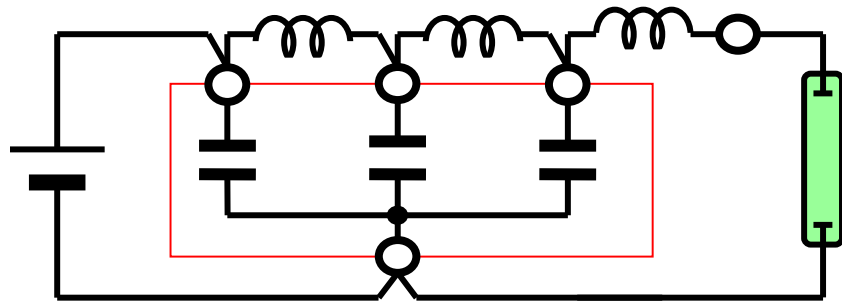
	FLA	RTA
Anneal Time	Millisecond order	second order
Heat Source	Xe Flash Lamp	W Halogen Lamp
Wavelength	White Light	Near Infrared



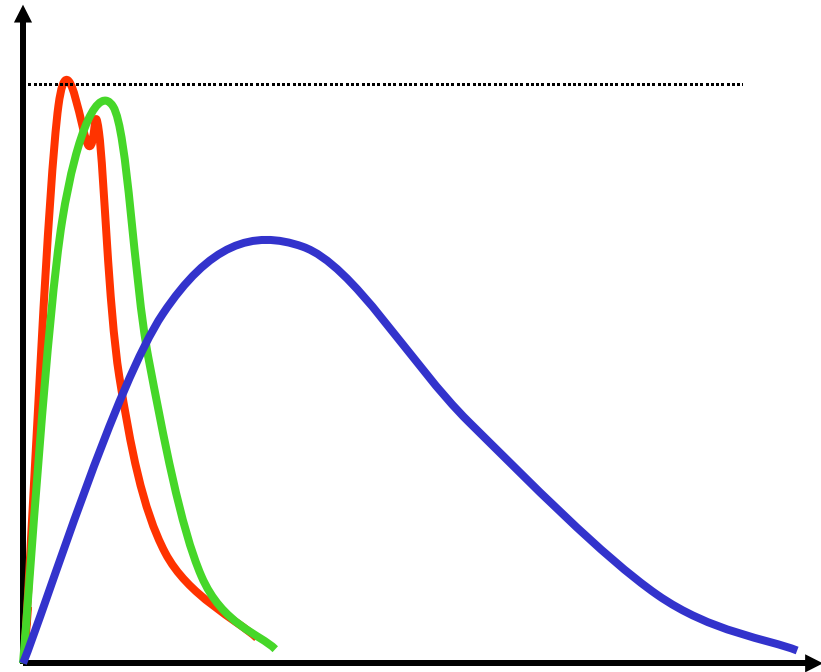
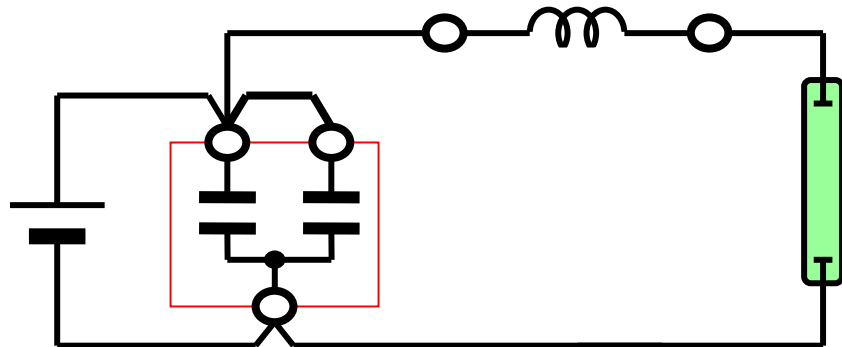
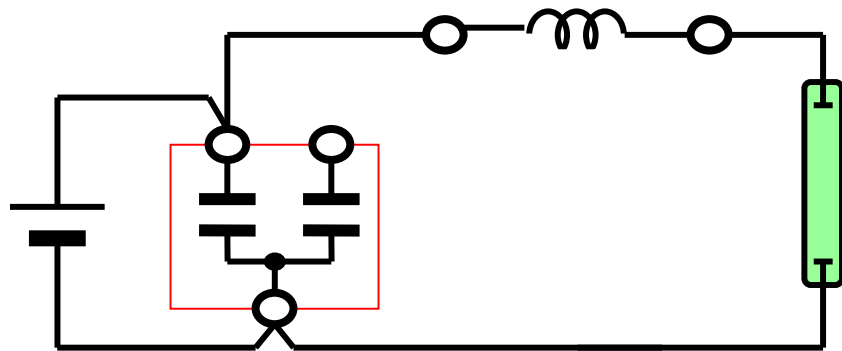
Wafer temperature



Conventional Flash Lamp Circuit

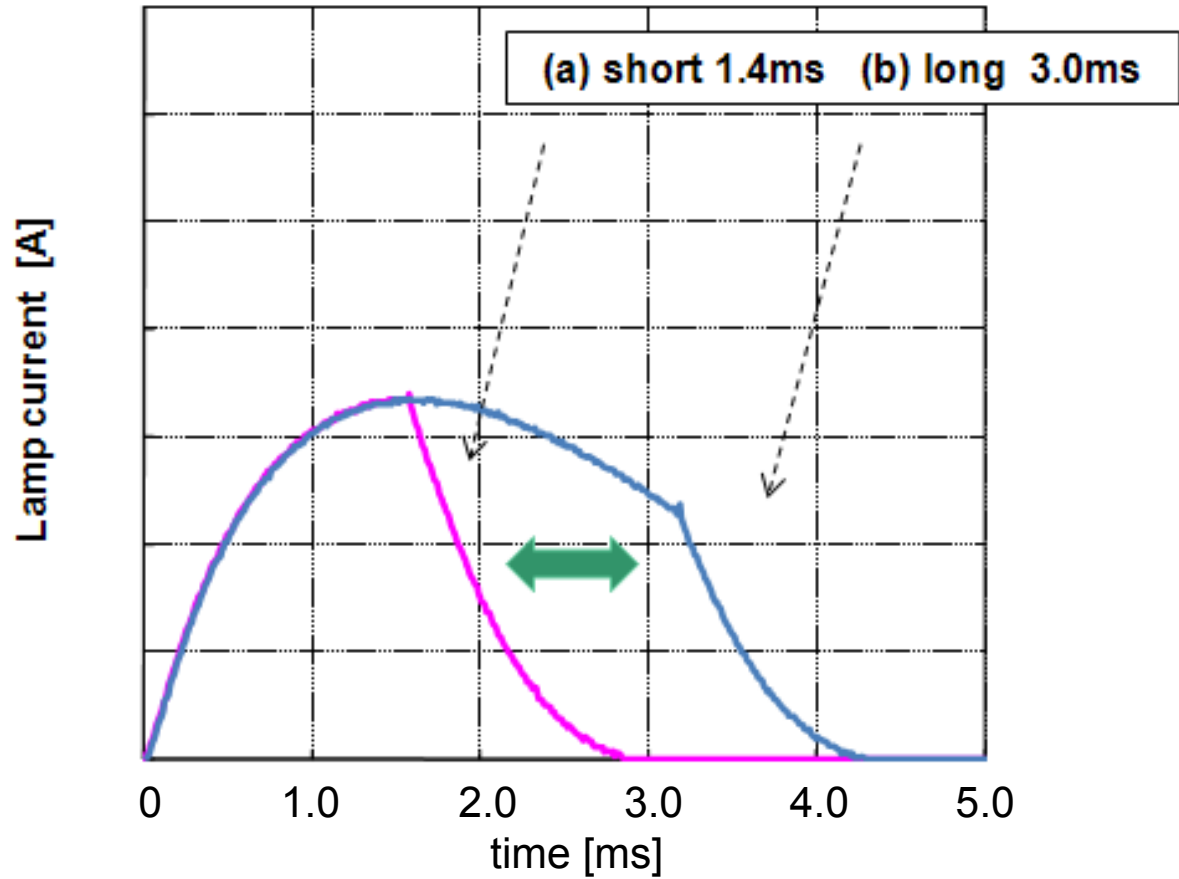


0.8 msec
1.0 msec
5.0 msec



Lamp current of cut off pulse

Variable pulse shape

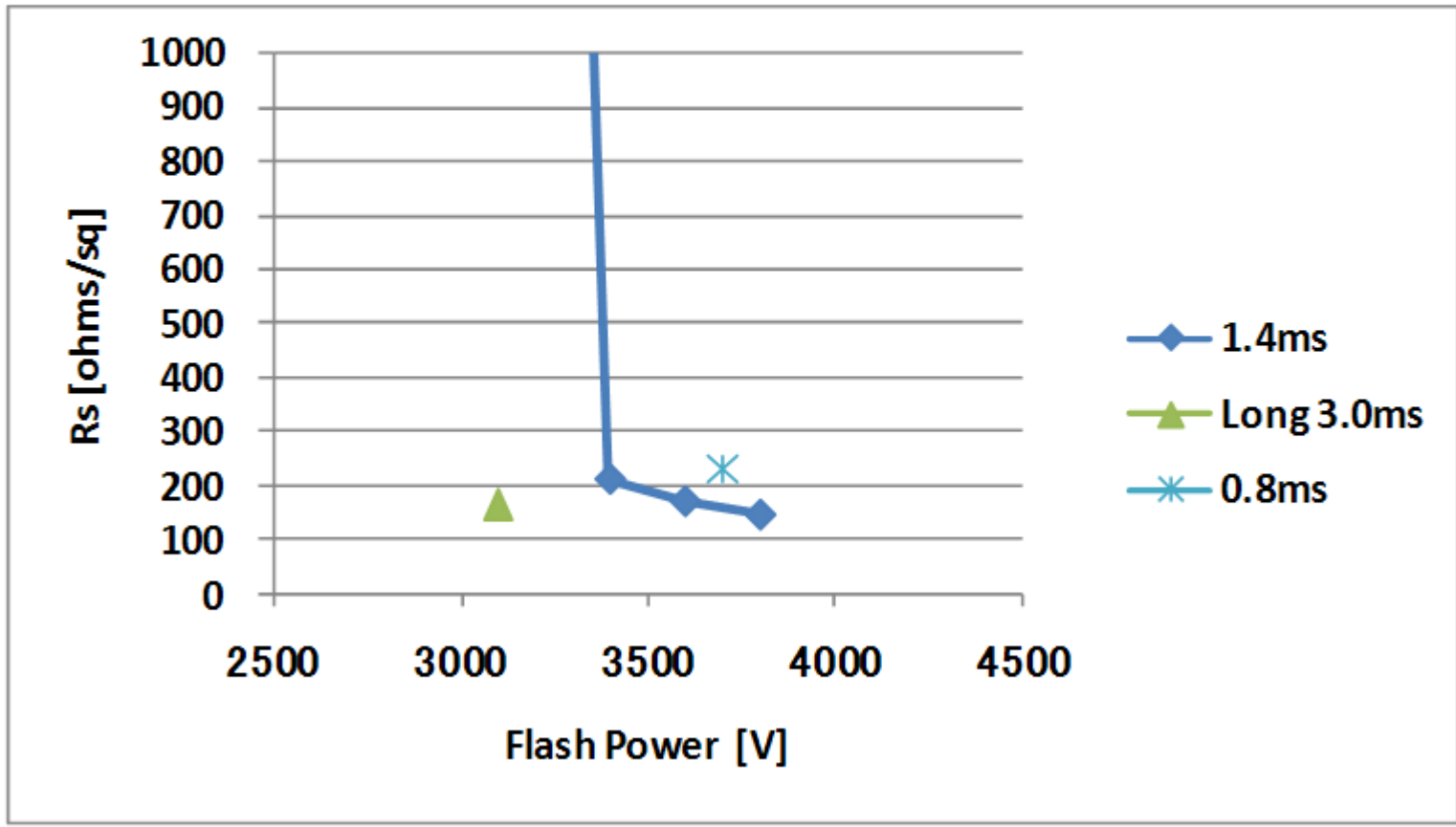


Lamp current of cut off pulse (a) Shorter 1.4ms (b) Long 3.0ms

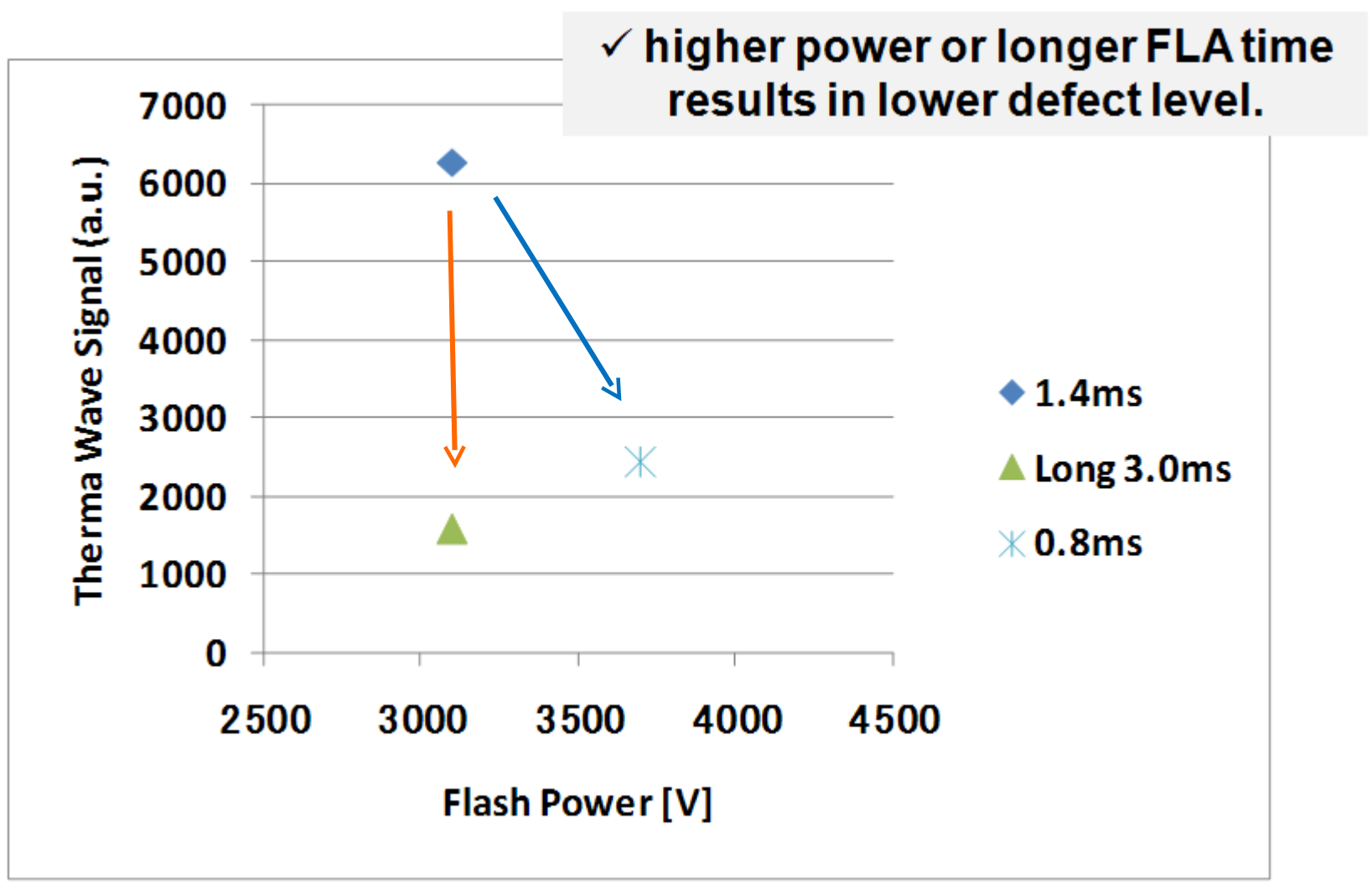
Rs and, FLA Power pulse comparison

✓ Longer Pulse accelerate activation

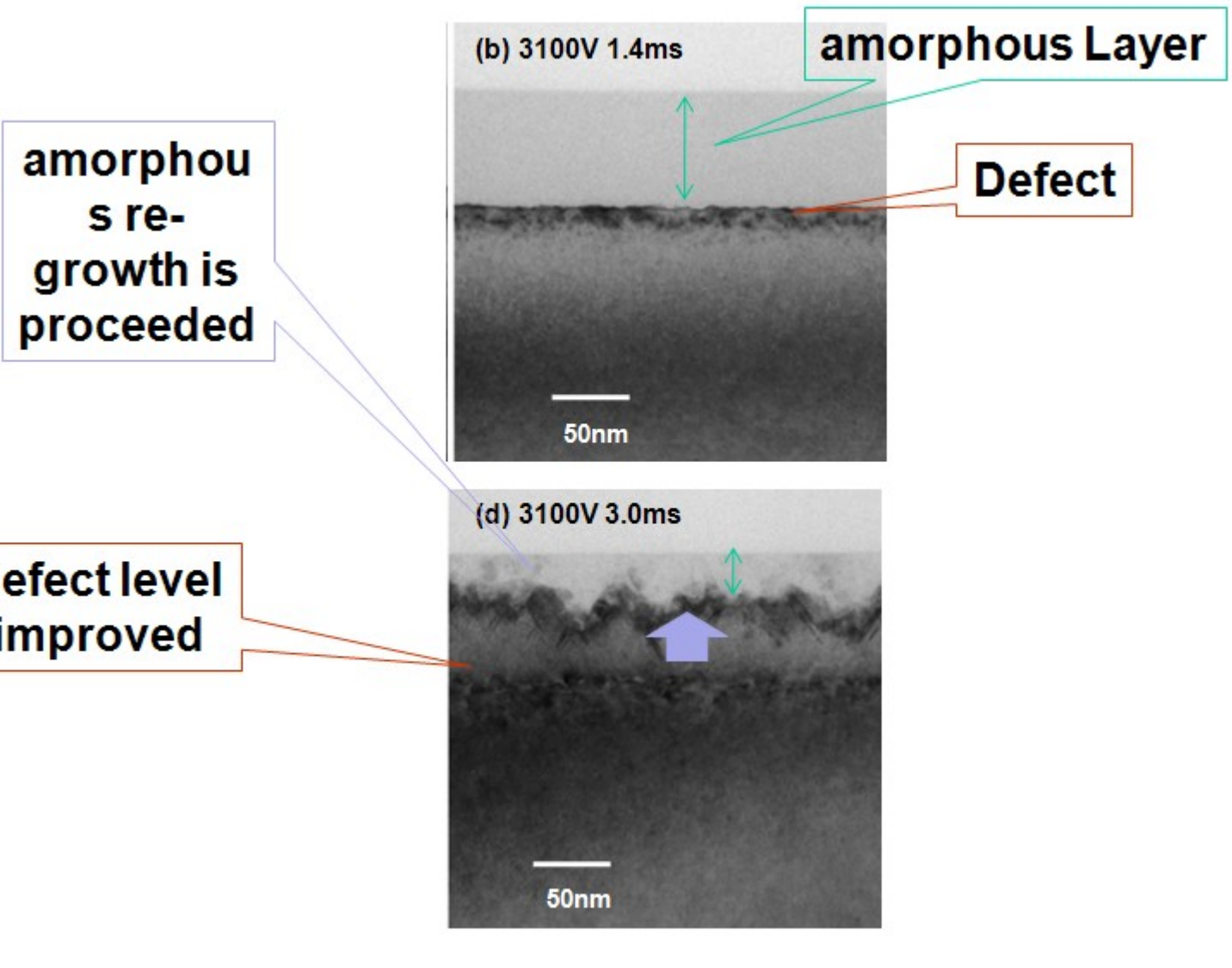
BF2 40KeV 5E15



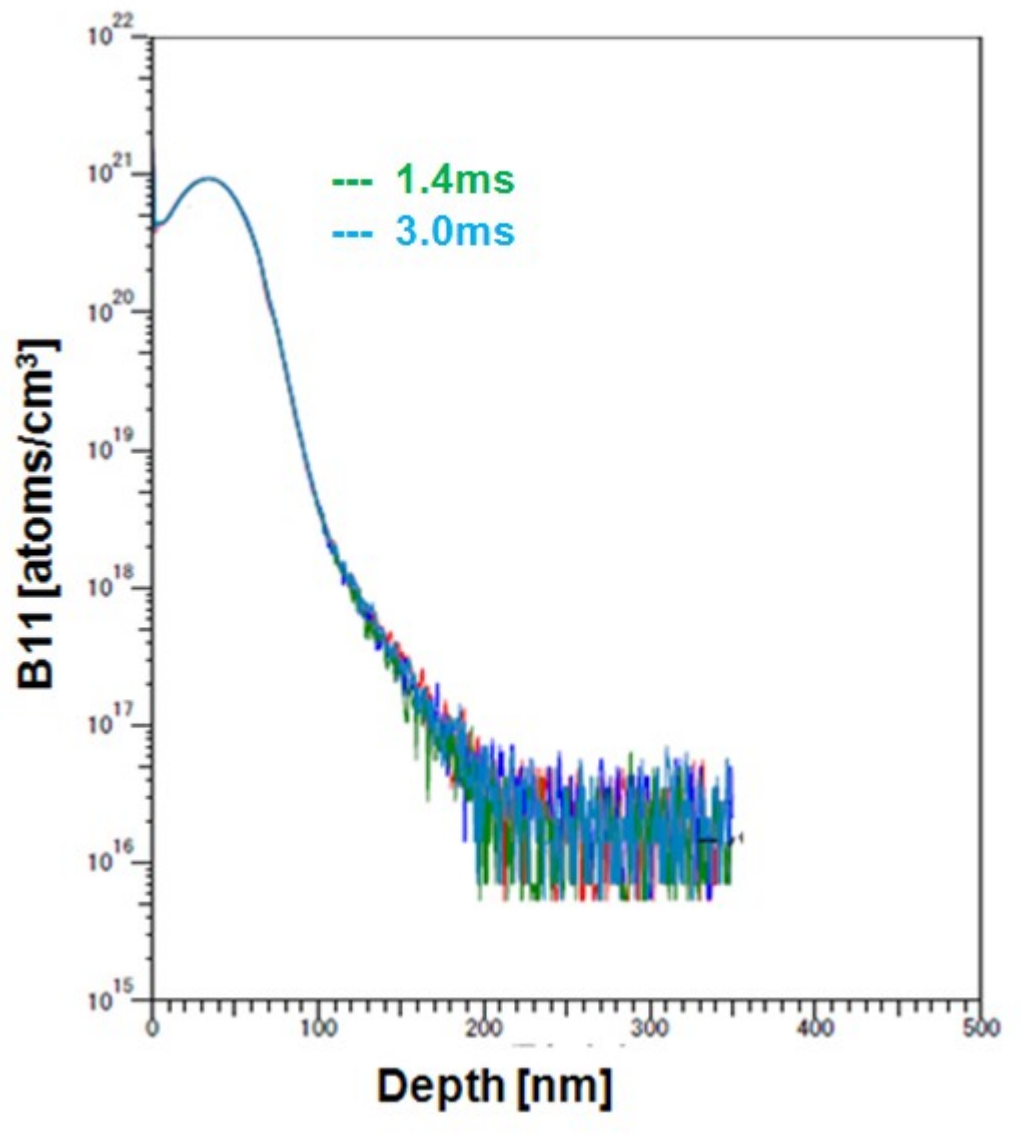
TW signal BF2 40KeV 5E15



X-TEM BF2 40KeV 5E15



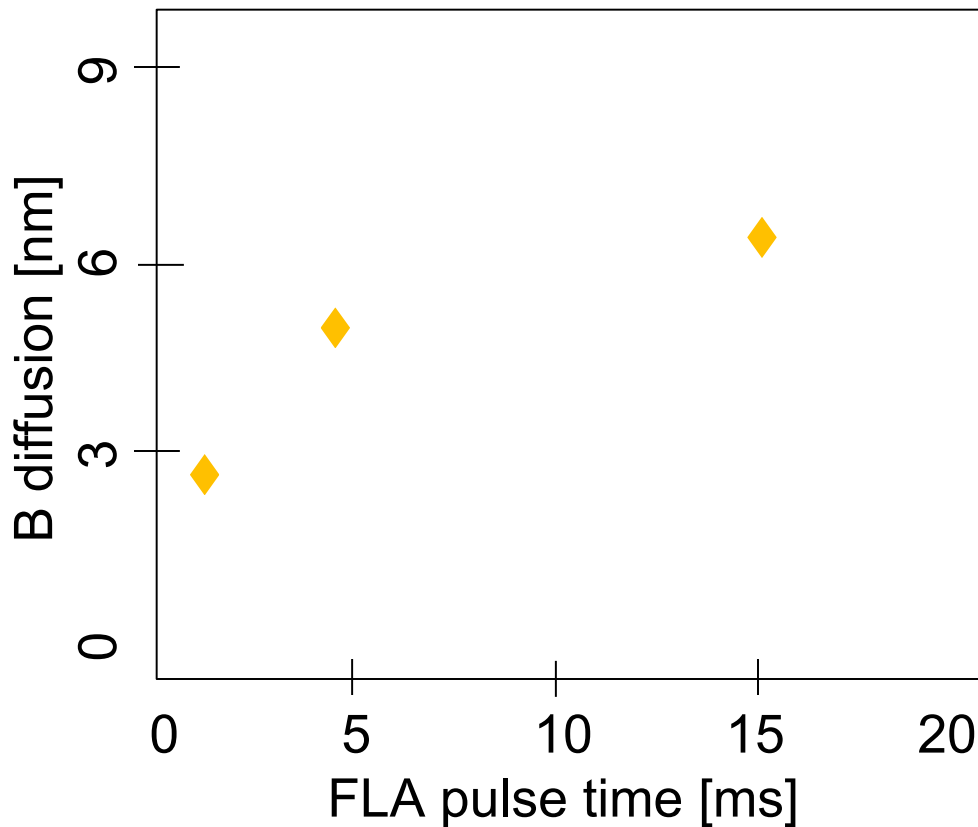
SIMS profile BF2 40KeV 5E15



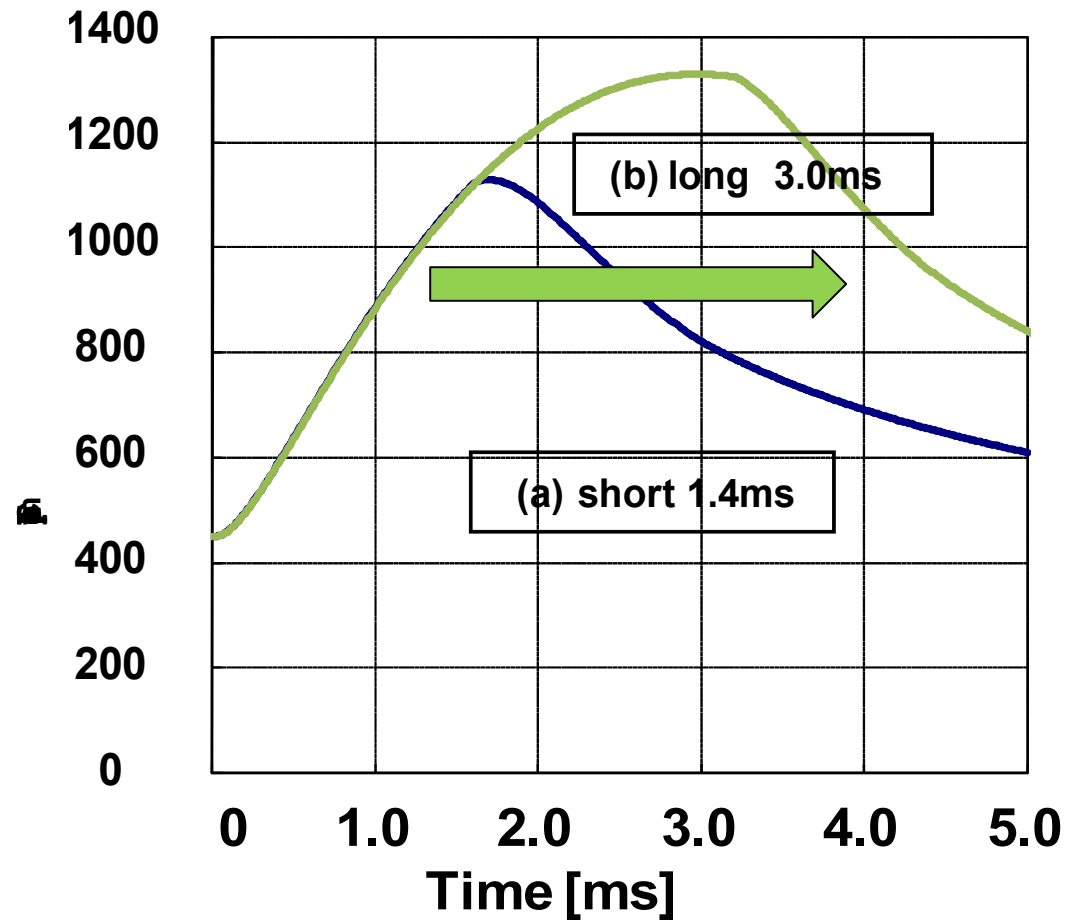
No diffusion observed

Longer pulse FLA

- ◆ Longer pulse FLA can improve defect recovery.
- ◆ Longer pulse (5ms <) B diffuse 5-6nm



Surface Temperature Simulation



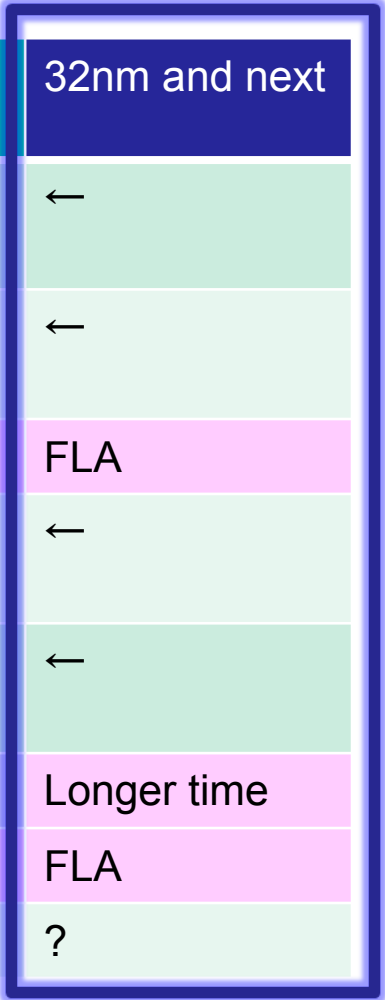
key issue for 32nm

- Our longer time FLA shows better EOR recovery like sRTA.
- Longer time FLA can be used as sRTA for 32nm High-K/Metal gate device.

FLA process flow example

For 32nm and future device, longer time FLA can enable process flow.

	65nm	45nm and next	45nm and next	32nm and next
gate formation	←	←	←	←
shallow, Halo implantation	←	←	←	←
annealing	not uses		FLA	FLA
spacer formation	←	←	←	←
deep S/D implantation	←	←	←	←
annealing	RTP	FLA	RTP low temp.	Longer time
	FLA	RTP low temp.	FLA	FLA
silicide	RTP	?	?	?

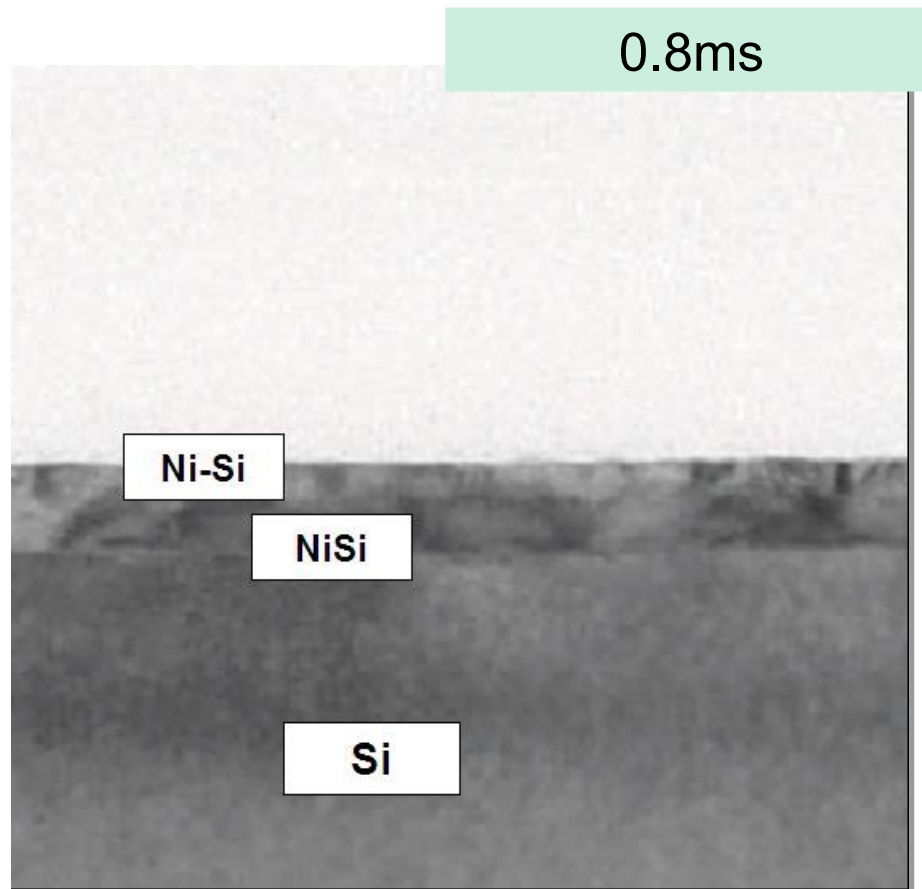


contents

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NiSi SEM Picture

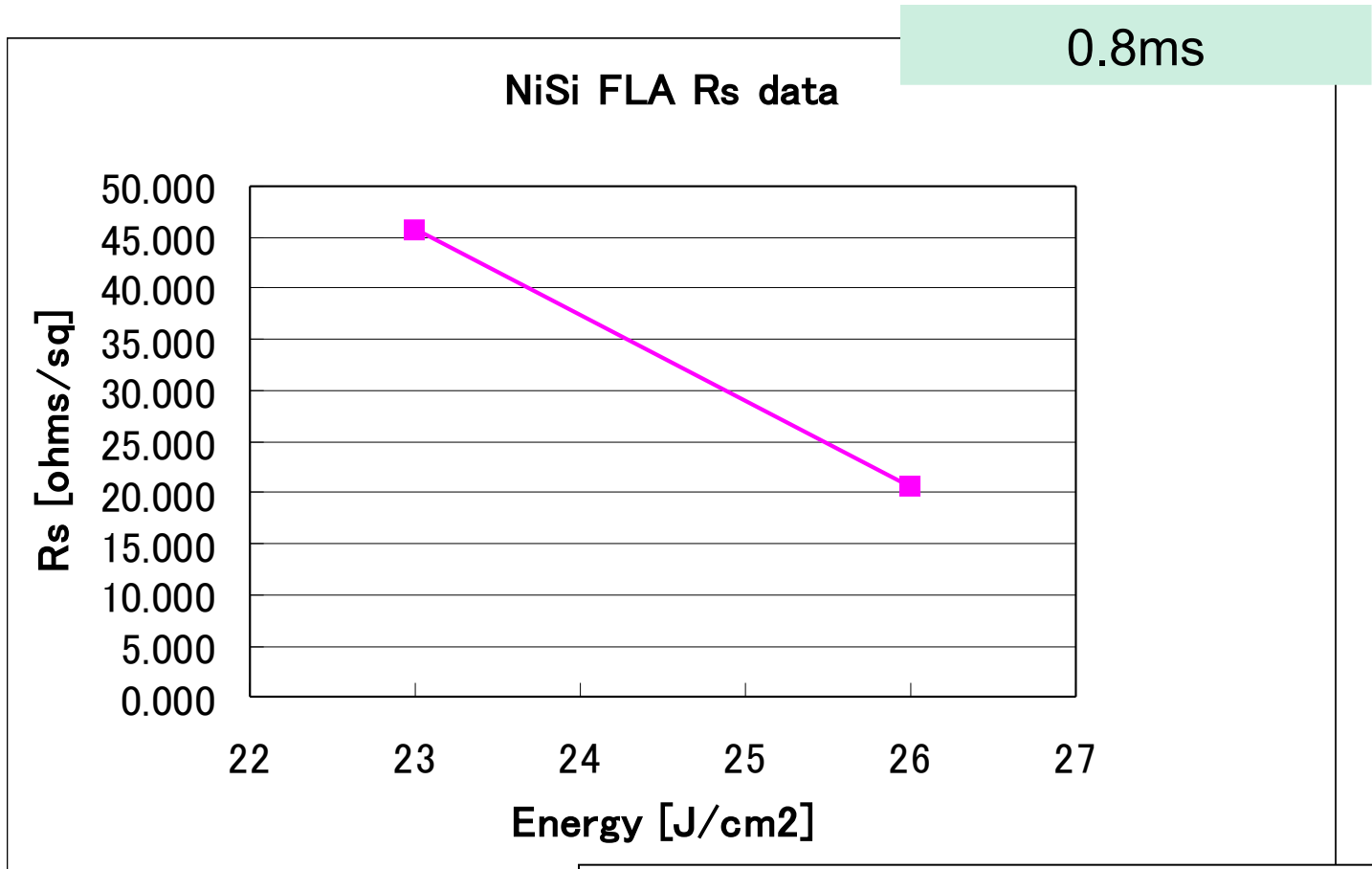
NiSi formation by FLA.
Surface Ni remain as Ni_xSi



ref : Kiyama , WC JTG 2007

Ni Silicide Rs Data

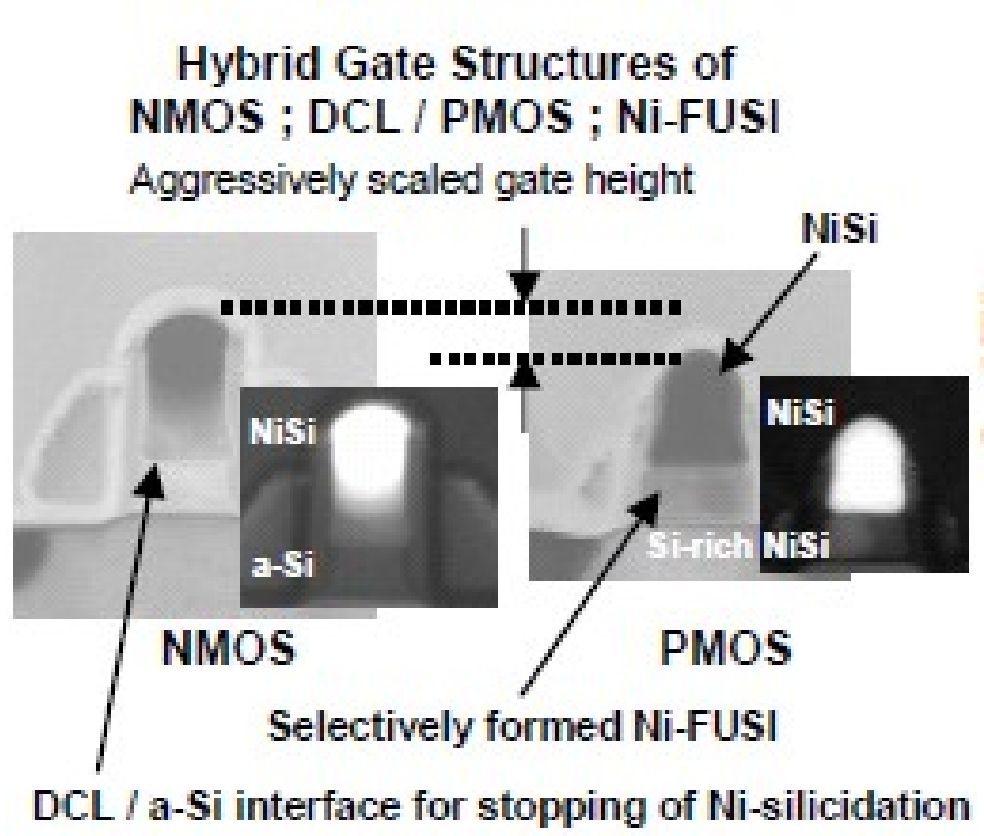
Higher flash power makes NiSi Rs go low.
 Surface Ni and Ni_xSi thickness decreases with higher flash power and NiSi thickness increases.



ref : Kiyama , WC JTG 2007

Application for FUSI gate

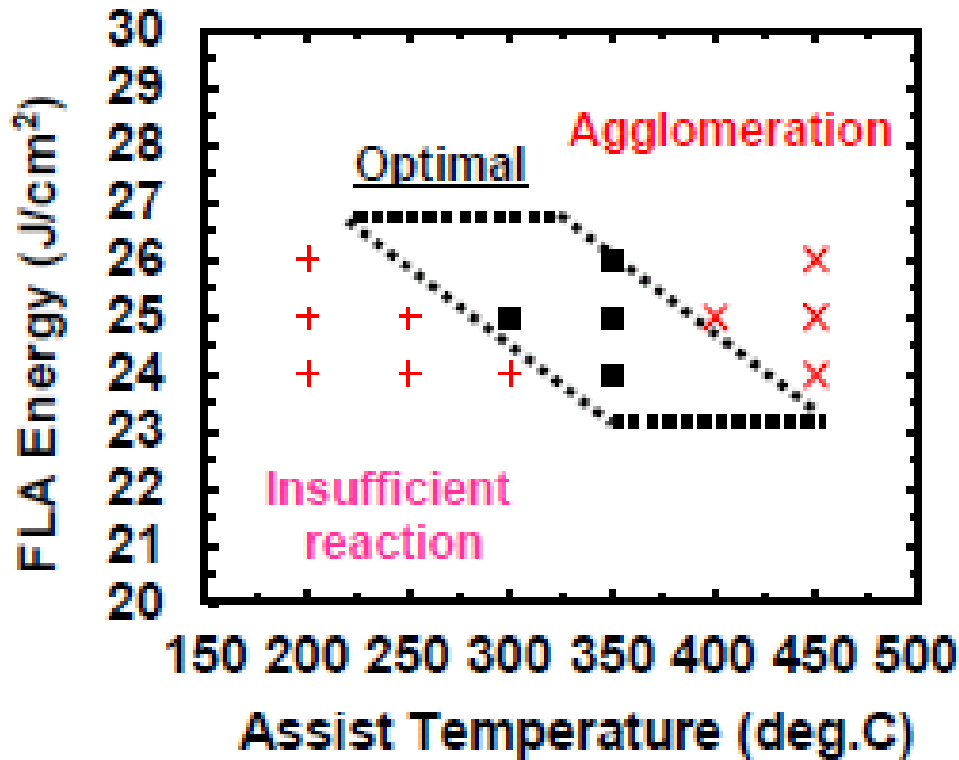
FLA is used for FUSI gate device.



ref : Ohta et. al., Fujitsu VLSI symposium 2008

Application for FUSI gate

Disclosed FLA process window is very wide.
FLA is conventional 0.8ms.



ref : Ohta et. al., Fujitsu VLSI symposium 2008

Application for FUSI gate

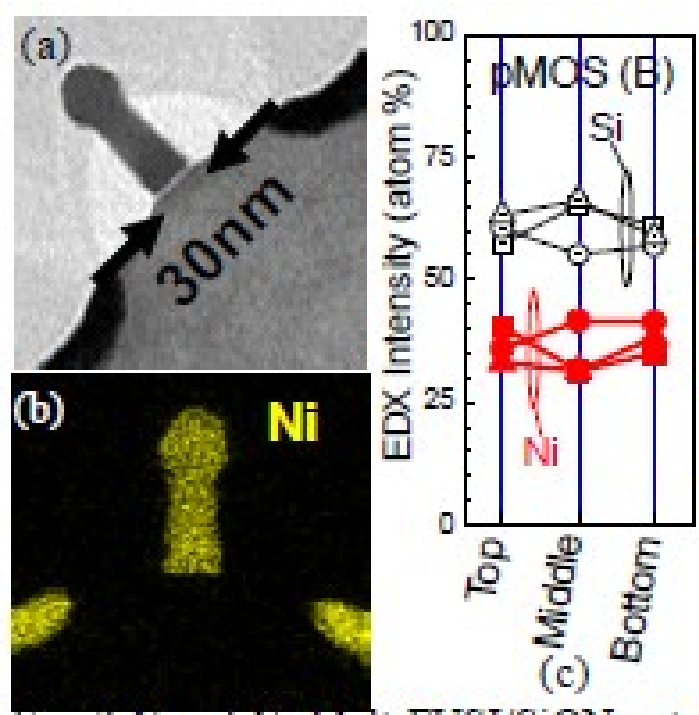
Process flow is very simple.
Same as conventional NiSi process.

- Ni deposition
- 1st Anneal
- Residual Ni removal
- 2nd Anneal **<= FLA**

ref : Fukutome et. al., Fujitsu VLSI symposium 2008

Application for FUSI gate

Using FLA, Si and Ni ratio has improved.
FLA is conventional 0.8ms.



Applying FLA for NiSi FUSI structure, Device performance dramatically improved (drive current , mobility)

ref : Fukutome et. al., Fujitsu VLSI symposium 2008

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Conclusions and Summary

- ◆ From the BF2 activation evaluation, we found millisecond time is effective for defect recovery and activation.
- ◆ Spike-RTA can be replaced by Longer time flash process.
- ◆ Longer time FLA can be used as a recovery annealing for High-K/Metal device.
This will enable no-diffusion process for 32nm device.
- ◆ Applying FLA for NiSi FUSI structure, device performance improved. FLA is a hopeful candidate for NiSi process.

LA-3000F Ecology Award

SCREEN

Flash Lamp Annealing system "LA-3000-F" has received a "Japan Machinery Federation Chairman's Award of Ecological System" for its low electrical power requirement.

La-3000-F has received the "Japan Machinery Federation Chairman's Award of Ecological System" at "28th excellent ecological system recognition"

This award is defined under strict assessment of initiative originality, promotion of energy efficiency, ecology, record and popularity, safety, low impact for environment.