Laser Spike Annealing for 32nm and beyond

Jeff Hebb, Yun Wang, and David Owen
Ultratech, Inc.

July 17, 2008

Outline

- Introduction to LSA

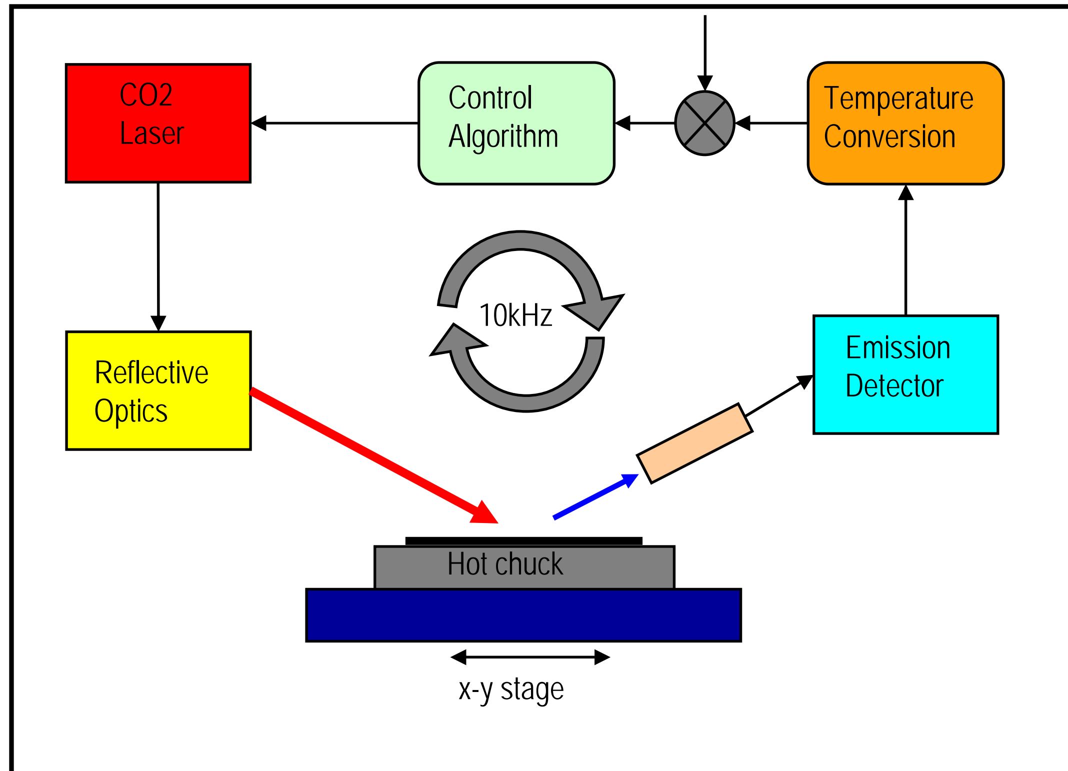
- LSA extendibility:
  - LSA Integration schemes
  - Compatibility with stress techniques
  - High k / Metal Gate
  - Advanced transistor architectures

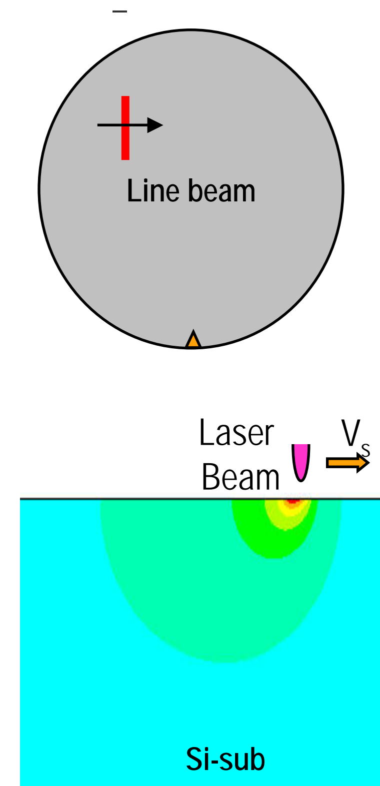
Outline

- Introduction to LSA

- LSA extendibility:
    - LSA Integration schemes
    - Compatibility with stress techniques
    - High k / Metal Gate
    - Advanced transistor architectures

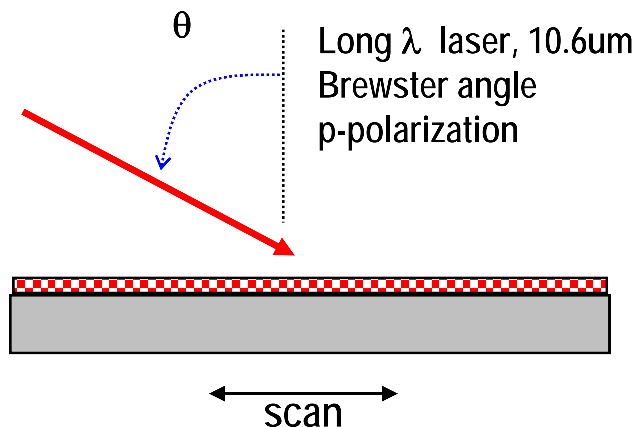
LSA Theory of Operation



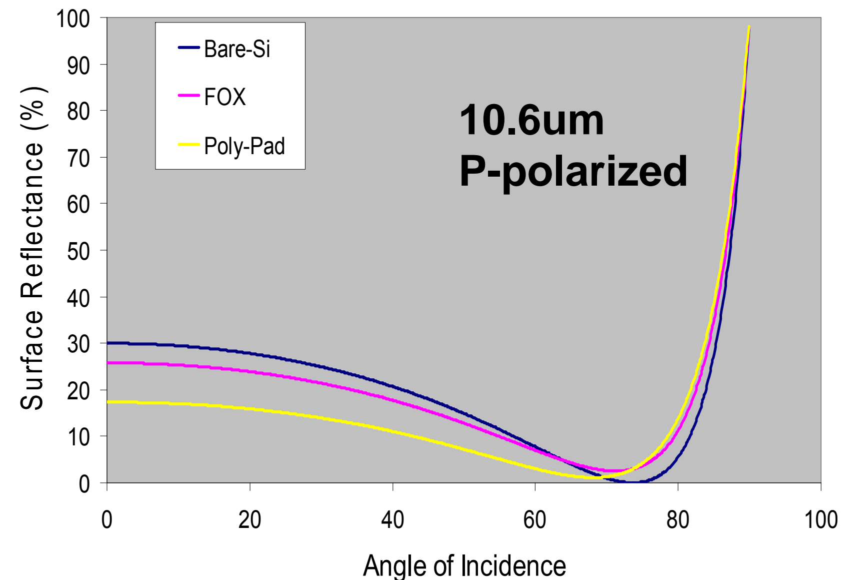


- **Long wavelength, p-polarized "line beam" incident on wafer at Brewster's angle to minimize pattern effects**
- **Wafer scanned under the beam, stage speed determines dwell time**
- **Real-time peak temperature measurement in feedback loop to laser.**

Suppression of Pattern Effects using LSA



LSA Heating Scheme

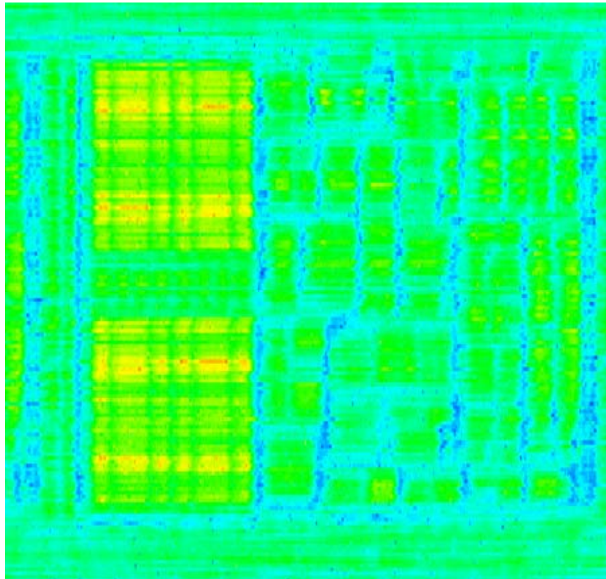


Reflectance vs. Angle of Incidence

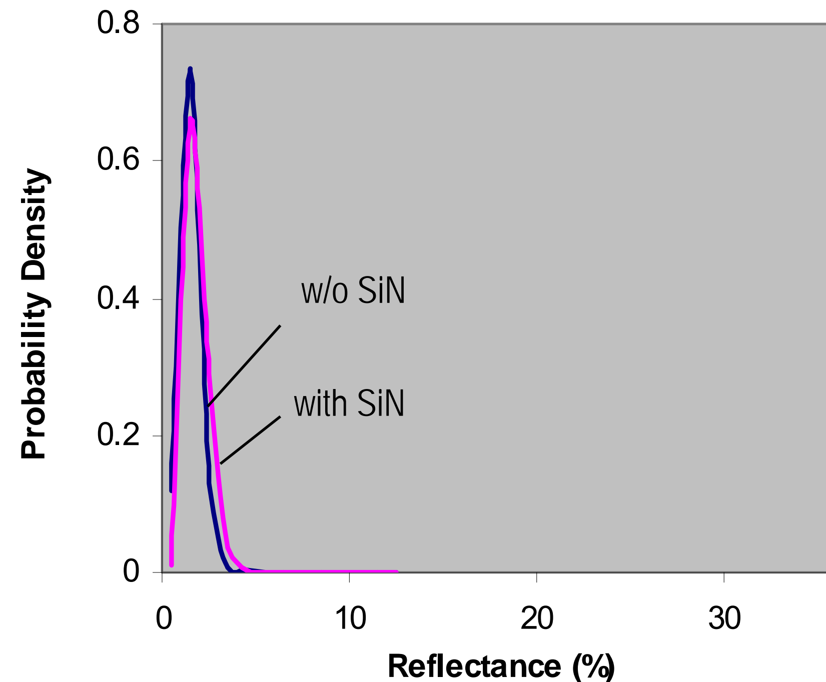
- Long wavelength: 10.6 um >> length scale of devices and films (100nm)
- P-polarization and Brewster angle make cross-die absorptivity uniform to ~ 1%

Measured Reflectance of Real Die

Measured reflectance of real die at 1300C



Probability density of measured Reflectance



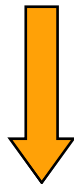
- Measurements confirm suppression of pattern effects for LSA.
- Allows LSA to achieve higher peak temperatures → increased device gain

LSA Benefits on IBM SOI Technology

"High Performance 65nm SOI Transistors Using Laser Spike Annealing"
(IBM SOI Alliance, published Sept 2006)

- **Ion/Ioff improvements:**
  - **10% NMOS**
  - **5% PMOS**

- **Improved within Die Ring Oscillator Delay uniformity**



Yield Enhancement

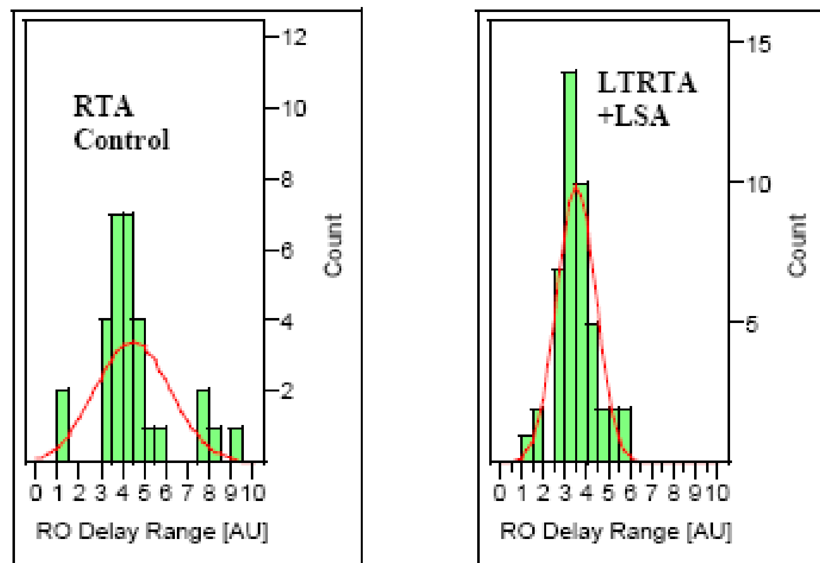
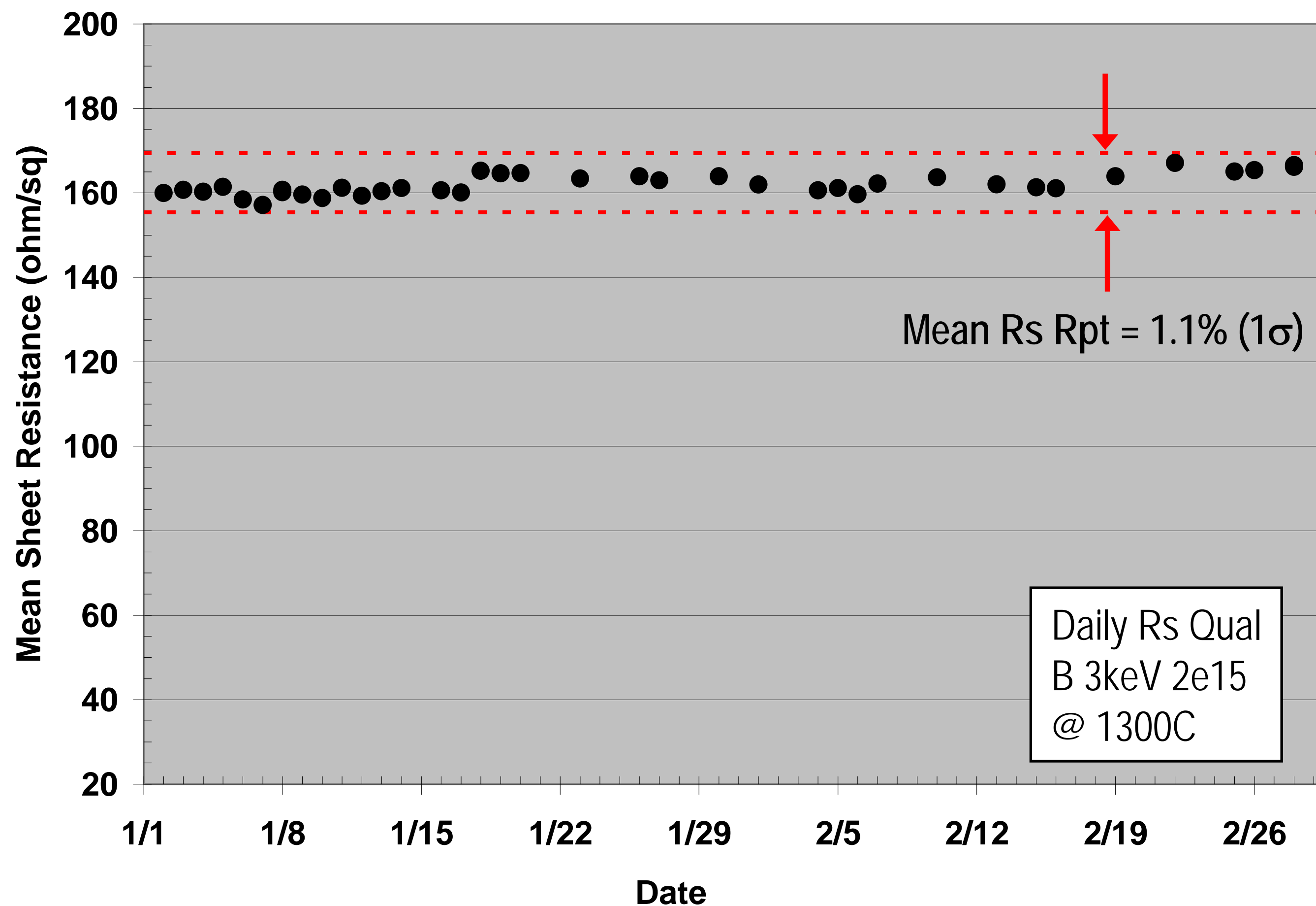


Fig.12 Cross-die RO delay range distributions as scaled percentage of delay value for RTA reference (left) and LTRTA+LSA(right).

Yamashita et al, presented at ESSDERC, Sept 2006

Ultratech

Field Data: Customer A Daily Rs Qual Repeatability

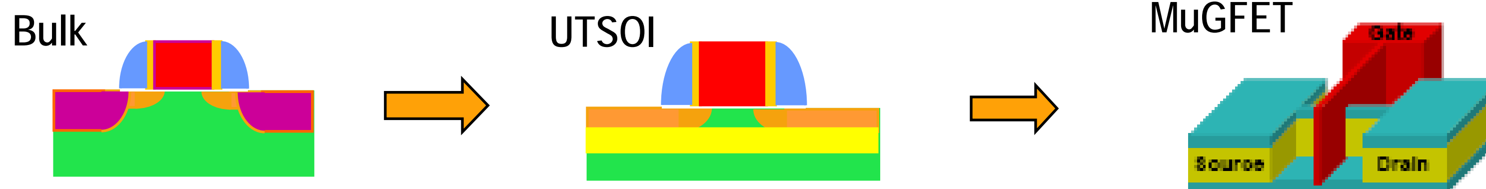


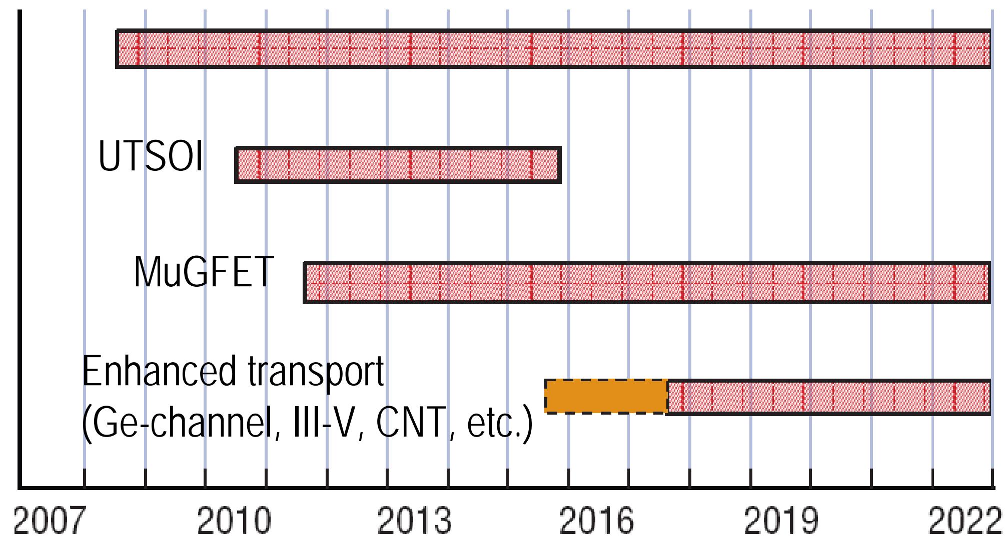
Rs stability ~ 1% (1σ) in high volume production

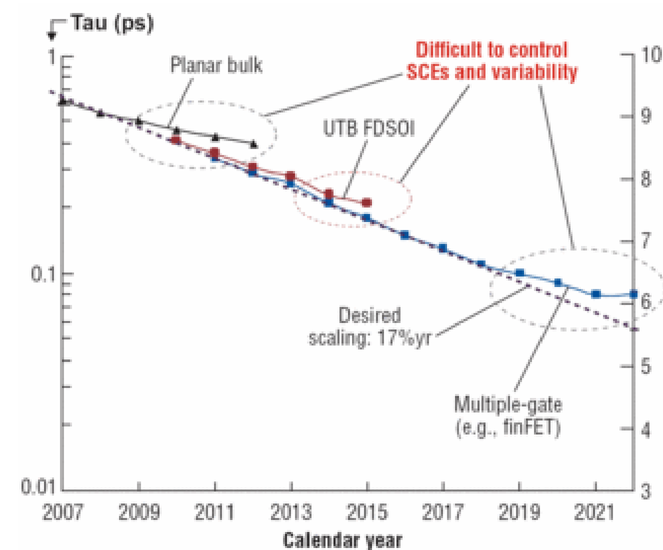
Outline

- Introduction to LSA
- LSA extendibility:
    - LSA Integration schemes
    - Compatibility with stress techniques
    - High k / Metal Gate
    - Advanced transistor architectures

2007 ITRS Update: Device Roadmap







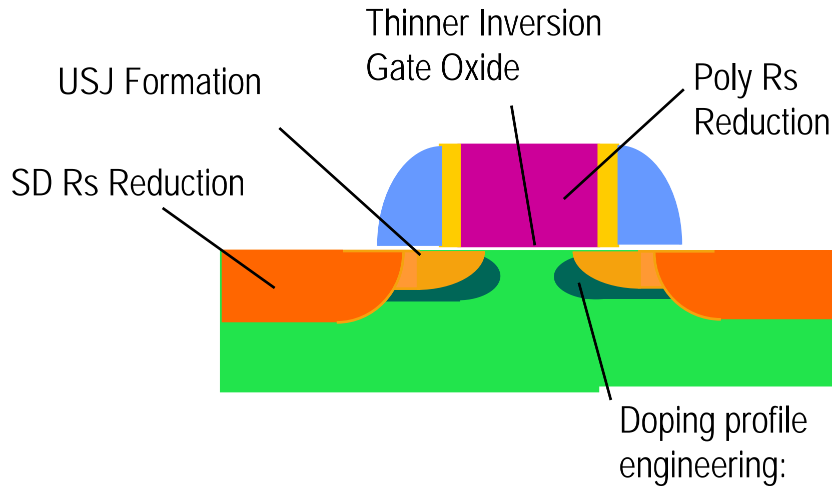
*Source: P..M. Zeitzoff, *Solid State Tech.*, 51(2), p. 35, 2008.

Outline

- Introduction to LSA
- LSA extendibility:
  - LSA Integration schemes
  - Compatibility with stress techniques
  - High k / Metal Gate
  - Advanced transistor architectures

Integration Schemes

Laser Spike Annealing for USJ Formation



- Thinner Tox_inv due to reduced poly depletion
- Improved Id due to reduced series resistance
- Reduced SCE due to ultra-shallow junction

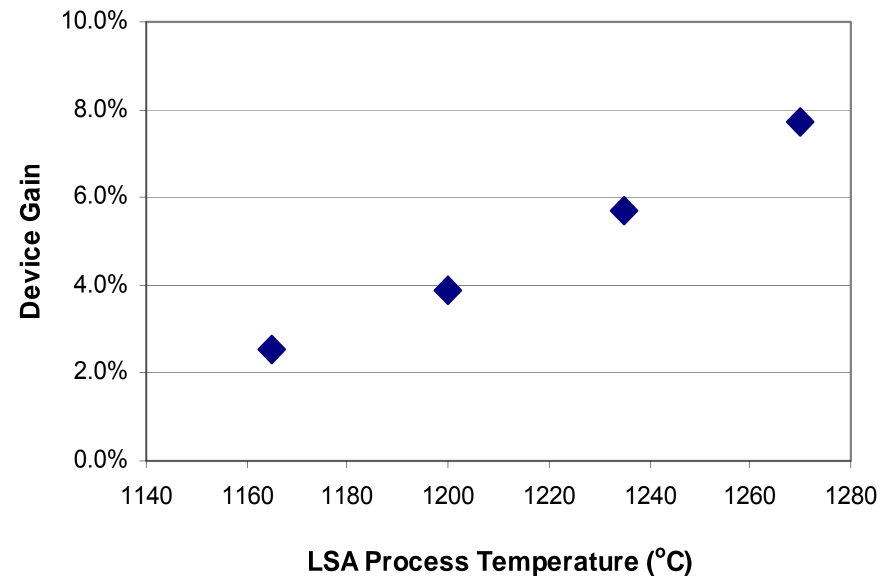
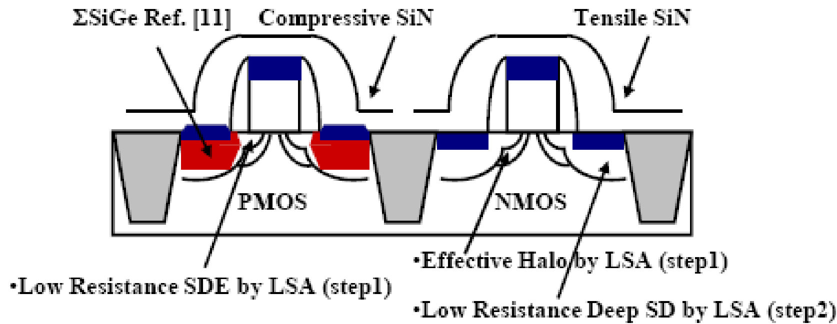


Fig. 1: NMOS drive current gain over the RTA baseline vs. LSA process temperature. (Chen et al., RTP2007)

Increase drive current for HP & reduce leakage for LP

Two Step LSA For HP45nm (Fujitsu, IEDM'07)



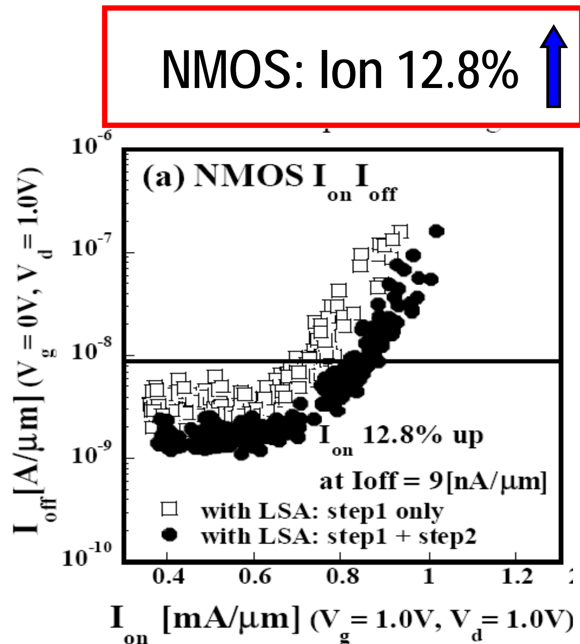
Process Sequence of This Work

- SDE & Halo Implant with Co-implant
- LSA (step1): optimum
- Sidewall Formation
- ΣSiGe Formation (PMOS)
- Deep SD Implant
- LSA (step2): optimum
- Spike RTA
- Silicidation

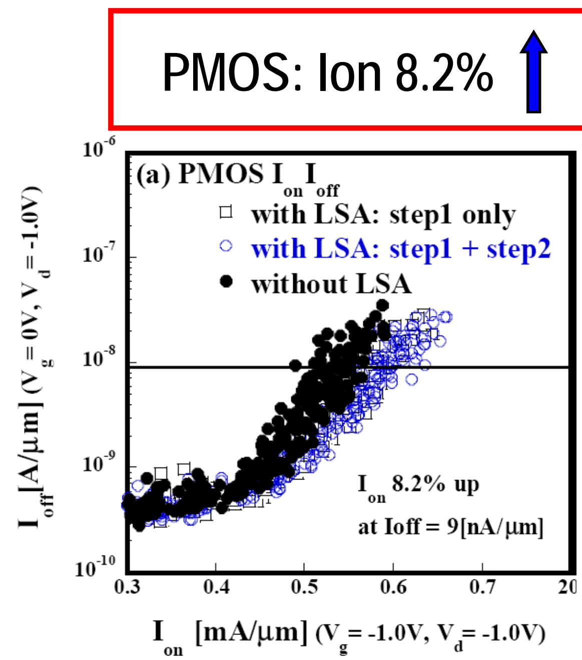
LSA1: after SDE and halo implant w/ F co-implant)

LSA2: after deep SD implant before spike-RTA.

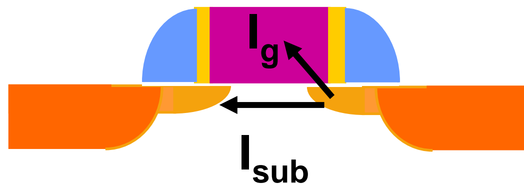
NMOS: Ion 12.8% ↑

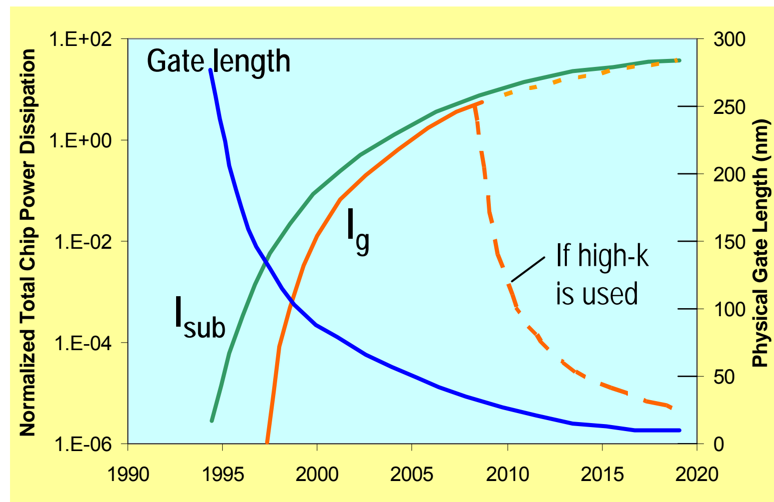


PMOS: Ion 8.2% ↑

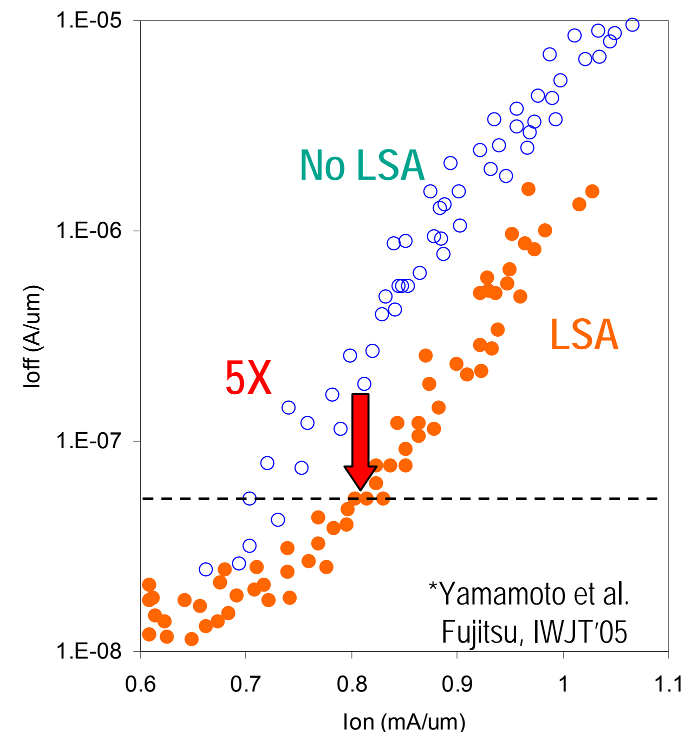


LSA For Leakage Reduction



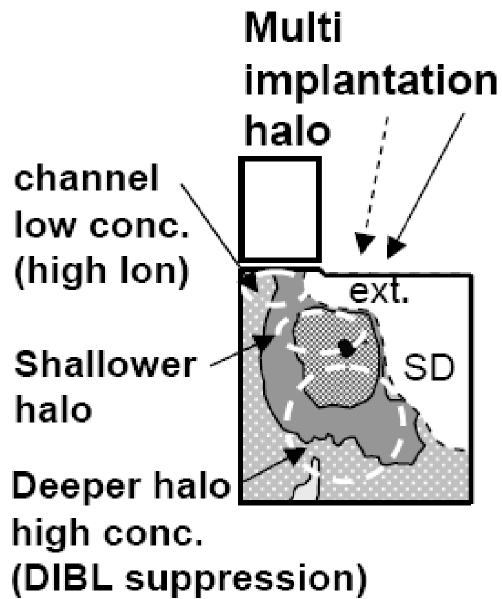


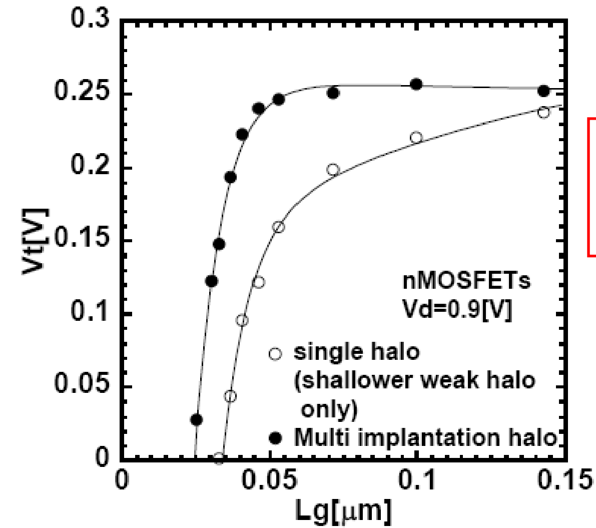
Gate leakage can be reduced by high-k, but subthreshold leakage control still needs shallow junction formed by LSA.



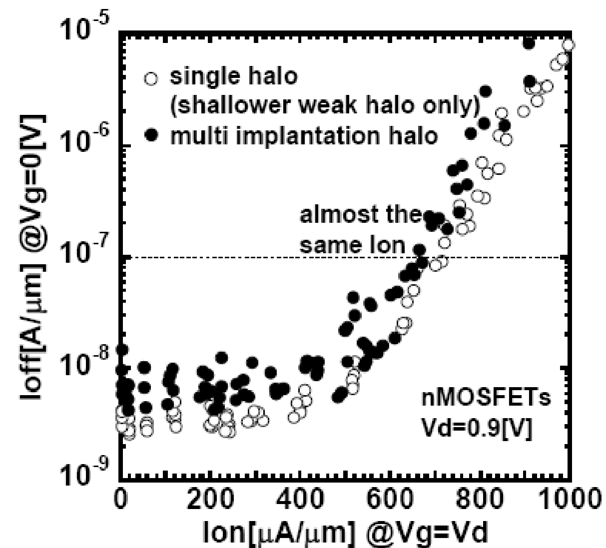
LSA is applicable to high performance as well as low power devices.

"LSA-only" (Diffusionless) Integration for Sub-30nm*





Improved Vt Roll-off



Same Ion / Ioff

Use of multiple halos enables LSA-only integration scheme

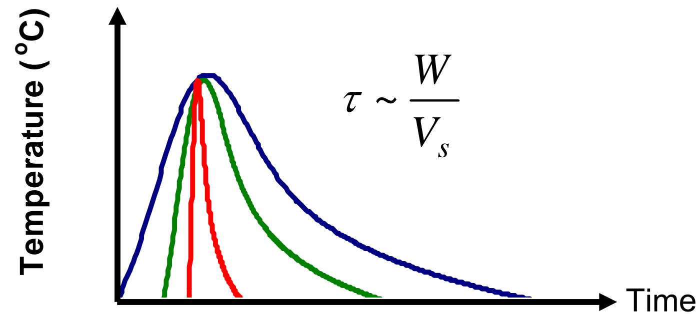
* Narihiro et. al (NEC), VLSI2008

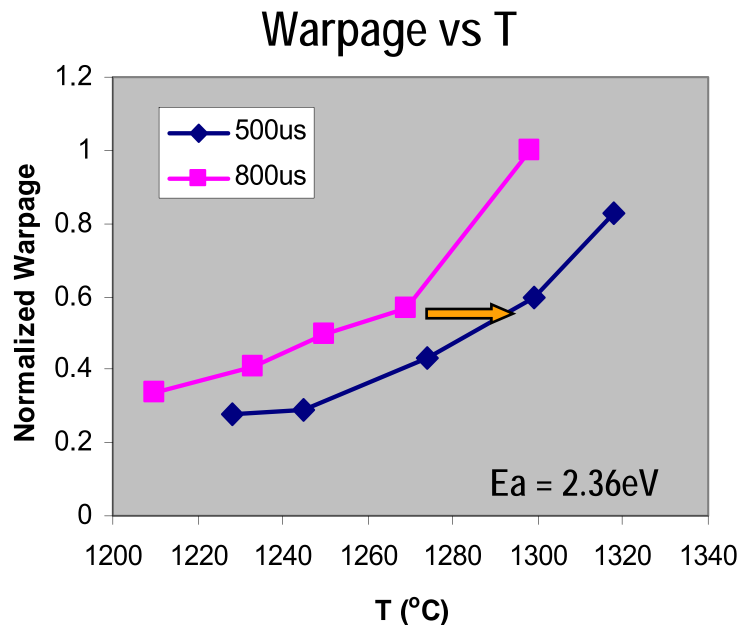
Outline

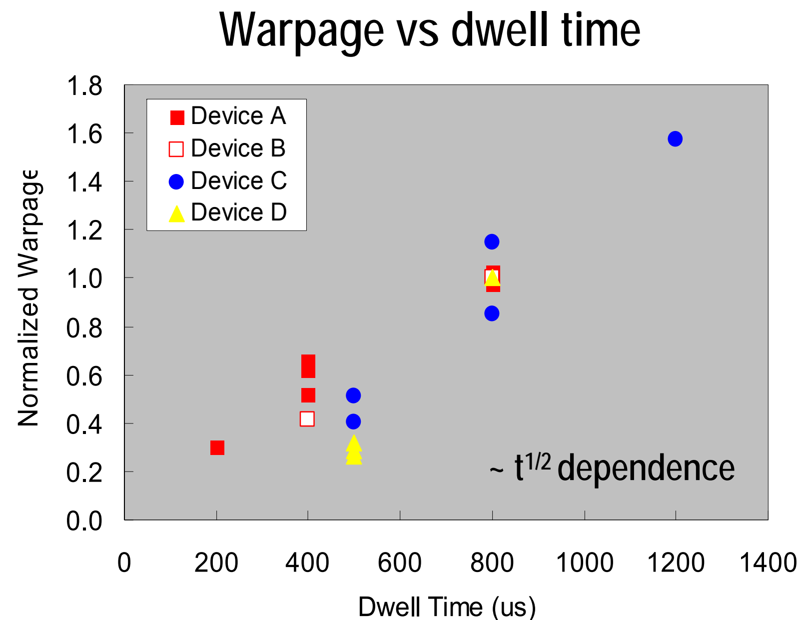
- Introduction to LSA

- LSA extendibility:
  - LSA Integration schemes
  - Compatibility with stress techniques
  - High k / Metal Gate
  - Advanced transistor architectures

Warpage Reduction By Short Dwell Time



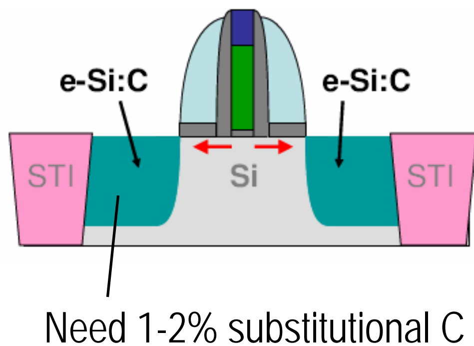




Reducing dwell time allows higher temperatures → Device performance gain

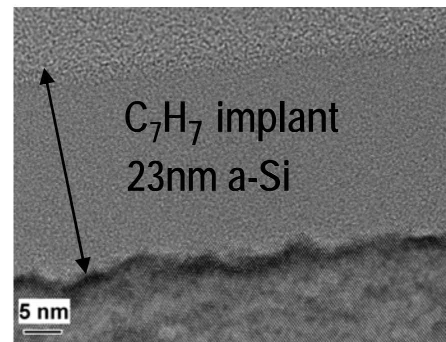
LSA Regrowth of $Si_{1-x}C_x$ For Tensile Strain

(a) NMOS with e-Si:C



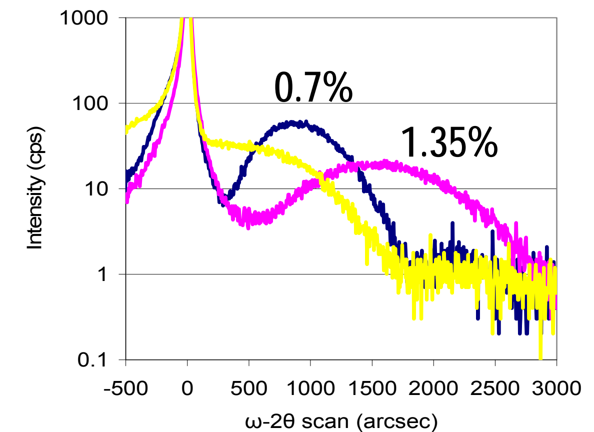
Need 1-2% substitutional C

(b) XTEM After C Implantation



*source: A.L. Fatou, ECS'07

(c) XRD After LSA



Implant Species	Substitutional Fraction (at%) (XRD)	Total Fraction (at%) (SIMS)
C_7H_7	0.7	0.7
$C_{14}H_{14}$	1.35	1.4

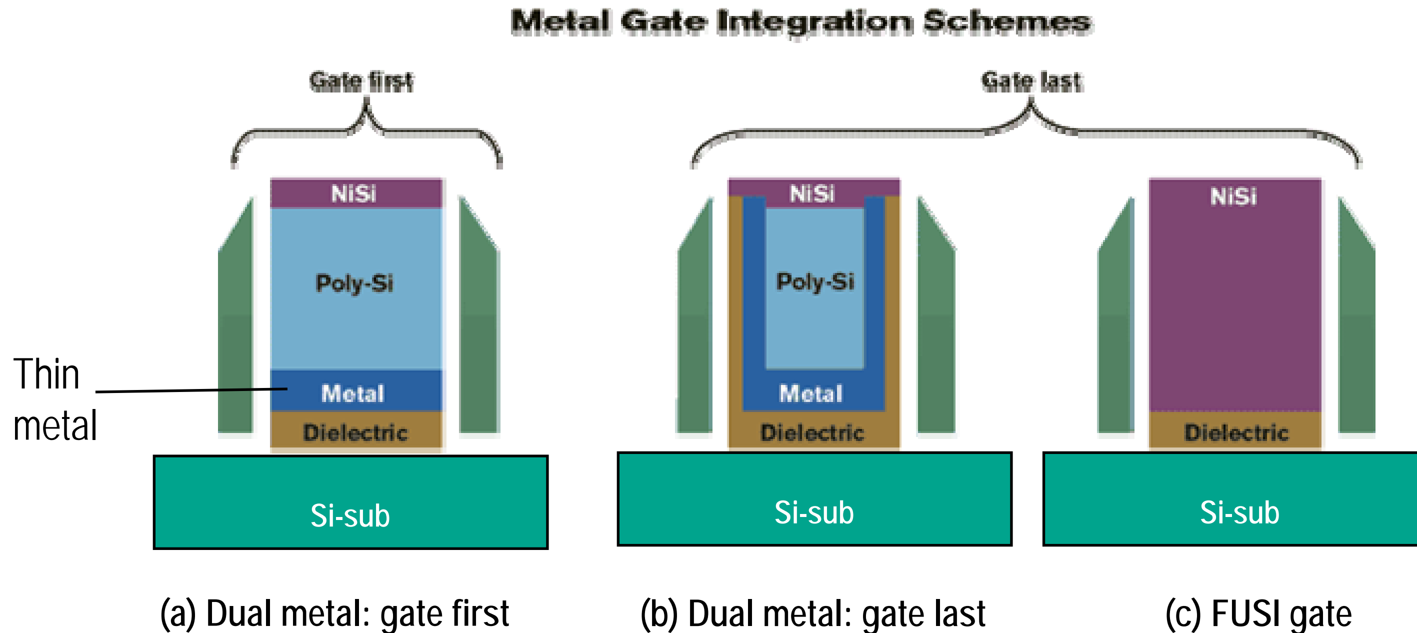
Almost 100% of carbon substitutionality can be achieved.

Outline

- Introduction to LSA
- LSA extendibility:
  - LSA Integration schemes
  - Compatibility with stress techniques
  - High k / Metal Gate
  - Advanced transistor architectures

Ultratech

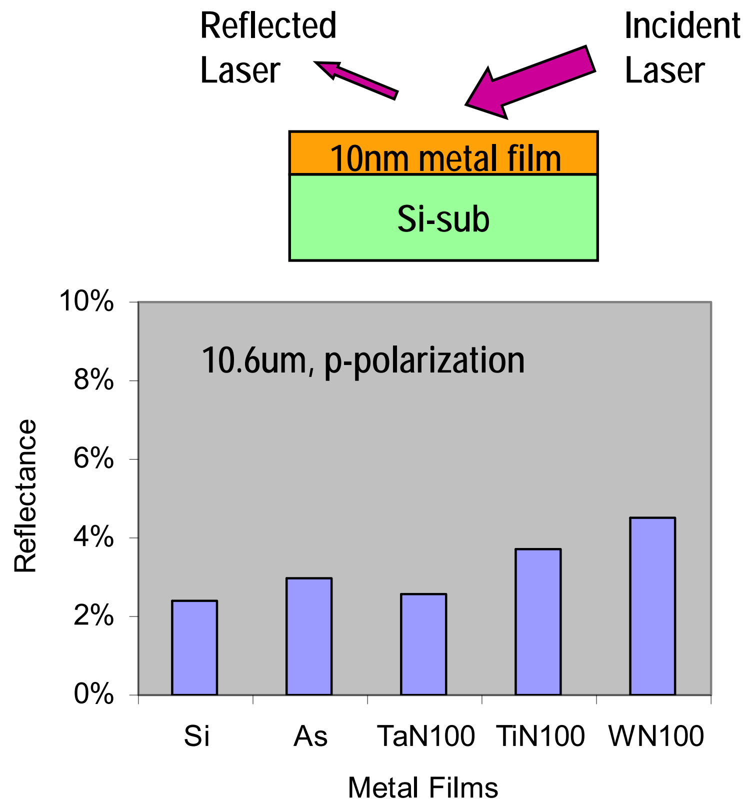
Compatibility of LSA with High-k/Metal Gate Process



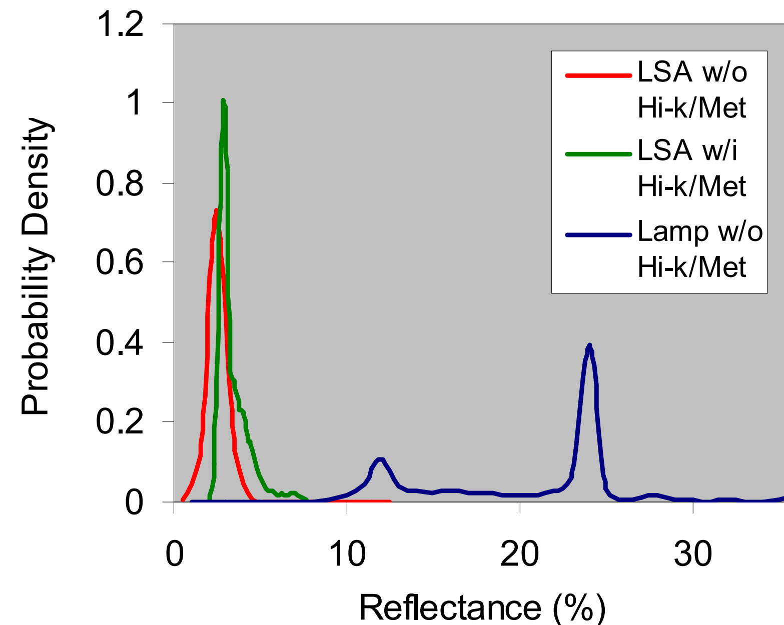
(a) Dual metal: gate first (b) Dual metal: gate last (c) FUSI gate

- **LSA compatible with "gate last" processes, as no metal present for LSA step**
- **For the gate first process, a thin layer of metal is placed under the normal poly gate. Typical metal thickness is ~10nm which is partially transparent at 10.6um. Reflectance will go up only by a small amount**

Pattern Suppression for High-k / Metal Gate



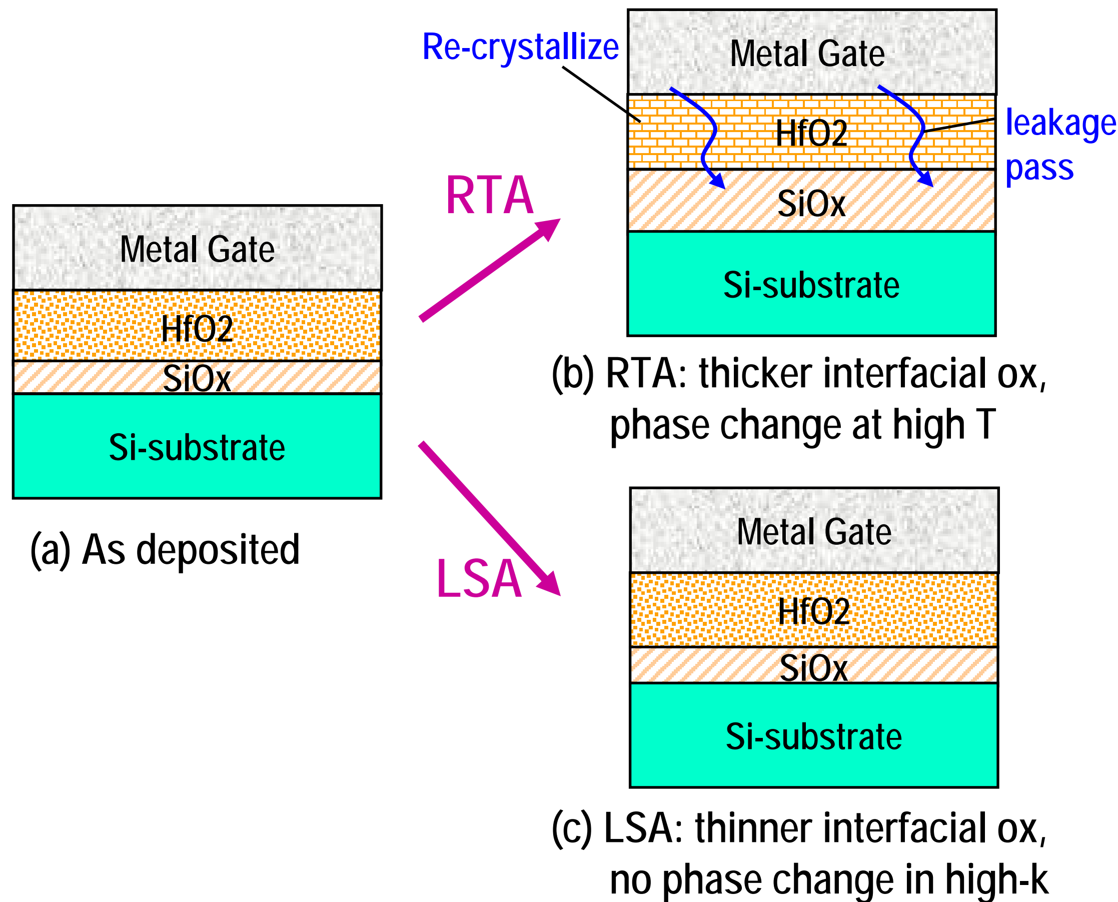
(a) Reflectance measured from various blanket metal films.



(b) Measured reflectance with and without metal gate

Pattern suppression is effective for high-k / metal gate

LSA For Metal Gate/High-k

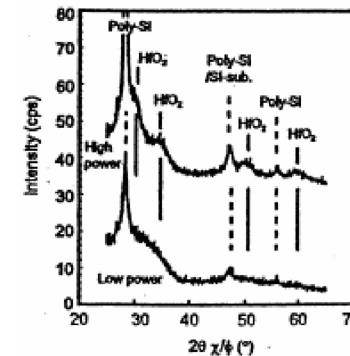


(a) As deposited

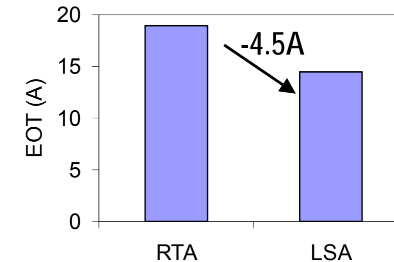
(b) RTA: thicker interfacial ox, phase change at high T

(c) LSA: thinner interfacial ox, no phase change in high-k

Published LSA Results



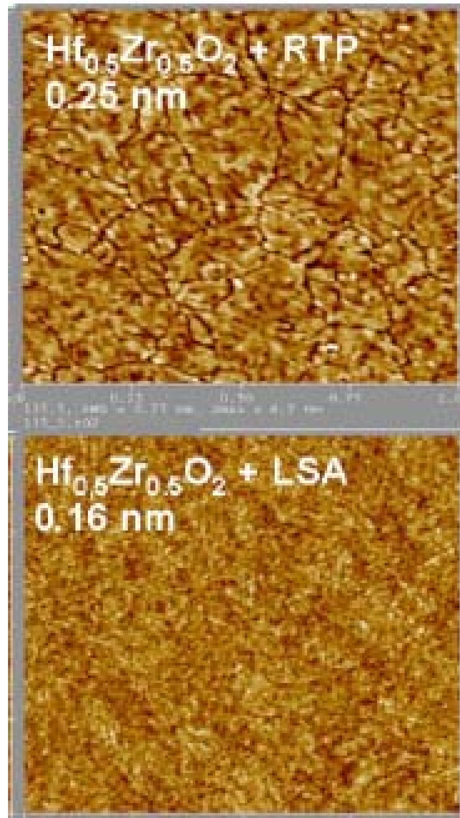
- Toshiba, VLSI, 2005
  No phase change ~1300°C



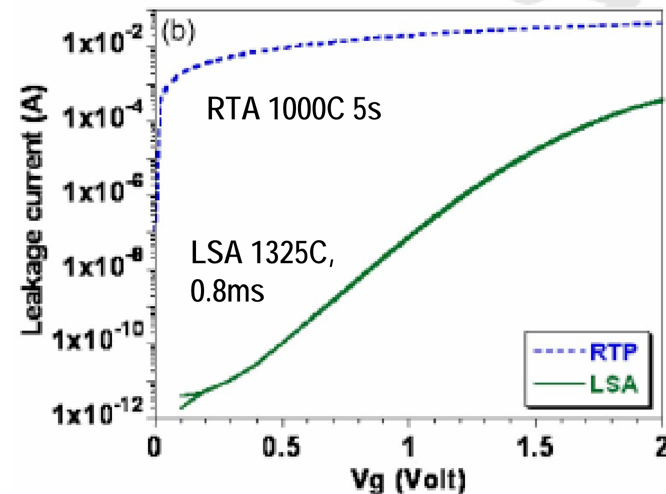
- Freescale, ESSDERC, 2006
  EOT reduction ~4.5A

LSA enables ultimate scaling of metal gate/high-k stacks.

High-k Morphology & Leakage Improvement



(a) AFM morphology



(b) Leakage characteristics

*source: D.H. Triyoso, to be published in APL

32nm LP With High-k/Metal Gate
(IBM Alliance, VLSI 2008)

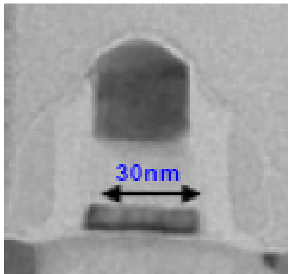


Fig.1: TEM of the Low power transistor with Lgate=30nm.

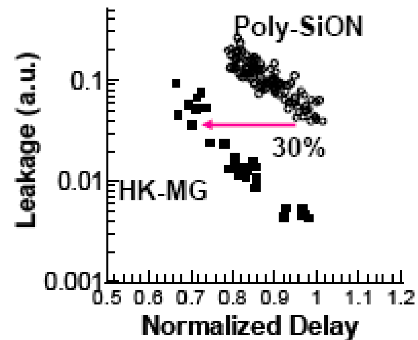
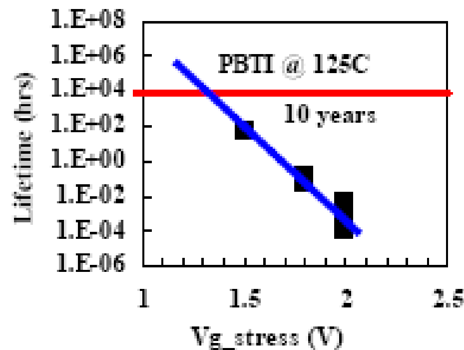
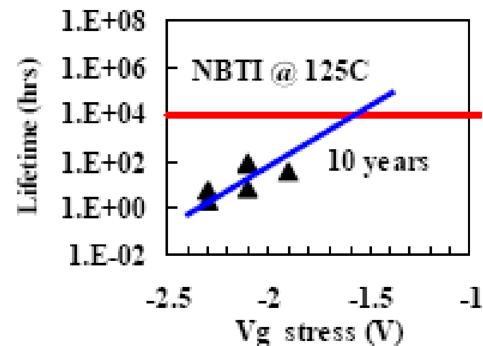


Fig.11: 30% RO delay reduction with HK-MG at same Vdd and leakage.





- Hf based high-k/single metal gate first process
- LSA used for USJ w/o negative impact on HK-MG
- Less than 3% total added cost with HK-MG

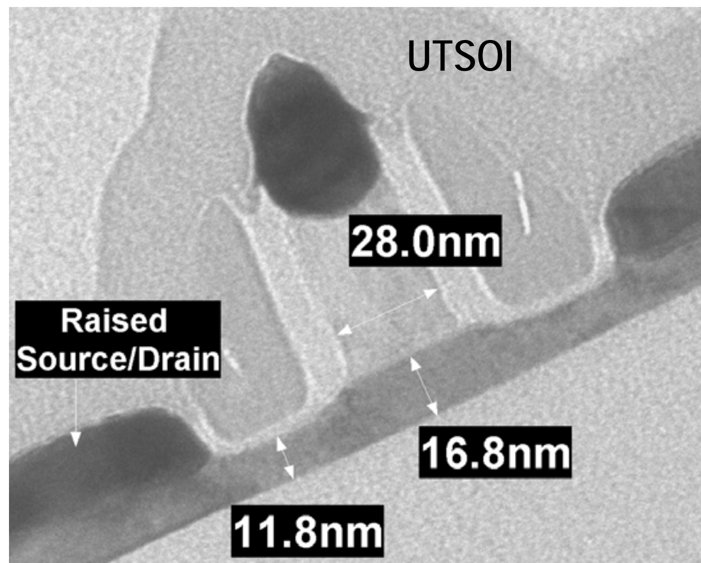
LSA compatible with HK-MG process at 32nm

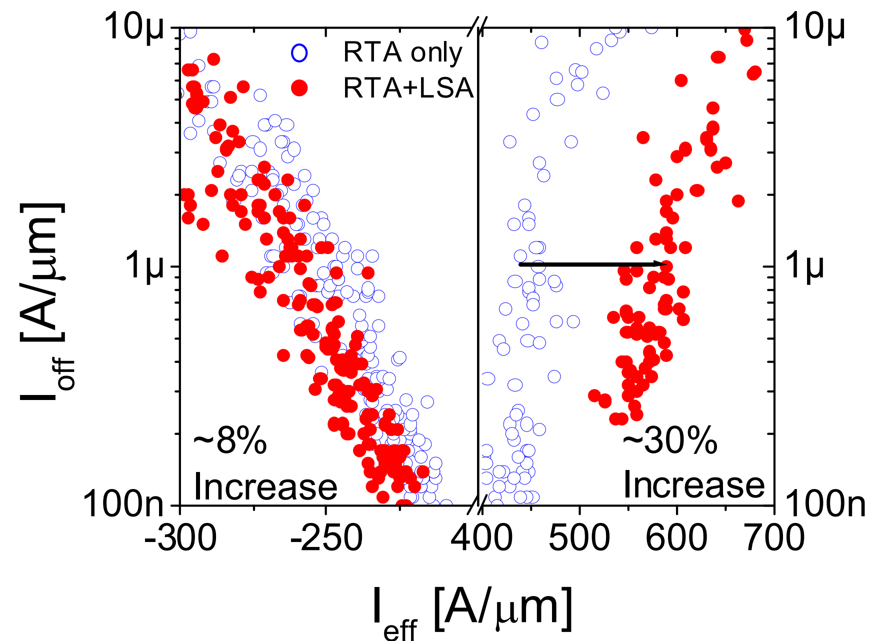
Outline

- Introduction to LSA
- LSA extendibility:
  - LSA Integration schemes
  - Compatibility with stress techniques
  - High k / Metal Gate
  - Advanced transistor architectures

LSA Application To UTSOI

IBM Alliance, VLSI-TSA 2006

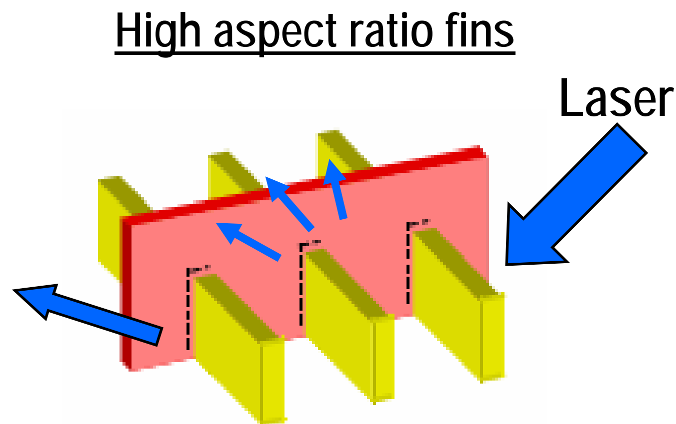




LSA gives 30% enhancement in Ieff & 10% improvement in RO speed for UTSOI

Compatibility With Non-Planar Structures

High aspect ratio fins

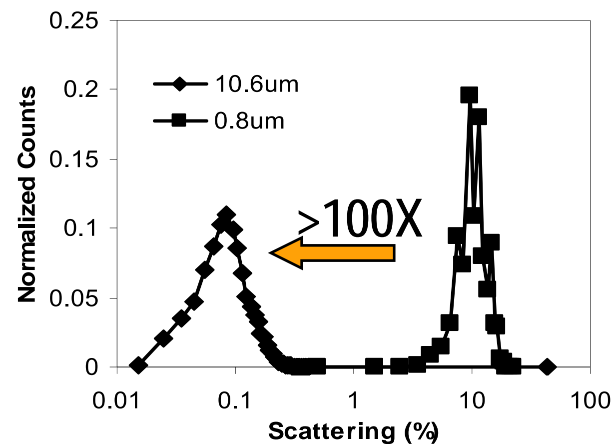


Total Integrated Scattering:

$$TIS = \frac{P_s}{RP_i} \approx \left(\frac{4\pi\sigma}{\lambda}\right)^2$$

σ is rms surface roughness

- Thin Si fin is transparent to CO2 wavelength, no shadowing effects
- Height is still << 10.6um, so scattering is minimal for LSA



- Long wavelength reduces total amount of scattering

Summary

- LSA tool design has unique advantages for extendibility to 32nm and beyond:
  - Long wavelength heating approach suppresses pattern effects, and enables high peak temperatures
  - Real time temperature control critical for manufacturing environment
- LSA has been demonstrated for multiple anneal schemes and LSA-only integration
- Low dwell time capability critical for integration of SiGe, especially for increasing Ge concentrations.
- LSA demonstrated to be compatible with high-k / metal gate