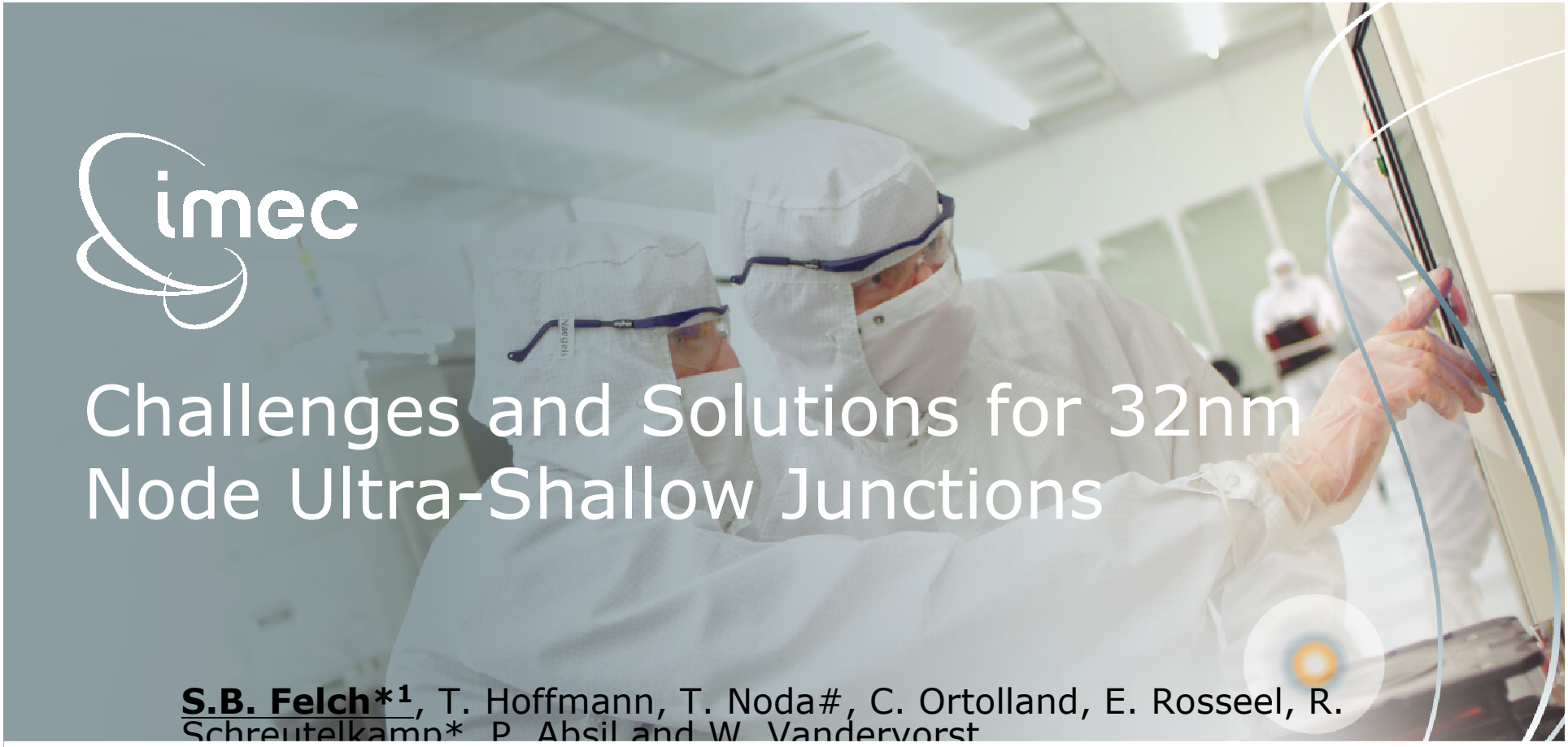


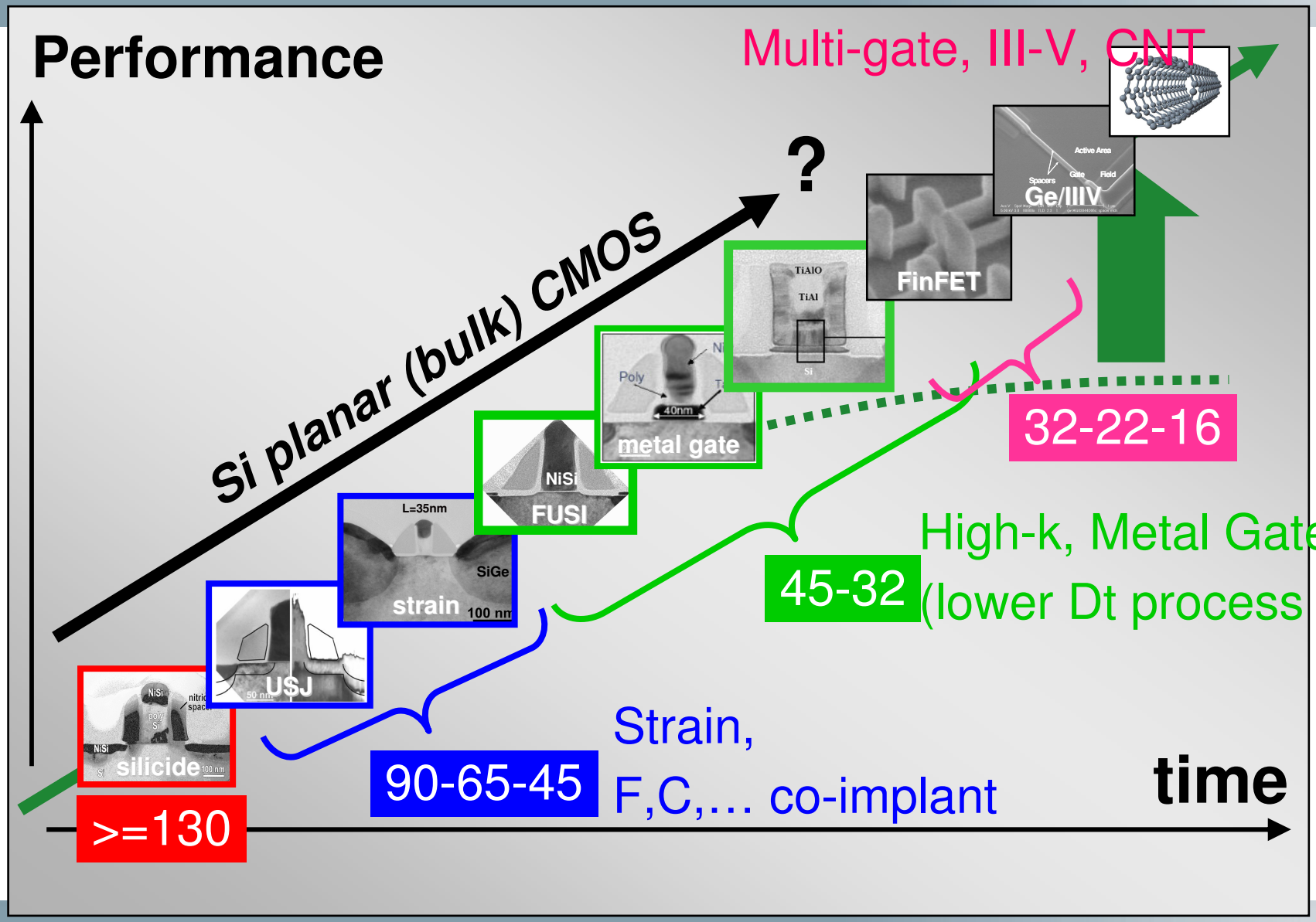
Challenges and Solutions for 32nm Node Ultra-Shallow Junctions

S.B. Felch*[1], T. Hoffmann, T. Noda#, C. Ortolland, E. Rosseel, R. Schreutelkamp*, P. Absil and W. Vandervorst

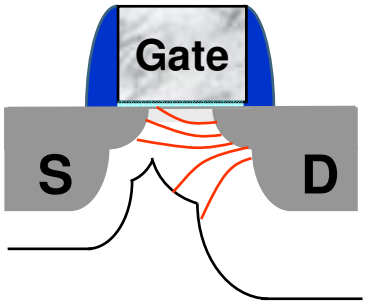
Outline

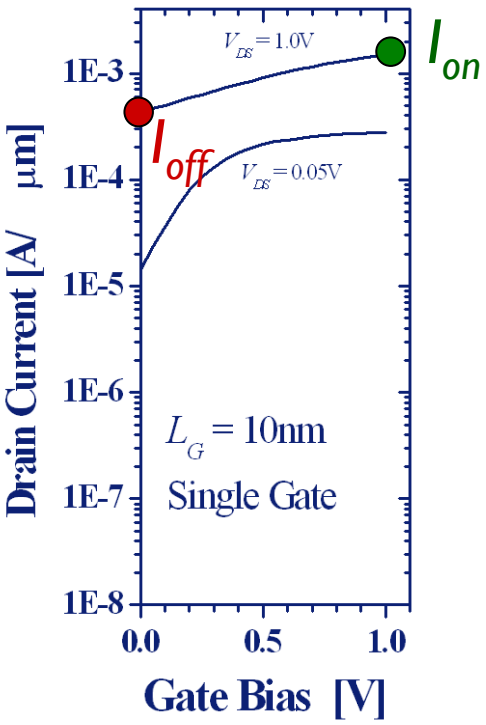
- Different paths for scaling & implications for USJ
- From low dopant diffusion with **co-implantation** …
- … to diffusion-less with **milli-second annealing**
- Summary

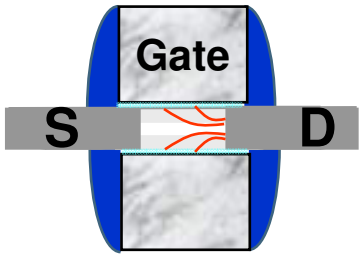
Device level : Scaling ⇔ SCE control !!!

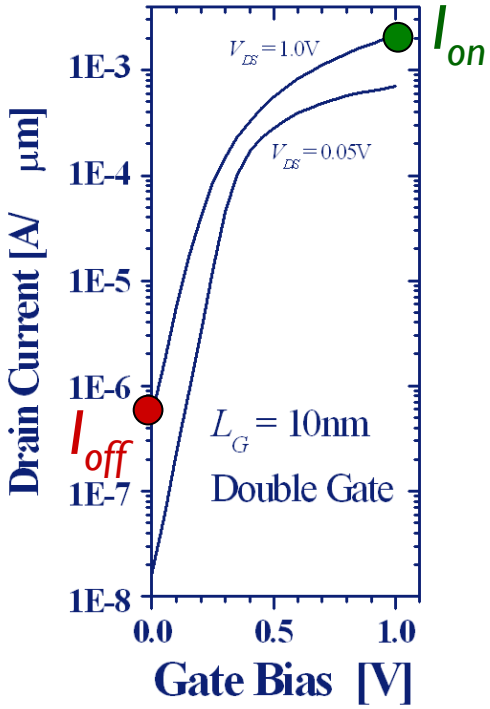


Why Multi-gate for 22nm & beyond ?





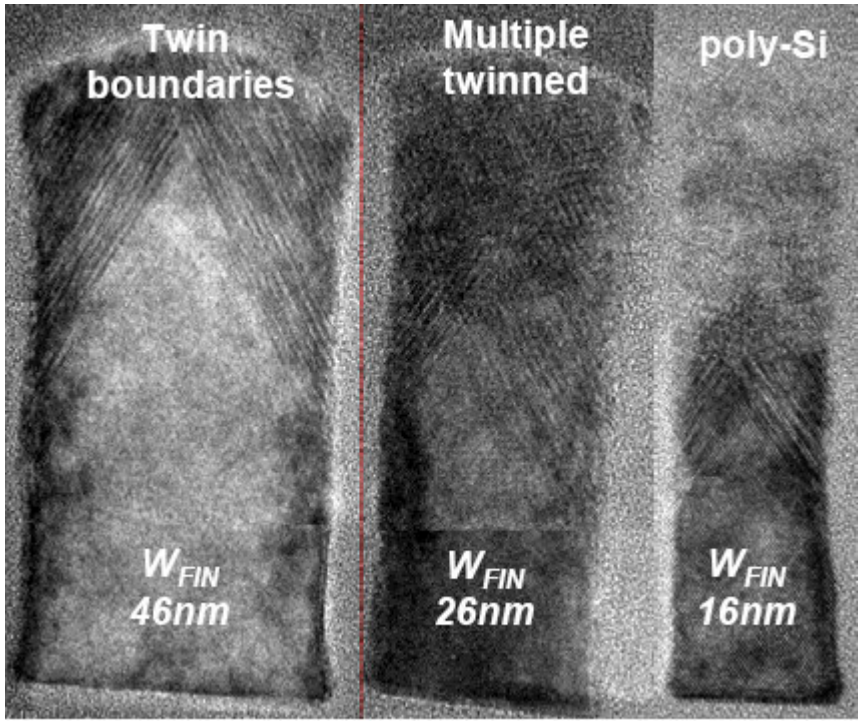




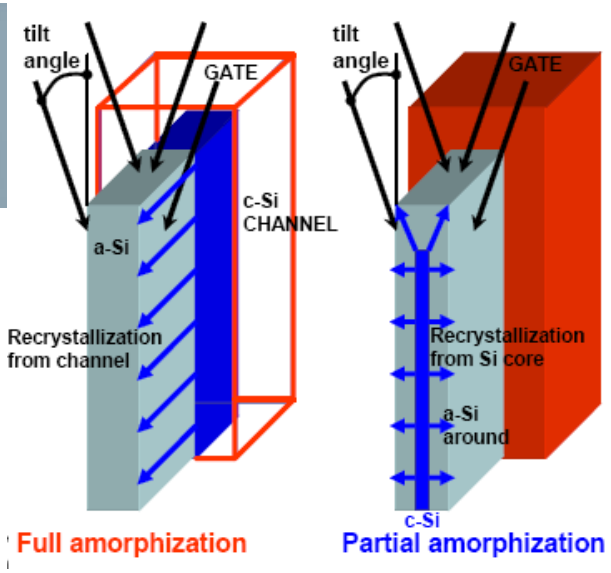
- Double gate structure much better gate-to-channel control
- ➔ better short channel effect immunity
- ➔ Lower leakage and higher mobility (no channel doping)
- ***In all looks nice & simple, BUT …***

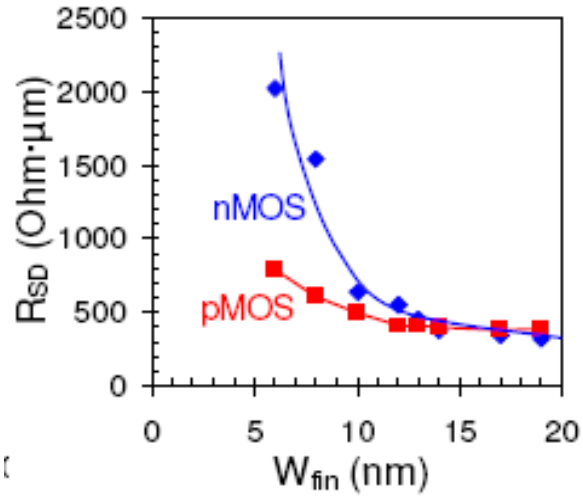
USJ challenges for FinFET
FIN amorphization /recristalization

FIN implanted with As + annealed
→ Poor re-crystallization



Duffy, APL, 90, 2007

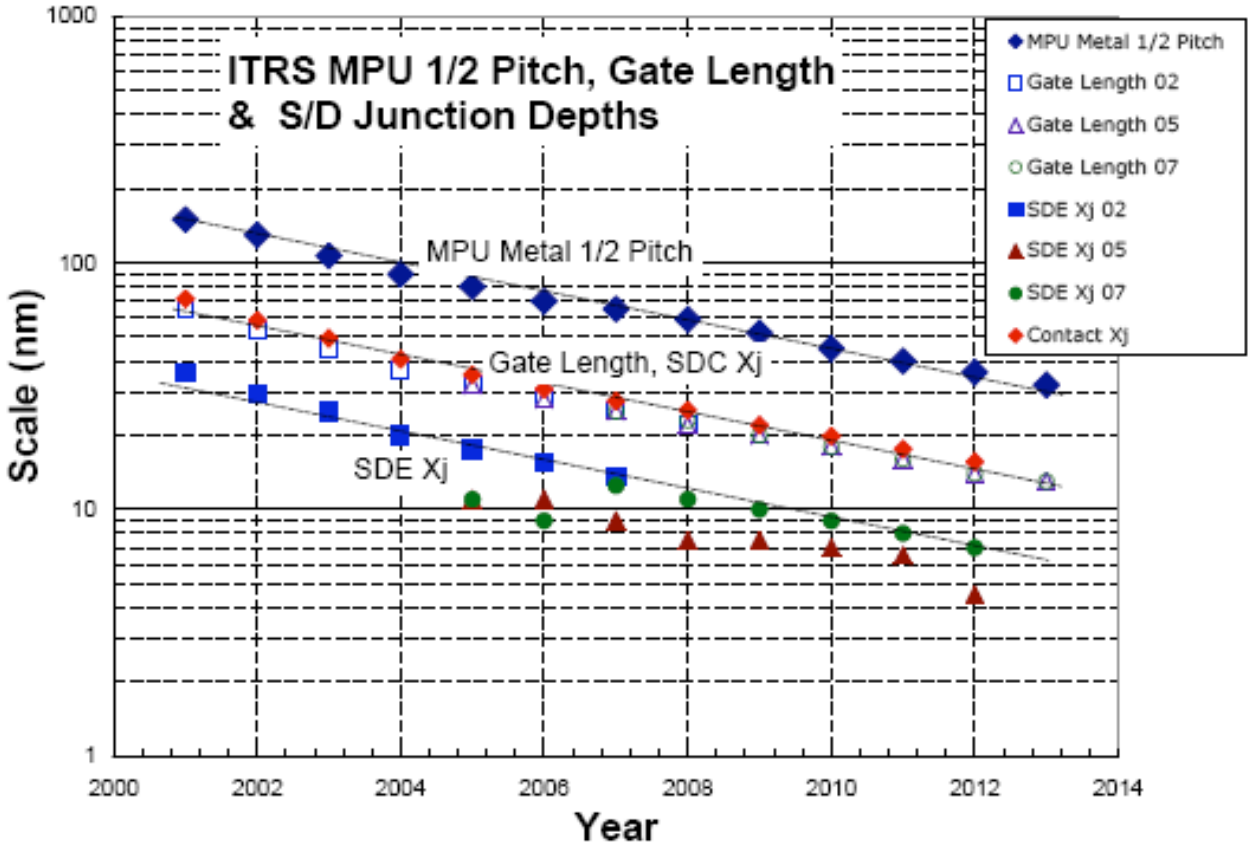




Van Dal, VLSI 2007

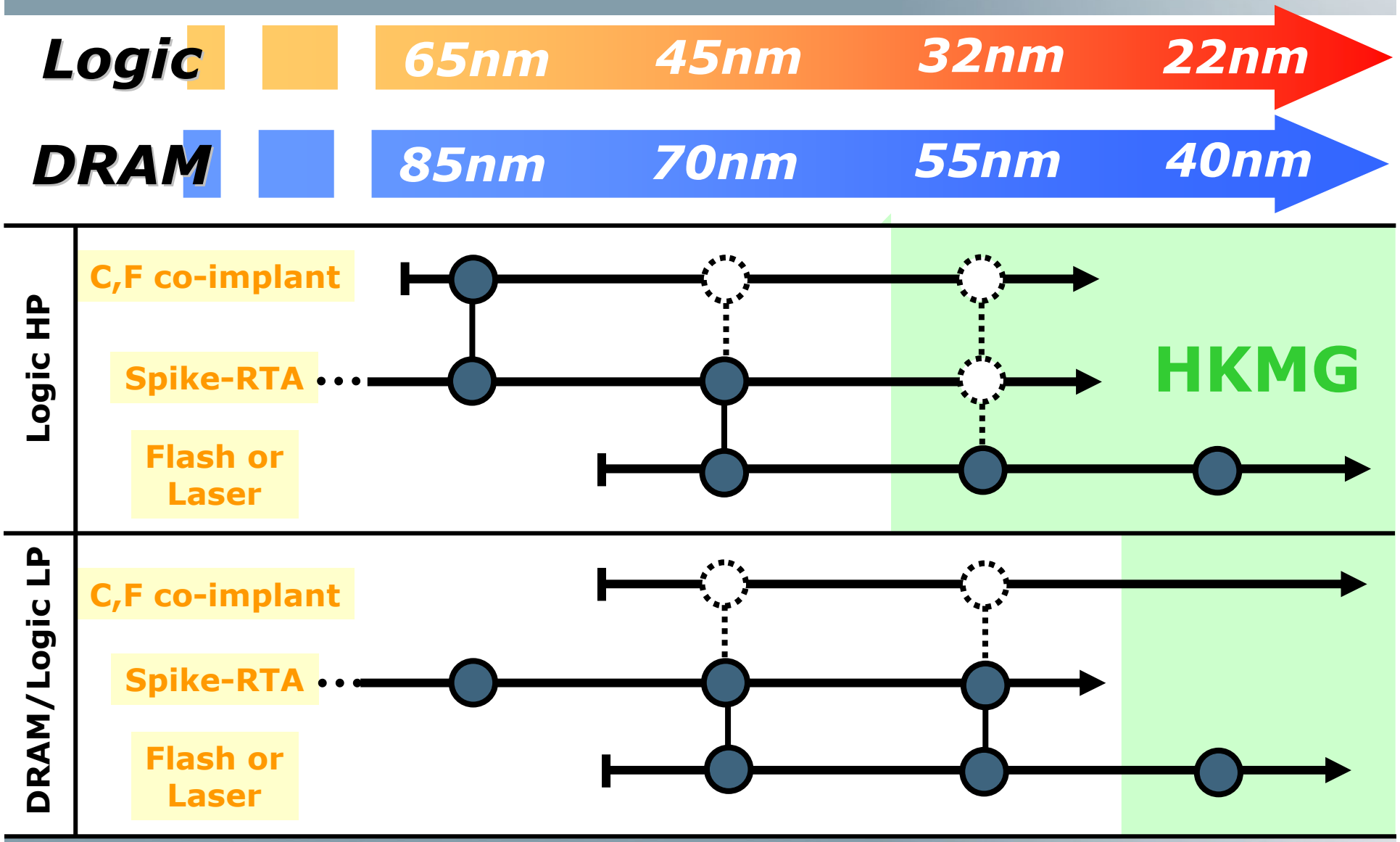
- FinFET has new set of challenges for junction formation (conformality, defectivity, etc …) !!

ITRS Scaling of L_g and X_j



Junctions are becoming extremely shallow and difficult to form

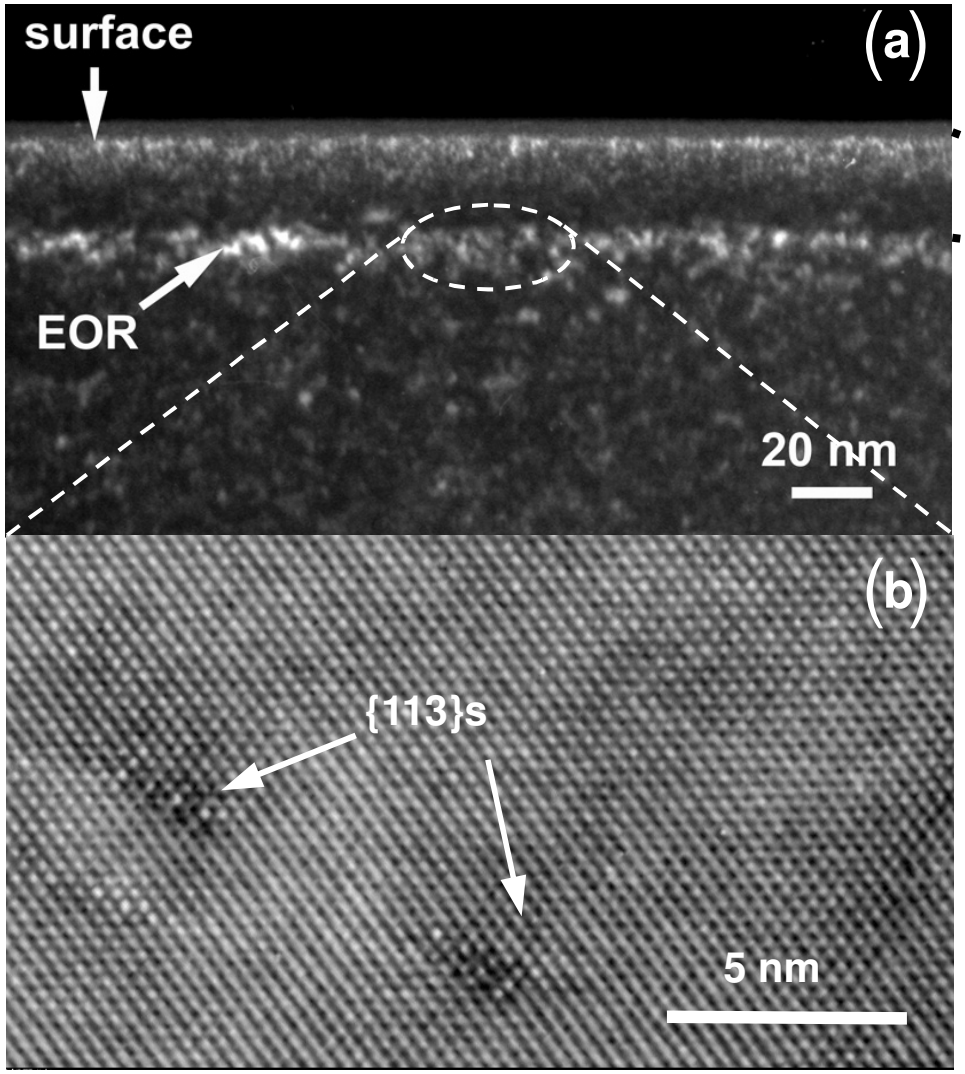
USJ roadmap *(IMEC view)*
… assuming Planar architecture

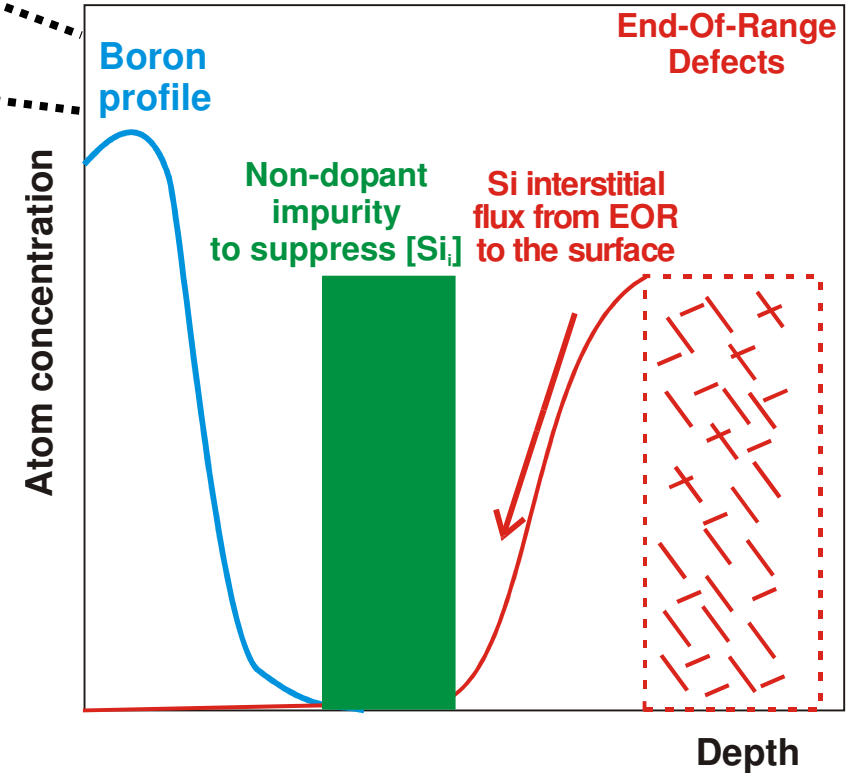


Outline

- Different paths for scaling & implications for USJ
- From low dopant diffusion with **co-implantation** …
- … to diffusion-less with **milli-second annealing**
- Summary

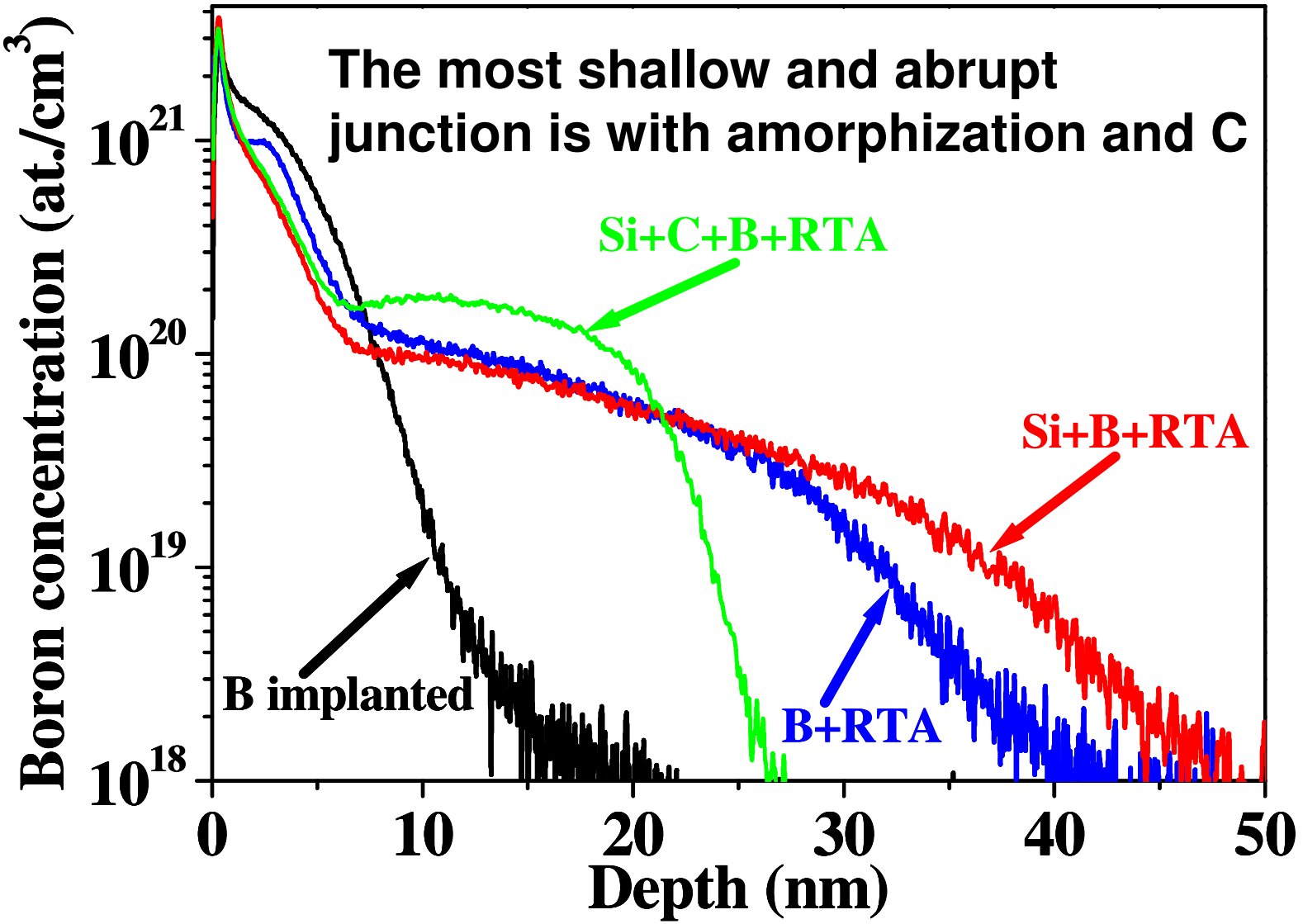
Concept of co-implants



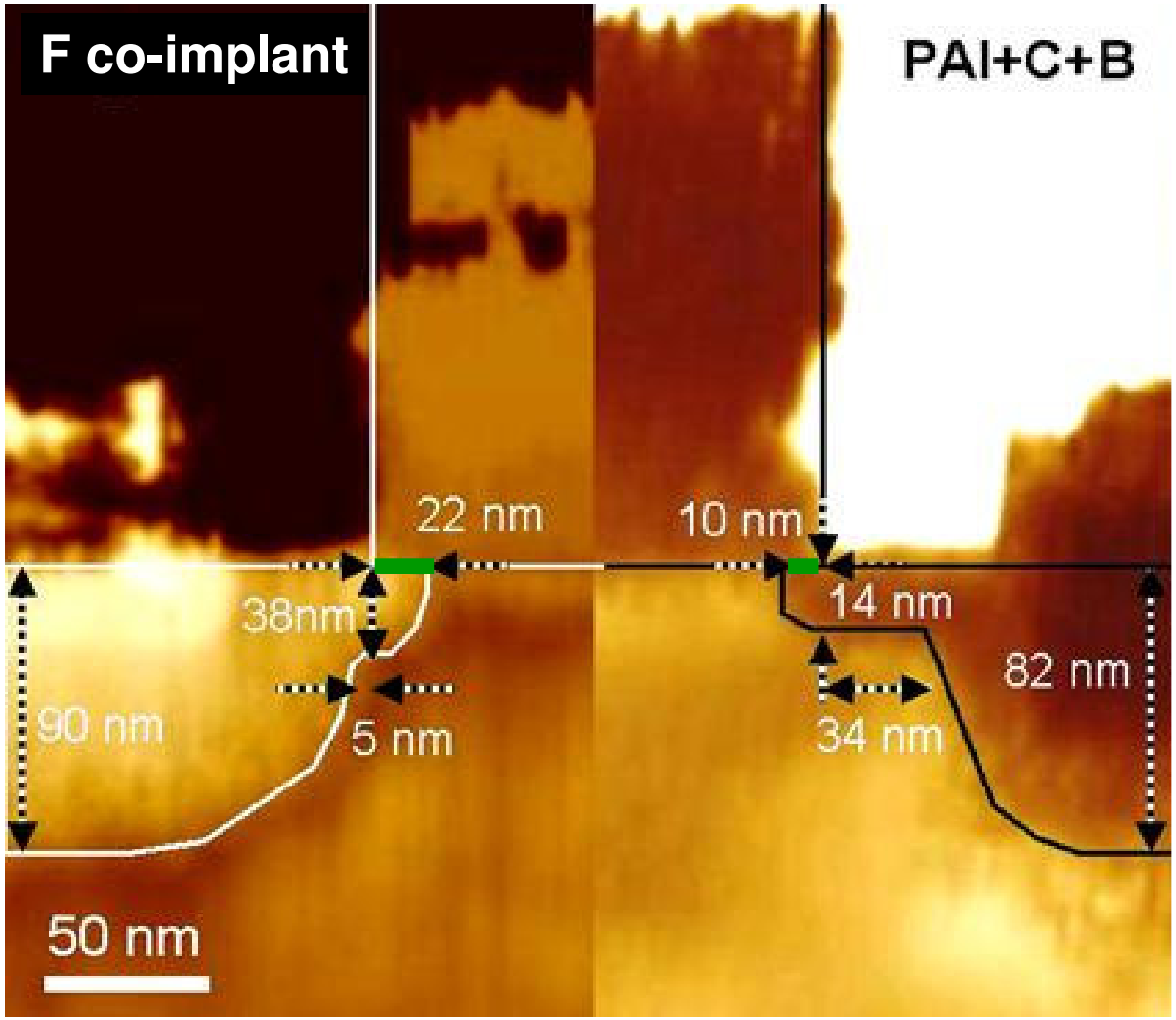


Co-implantation suppresses diffusion of Si interstitials from End-Of-Range

1D : Carbon co-implanted p-type junction



2D electrical profiling of pMOSFET
SSRM (Scanning Spreading Resistance Microscopy)

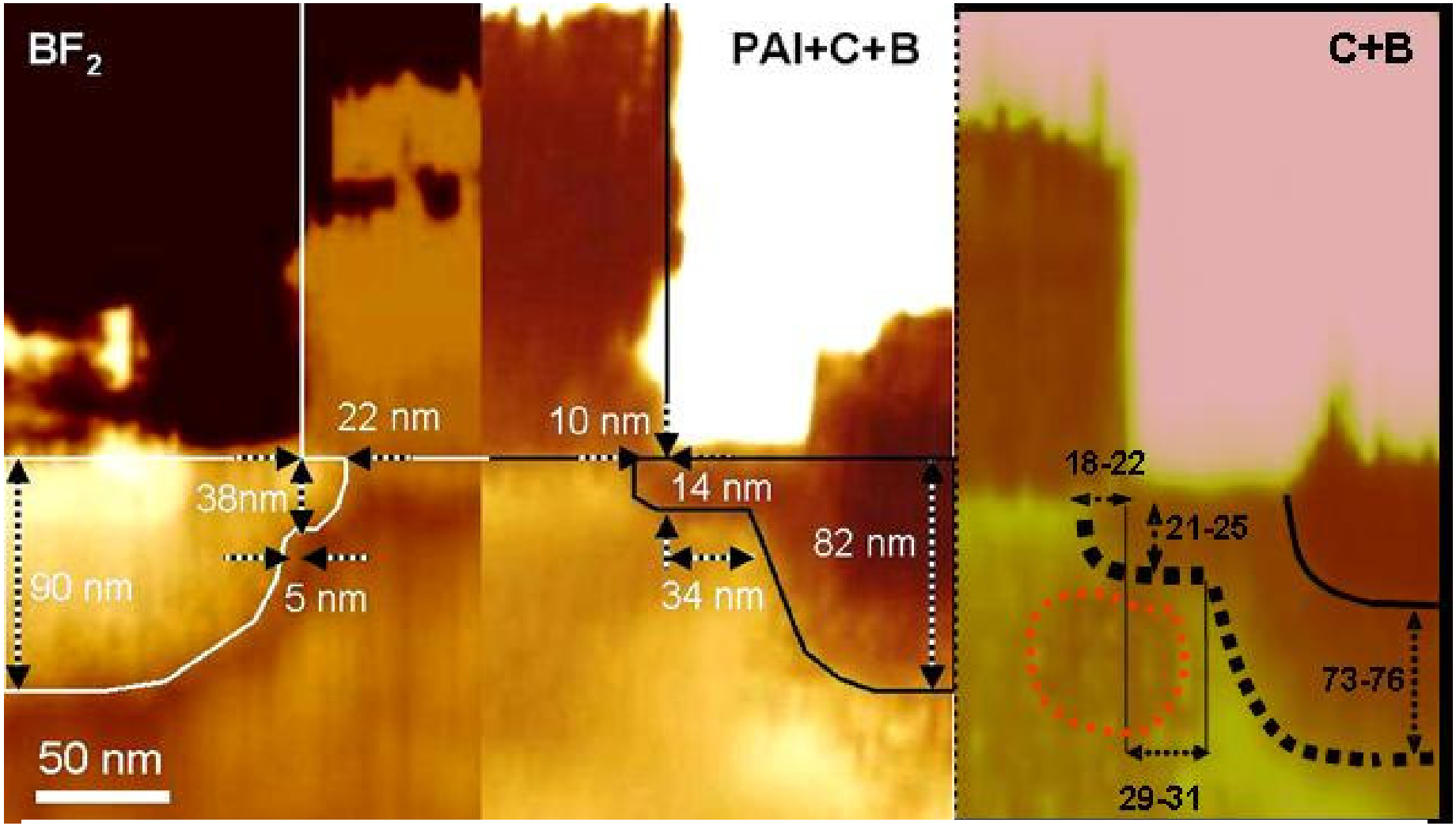


Courtesy: P. Eyben [IMEC]

Co-implantation with Carbon:

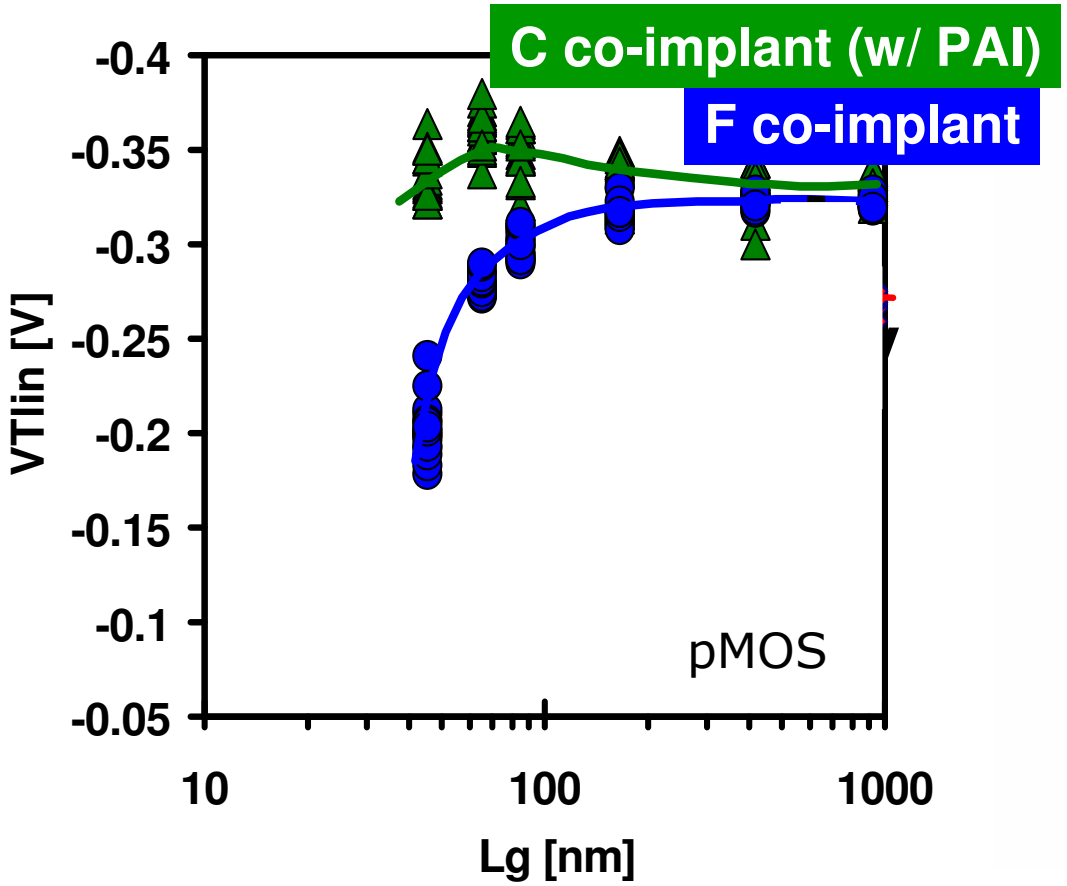
- **Reduces extension overlap**
- **Suppresses HDD diffusion towards gate edge**

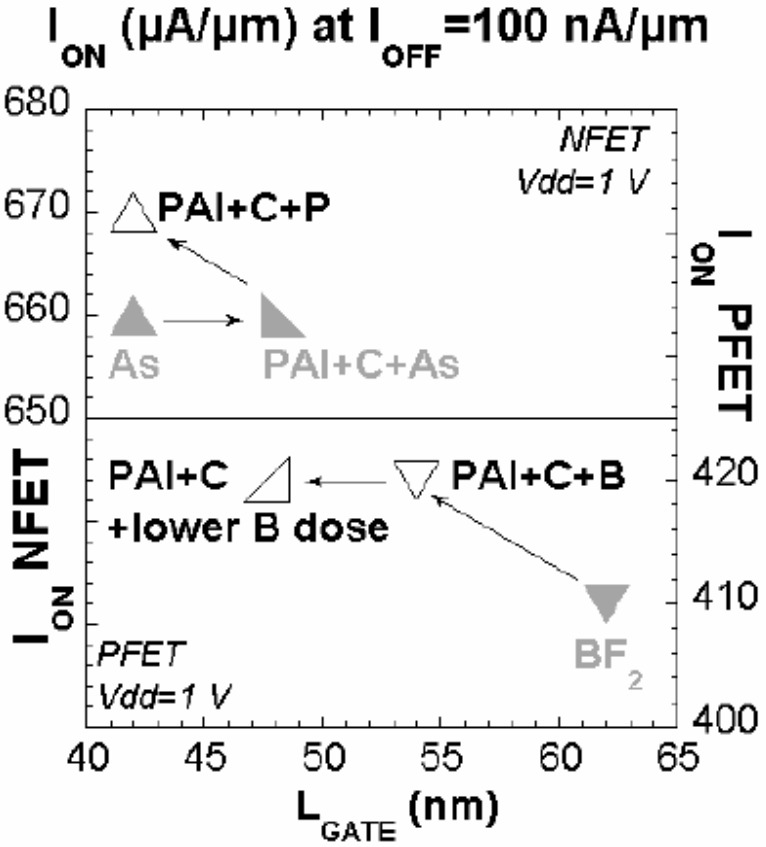
2D electrical profiling of pMOSFET
SSRM (Scanning Spreading Resistance Microscopy)



C without pre-amorphization does not reduce junction overlap

Carbon co-implant
Transistor performance

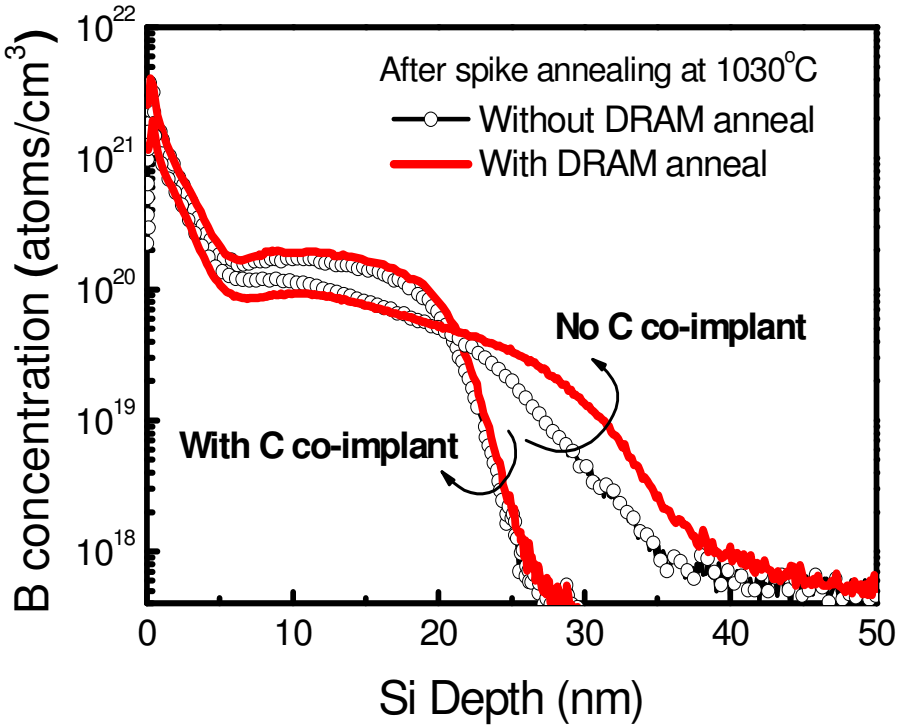


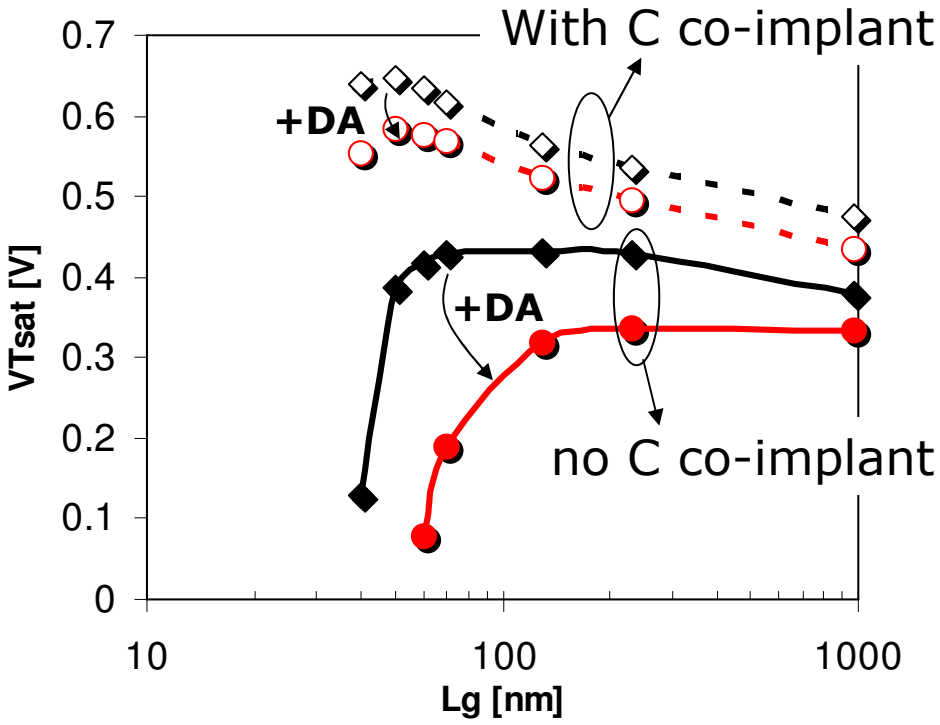


- Improved SCE with no performance loss demonstrated with PAI+C (specially for pMOS)

Carbon for junction thermal stability

DRAM anneal (DA) = 750C-30min



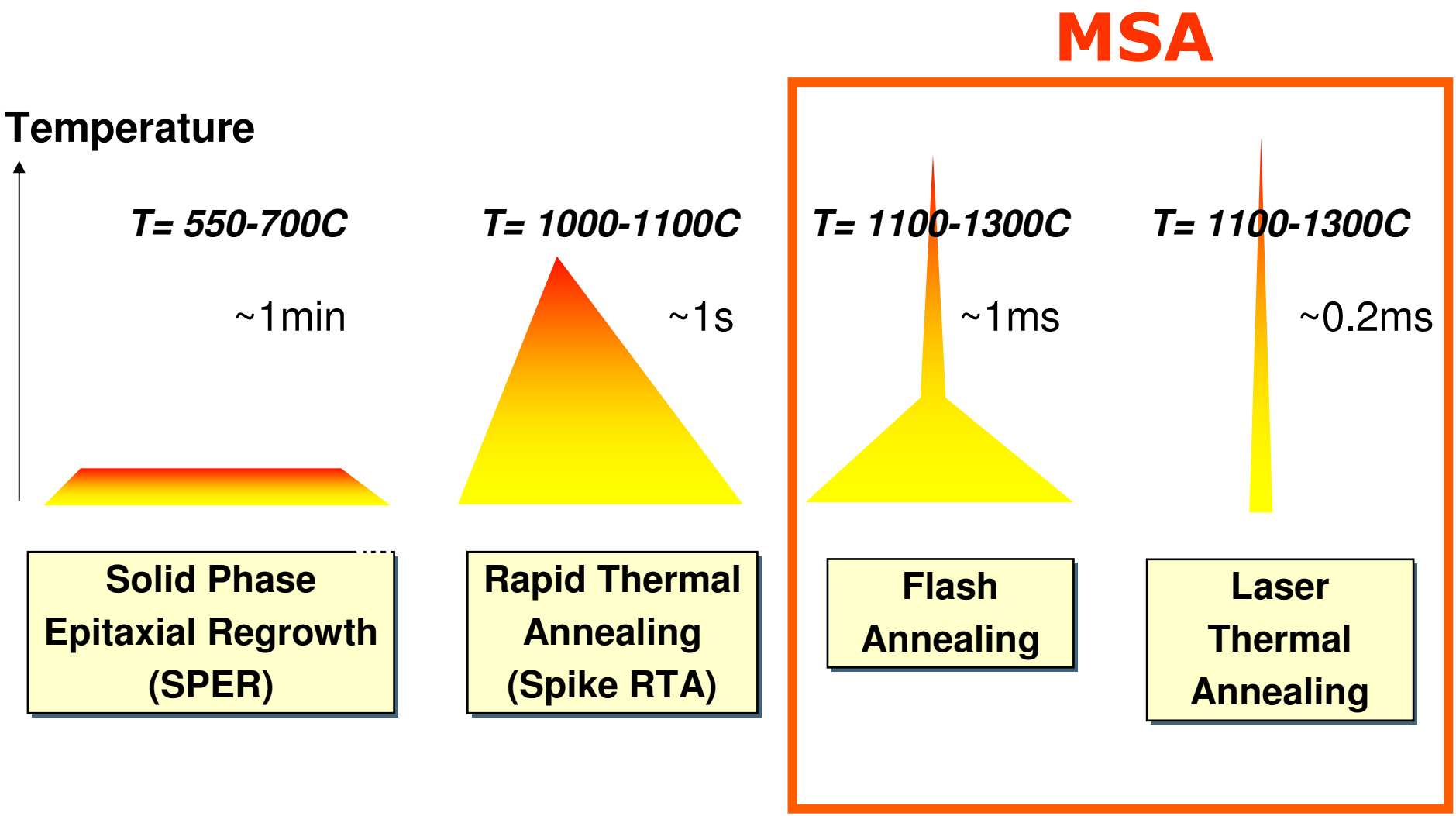


- Junction thermal stability is critical for some application (e.g., DRAM periphery)
- Carbon can improve significantly the junction thermal stability

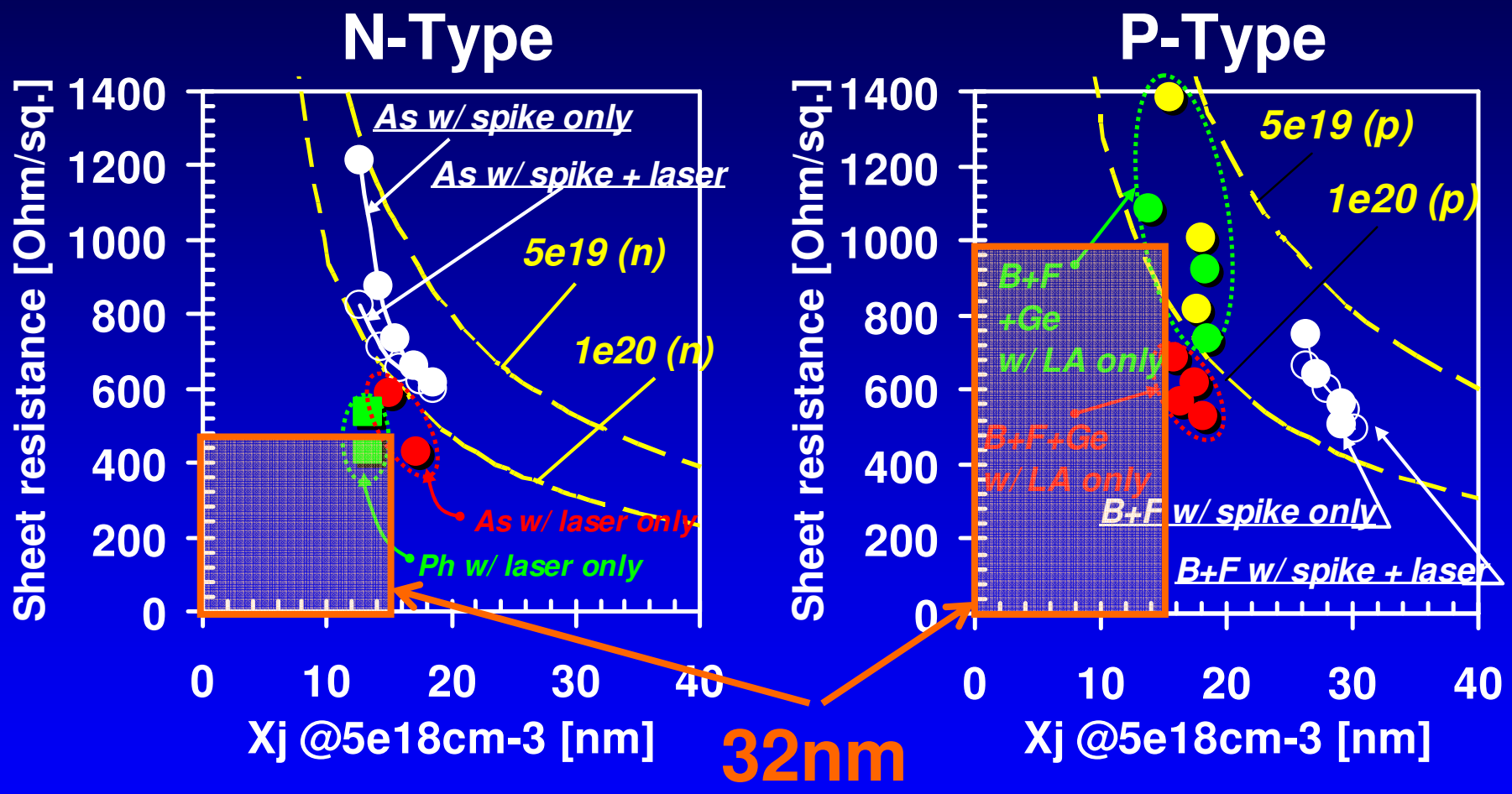
Outline

- Different paths for scaling & implications for USJ
- From low dopant diffusion with **co-implantation** …
- … to diffusion-less with **milli-second annealing (MSA)**
  - Fundamental advantage of milli-second anneal
  - Milli-second annealing entry point : combination with Spike
  - Aggressive junctions design with MSA-only
  - Impact on junction leakage (residual defects)
  - Compatibility with HKMG stacks
  - Compatibility with strain boosters
  - Process control & manufacturability
- Summary

Thermal Budget



32nm specifications



Laser anneal only enables to meet 32nm specs.

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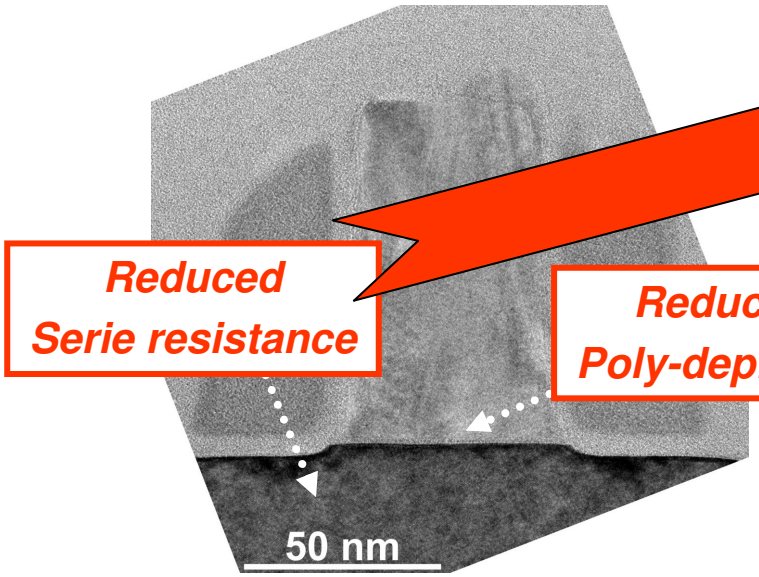
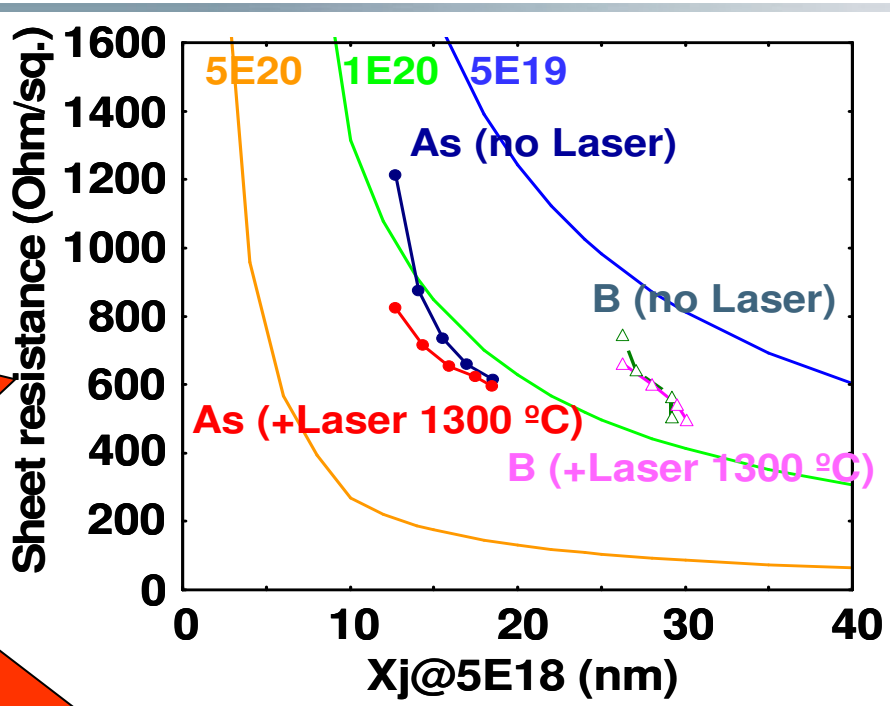
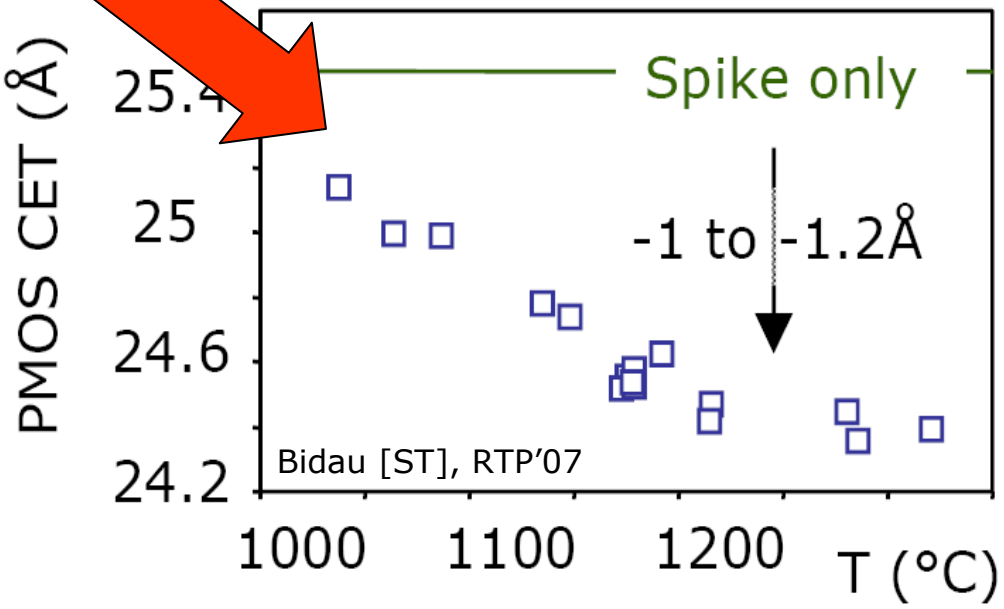
MSA in addition to Spike
Performance 'booster'



Reduced Serie resistance

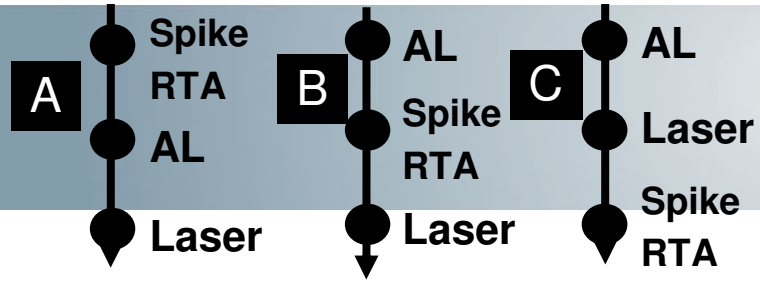
Reduced Poly-depletion



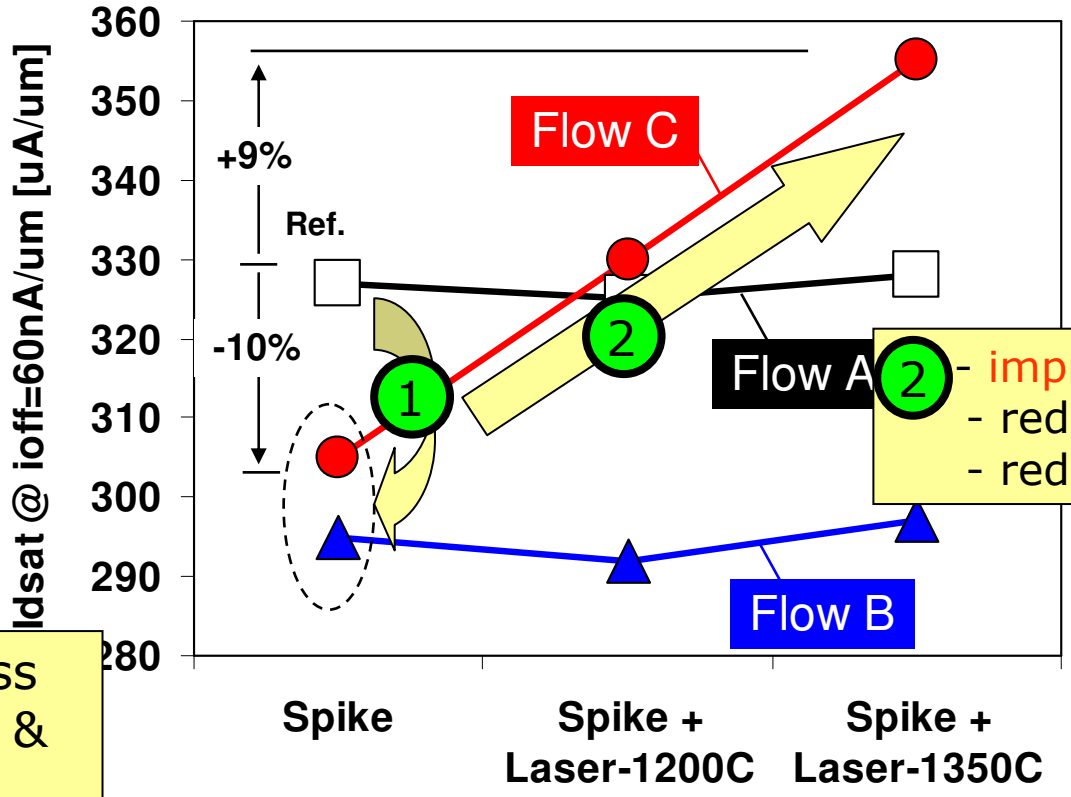


- Laser anneals improves:
  - **Poly-gate doping**
  - **Junctions activation**

Spike-Laser sequence impact
pMOS



Hoffmann [IMEC], IWJT'07



2 - improved Bo activation
- reduced dose loss
- reduced mobility loss

1 Bo dose loss (extension & poly-gate)

- Up to 9% performance improvement demonstrated with additional Laser anneal with "Spike-last" sequence.
- KMC simulation confirmed it is due to **less B-I clusters** formed during Spike with a pre-Laser anneal

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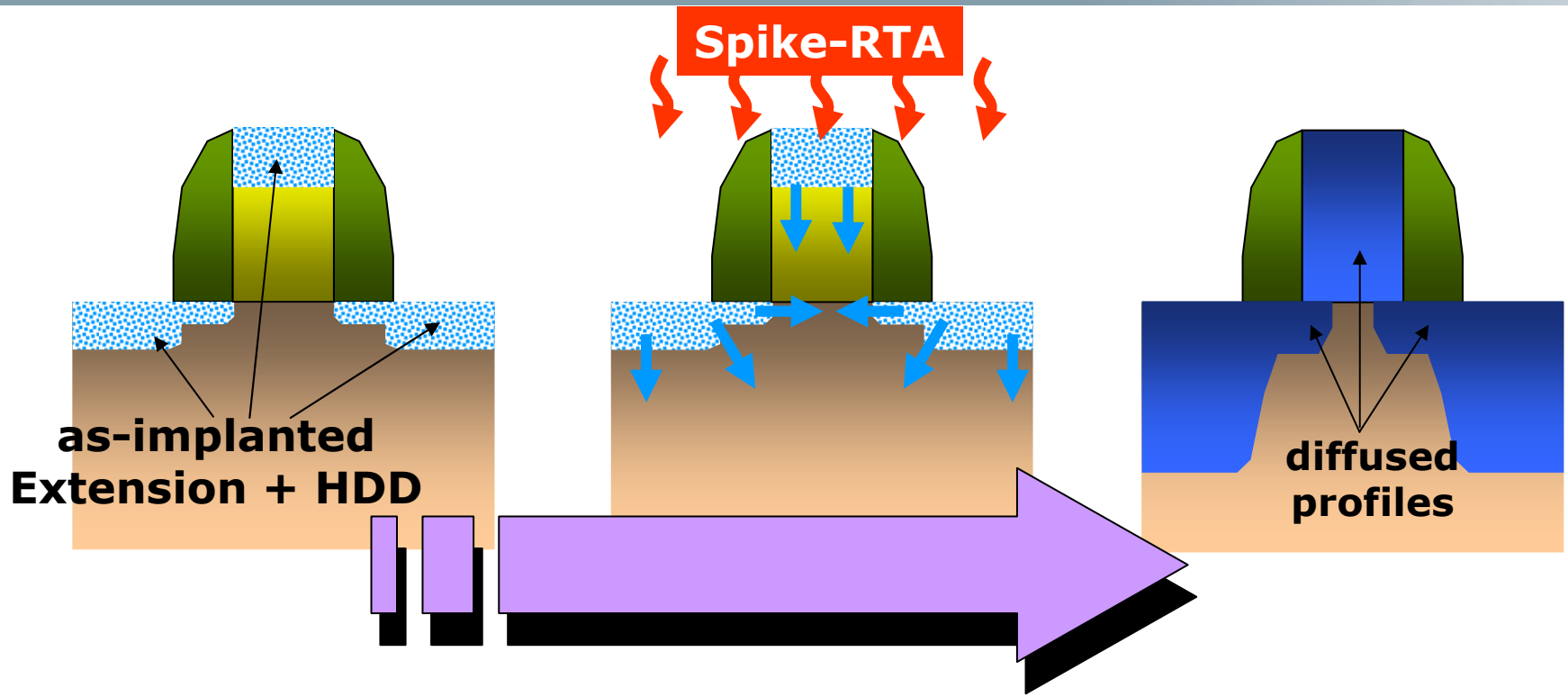
- Summary

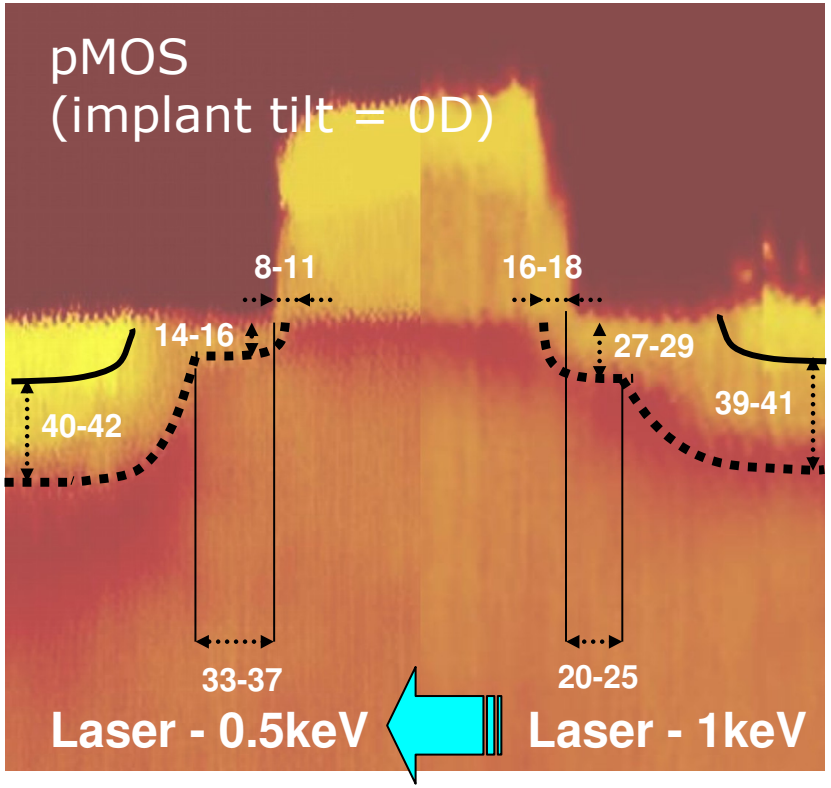
USJ opportunities with advanced gate stacks

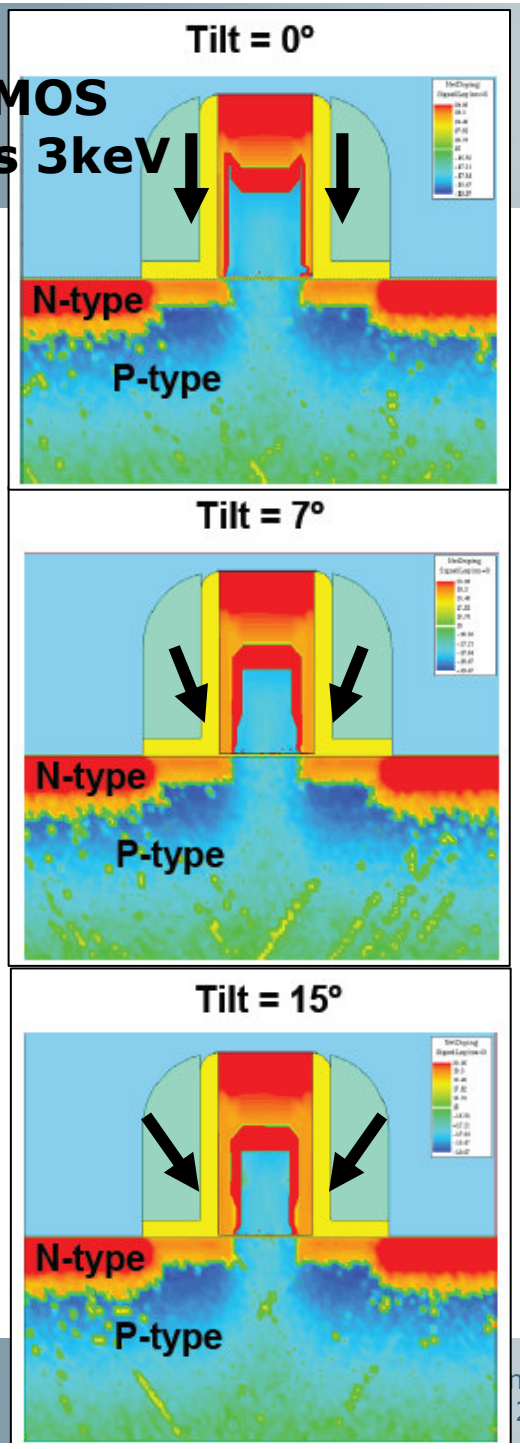


- Aggressive USJ requires low Thermal budget, BUT :
  1. Leakage from remaining EOR → *SOLUTION* : remove PAI (eg, Cluster I/I)
  2. Poly gate doping/activation → *SOLUTION* : Metal Gate

COMPATIBLE with MSA

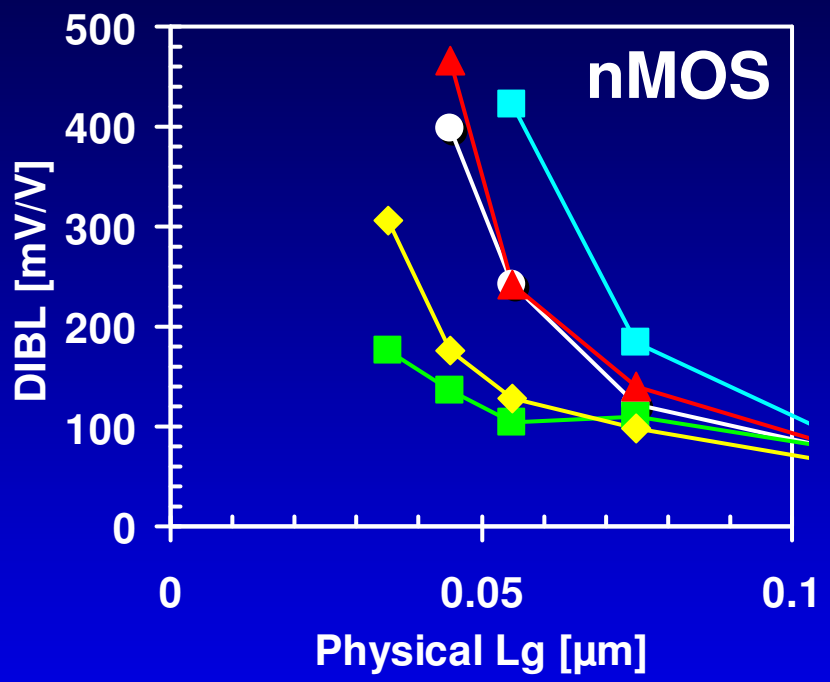
Laser-only junctions design
Methodology

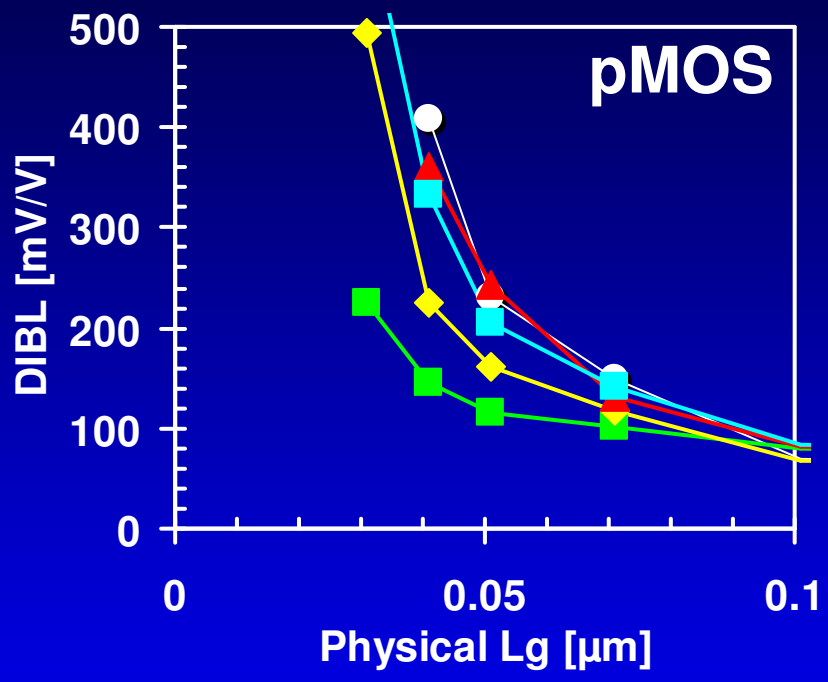




- Use of SSRM and TCAD for successful device targeting:
  - nMOS → As (3keV) need to be tilted (> 7D)
  - pMOS → B (0.5keV) : OK with tilt = 0°

Extensions redesign with MSA

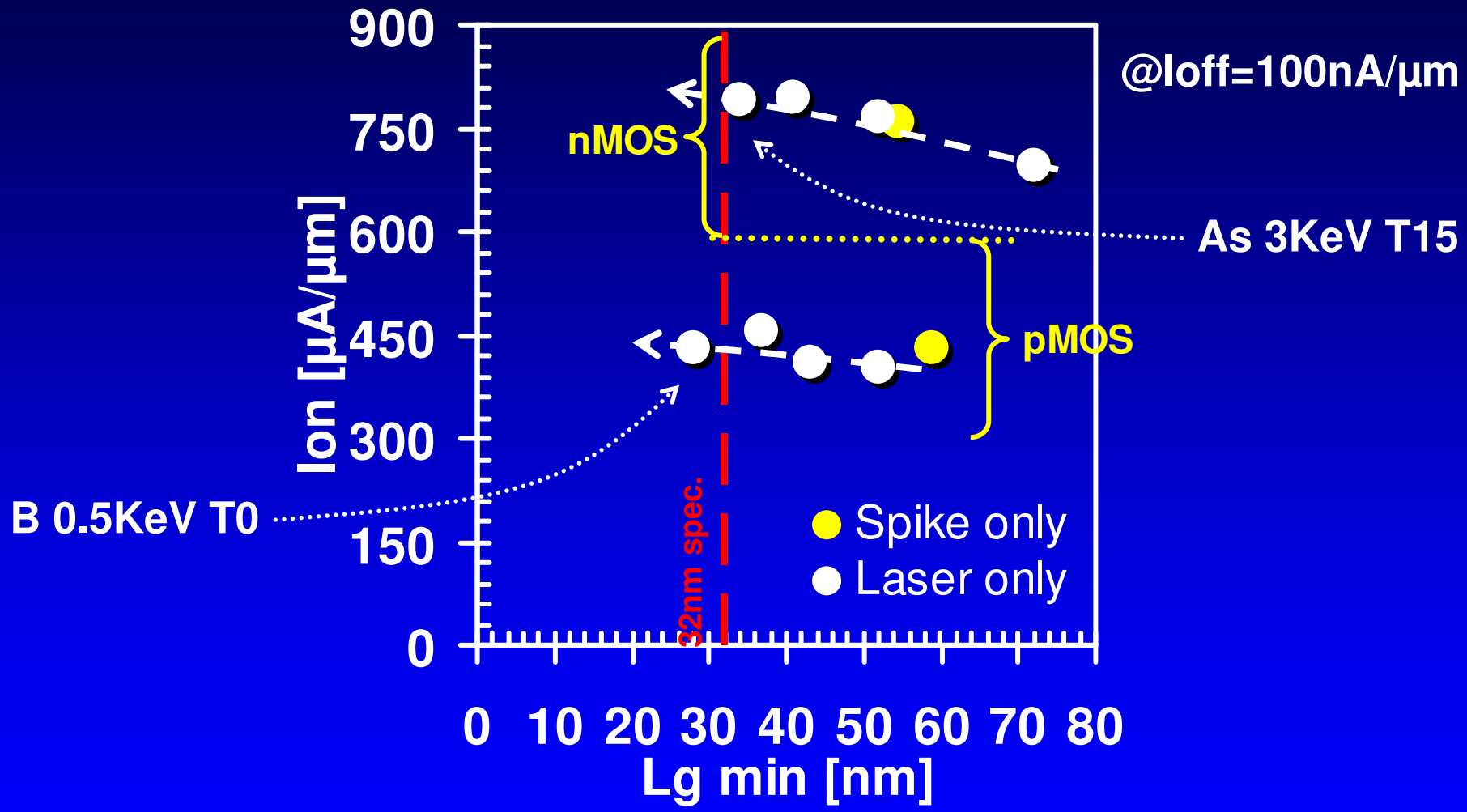




NMOS (As)	PMOS (B)
1KeV T0	0.5KeV T0
3KeV T15	1KeV T0
5KeV T15	1.5KeV T0
5KeV T30	1KeV T15
Spike reference	

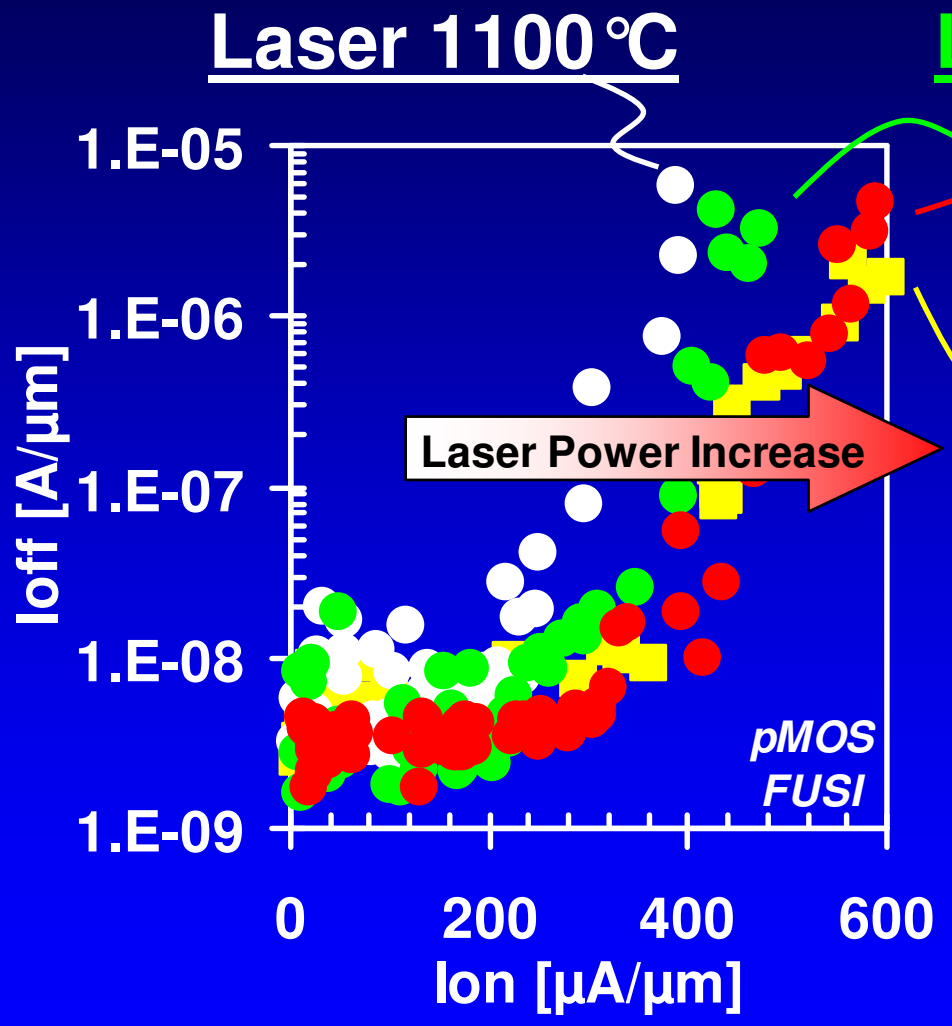
Proper placement of dopants (Tilt, energy) is even more critical with diffusion less approach

Device scaling with Laser



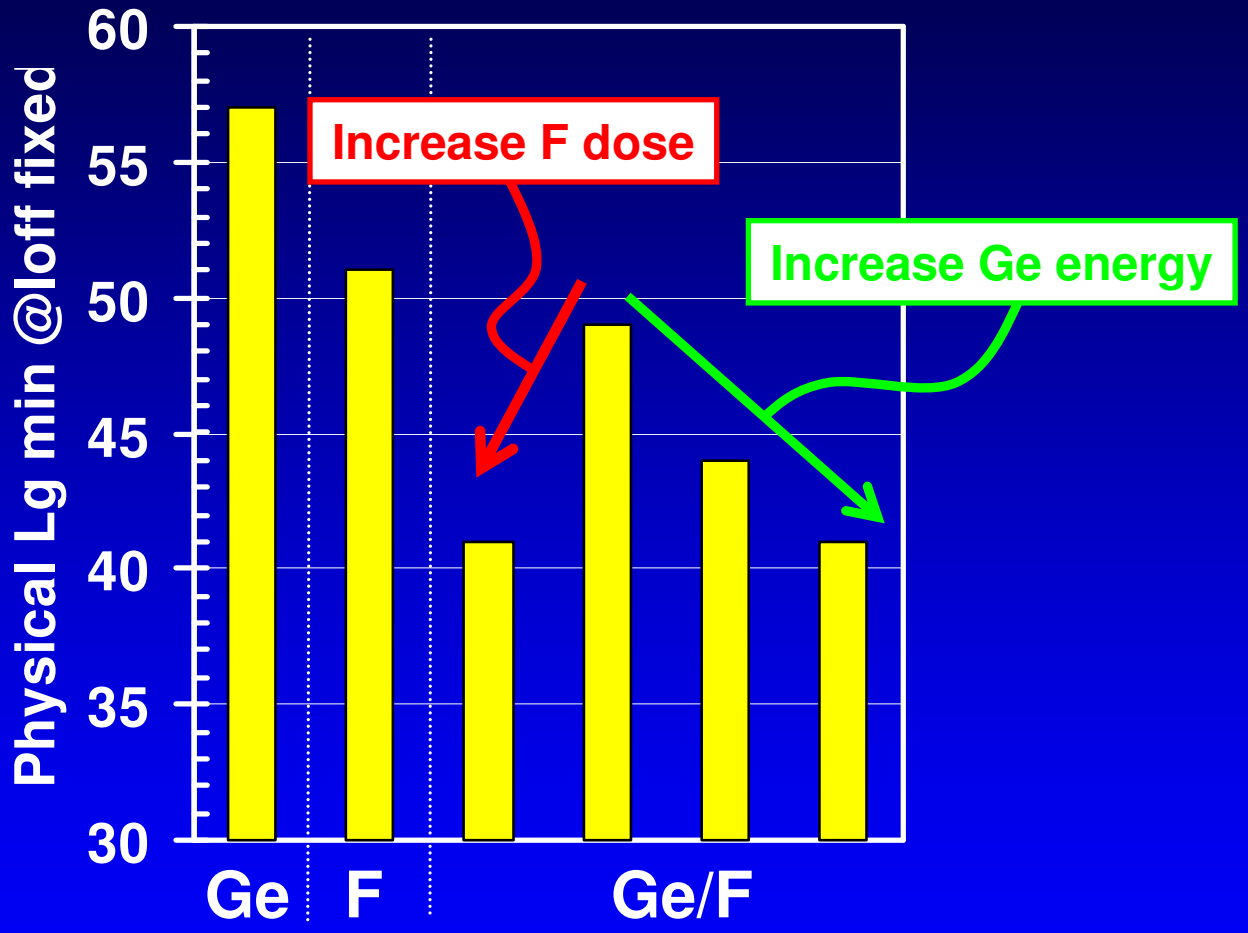
32nm requirement has been achieved

Laser Power



Laser power optimization is very important to achieve high performance

Co-implantation with MSA



Co-implantation still mandatory to avoid channeling and Boron TED

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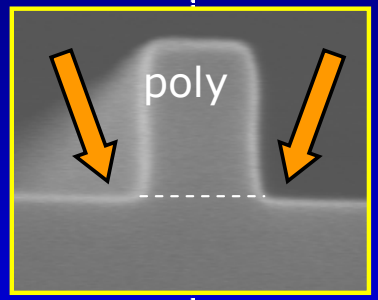
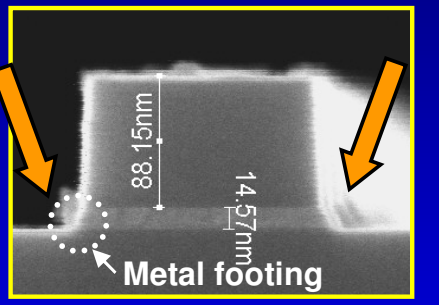
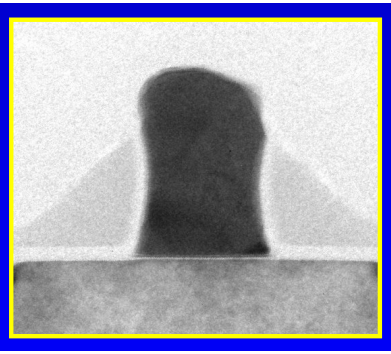
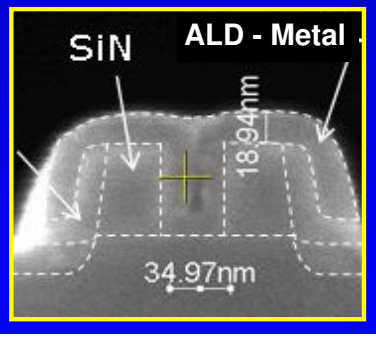
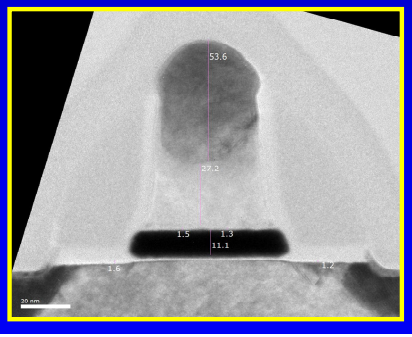
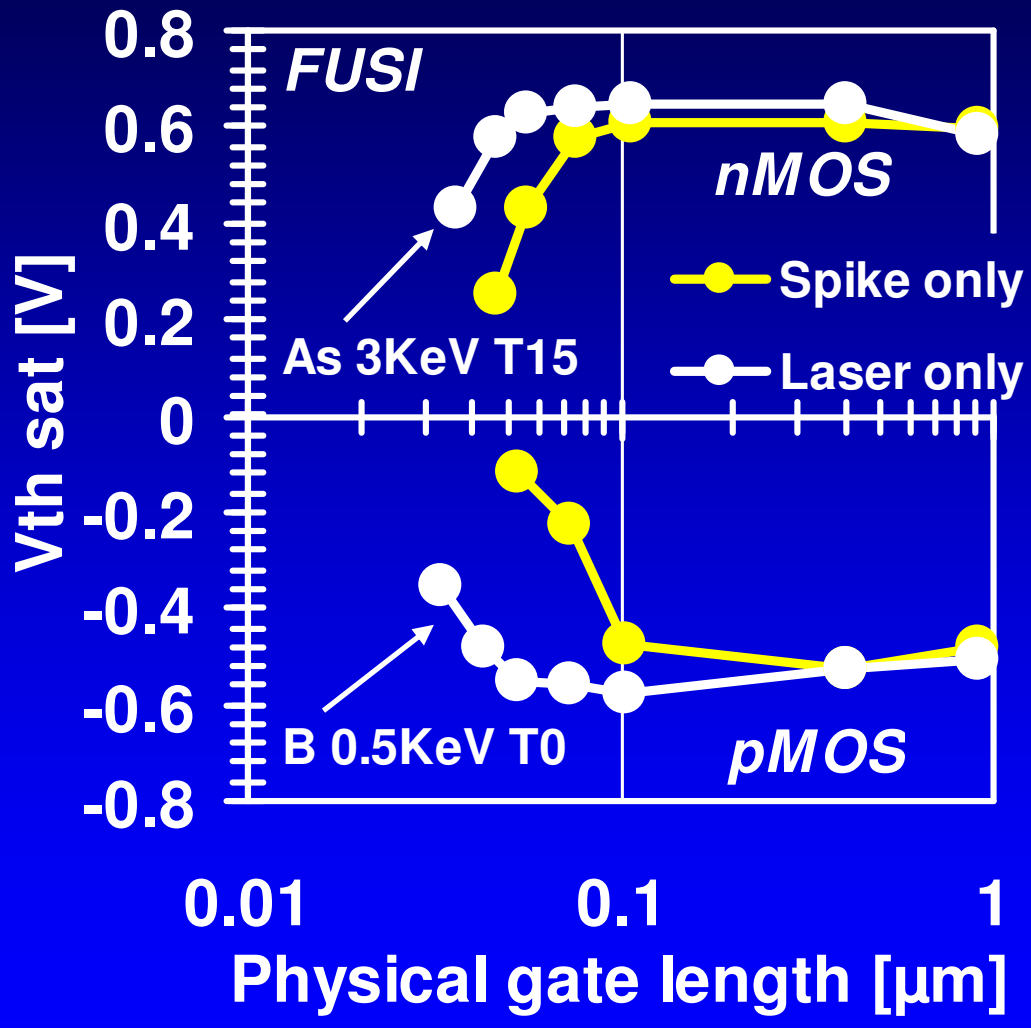
Advanced gate stack option

	FUSI	RPG	MIPS
	Gate last	*Gate last*	*Gate first*
@ LDD & Halo implant step			
@ end of process			

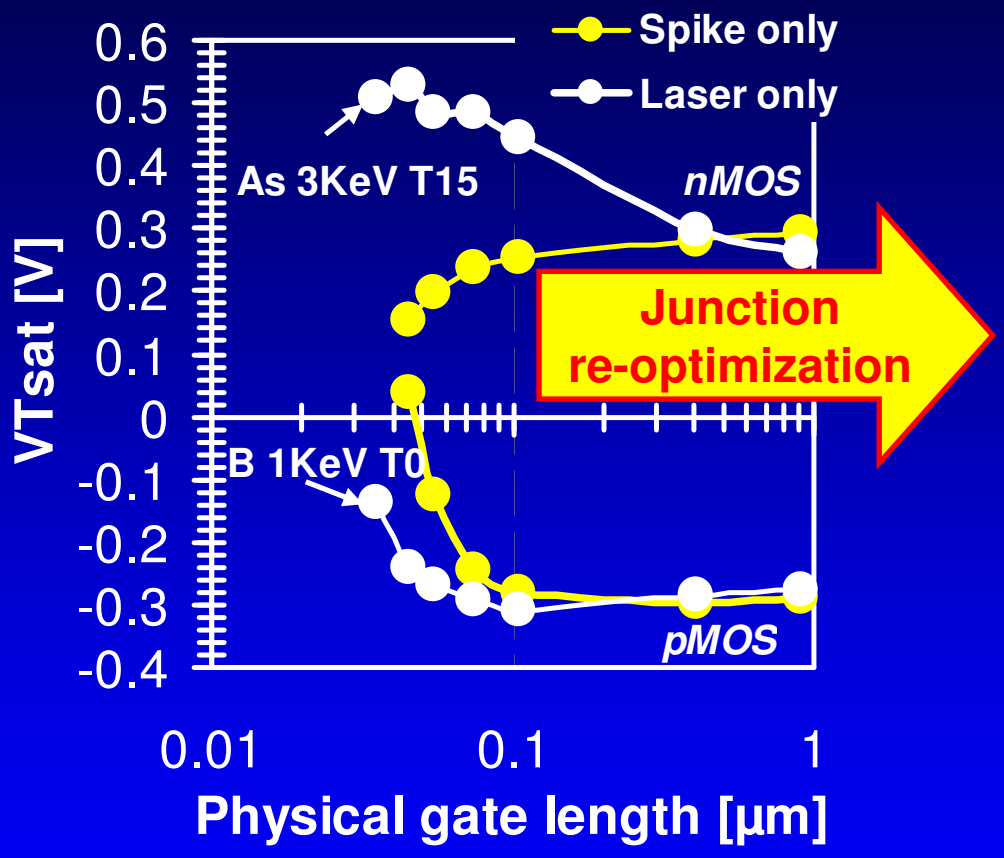
FUSI case



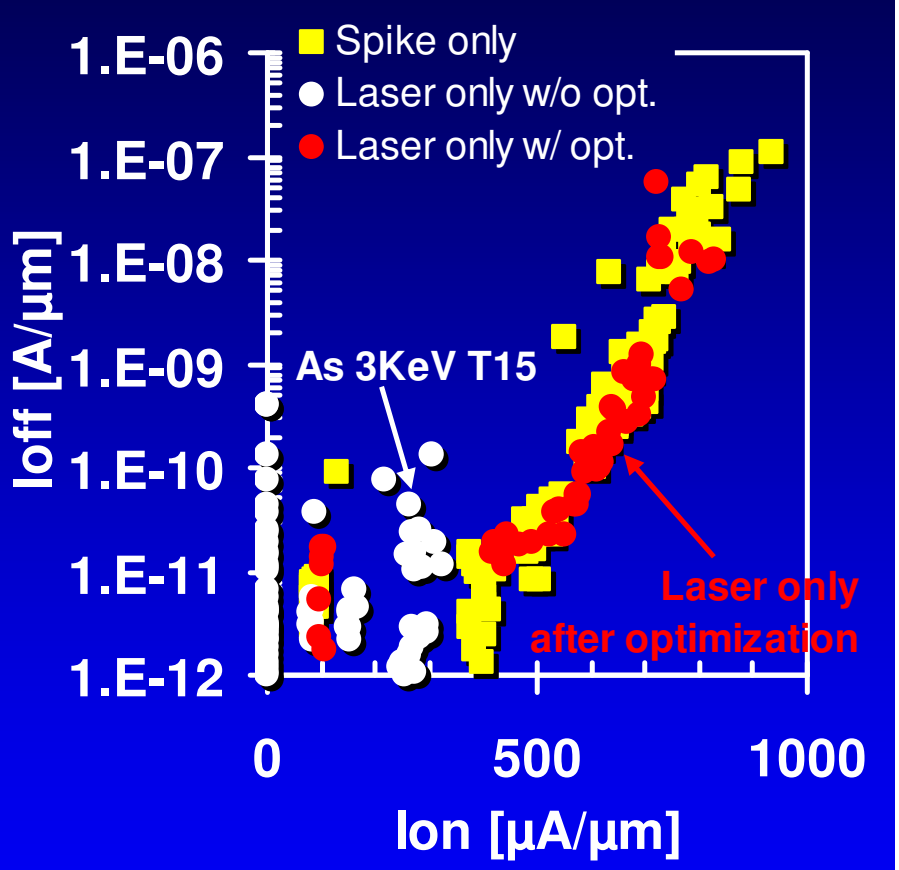
Excellent scaling has been observed on FUSI

(Gate last process)

Metal Insert Poly-Silicon case



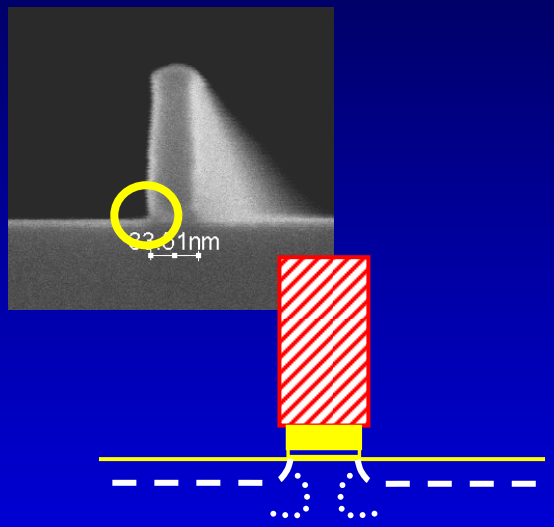
Junction re-optimization



Junction design can be highly sensitive to the gate stack chosen

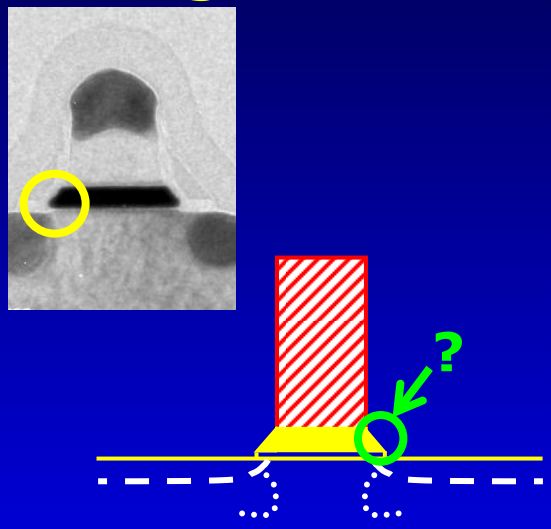
Typical gate profile

Undercut



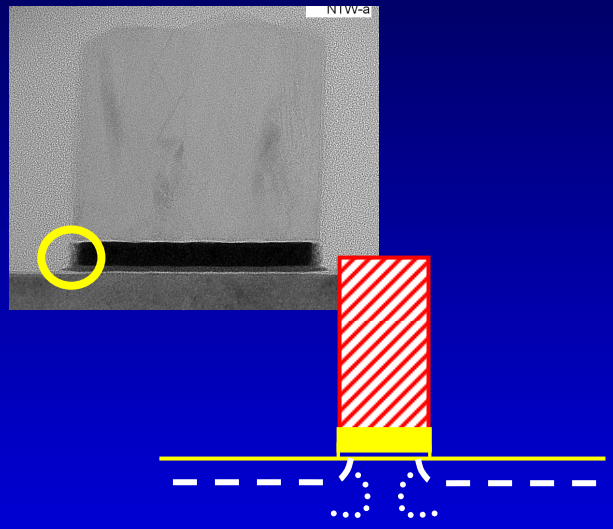
- Poor overlap between gate and junction
- USJ re-targetting would allow good overlap

Footing



- Overlaps depends if the taper is electrically part of the electrode
- USJ re-targetting would allow good overlap

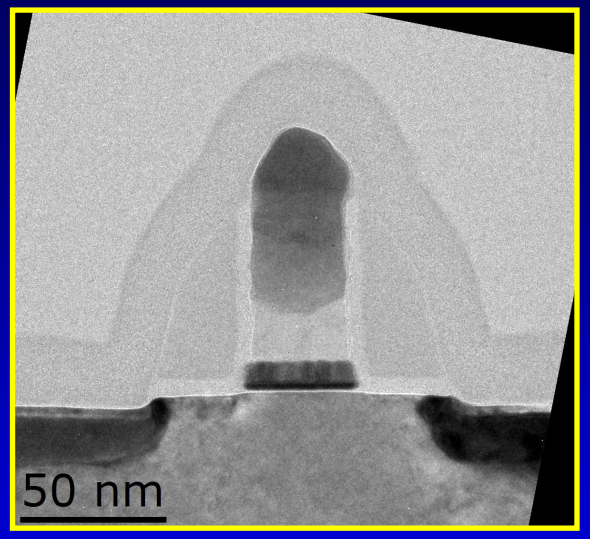
Straight

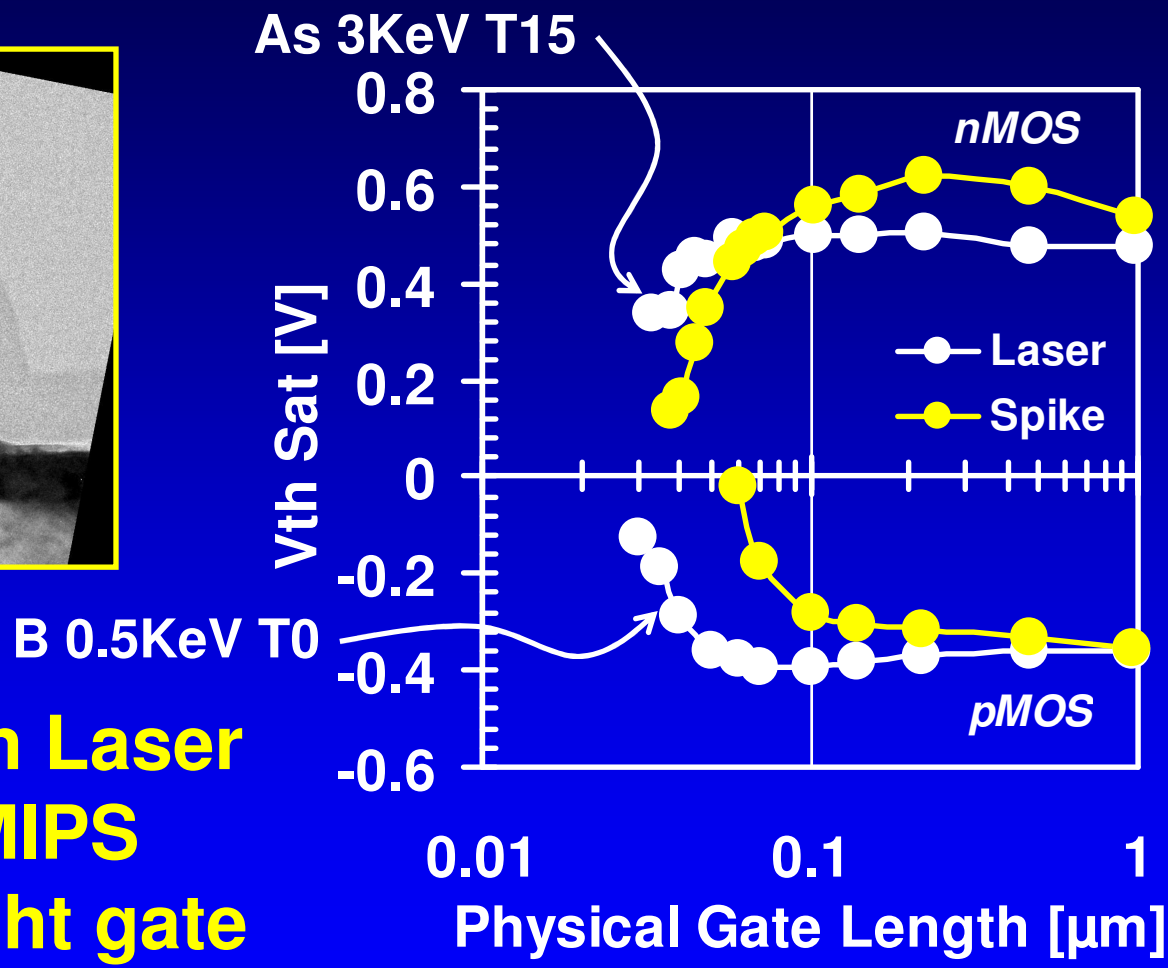


- Good USJ alignment with gate edge

Dopant implantation and placement are very sensitive to gate profile with diffusion less anneal

MIPS with straight gate profile

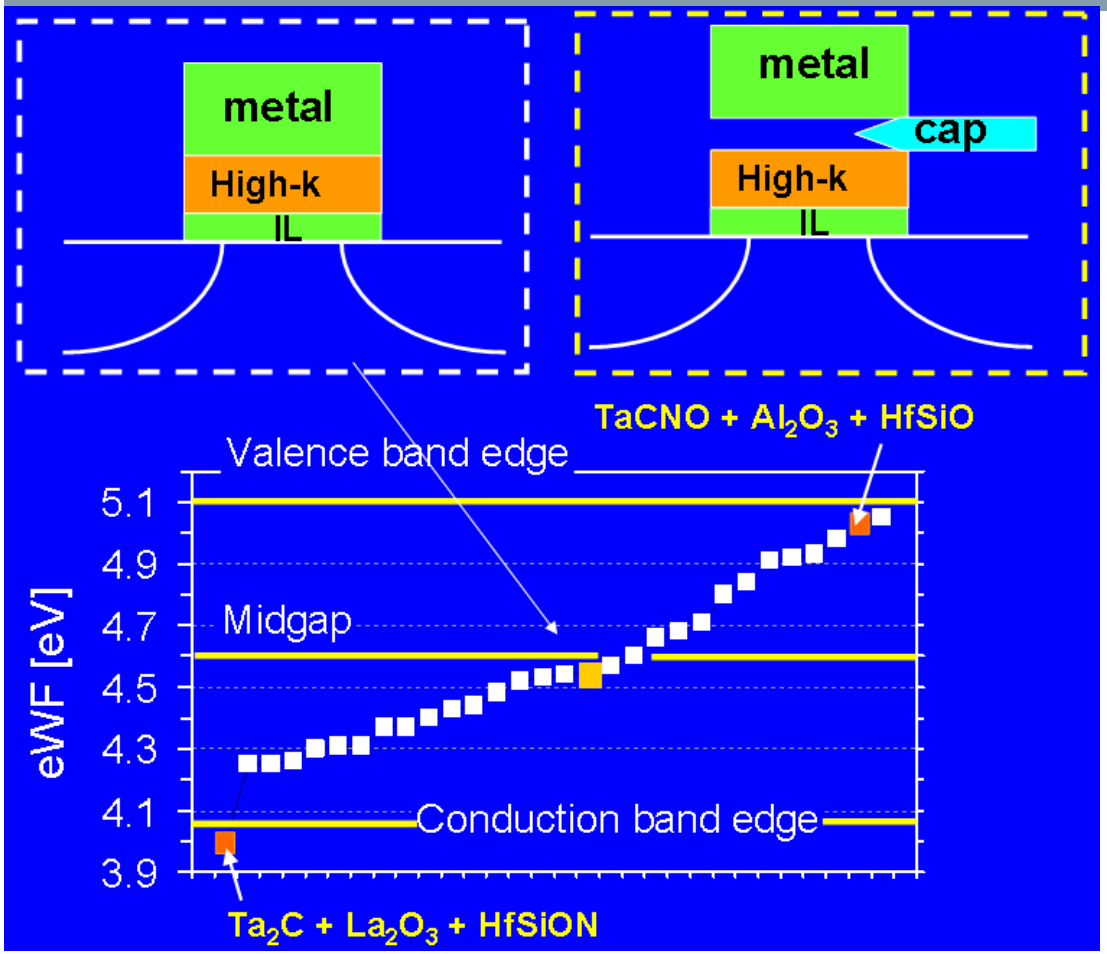


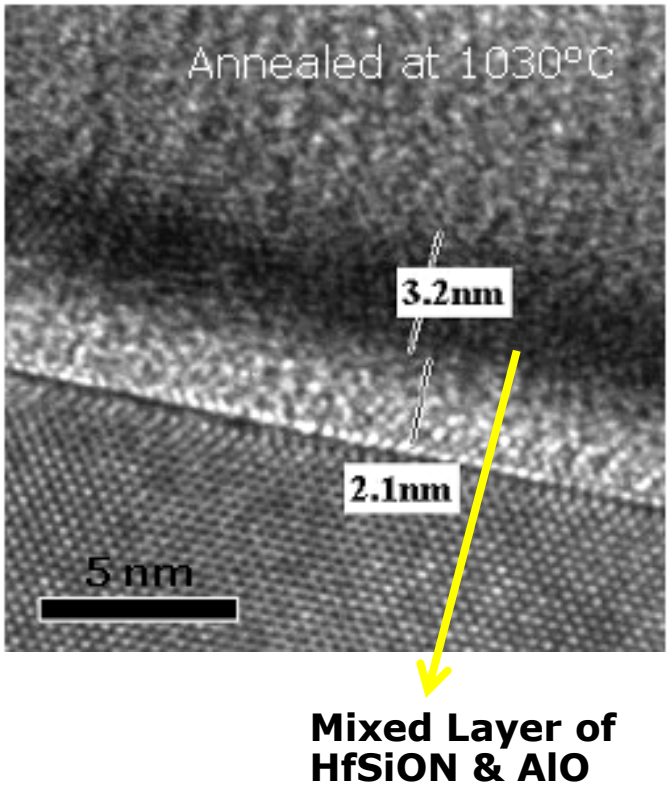


Scalability with Laser anneal on MIPS required straight gate profile

Use of capping for low-VT MIPS
High-K doping

S. Kubicek et al., IEDM 2007

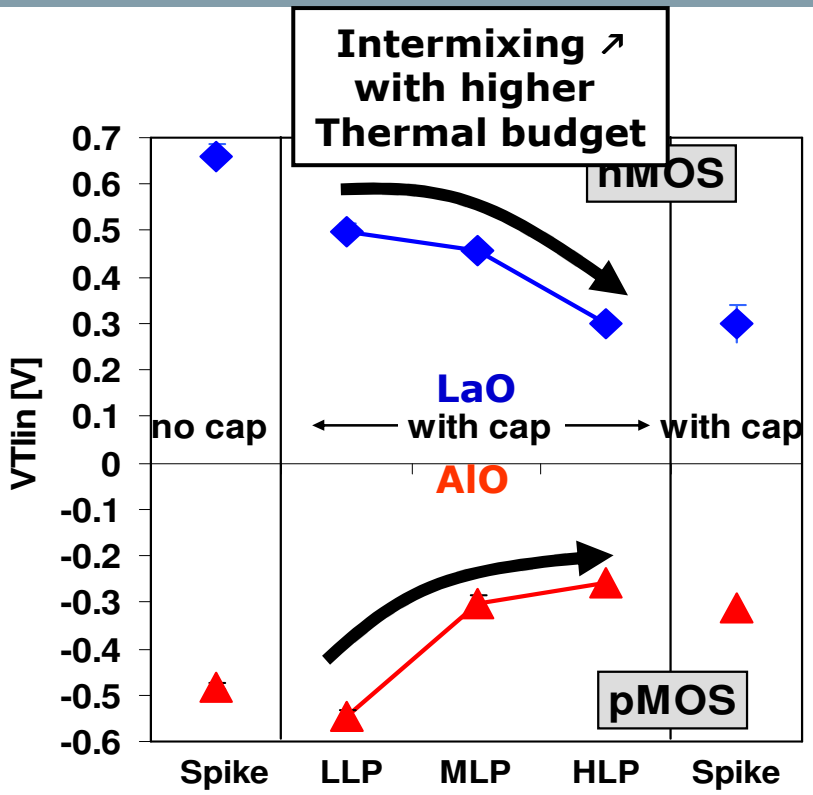


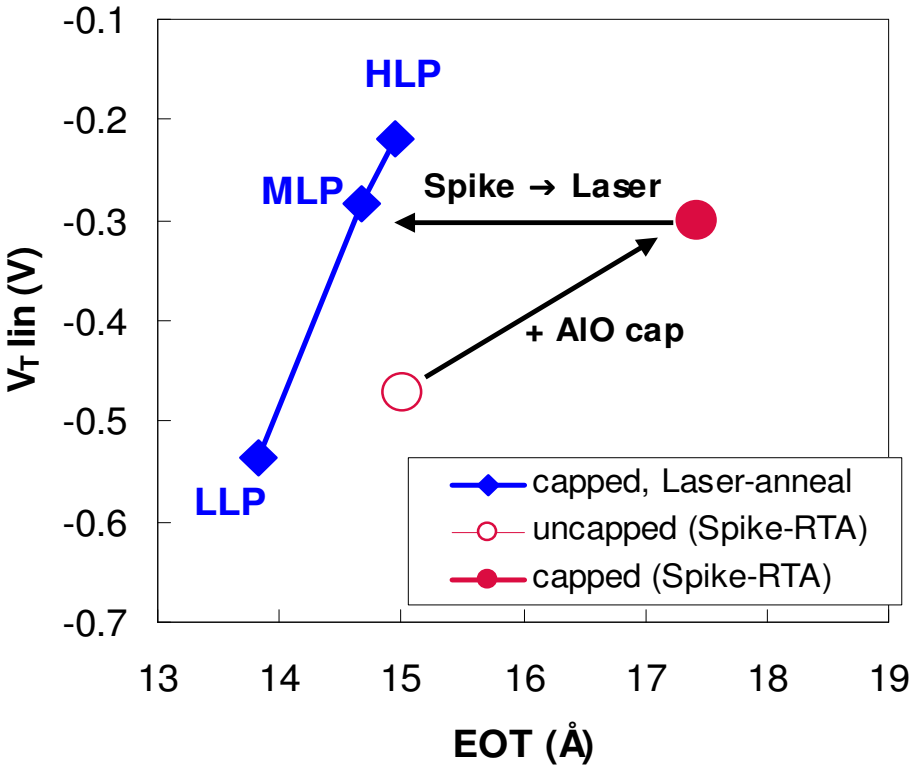


- High-K 'doping' with capping (eg, LaO, AlO) shifts eWF to band-edge → low nMOS & pMOS Vt's
- Thermal budget impacts capping "efficiency"

Controlled capping mixing with Laser

S. Kubicek et al., IEDM 2007



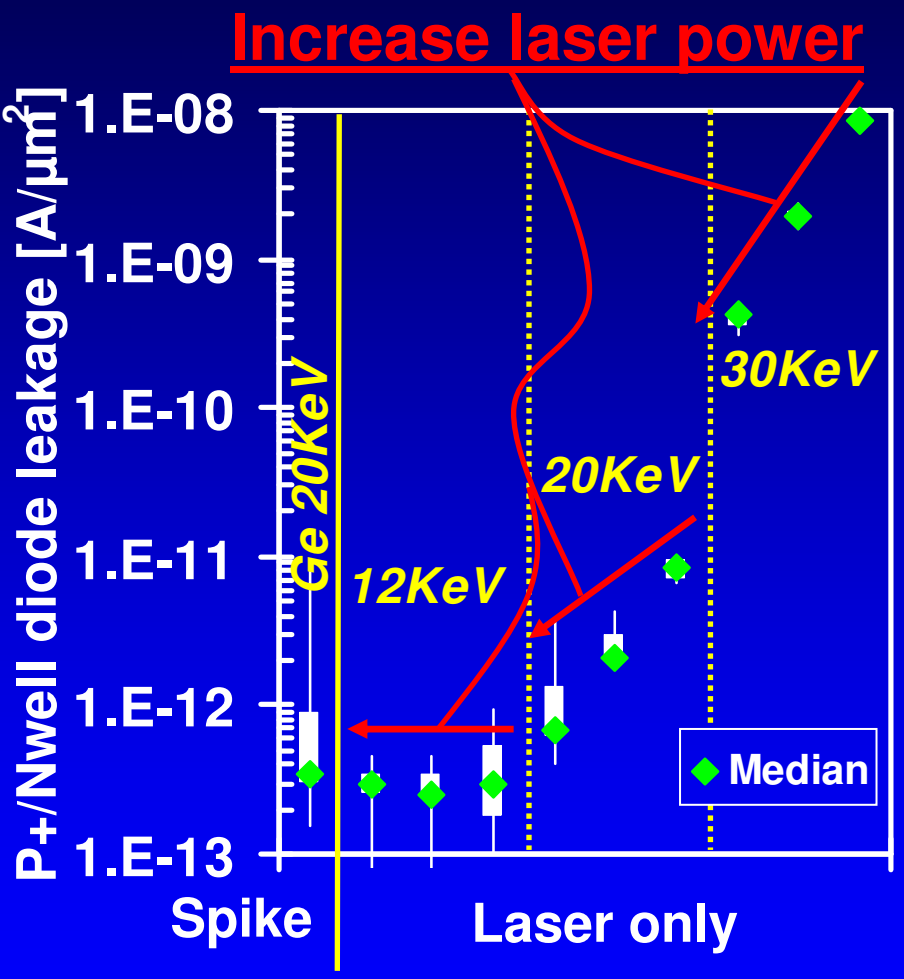


- Beside known potential for Lg scaling, Laser anneal has :
  - Benefit in EOT regrowth containment
  - Controlled capping mixing with High-K and/or IL

Outline

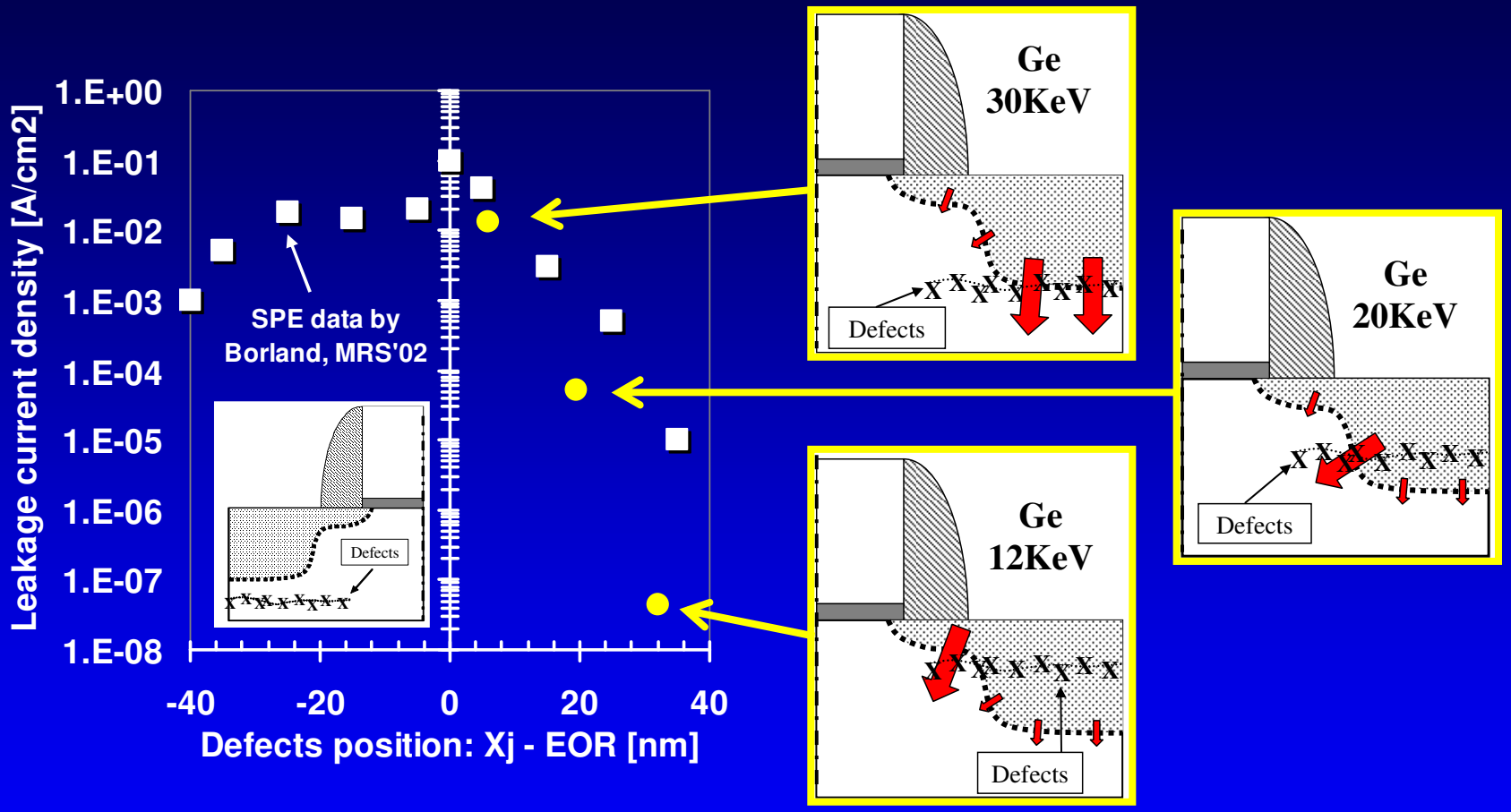
- Different paths for scaling & implications for USJ
- From low dopant diffusion with **co-implantation** …
- … to diffusion-less with **milli-second annealing (MSA)**
  - Fundamental advantage of milli-second anneal
  - Milli-second annealing entry point : combination with Spike
  - Aggressive junctions design with MSA-only
  - Compatibility with HKMG stacks
  - Impact on junction leakage (residual defects)
  - Compatibility with strain boosters
  - Process control & manufacturability
- Summary

Diode leakage



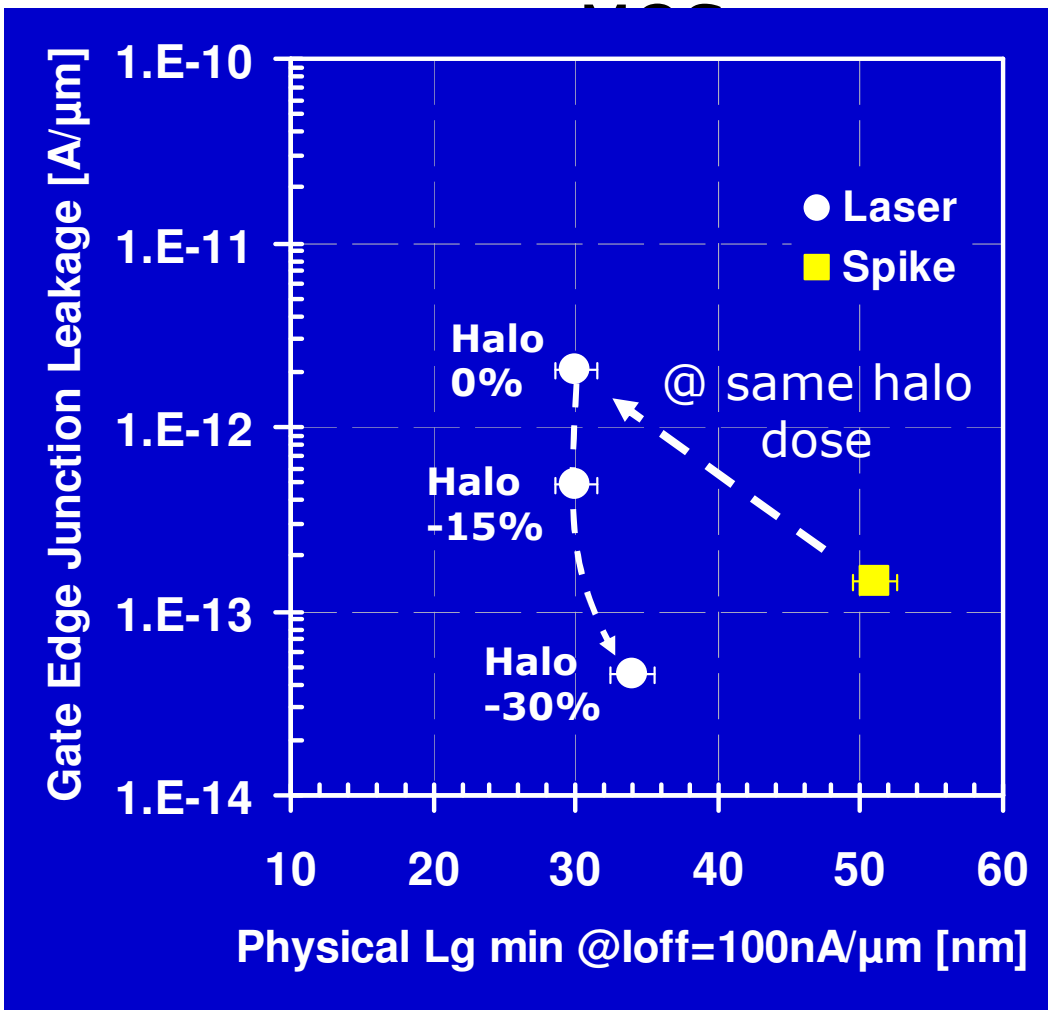
- High Ge energy increase dramatically the diode leakage
- Large leakage reduction for high power laser
- Similar leakage as spike could easily be achieved

Defects position



Defect position as function of junction depth is very important to contain the leakage

Junction leakage 'pragmatic' containment
Halo dose reduction



- Spike → Laser : 10x penalty in junction leakage
- Diffusion-less → **halo strength can be dramatically reduced** without SCE control loss
- Huge reduction in Band-To-Band tunneling leakage

Halo dose: 0% → As 3.5e13 cm^{-2}

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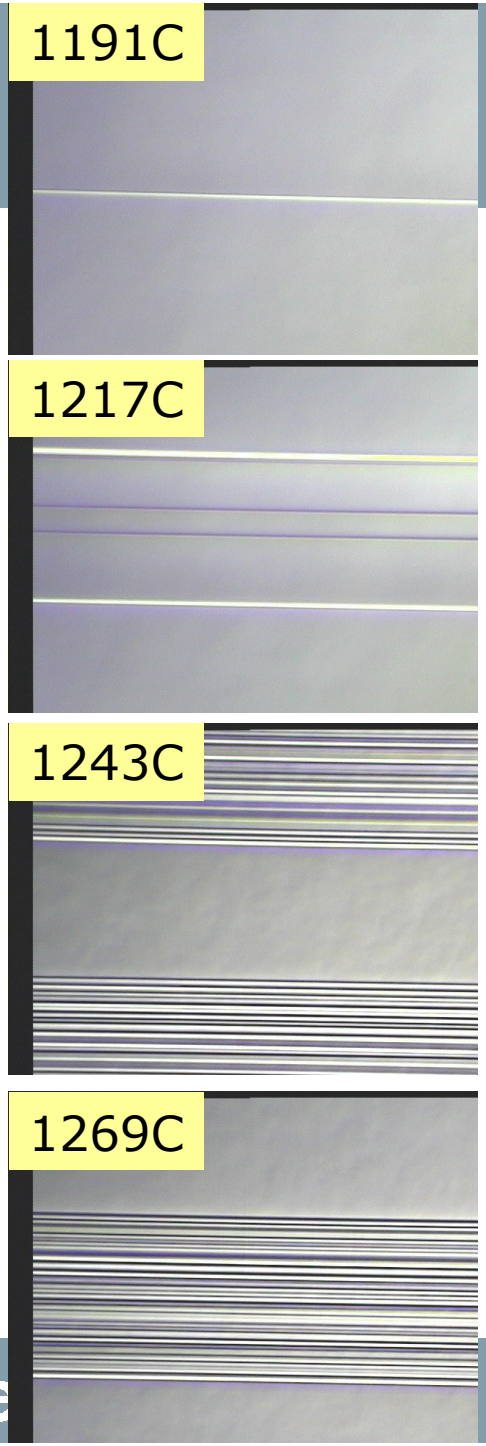
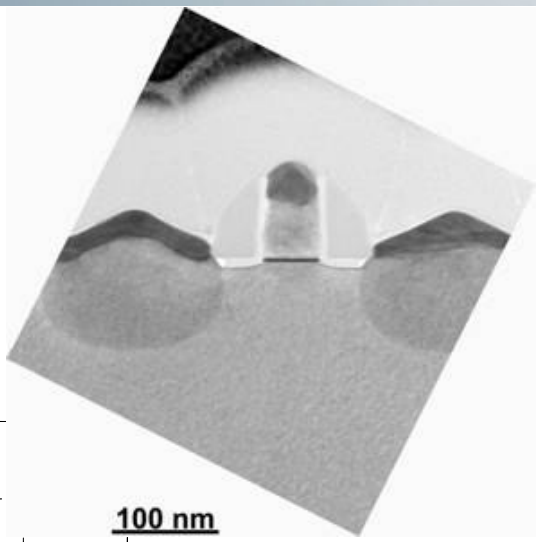
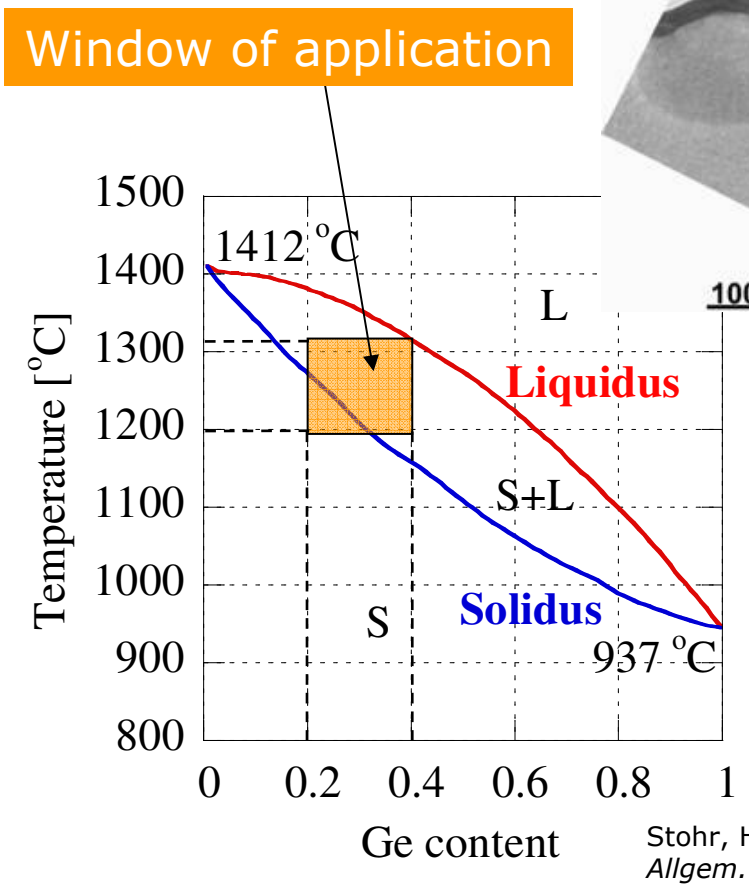
Impact of MSA peak Temperature on SiGe

Nomarsky images (SiGe ~25% Ge)



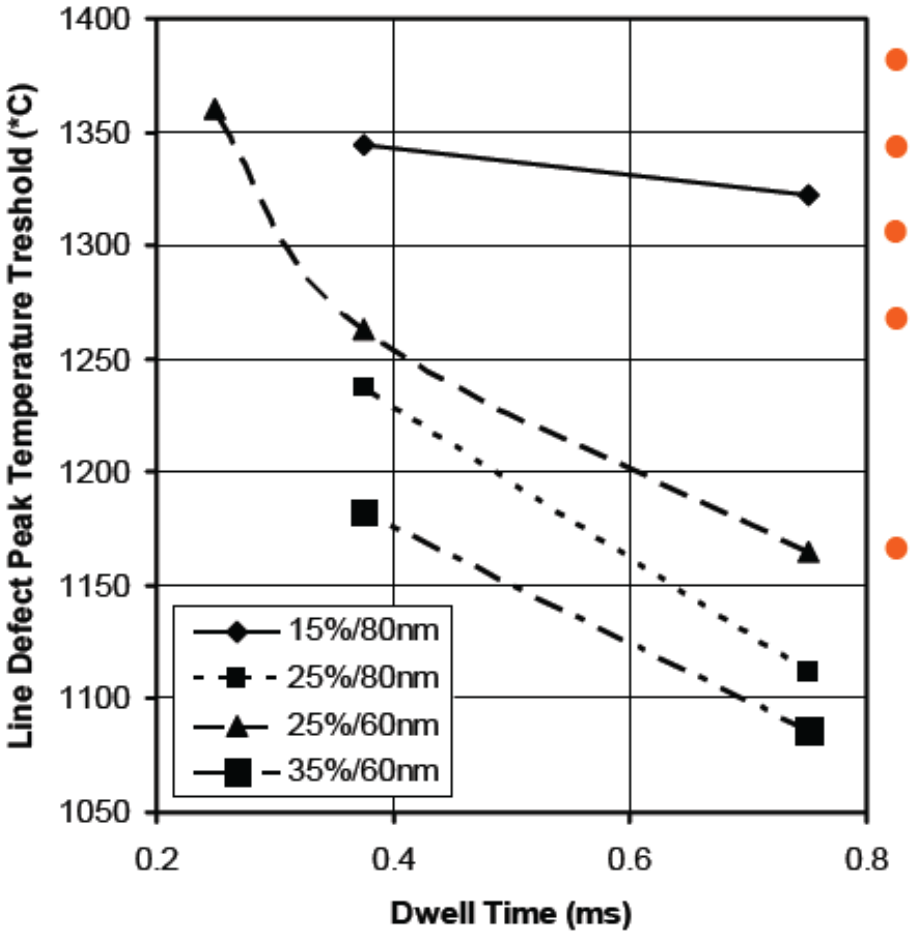
E. Rosseel [IMEC], RTP'07





Stohr, H., W. Klemm, *Z. Anorg. Allgem. Chem.* **241** , 1954, 305.

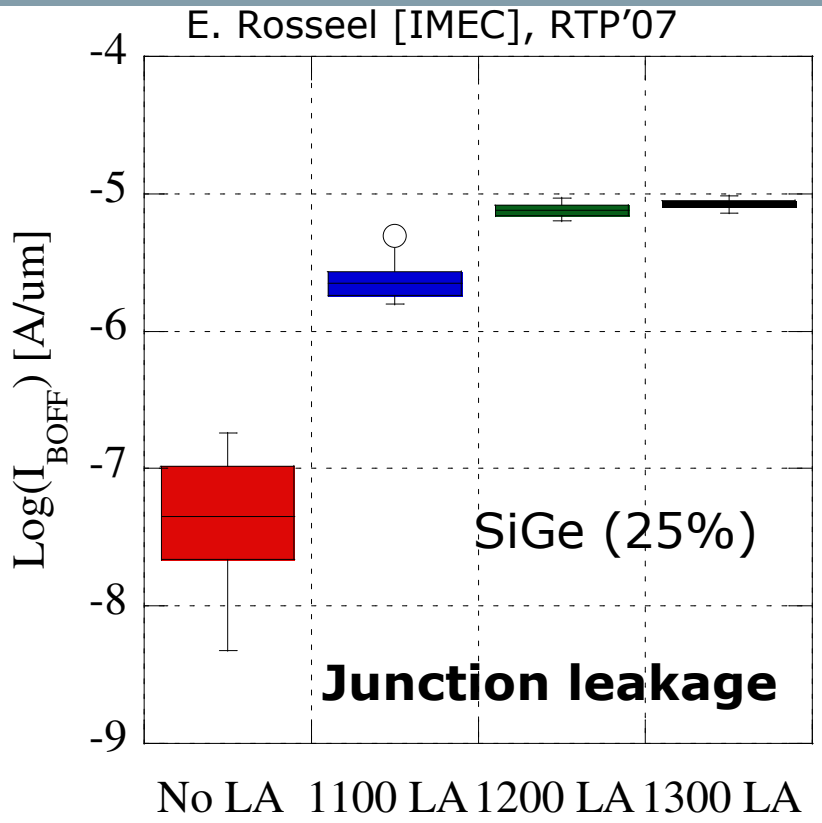
Effect of Dwell Time and Ge % on Temperature Onset of Line Defects

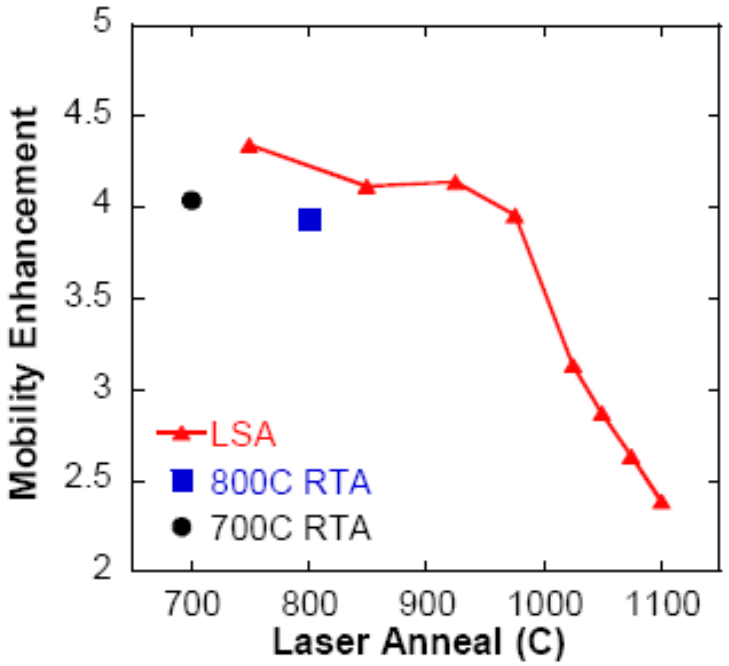


- Decrease with $\uparrow\tau$
- Lower LDPTT with ↑[Ge]
- Lower LDPTT with $\uparrow t_{SIGe}$
- Seems to be determined by effective stress and stress rate
- Shorter dwell times enable larger LDPTTs

E. Rosseel et al., IMEC/AMAT: IEEE RTP2007 Conference.

Impact of MSA peak Temperature on SiGe





C. Cheirigh et al., MIT, ECS Trans.,3(2), 2006

- Large junction leakage increase after Laser-anneal ➔ alternative integration flow required to alleviate the problem

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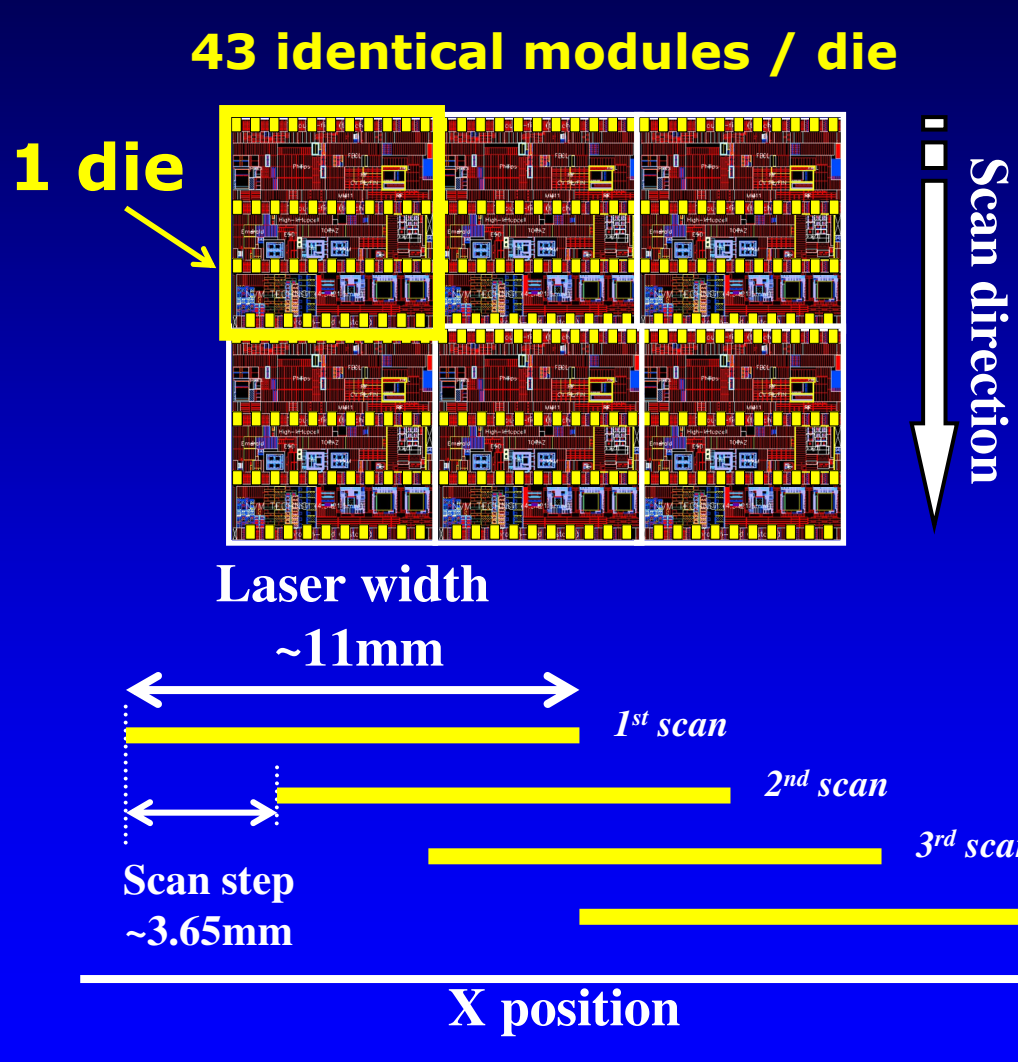
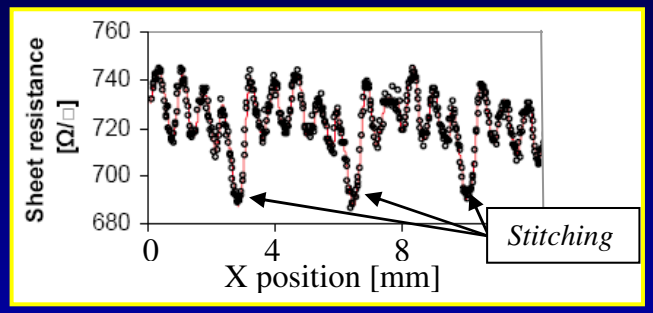
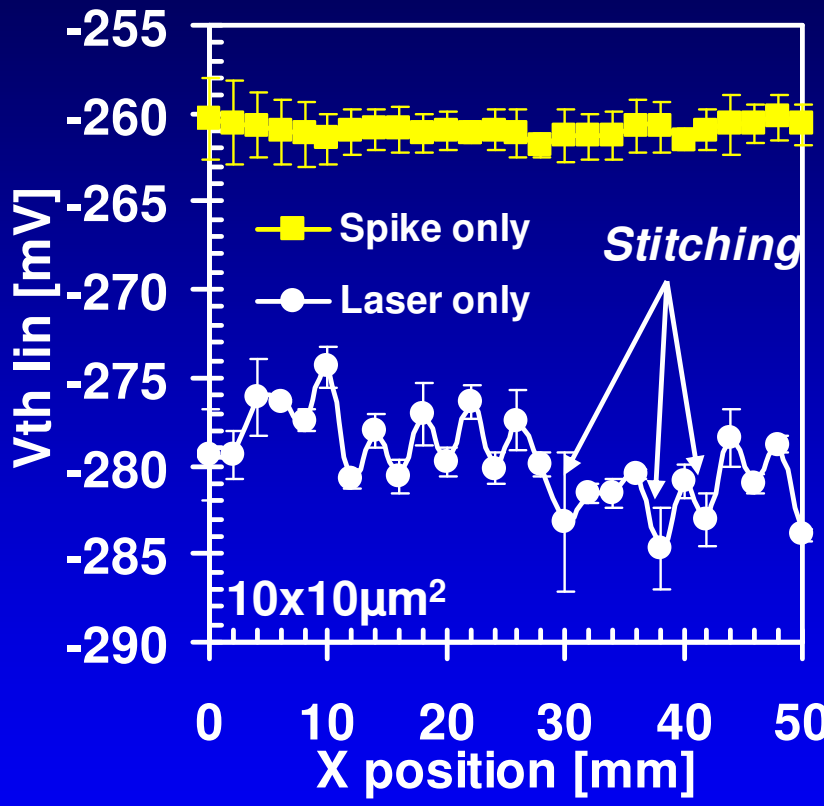
Stitching on devices?

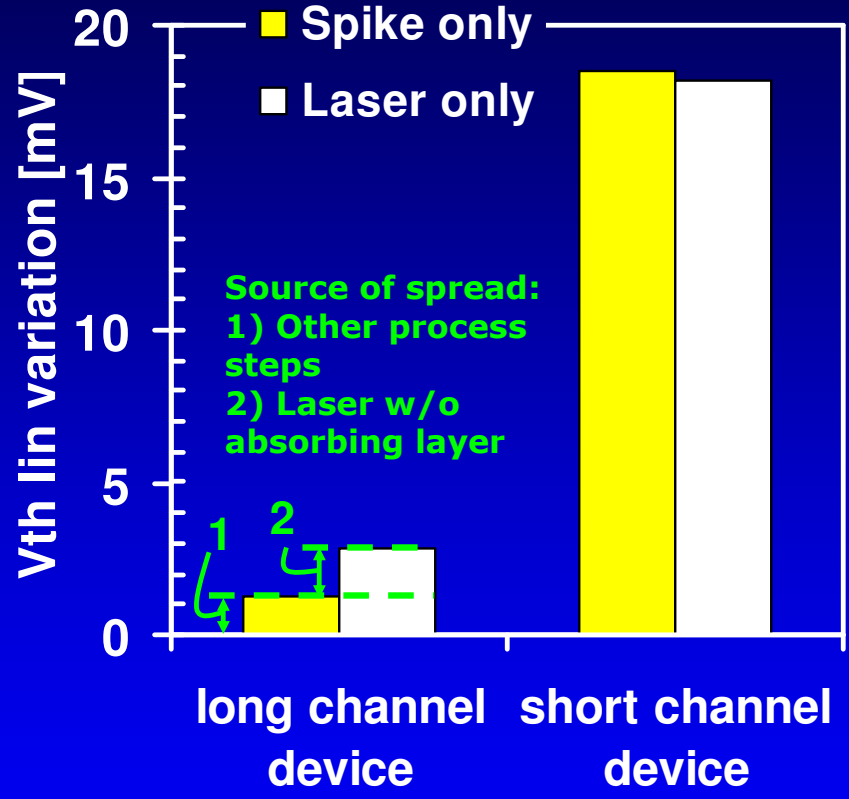




With the help of the Through Field module we have developed a methodology to quantify the electrical impact of the stitching

Impact on devices



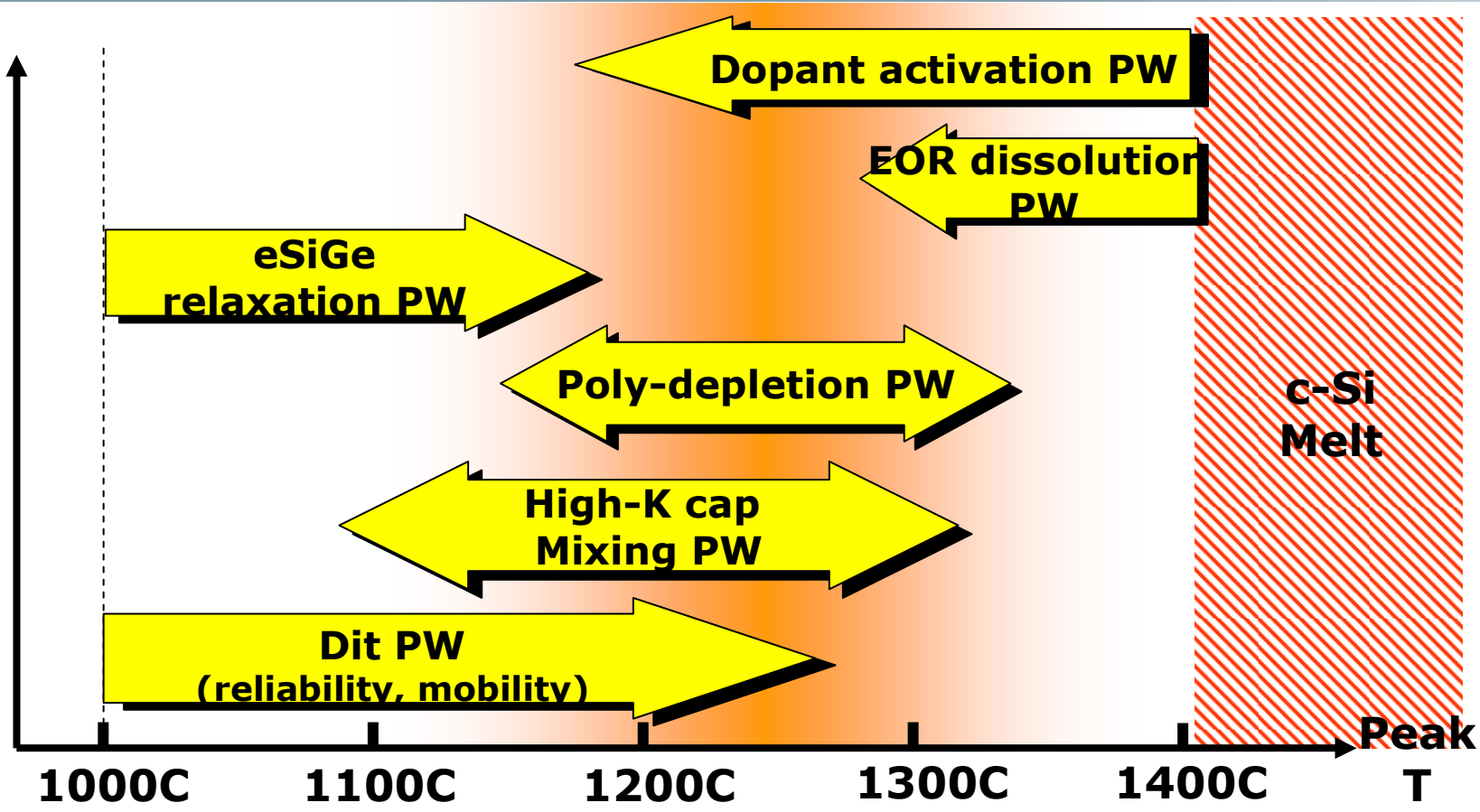


- Laser signature is clearly visible in long channel
- Impact is negligible in short channel compared to other sources of spread

Outline

- Different paths for scaling & implications for USJ
- From low dopant diffusion with **co-implantation** …
- … to diffusion-less with **milli-second annealing**
  - Fundamental advantage of milli-second anneal
  - Aggressive junctions design (with or without additional Spike-RTA)
  - Impact on junction leakage (residual defects)
  - Compatibility with HKMG stacks
  - Compatibility with strain boosters
  - Compatibility with alternative doping techniques
  - Process control & manufacturability
- Summary

Non-melt MSA : Process window is function of device architecture !



- MSA has many challenges/opportunities in advanced devices
- Overall Process Window is not unique = f(application, perf. boosters)