Performance of Laser Annealed Junctions in Advanced CMOS Devices

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think it. apply it.

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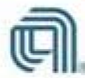
Ultra-Shallow Junction Challenges

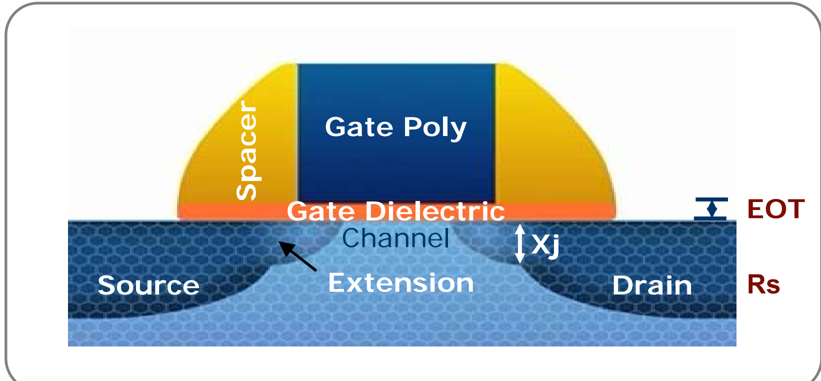


- Reducing junction depth
- Maintaining target sheet resistance
- More abrupt junctions
- Optimized gate/SDE overlap

- Two candidate USJ technologies
  - Co-implantation of diffusion-retarding species with spike anneal
  - Ultra-fast anneal (sub-melt laser anneal)

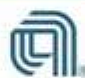
ITRS 2005

Tech. Node	90nm	65nm	45nm	32nm
X_j	<250Å	<170Å	<81Å	<59Å
PMOS R_s	<660Ω/sq	<760Ω/sq	<1430Ω/sq	<1380Ω/sq
Abruptness	4.1 nm/dec	2.8 nm/dec	2.0 nm/dec	1.4 nm/dec
Anneal	Spike	Transition		Advanced



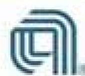
Junctions are becoming shallower and more difficult to form; Novel solutions required for implant and activation anneal

Purpose



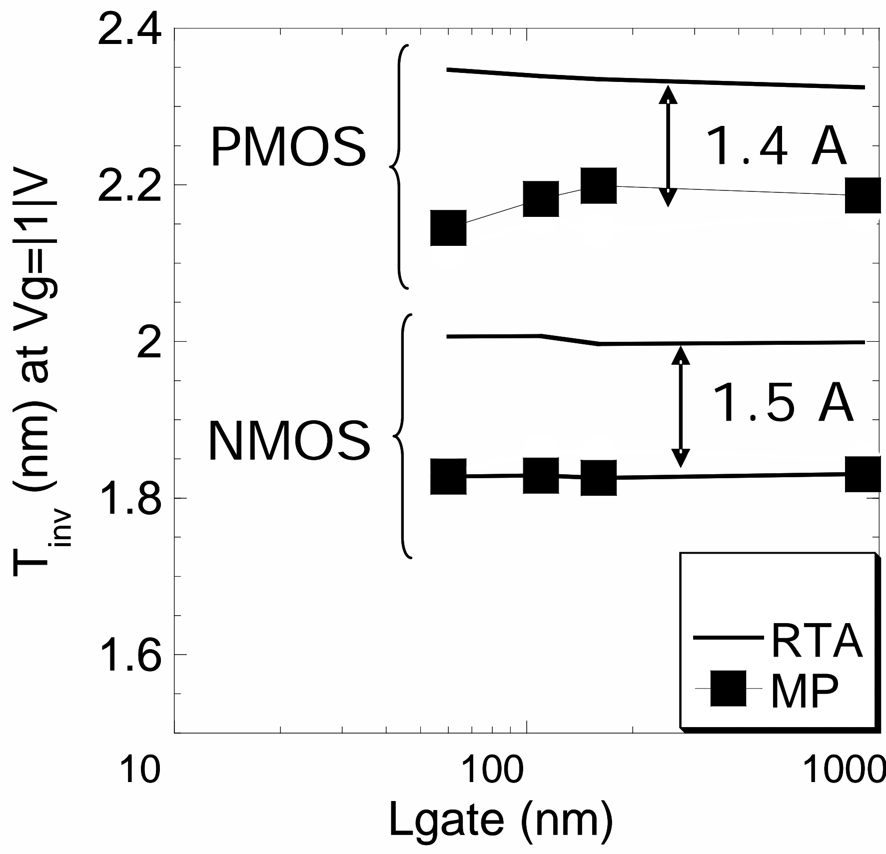
- Sub-melt laser anneal (LA) with minimal diffusion enables further transistor scaling
- Spike RTA plus LA improves Polysilicon Gate depletion
  - Delays introduction of complex metal gates
- Spike RTA plus LA improves SDE dopant activation
- Steep thermal gradients of LA induce mechanical stress at Si-SiON interface
  - Impact on transistor performance and reliability
- Study of influence of process conditions on transistor characteristics
  - LA temperature
  - N content in gate dielectric
  - Co-implanted F
  - Sequence of spike anneal, LA, and absorber layer deposition

Experimental Approach



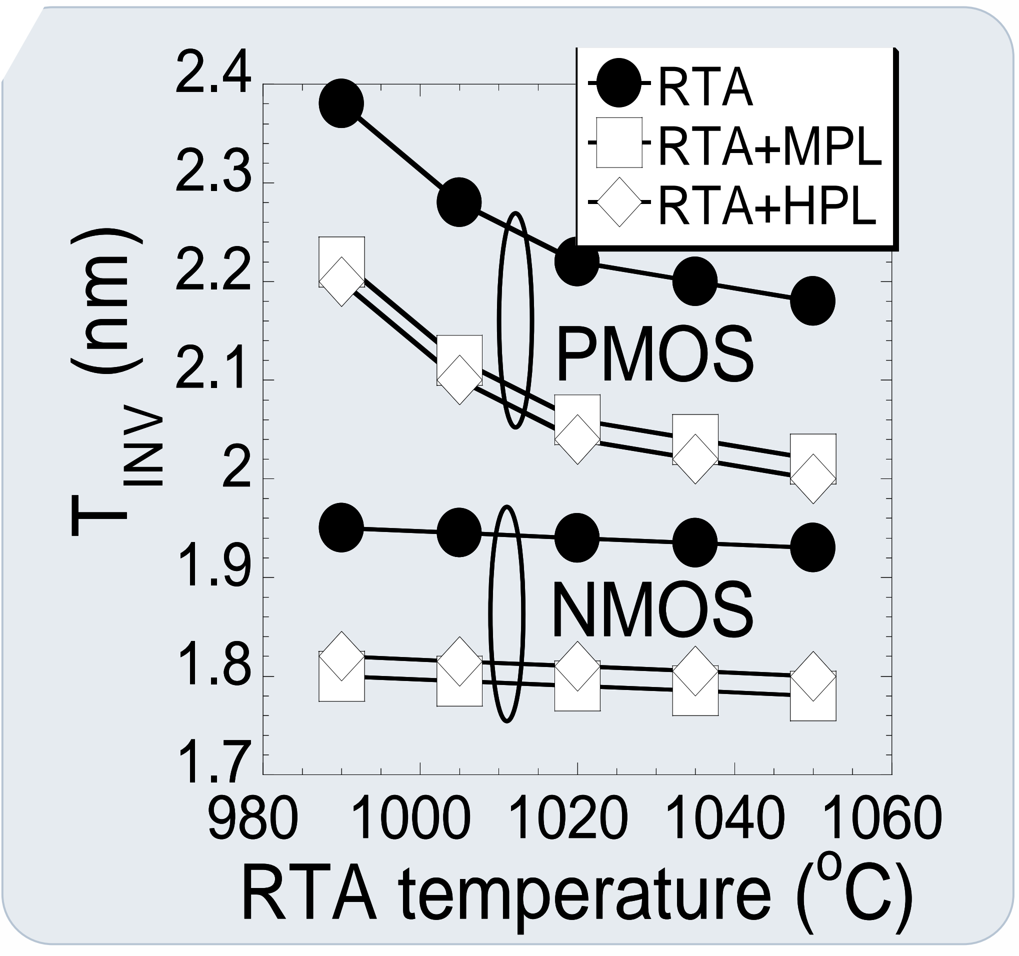
- Conventional SiON/poly-Si CMOS baseline
  - Gate dielectric
    - 1.5nm and 2.0nm thin oxides with 14% N
    - 1.5nm thin oxides with 5% and 10% N
  - B co-implanted with F into PMOS source/drain extension and poly-Si gate
    - High dose F
    - Lower dose F
    - No F
  - 65nm wide spacer
  - HDD implants
  - Spike anneal followed by LA
    - Modulate peak LA temperature by changing laser power
    - 1200°C (MPL) and 1300°C (HPL)
  - NiSi formation

Polysilicon Gate Depletion Improvement (T_{inv}) with Laser Anneal after Spike Anneal



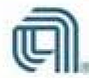
- 1.4-1.5Å reduction in T_{inv} with LA after spike anneal for PMOS and NMOS due to improved dopant activation in Polysilicon Gates
- Delays need to introduce Metal Gates

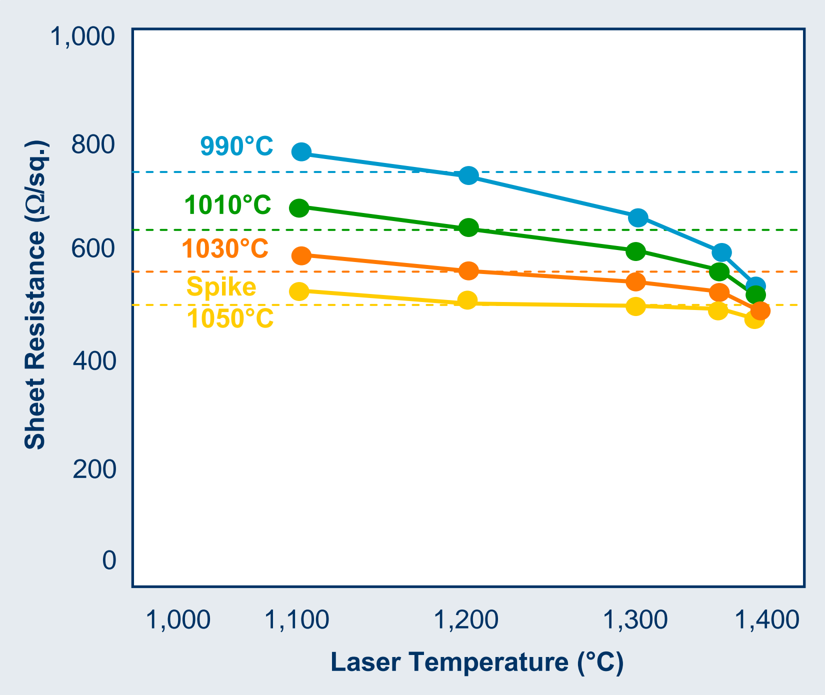
Polysilicon Gate Depletion Improvement (T_{INV}) with LA after Spike Anneal



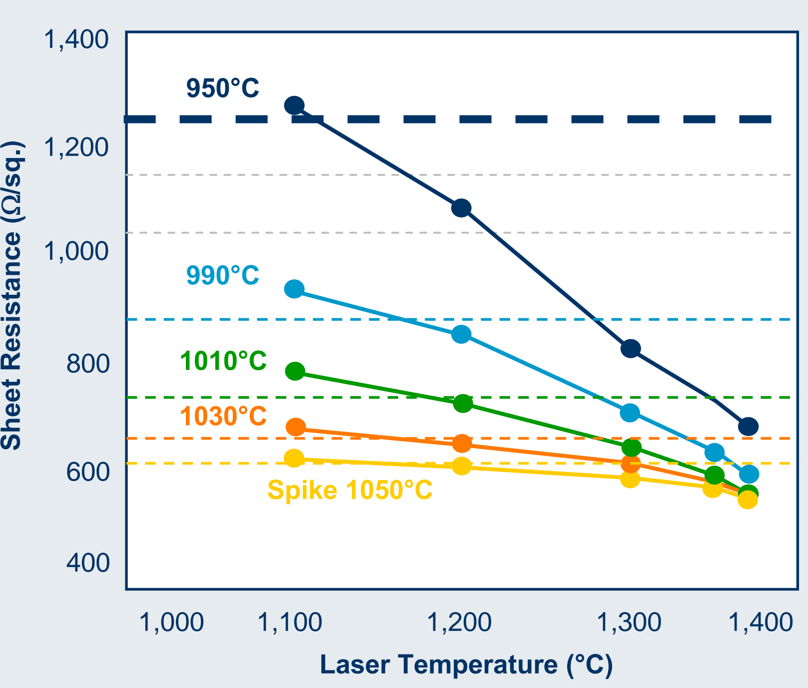
- **1.5Å reduction in T_{INV} with LA after spike anneal for PMOS and NMOS**
- **Both high and medium power LA lead to equivalent gain**

Spike + Laser Impact on R_s





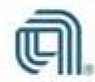
As 1 keV, 1E15/cm2

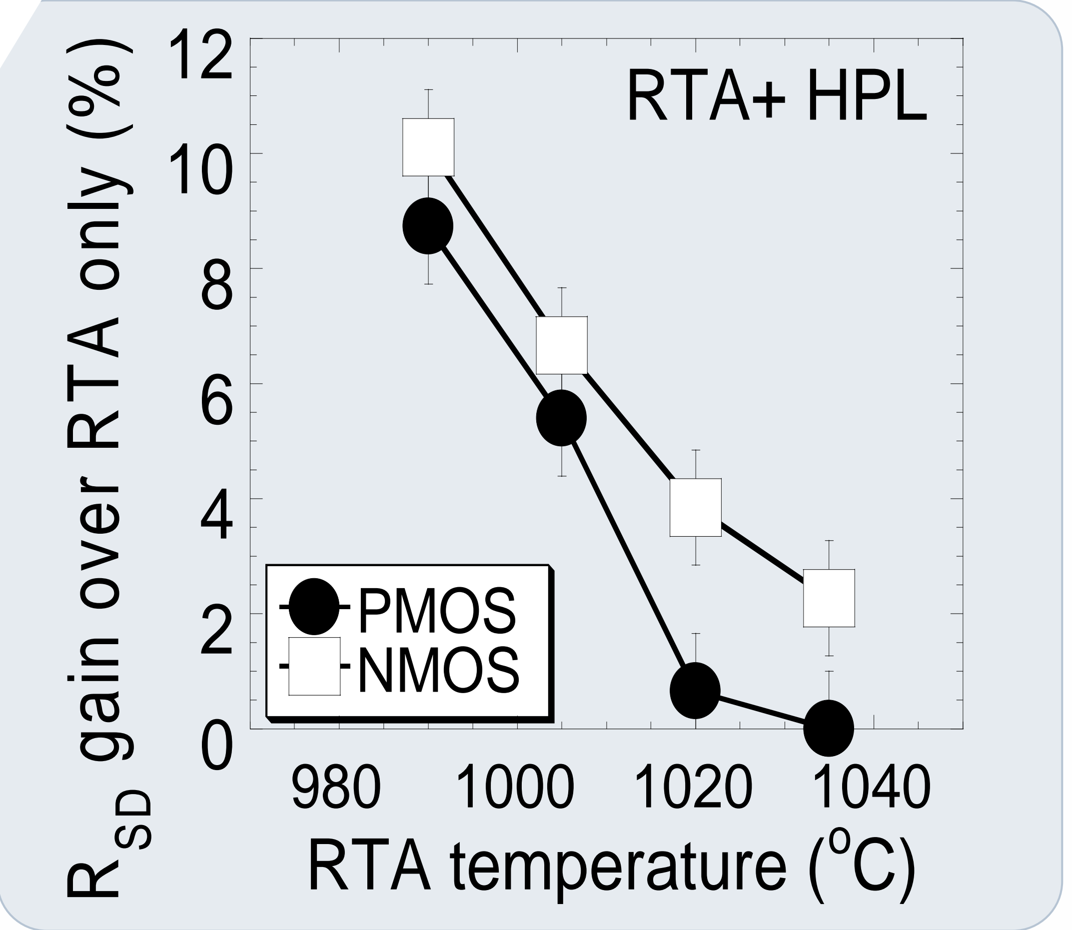


- Spike + Laser is optimal for low-T Spike (<1010°C)
- Spike + Laser impact is significant on Arsenic

R_s sensitivity to LA temperature increases dramatically as spike T decreases (i.e. ≤ 32nm devices)

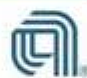
Improvement in Transistor Series Resistance (R_{SD}) with Spike RTA + LA





RTA + high power LA (HPL) produces additional gain in R_{SD}, especially for lower RTA temperatures

Spike Plus LA for 32nm C Co-Implant Junctions



Sheet Resistance (ohms/sq.)

1200
1000
800
600
400
200
0

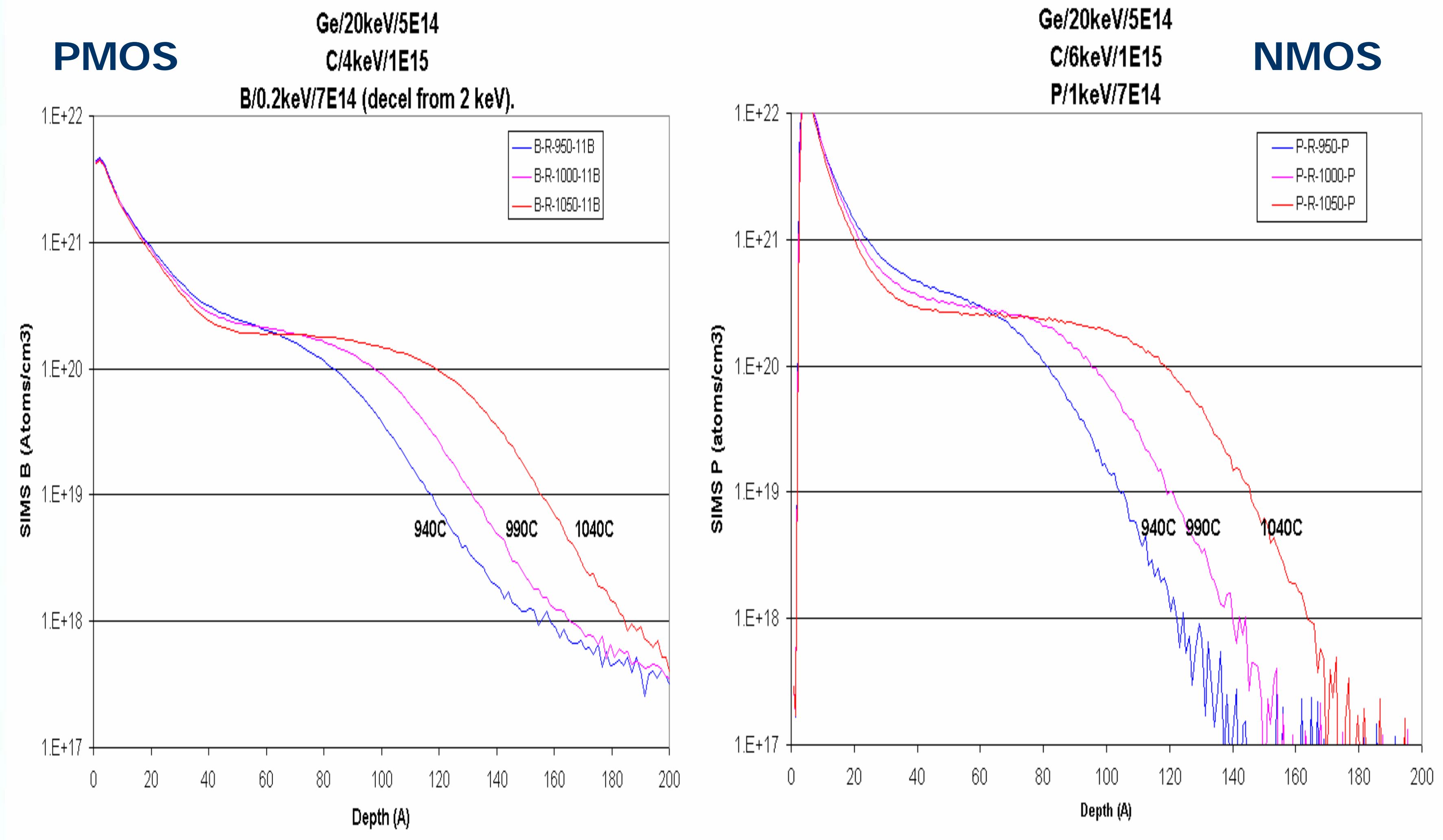
900 950 1000 1050 1100

Spike Temperature (C)

- Spike + 1350C LA
- Spike + 1200C LA
- Spike Only

High-temperature LA produces ~20% dopant activation boost for 32nm PMOS junctions (Xj ~ 15nm)

Further Extendibility of C Co-Implant with Spike Anneal



Continued decrease of spike temperature extends co-implant technology to ≤32 nm junctions

Improved S/D Resistance with F or C Co-Implant with Spike + Laser Anneal (SiON + FUSI Gate)

C + 1030°C Spike + Laser

Ref. BF_2 + 1050°C Spike

C + 1050°C Spike + Laser

F + 1030°C Spike + Laser

F + 1050°C Spike + Laser

Ref. BF2

1100C Laser

1300C Laser

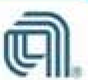
Rsd (Ohm um)

600
550
500
450
400
350
300

0
20
40
60
80

Lgate at Ioff=60nA/um

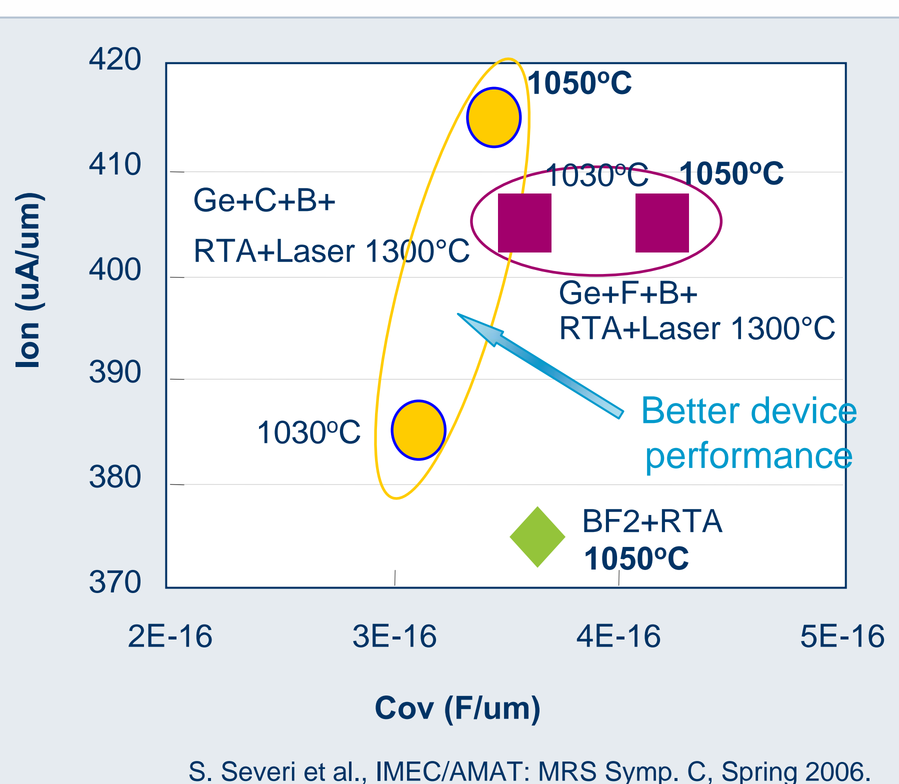
- C co-implantation improves both short channel effects and series resistance
- Higher laser anneal temperature provides further R_{sd} reduction (enhanced dopant activation)



Improved Device Performance and S/D Activation with LA

PMOS B Co-Implant with Spike RTA + Laser Anneal (SiON + FUSI Gate)

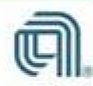
- 10% I_{on} gain is obtained for same C_{ov} due to enhanced dopant activation and reduced R_{sd}
- Lateral dopant diffusion is suppressed with C co-implant, producing smaller C_{ov}



S. Severi et al., IMEC/AMAT: MRS Symp. C, Spring 2006.

Laser anneal enhances I_{on} and maintains reduced C_{ov} obtained with C co-implant

Improvement in Performance/Short Channel Effect Trade-Off due to C Co-Implant and Spike + Laser Anneal



Idsat @ Ioff=60nA/um (uA/um)

800
750
700
650
600
550
500
450
400
350
300

20 30 40 50 60

Lgmin @ Ioff=60nA/um

NMOS

PMOS

◆ Ge+C+P Spike + 1200C Laser
■ As Spike + 1200C Laser
▲ Ge+C+B Spike
× Ge+C+B Spike + 1200C Laser
⋇ Ge+C+B Spike + 1300C Laser

PMOS: Reduced SCE (L_{gmin}) and small I_{dsat} improvement with Laser Anneal
NMOS: High P activation leads to better performance than As

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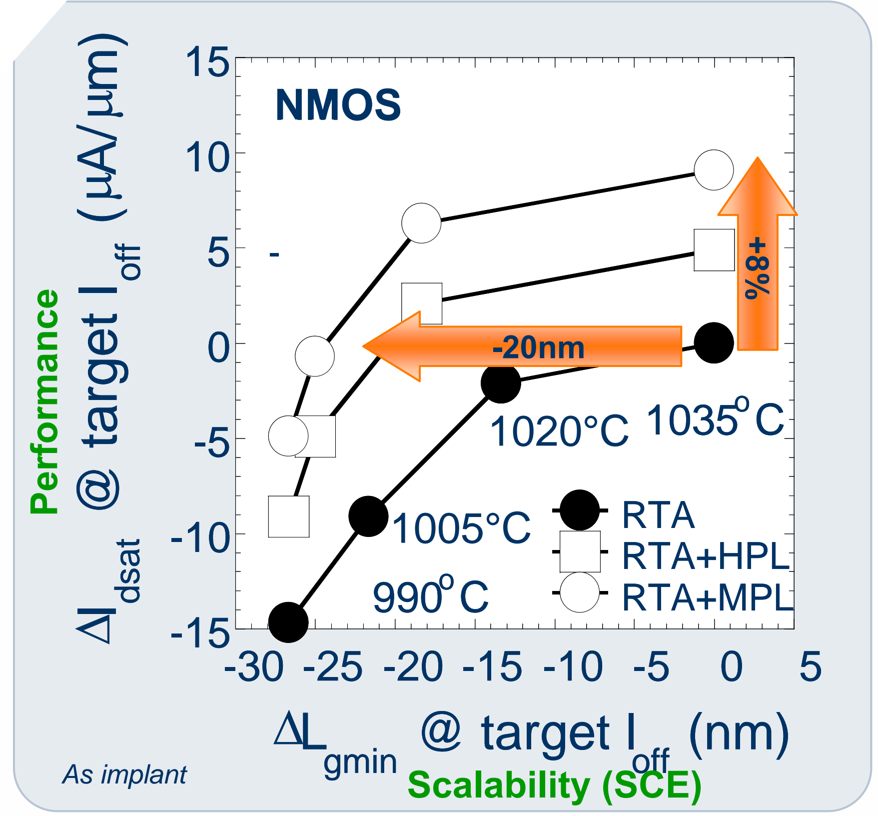
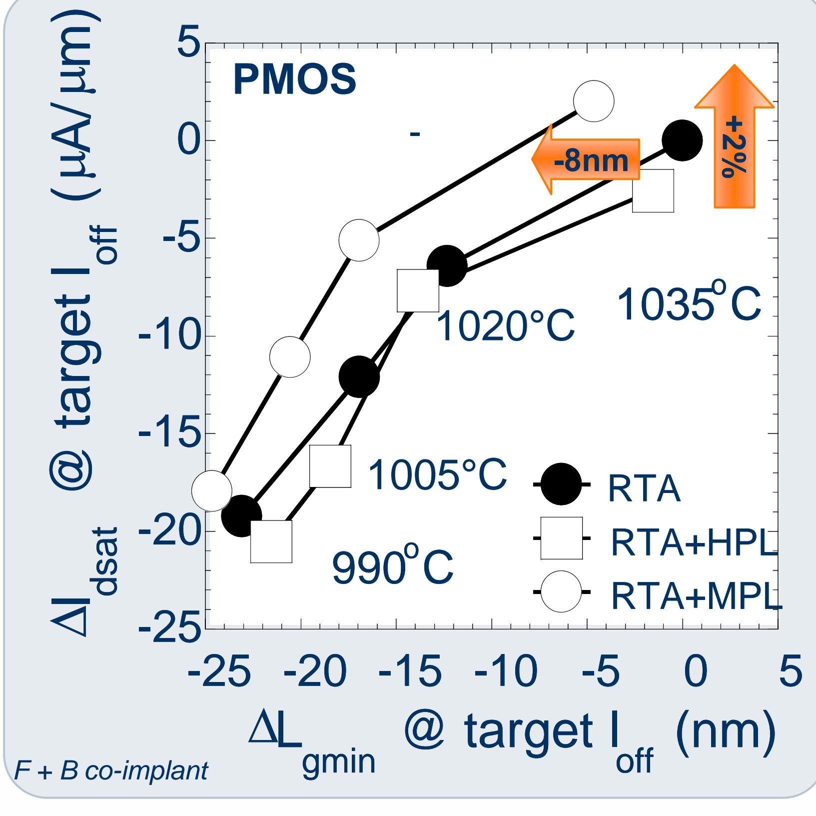
Spike Anneal + LA Enables Drive Current and Short Channel Effect (SCE) Improvements





- T_{INV} and R_{SD} gains lead to improvement in performance/short channel effect trade-off for NMOS and PMOS
- Medium power LA leads to higher performance than high power LA

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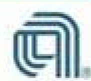
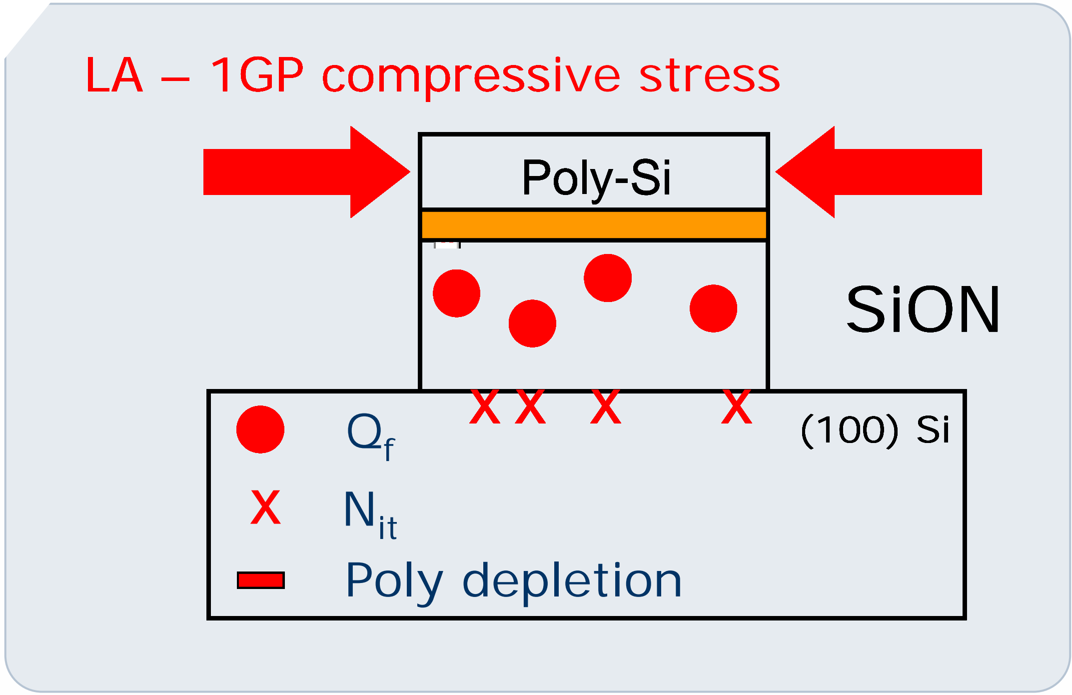
APPLIED MATERIALS.

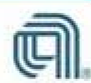
Model of Thermo-Mechanical Stress (TMS) at SiON Interface due to LA

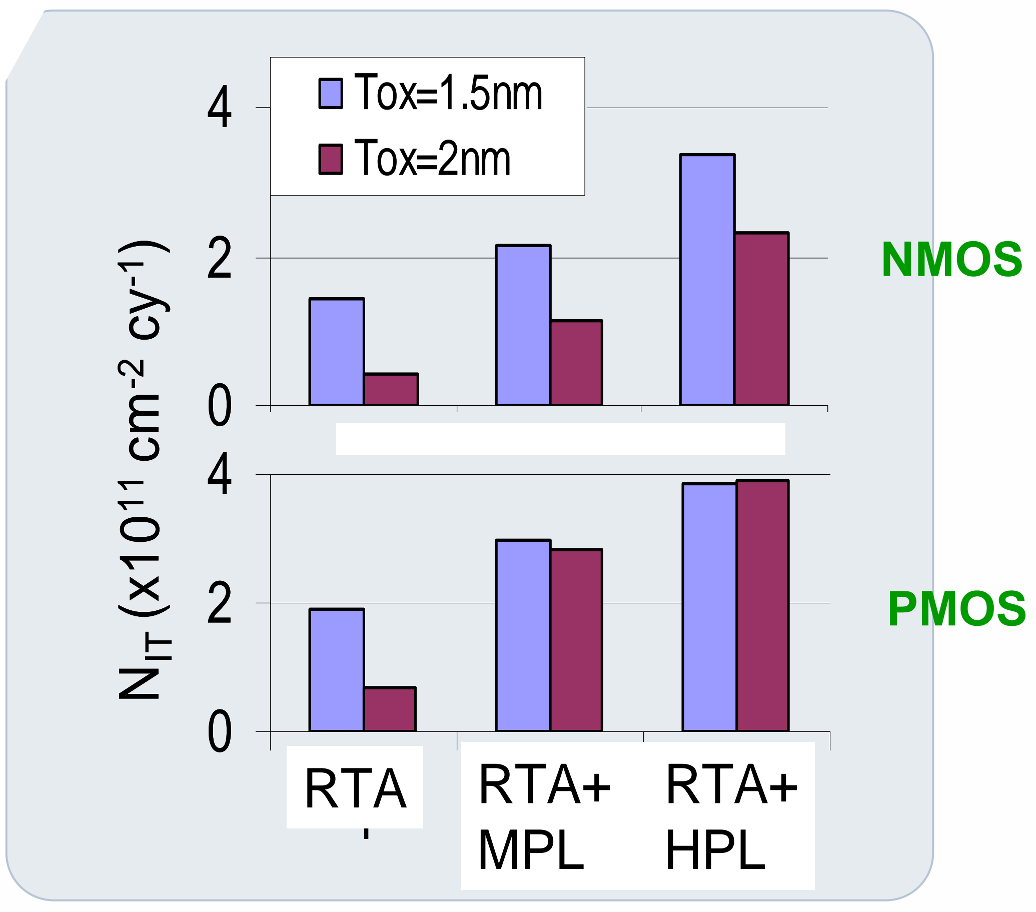




Thermal and mechanical stresses during high-temperature LA induce additional interface traps (N_{it}) and fixed charges (Q_f) in gate dielectric

Increase in Interface State Density due to LA



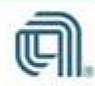


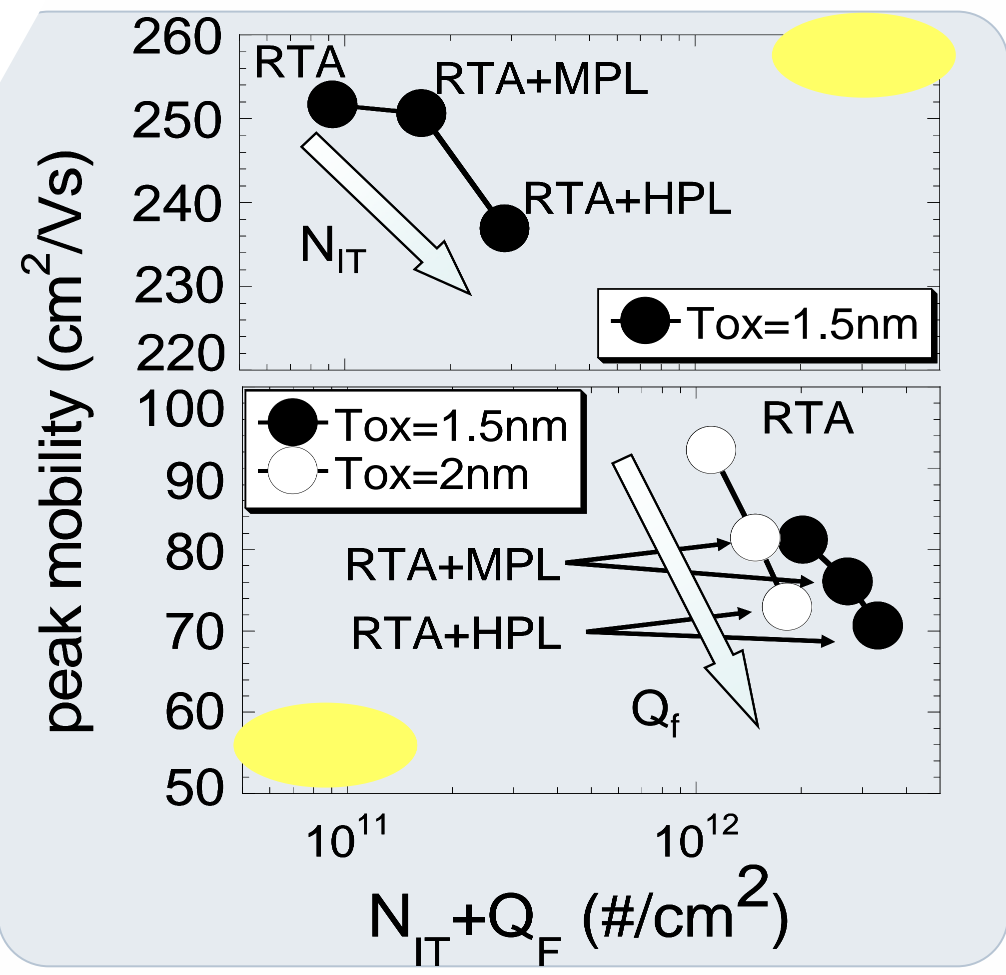
NMOS

PMOS

Higher LA temperature increases Si dangling bonds and interface traps at Si/SiON interface

Effect of Interface Traps and Fixed Charges in Gate Dielectrics on Peak Mobility





Medium power LA minimizes stress, N_{it} and Q_f, and mobility and device performance degradation

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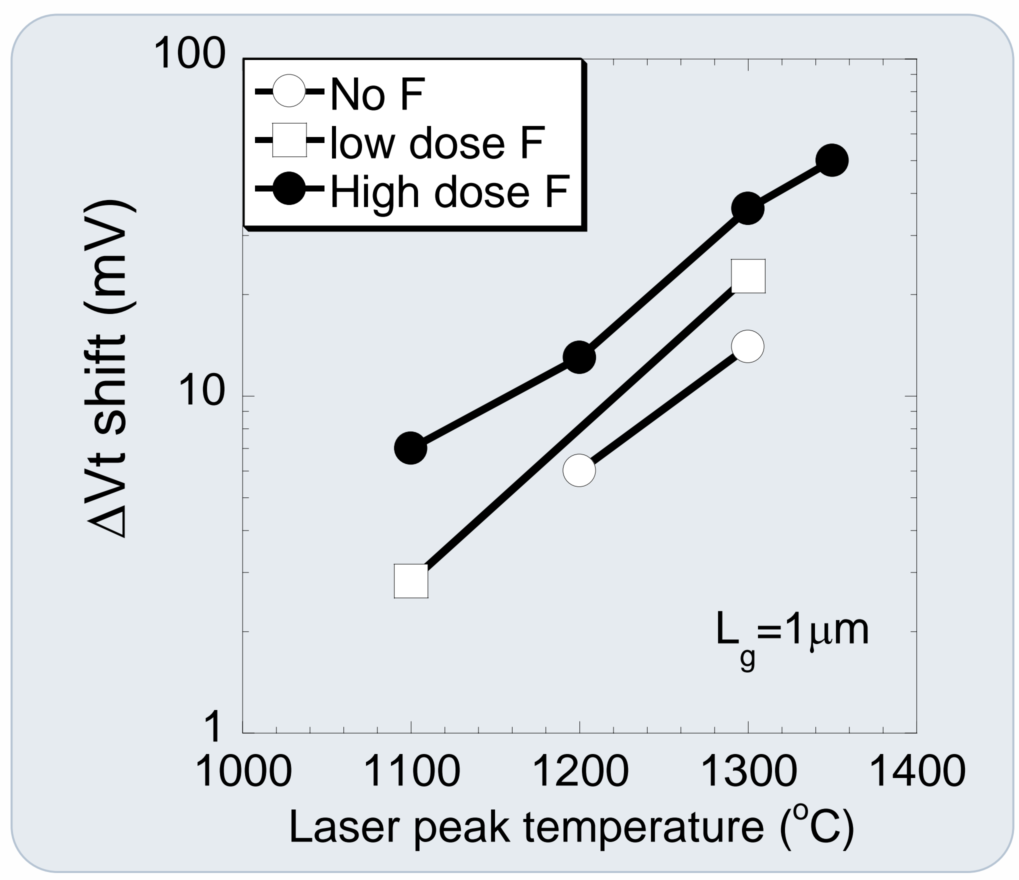
Effect of Co-Implant on Long Channel Transistor Threshold Voltage (V_t) Difference between RTA and RTA+LA



- ΔV_t shift is reduced by decreasing or eliminating (use C) co-implanted F
- Indicates smaller amount of added interface states at Si-SiON interface due to stresses from LA thermal gradients

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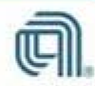
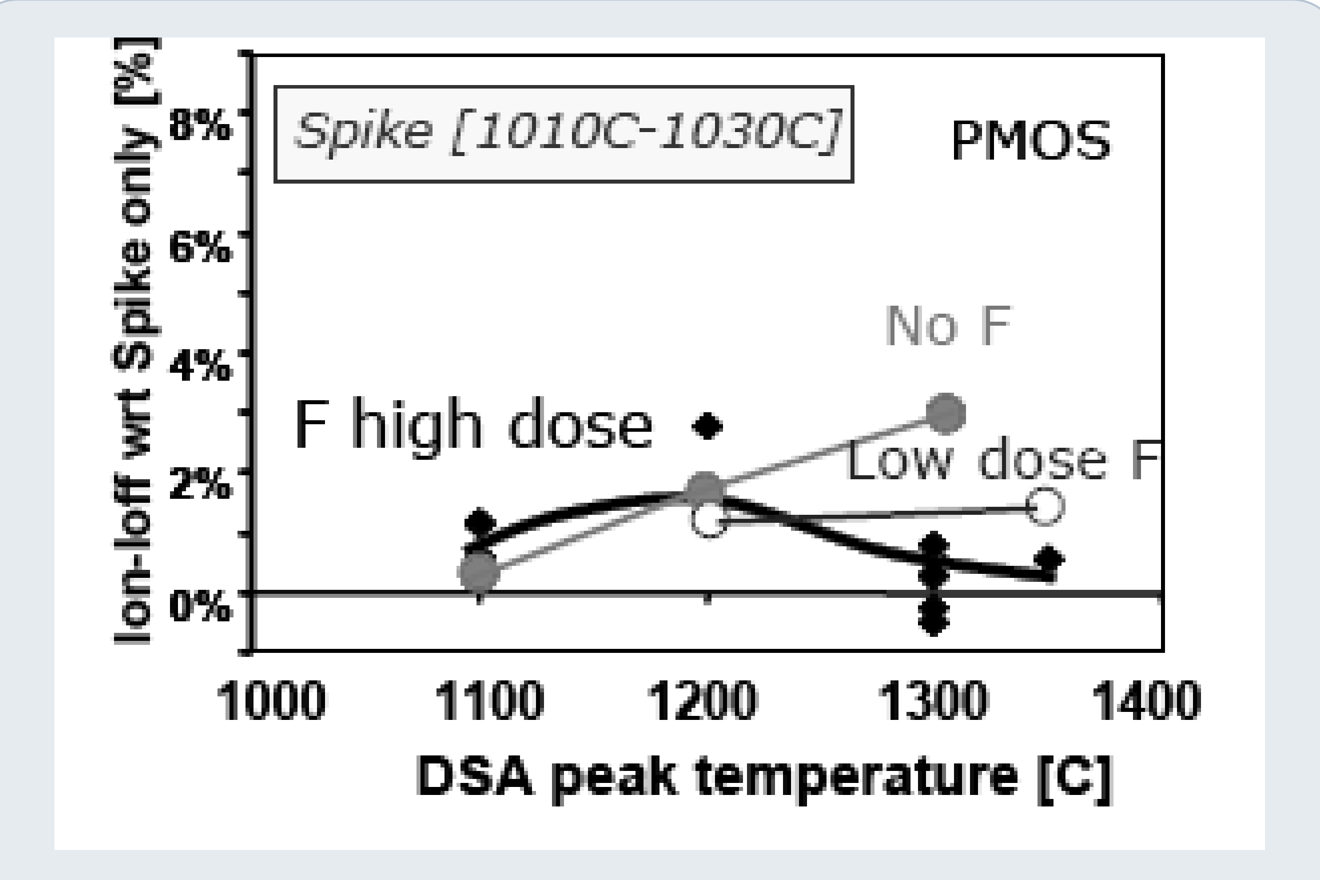
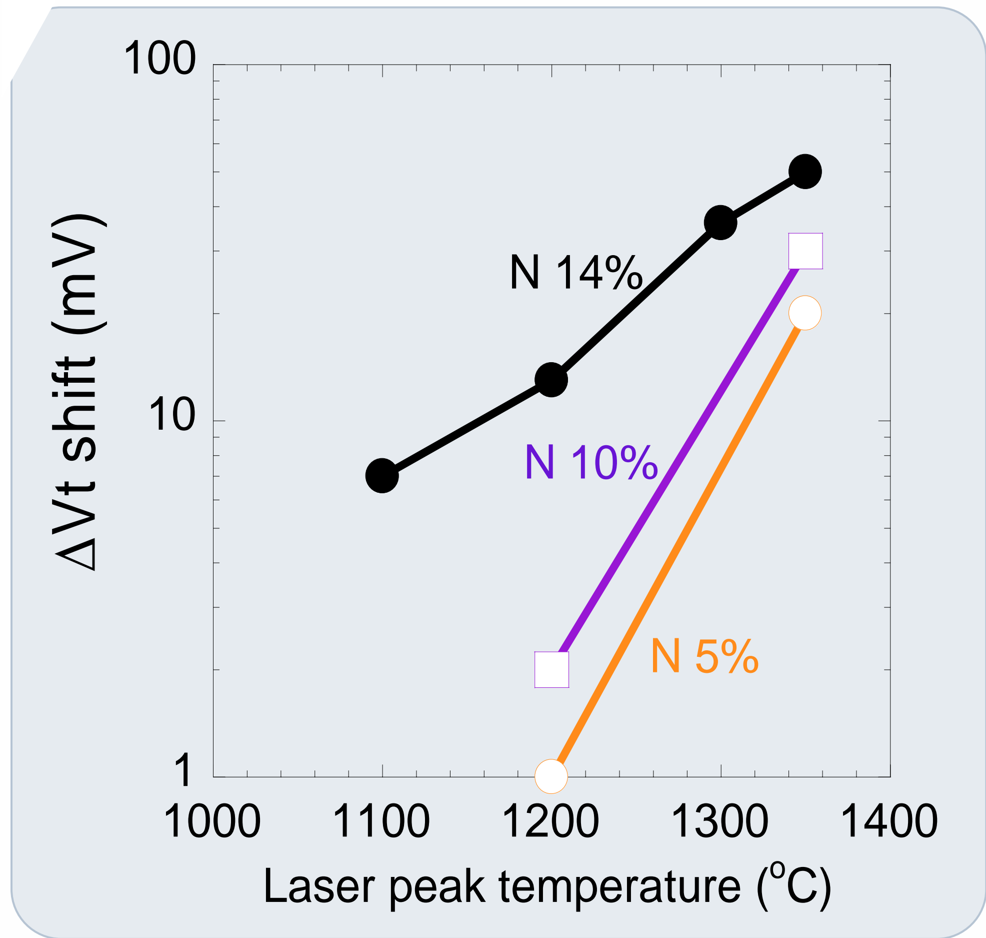
Performance Improvement with C Co-Implant and Spike + High-Temperature Laser Anneal





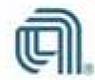
- High-dose F co-implant results in no I_{on}-I_{off} improvement with additional 1300˚C LA
- C co-implant (no F) produces increasing I_{on}-I_{off} improvement with LA temperature, reflecting lower generation of interface states

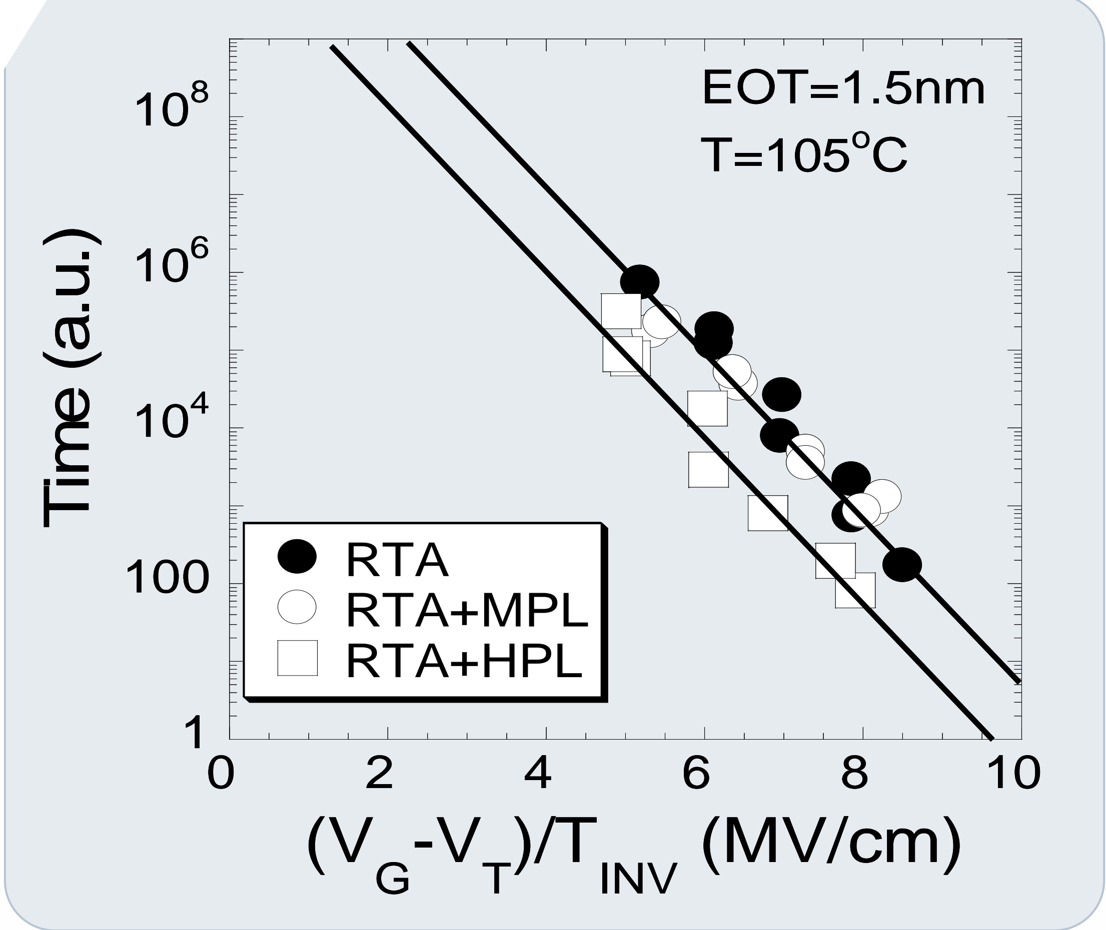
Effect of Gate Dielectric N Content on Long Channel Transistor V_t Difference between RTA and RTA+LA



Decreasing N content in dielectric reduces N_{it} and ΔV_t shift and improves possibility to use higher LA power

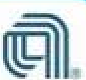
Transistor Lifetime (NBTI) for RTA alone, RTA+MPL and RTA+HPL





Transistor lifetime with medium power LA is same as for spike RTA alone, even with high F dose and high N content in dielectric

Effect of Absorber Layer (AL) and Thermal (Spike + LA) Process Sequence



PMOS

Idsat @ Ioff=80nA/um [uA/um]

380, 360, 340, 330, 320, 310, 300, 290, 280

+9%

-10%

Ref.

Flow C

Flow A

Flow B

Spike | Spike + Laser-1200C | Spike + Laser-1350C

NMOS

AL bef. Spike ← AL aft. Spike

Idsat @ Ioff=80nA/um [uA/um]

800, 780, 760, 740, 720, 700

Flow B

Flow A

Flow C

+7 %

A L/Spike

Spike ref.

40, 45, 50, 55, 60, 65, 70

Lgmin @ 80nA/um [nm]

SDE

Spacer

HDD

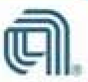
A	B	C
Spike RTA	AL	AL
AL	Spike RTA	Laser
Laser	Laser	Spike RTA

AL removal

NiSi

9% PMOS performance improvement over spike reference with AL/LA/spike, while maintaining 7% NMOS gain

Device Mobility and Reliability with AL/LA/Spike Sequence



Mobility

SDE
Spacer
HDD
A: Spike RTA → AL → Laser
B: AL → Spike RTA → Laser
C: AL → Laser → Spike RTA
AL removal
NiSi

μ[cm^2/Vs]: 0, 20, 40, 60, 80, 100

E_{eff}[cm/MV]: 0.2, 0.5, 0.8

A — D7 1350C LA
B — D8 1350C LA
C — D10 1350C LA
A ----- D7 spike
B ----- D8 spike
C ----- D10 spike

NBTI Lifetime

Lifetime@30mV V_{th} shift [s]: 10, 100, 1000, 10^4, 10^5, 10^6, 10^7, 10^8, 10^9

$(V_G - V_{th})$[V]: 0.7, 1

10years

A ◆ D7 1350C LA
B ● D8 1350C LA
C ■ D10 1350C LA
○ Spike anneal

AL/LA/spike results in same NBTI lifetime and mobility with 1350°C LA as spike reference

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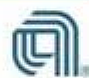
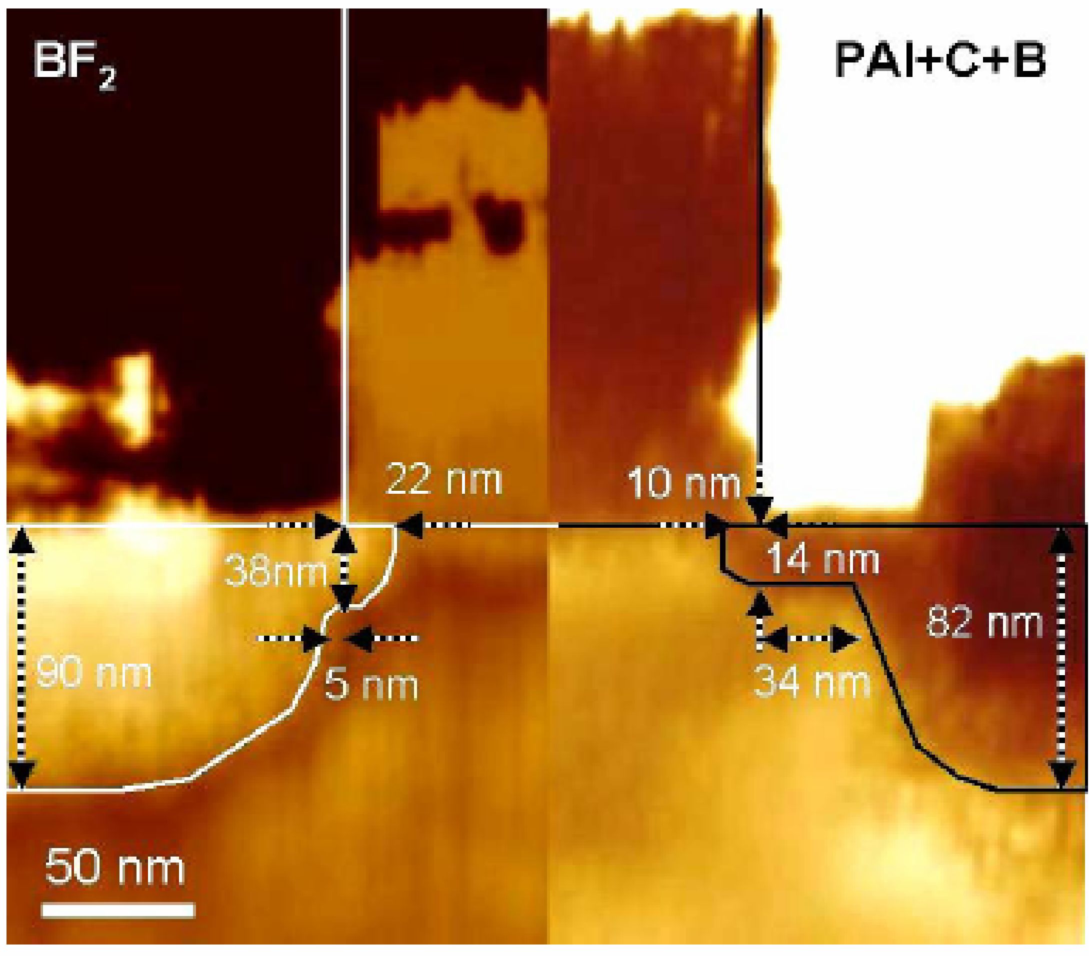
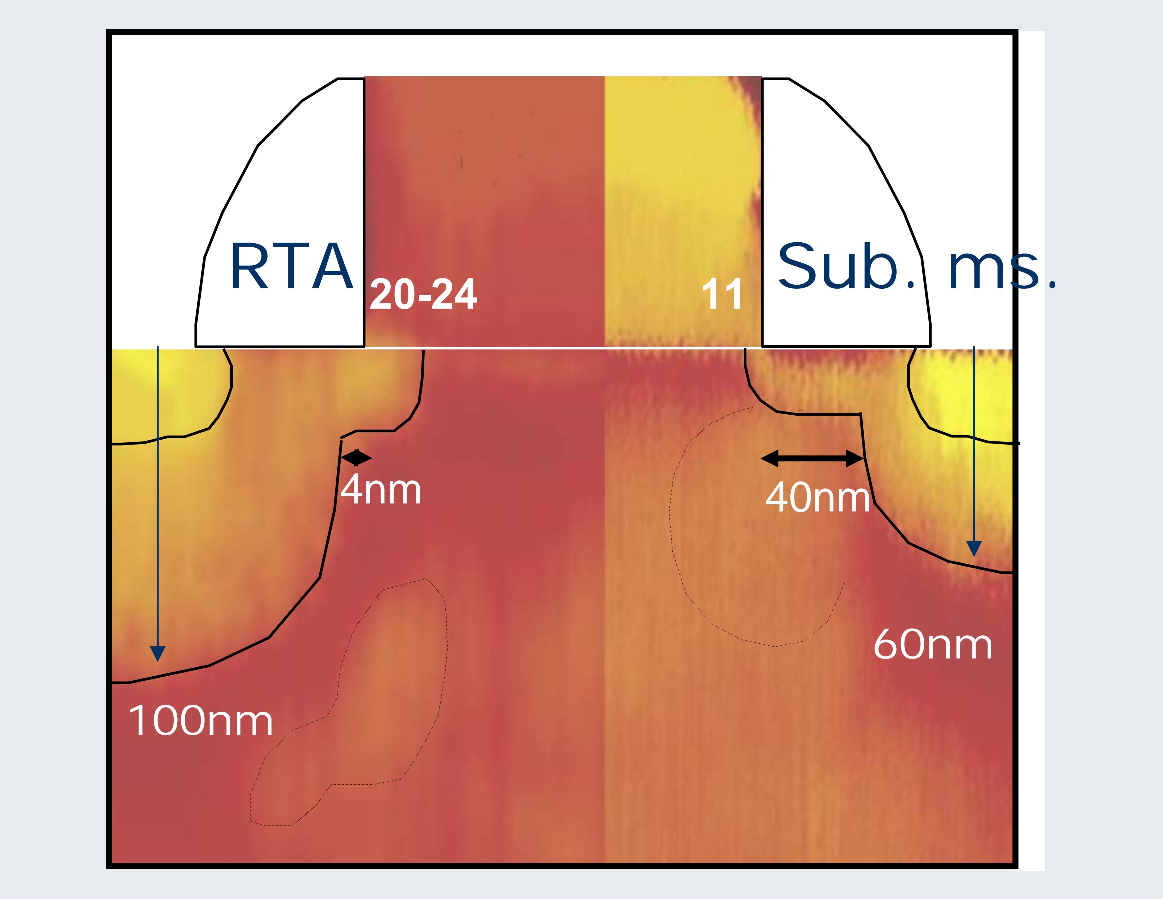
SSRM Image of C Co-Implant with Spike Anneal





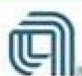
C co-implant reduces vertical junction depth and lateral diffusion, consistent with SIMS profiles and reduced C_{ov}

SSRM Image of Device with LA-only

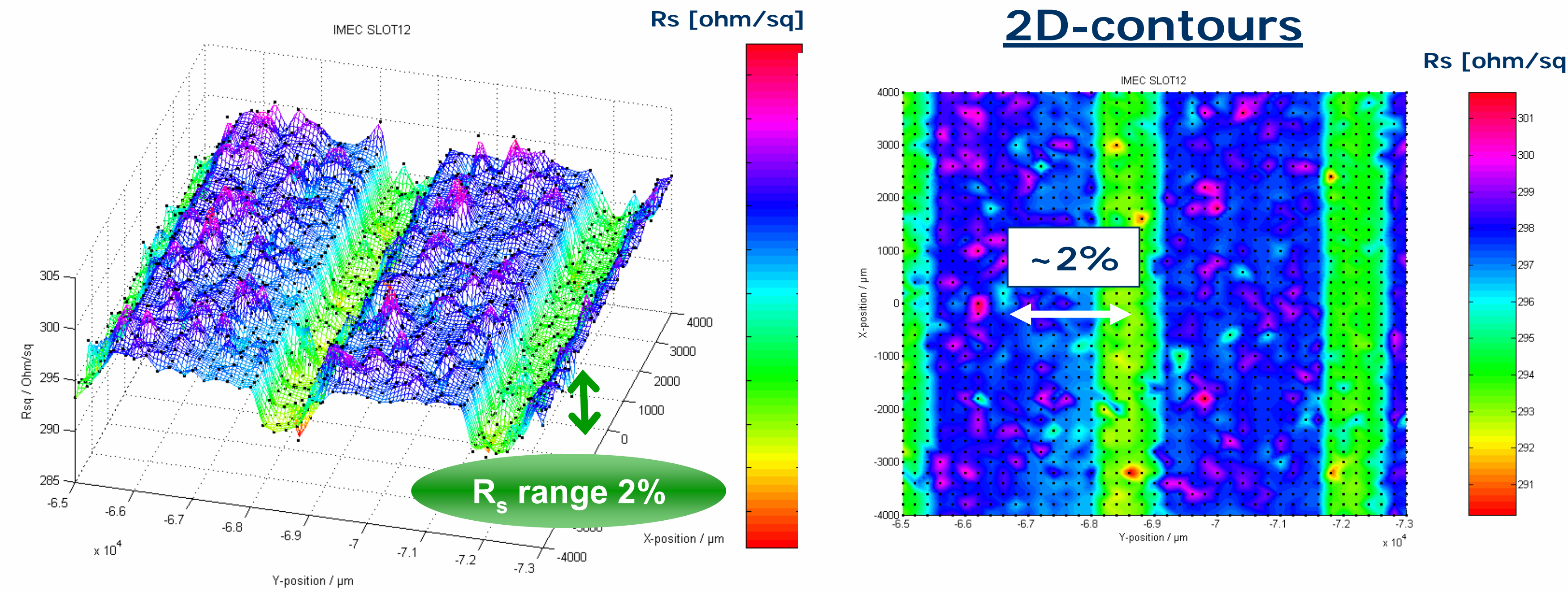


LA only reduces vertical junction depth and lateral diffusion, consistent with SIMS profiles and reduced C_{ov}

LA Micro-Uniformity Measured by Capres



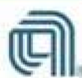
(Courtesy: W. VanDerVorst, IMEC)



- Sample:
  - 1200C Laser-annealed sample (As - 5keV) (no absorbing layer film)

Excellent uniformity with min-max range ~ 2%

Summary



- **Spike RTA plus medium power LA is compatible with POR CMOS processes**
  - Maintains poly depletion improvement
  - Maximizes device performance
  - Preserves dielectric quality and transistor lifetime
- **Lowering F dose and gate dielectric N content are beneficial**
  - Reduce additional charges generated by LA
  - Should enable optimized device performance and lifetime, even with high power LA
- **Altering thermal process sequence to have spike RTA after LA produces best results**
  - Large PMOS performance improvement with high power LA
  - No mobility or lifetime degradation
  - Spike RTA “heals” dielectric damage and charges induced by LA