# APPLICATIONS OF FLASH LAMP ANNEALING

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# outline

- Introduction of FLA
- S/D (Source Drain) activation and Pulse study
- PAI effect study
- Silicidation
- Summary

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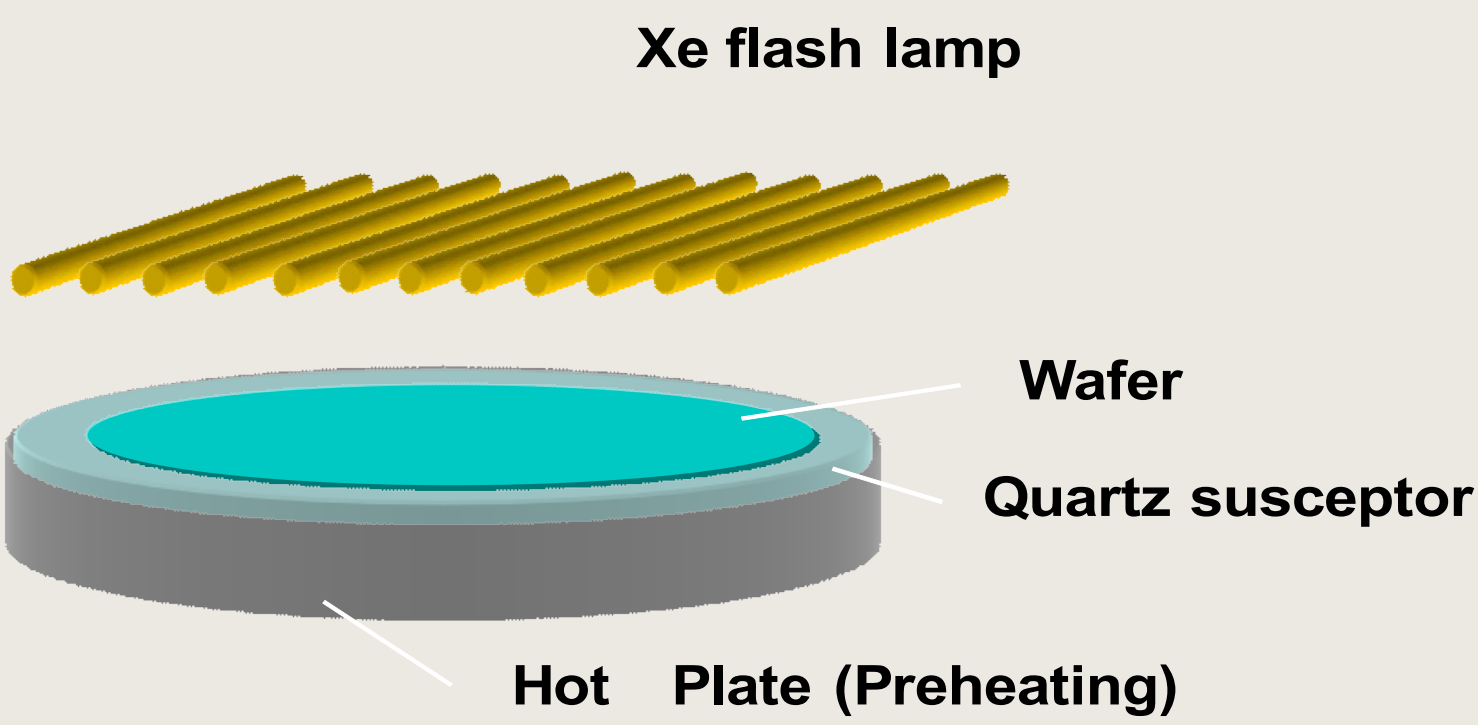
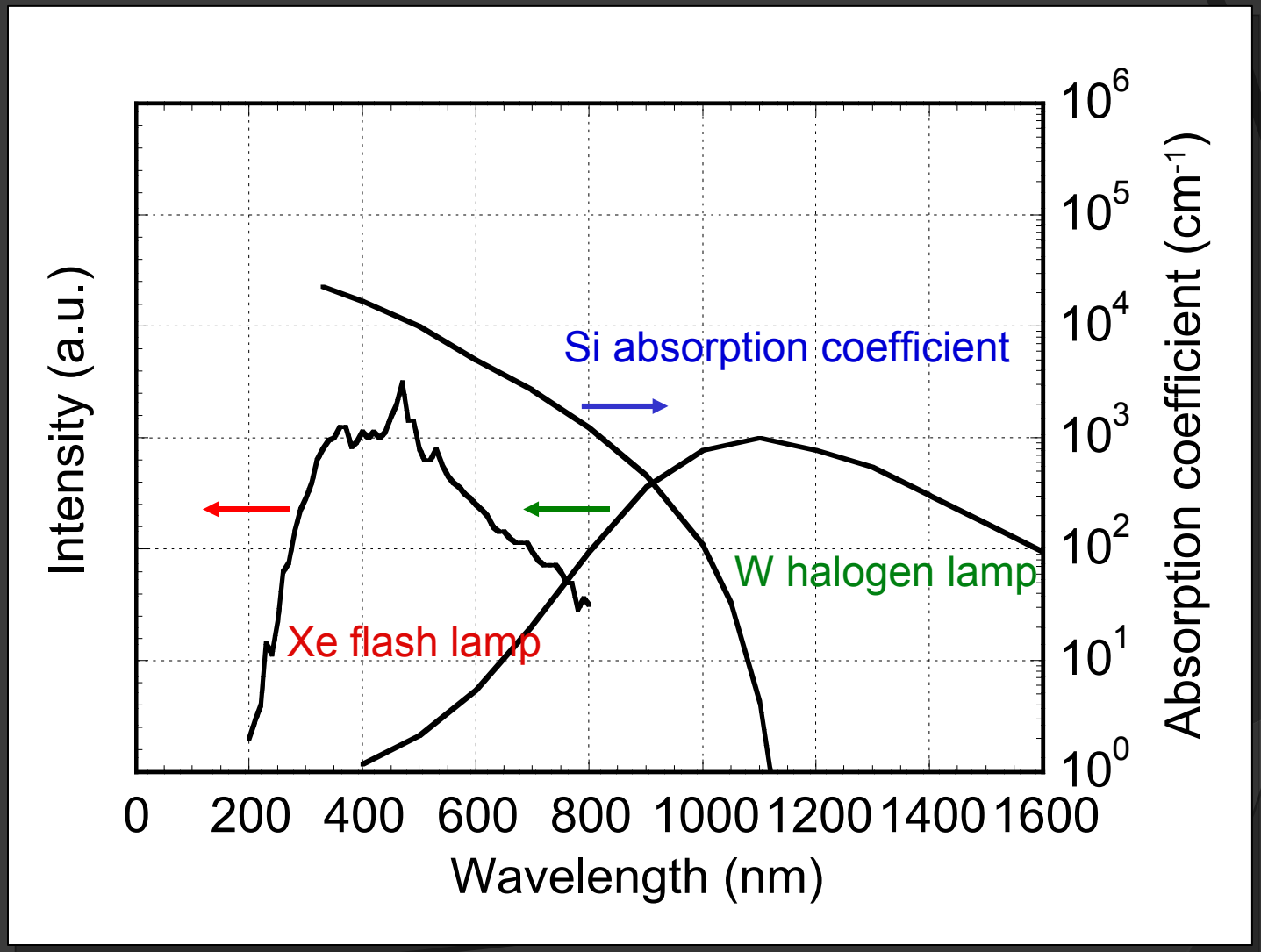
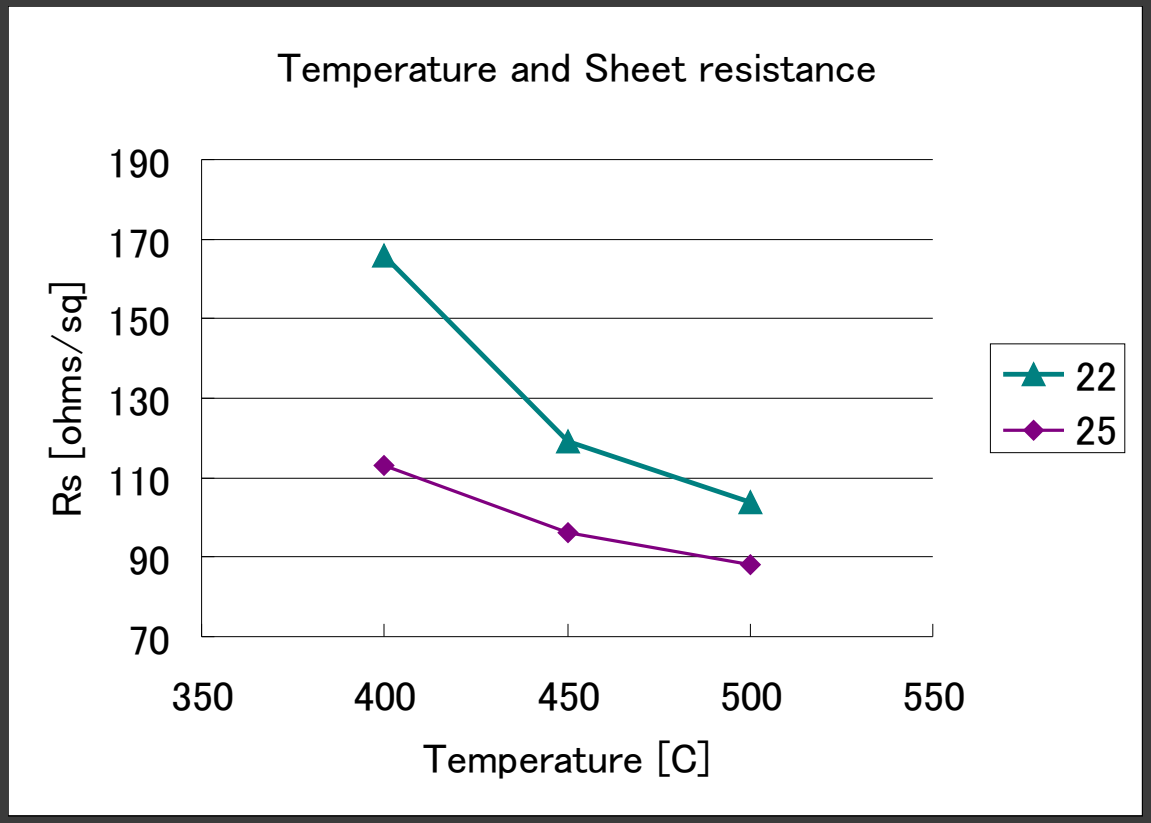
# FLA Hardware concept



# Wavelength Characteristic



# Pre-Heat temp. and Rs




Flash power

22J
25J

Relationship between pre-heating temperature and Rs
Also flash power and Rs shows good relationship.
From these data, we can estimate the wafer temperature.

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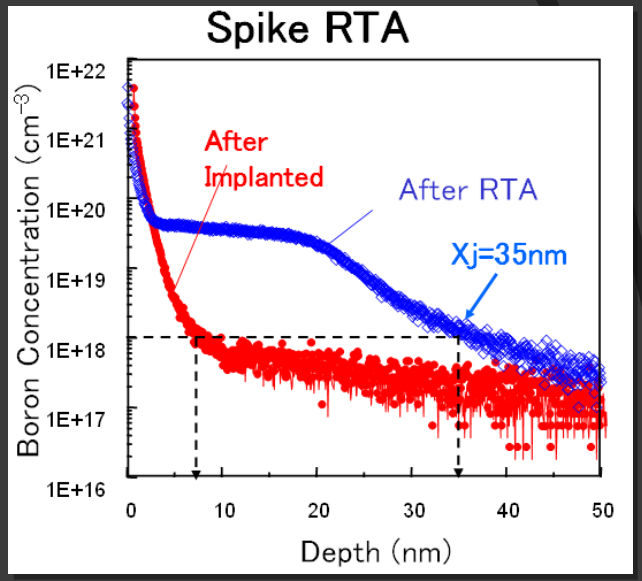
# Rapid Thermal Process

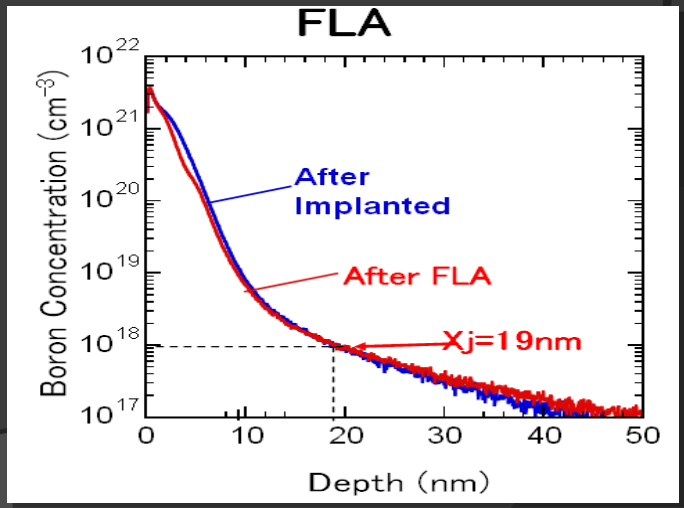
Spike RTA

Doping → Diffuse

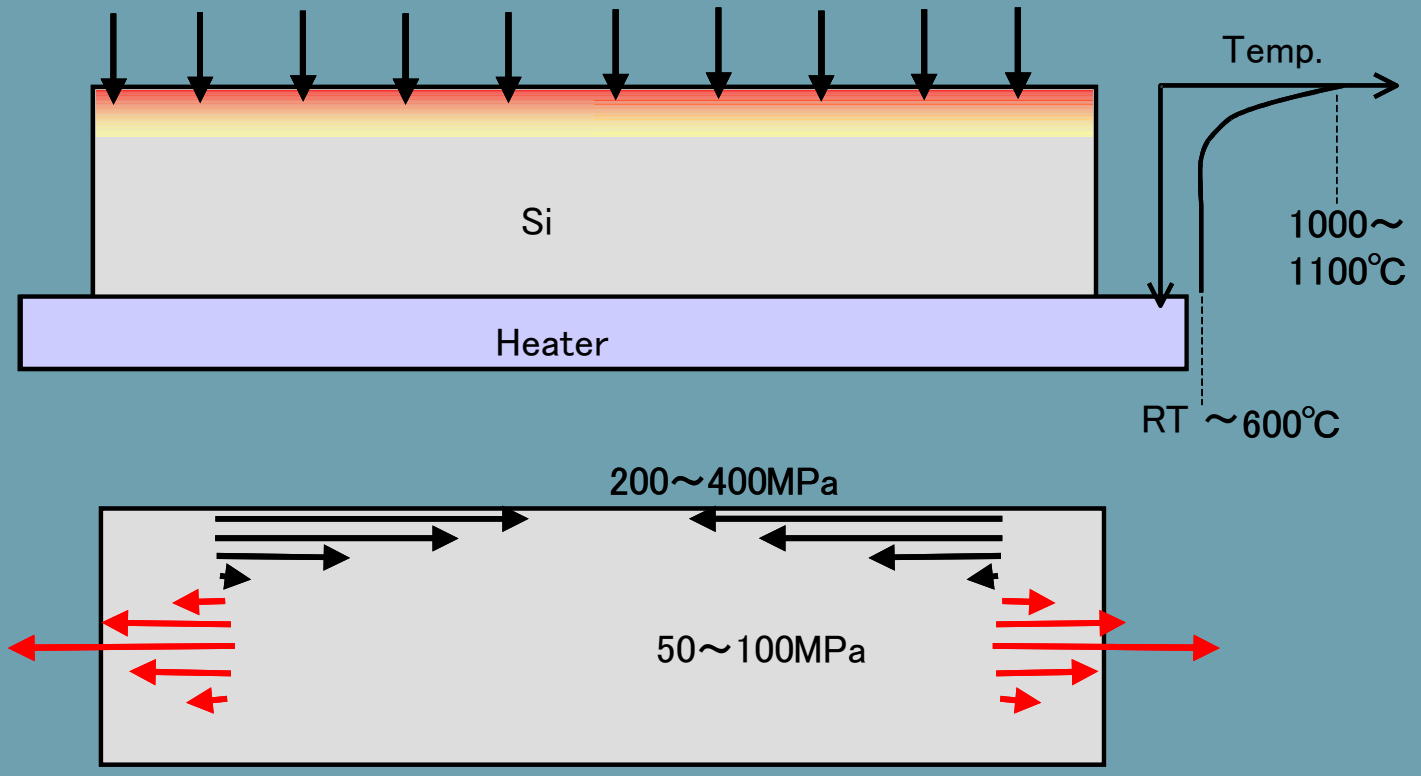
FLA

Doping → No time to Diffuse



# Temperature and Stress Simulation



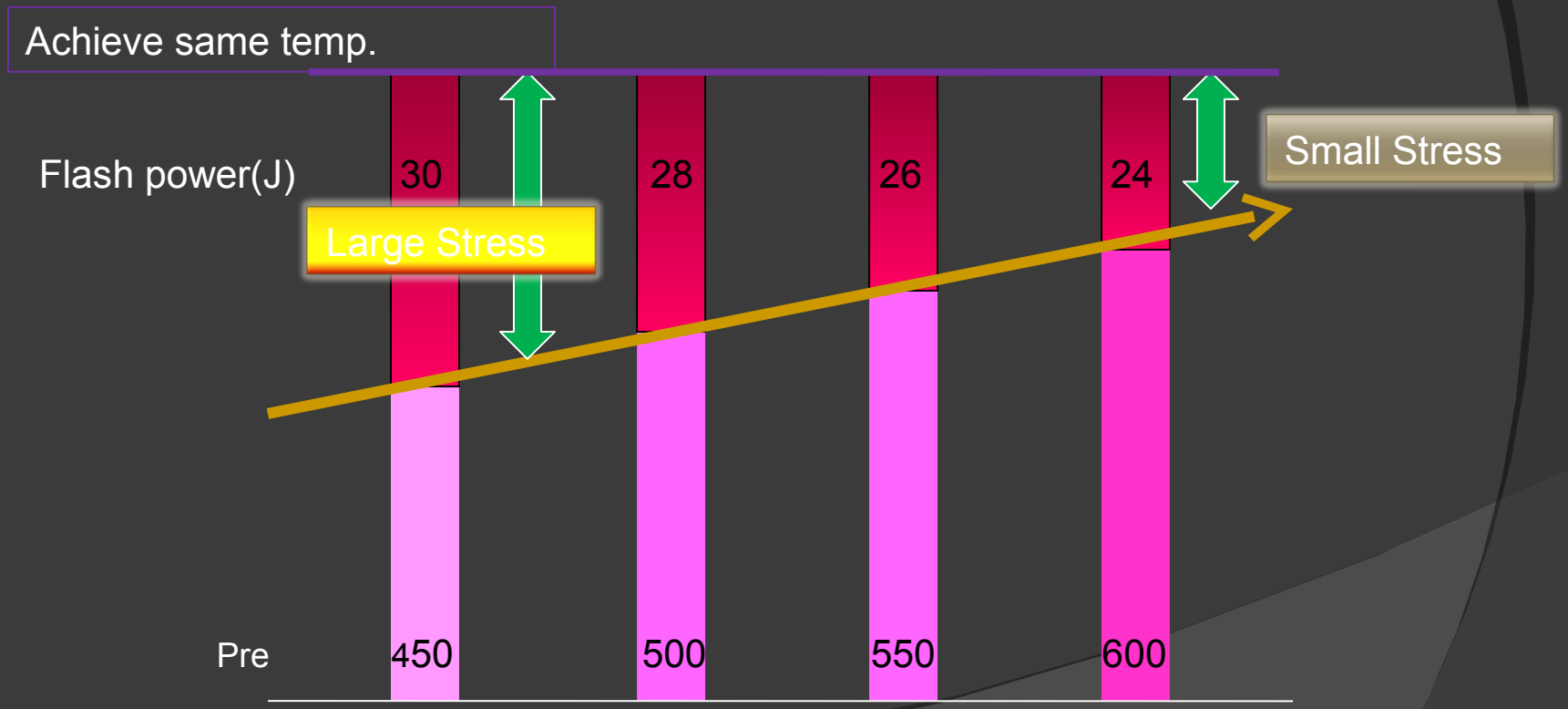

K.Suguro, T. Ito, and T. Itani Toshiba co. , "Flash Lamp Annealing Technology for Ultra-shallow Junction Formation" , Screen Technology Seminar 2002

# FLA Thermal stress control

- Changing the preheating temperature, we can control the thermal stress.

# Pre-Heat and Stress

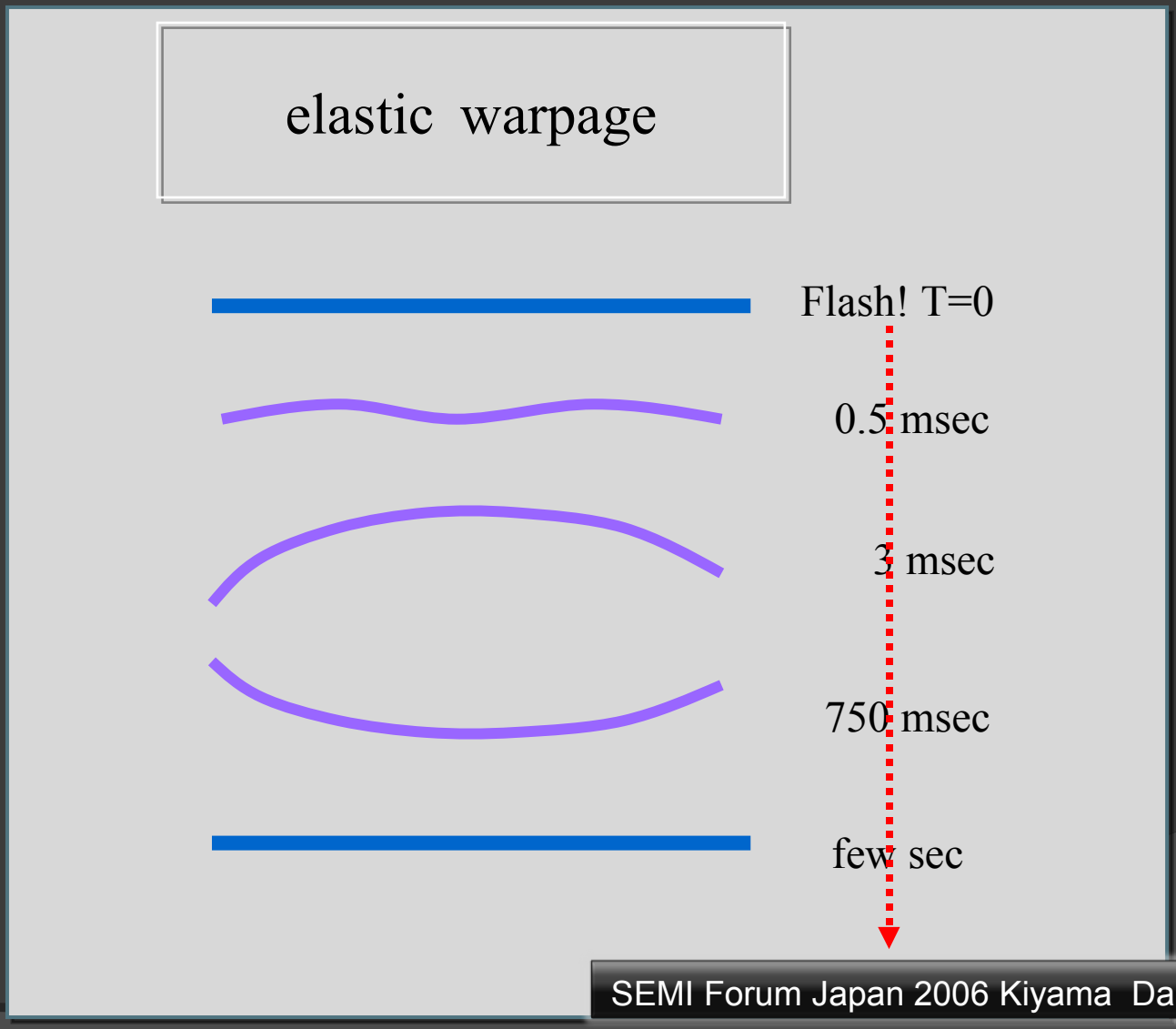
Increase Pre and reduce Flash power
for lower damage



# Wafer holding

- FLA has a difficulties in Wafer holding because of wafer motion.

# Wafer motion at Flash

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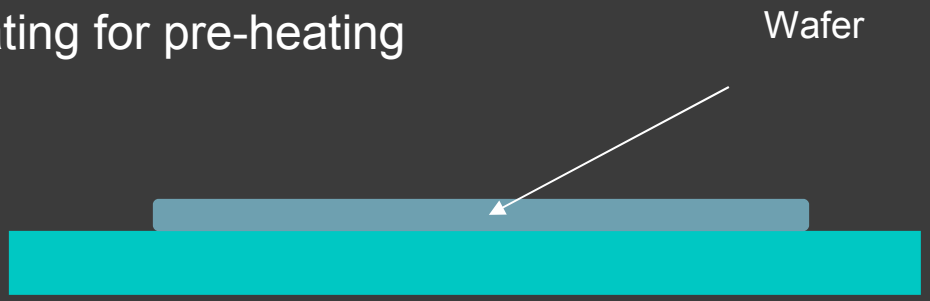
# Wafer Holding

LA-3000-F uses plate heating for pre-heating




Damages from wafer holding.

- wafer chuck (mechanical, vacuum) => wafer break
- Pins => backside scratch
- Edge hold => break

Best solution

- Let the wafer free

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# S/D Activation

- FLA is used for shallow junction activation. But milliseconds annealing, it is not easy to activate deep and heavy implanted S/D.

- FLA process of moderated ramping up speed and longer pulse has succeeded in deep implantation activation and re-crystallization.

# Conventional Pulse Data

- Higher flash power can re-crystallize the ion implantation damage.
- but too high flash power will create damage to device pattern

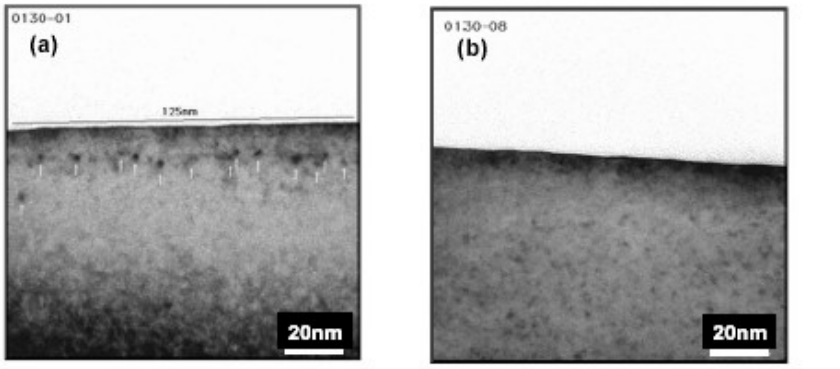



Fig. 1 Cross-sectional TEM image of the $p^+/n$ junction region for B with Ge PAI after FLA in the case of (a) lower power density and (b) higher power density.

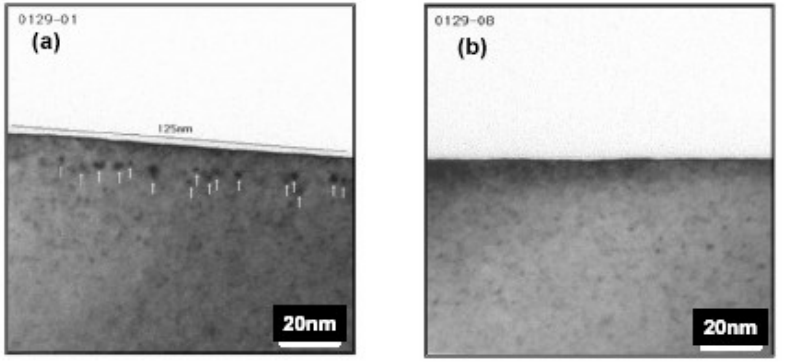



Fig. 2 Cross-sectional TEM image of the $n^+/p$ junction region for As after FLA in the case of (a) lower power density and (b) higher power density.

IWJT 2005 Ito et al Toshiba

# Long Pulse Data

- Longer pulse can activate deep junction and re-crystallize the defect from heavy implantation.
- No device damage created with longer pulse.

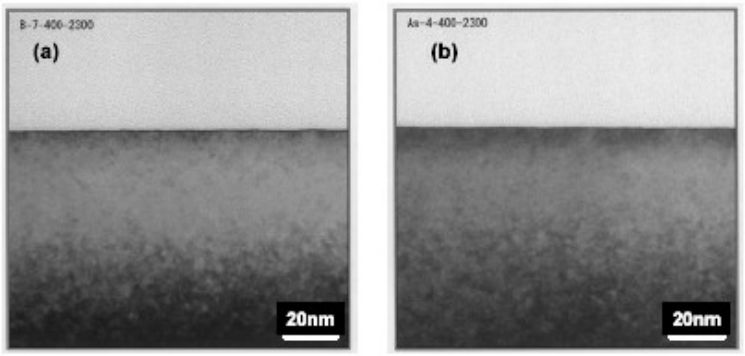
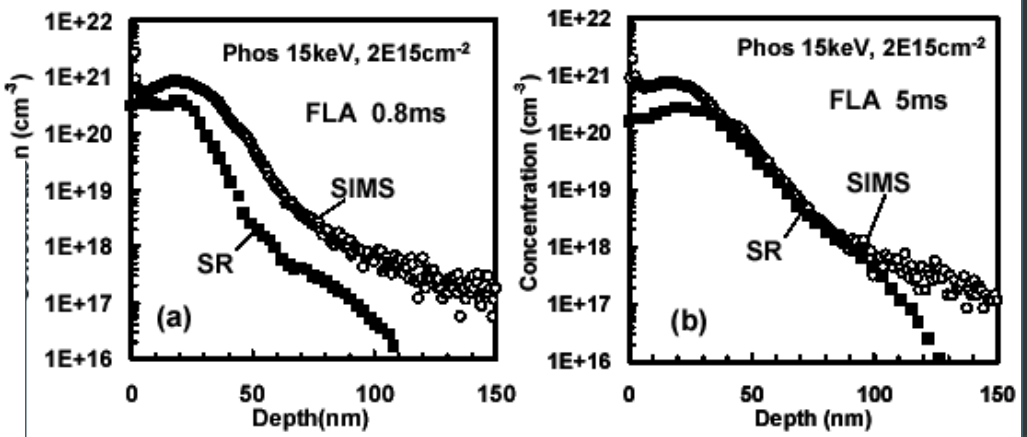



Fig. 12 Cross-sectional TEM image of (a) the $p^+/n$ junction region for B with Ge PAI, and (b) the $n^+/p$ junction region for As, after FLA with pulse duration of 5 ms in the case of using cap layers.




g. 6 Carrier depth profiles by SR measurement and SIMS depth profiles for P ter FLA with pulse duration of (a) 0.8 ms and (b) 5 ms.

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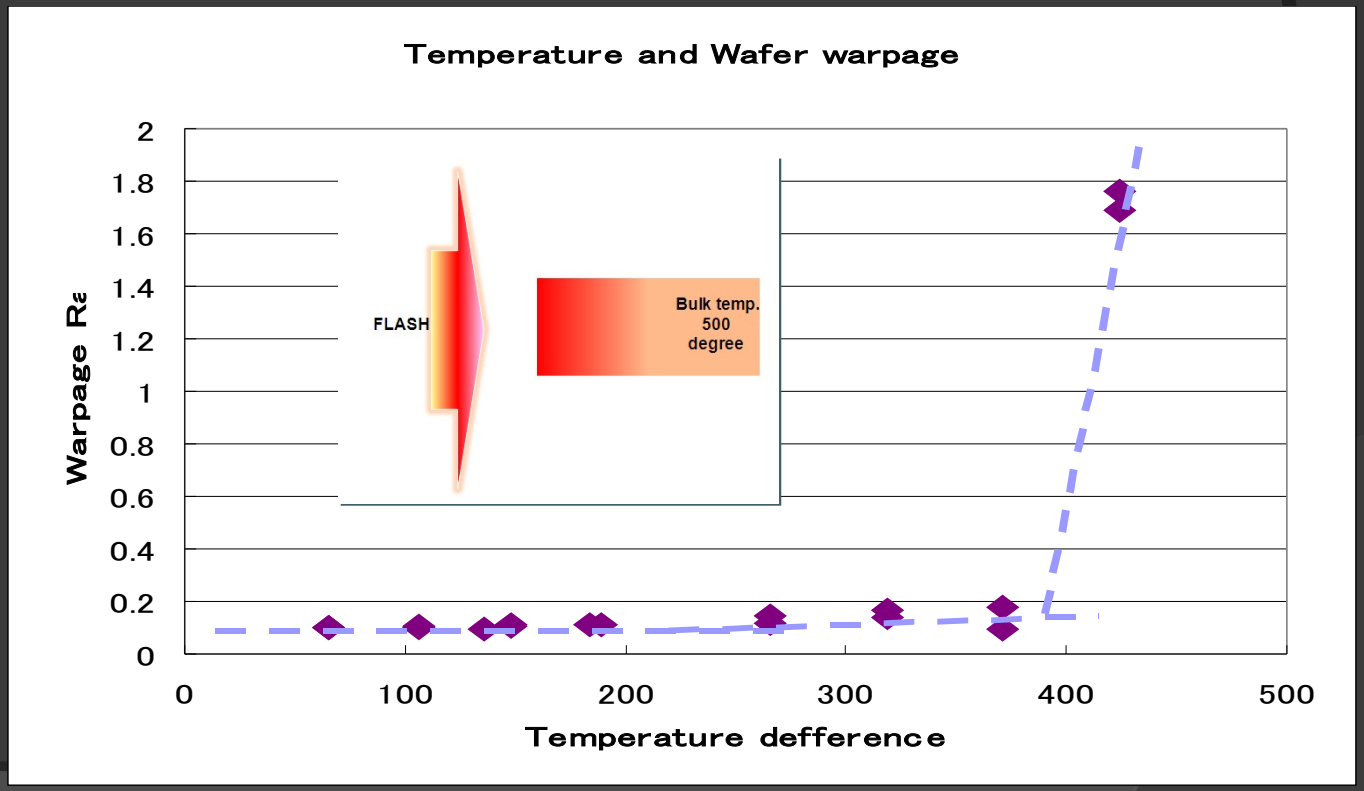
# S/D Activation

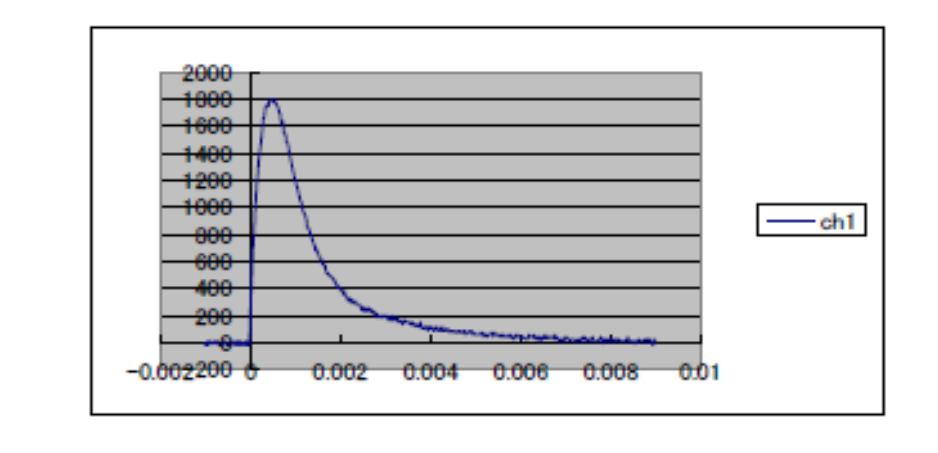
- Longer annealing time create dopant diffusion and larger wafer damage ?

# Concerning for Wafer Damage - Warp

conventional pulse:
Increasing the temperature difference of surface from backside, thermal stress create wafer warpage.

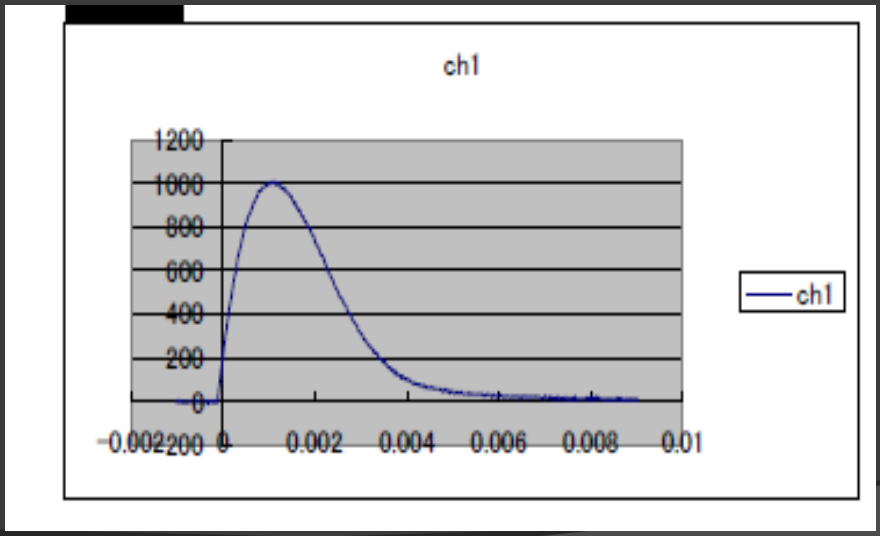


# Examples of Pulse length




1. 0ms

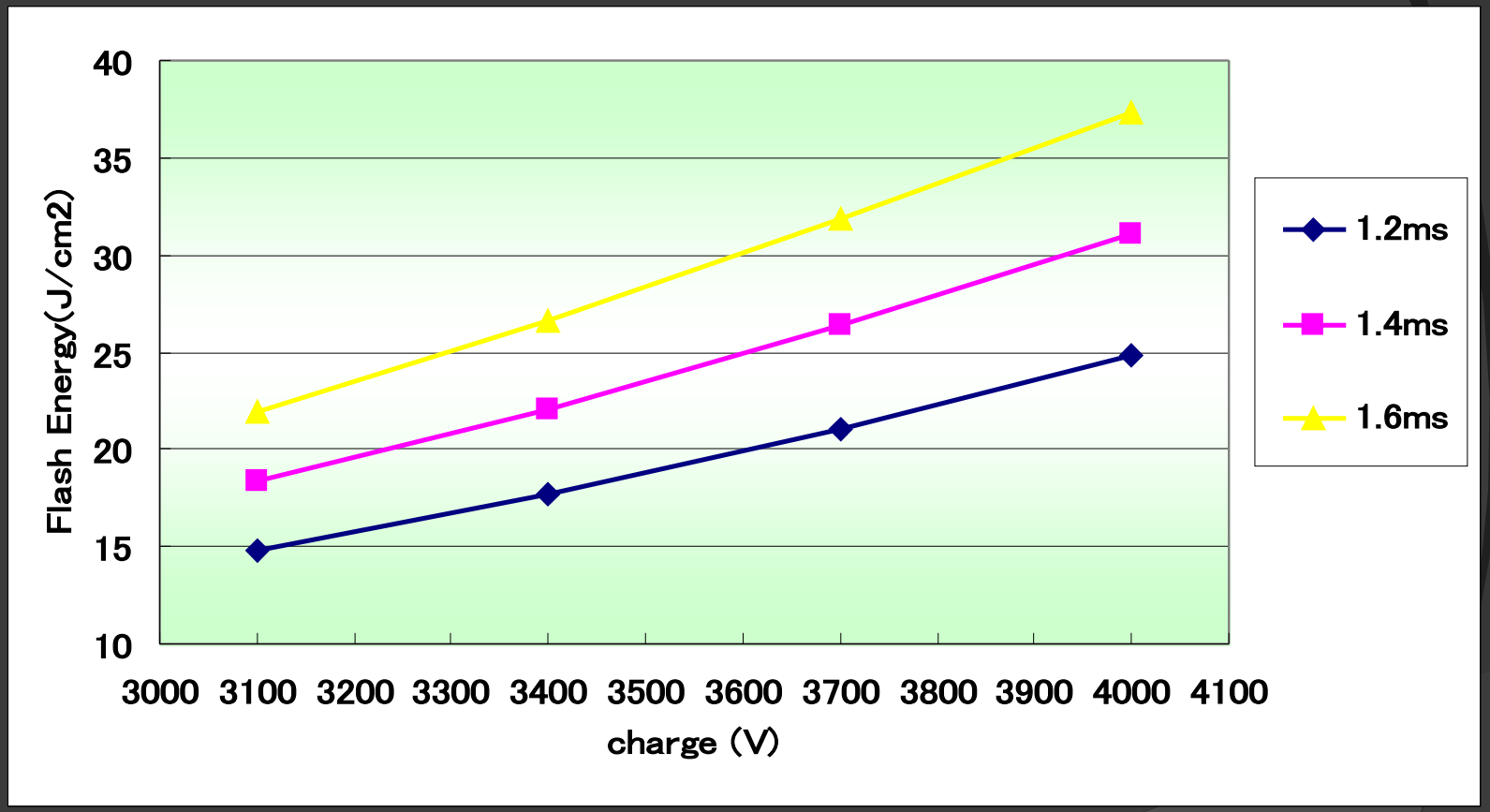
4000V



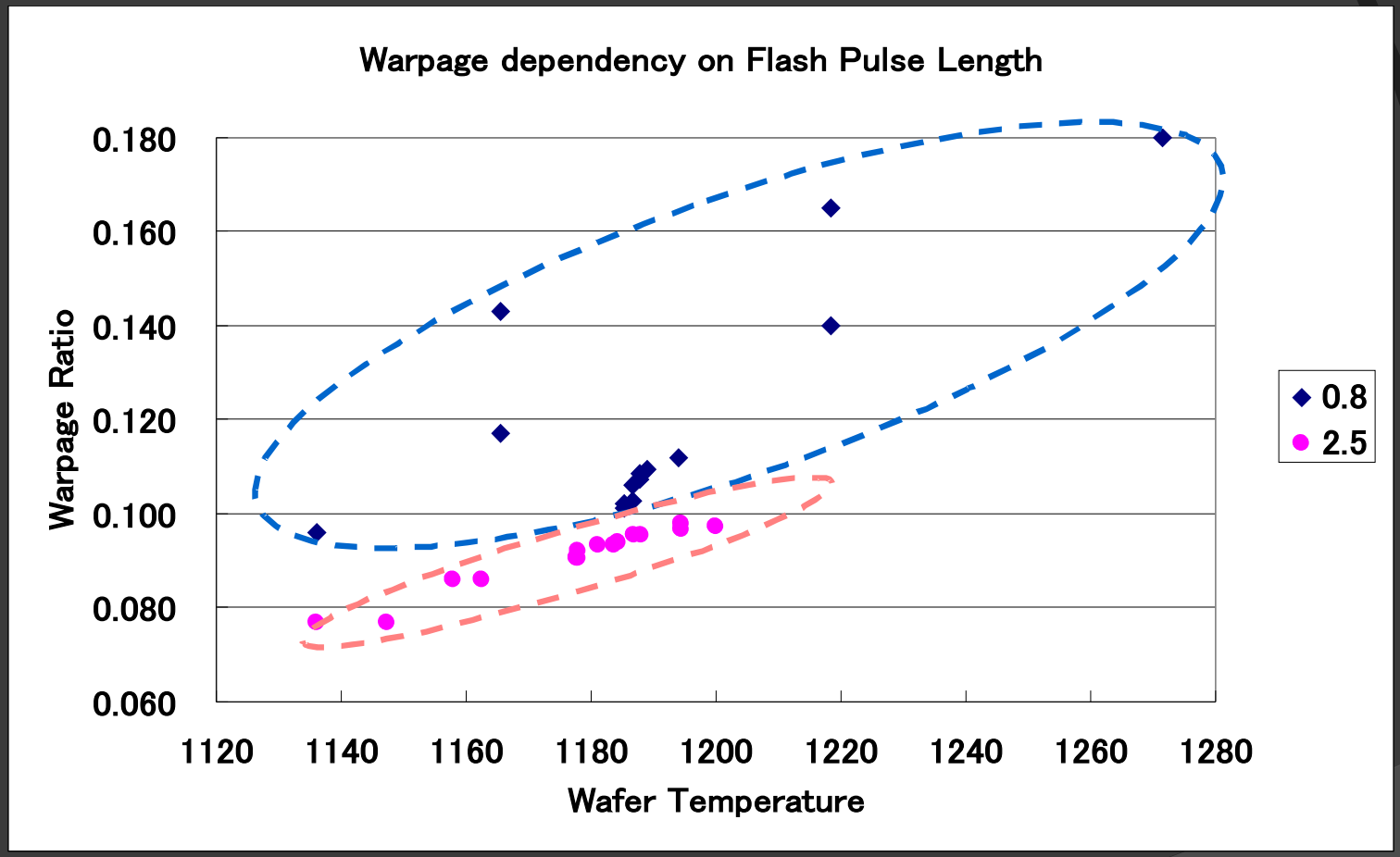

2.5ms

3500V

# Energy Characteristics



# 0.8ms vs 2.5 ms  Warpage Comparison




Longer pulse create lower wafer warpage.

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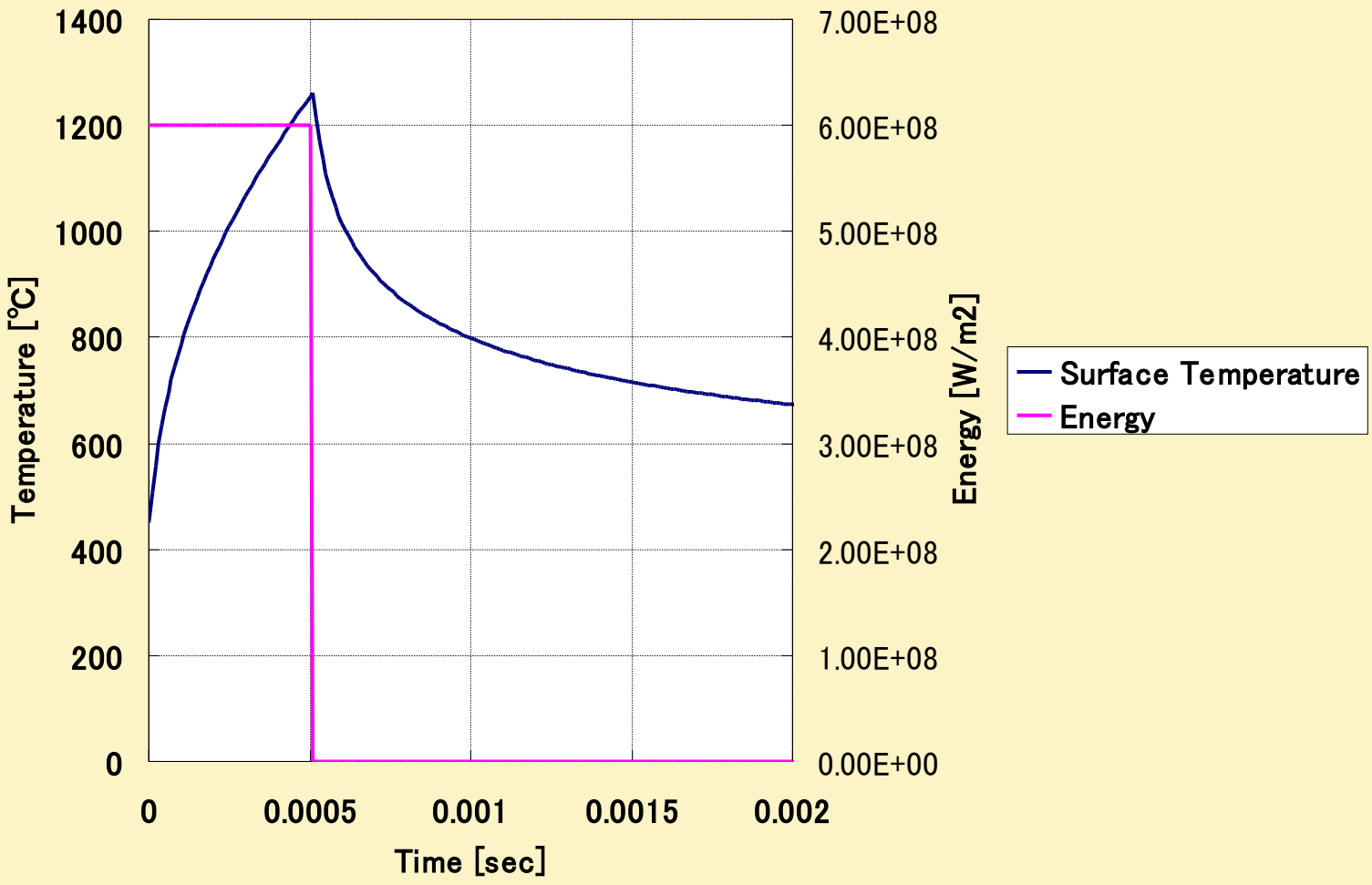
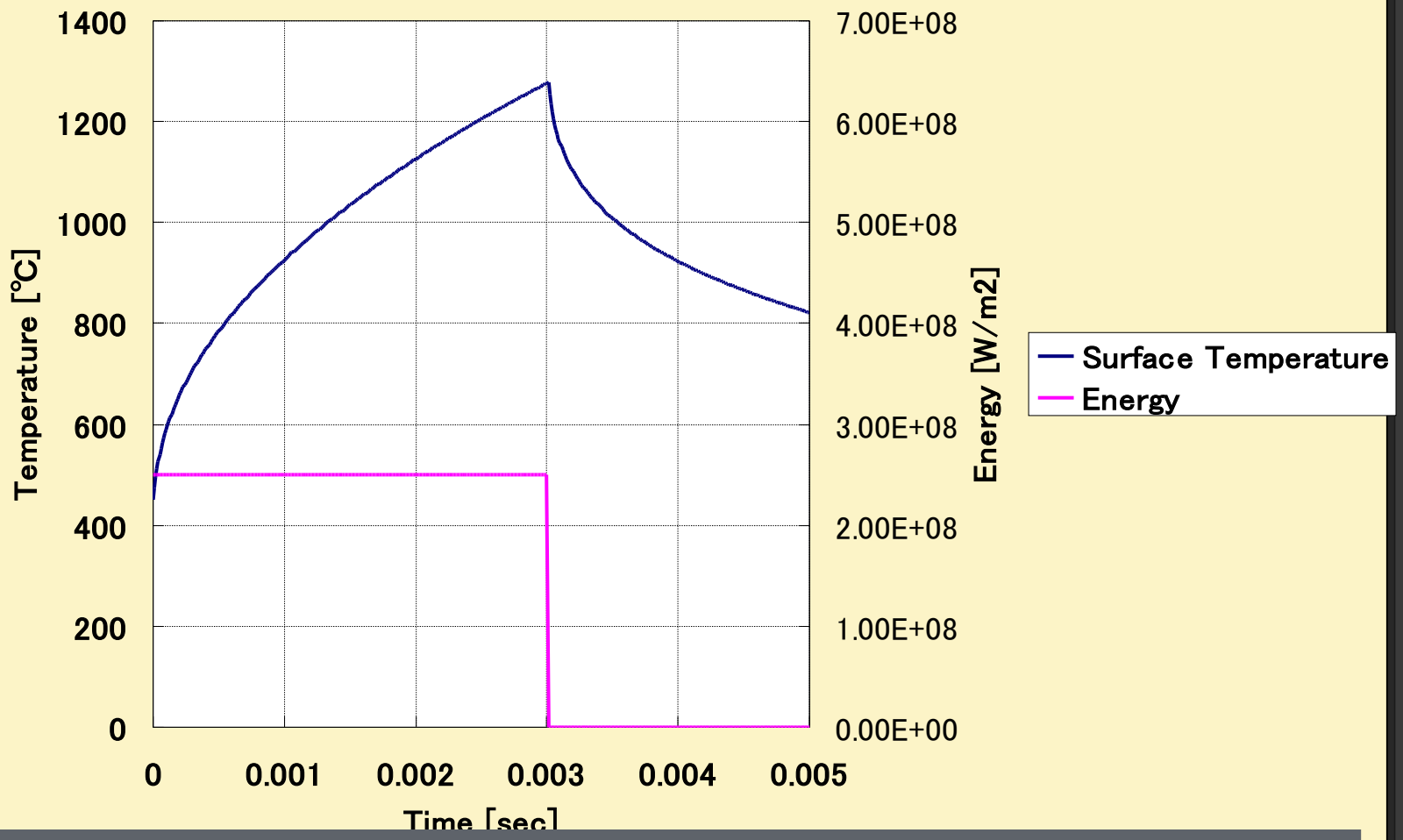
# 0.5 ms Heat conduction Calculation

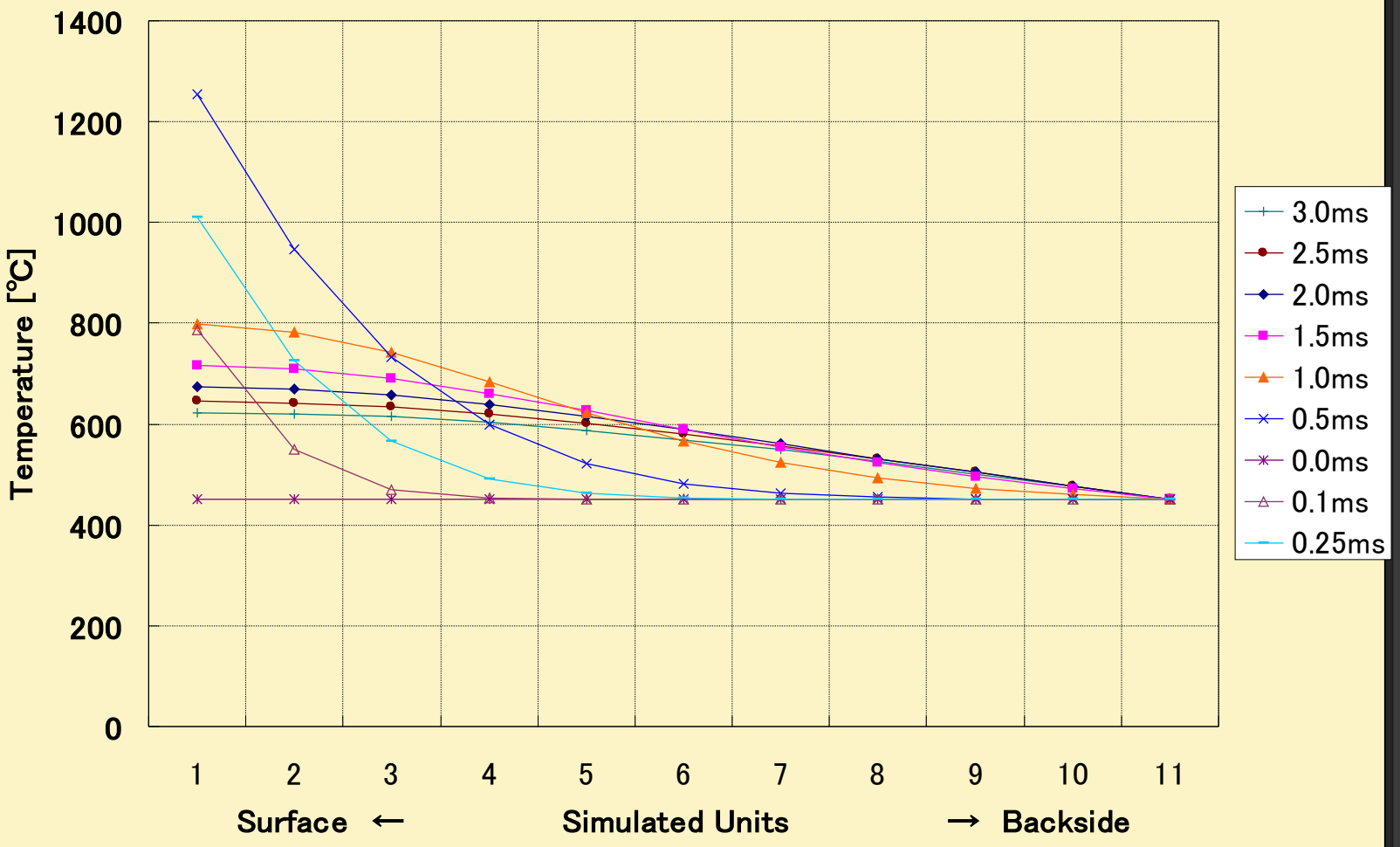


# 3.0 ms Heat conduction Calculation

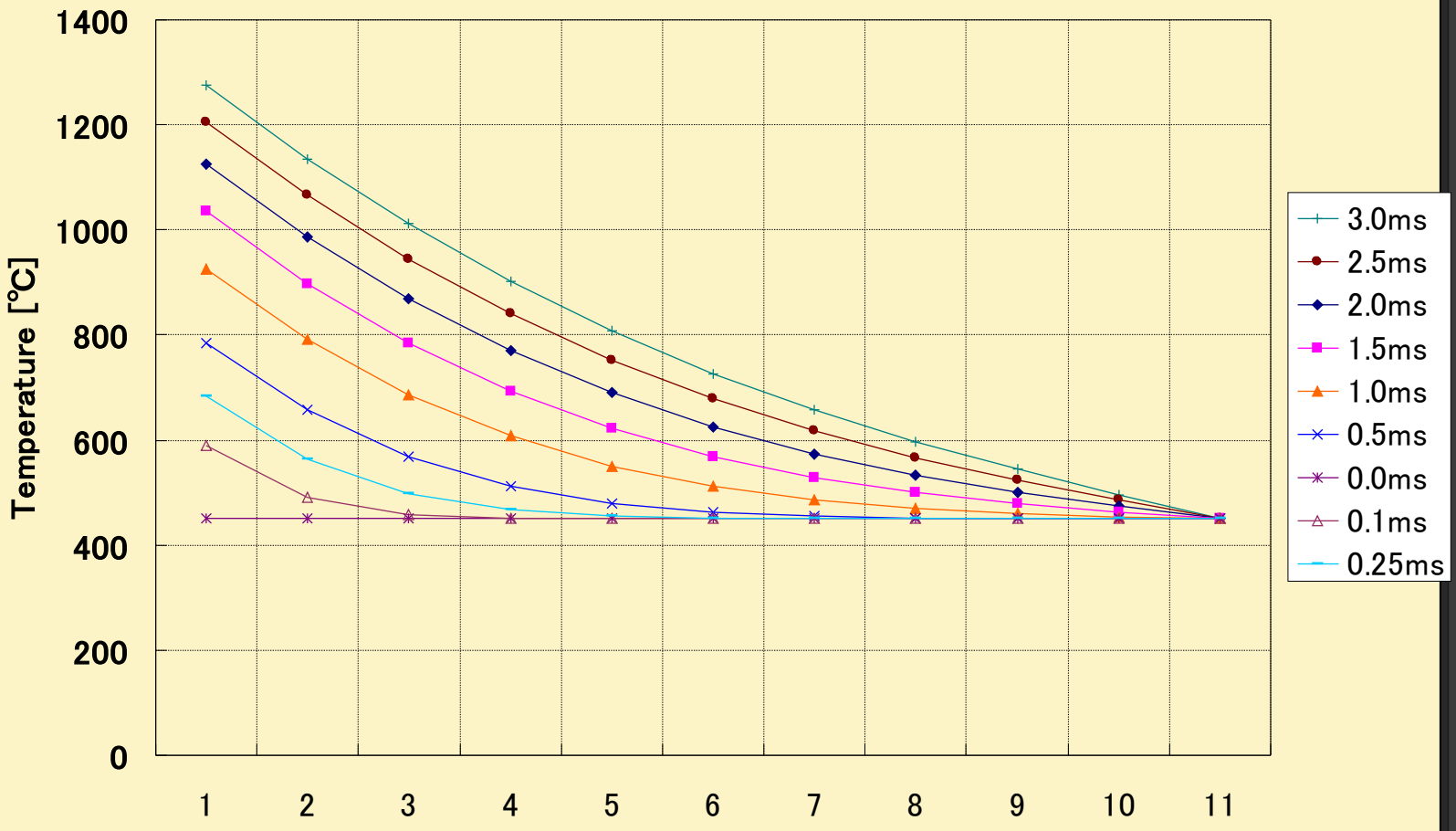



longer pulse can reach the same temperature with lower peak power

# 0.5 ms Heat conduction Calculation

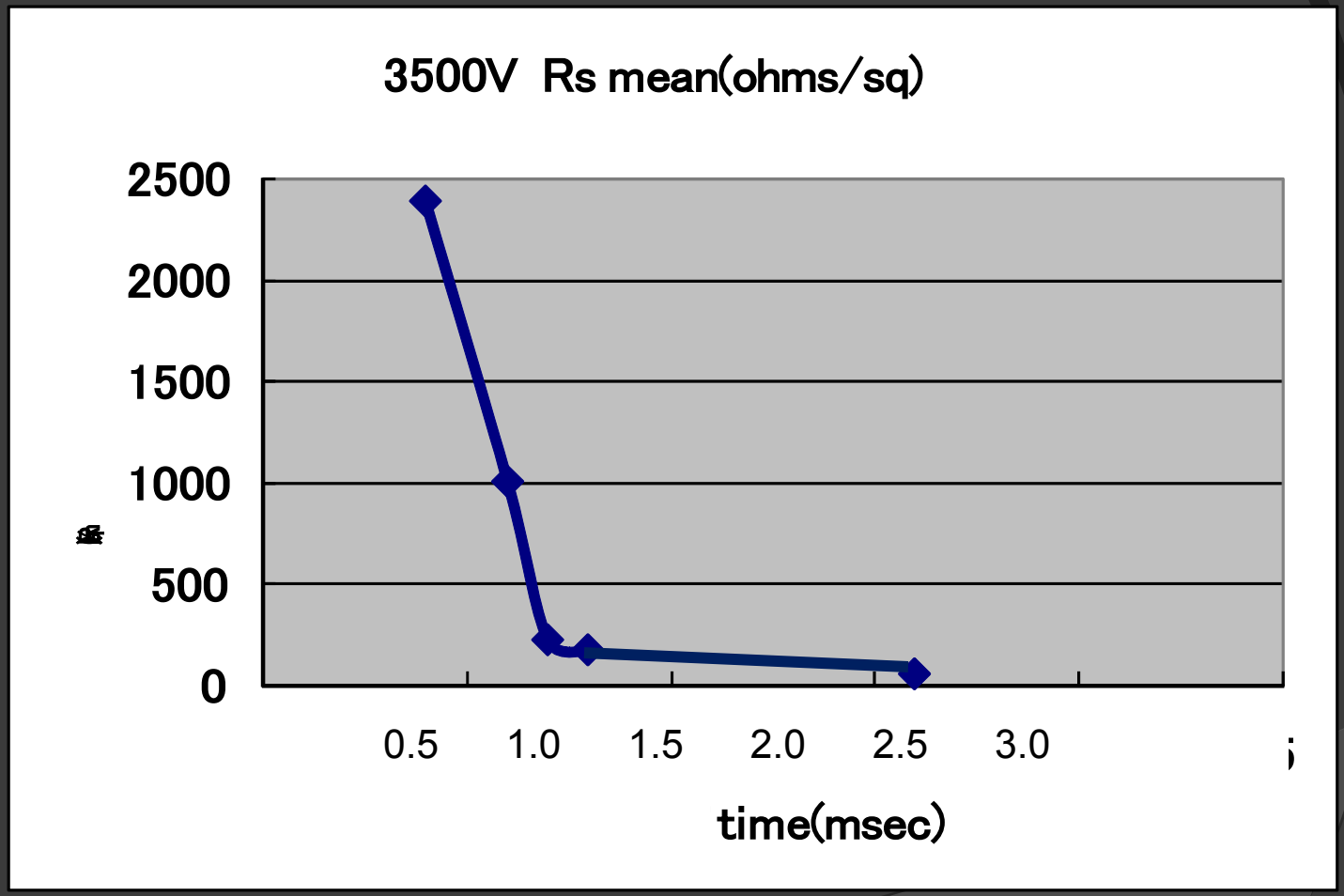


# 3.0 ms Heat conduction Calculation




Surface and backside temperature gradient is lower with longer pulse

# Dopant diffusion and Pulse Study

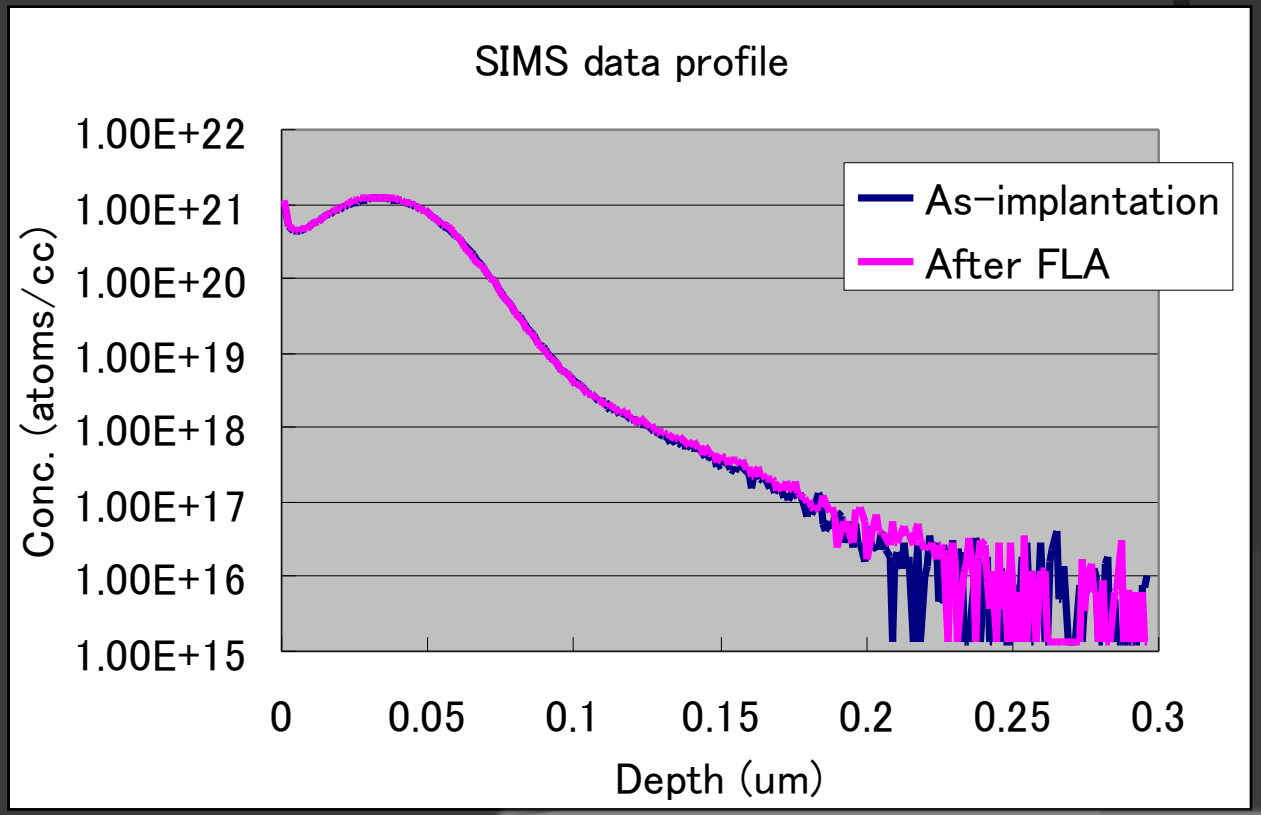



Longer the pulse lower the Rs

# SIMS Profile 2.5ms

Wafer ： BF2 40keV 5E15 , Rs : 210 Ohms/sq.

No dopant diffusion observed.

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# S/D Activation

- Longer  pulse shows smaller thermal stress for the wafer.
- 2.5 ms FLA dopant diffusion is same level of 0.8 ms.
- Using preheating stress control and longer pulse technology, we can process low damage flash annealing.

# Recent topic : Process Flow

- How about Process flow of FLA
- Current process flow is combining with RTP. As shown at RTP2006, it is normal process flow for millisecond annealing technology.
- For 45nm and beyond, is it same ?
  It was discussed about process flow using laser annealing at IWJT 2007.

# FLA process flow example

For 45nm and future device, diffusion control is much more important. Only FLA will be most hopeful solution.

| | 65nm | 45nm and next | 45nm and next | 45nm and next |
|---|---|---|---|---|
| gate formation | ← | ← | ← | ← |
| shallow S/D implantation | ← | ← | ← | ← |
| annealing | not uses | | FLA | FLA |
| spacer formation | ← | ← | ← | ← |
| deep S/D implantation | ← | ← | ← | ← |
| annealing | RTP | FLA | RTP low temp. | FLA |
| | FLA | RTP low temp. | FLA | |
| silicide | RTP | ? | ? | ? |

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# PAI effect study : Ge + B

- The energy of the Ge implant can control the Rs of B.
  (Rs decreases with increasing Ge I/I energy)
- This reason is related to depth of B implant and the amorphous layer.

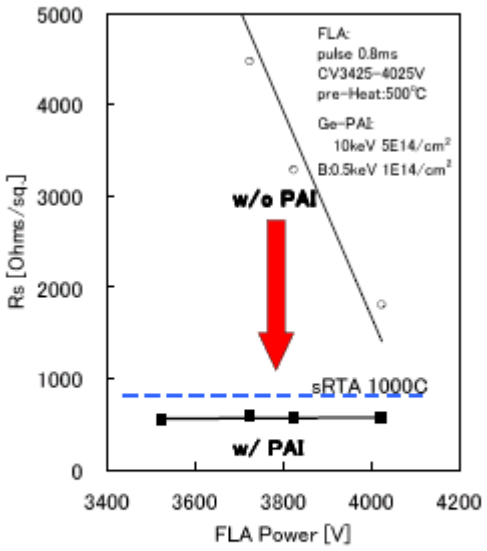



Fig.1 The dependence of lamp power in FLA on Rs of B doped P+/n junction

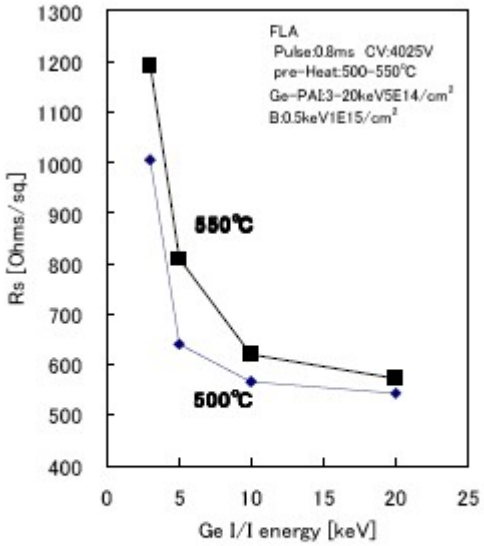



Fig.2 The dependence of Ge I/I energy on Rs of p+/n junction

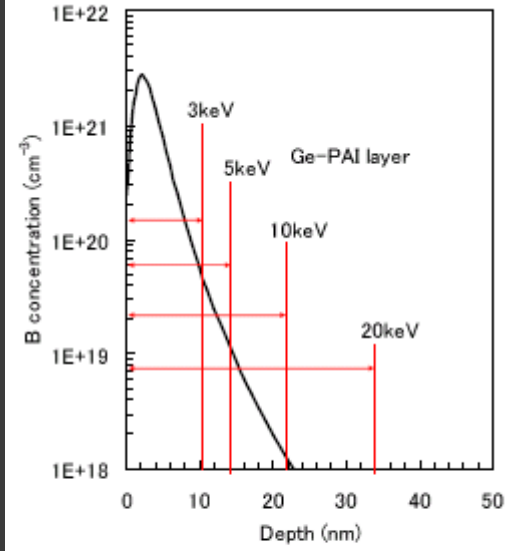



Fig.3 The schematic drawing of relationship between Ge-PAI depth and B profile

- The dependency of the Rs on FLA power is very low for samples w/ PAI.

Data from IWJT2007 Kato et al SELETE

# PAI effect study : Ge + B

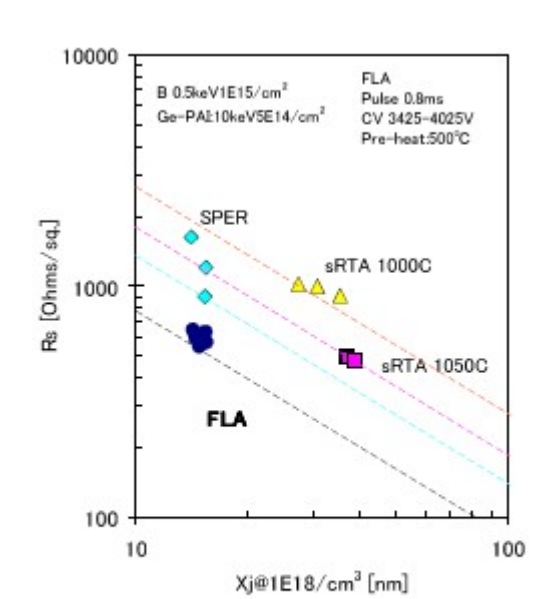



Fig.4 Rs-Xj characteristics annealed by FLA, SPER and sRTA

- Rs is lowest in the samples annealed by FLA.

- TW signal shows the defects in FLA and SPER samples are almost the same.

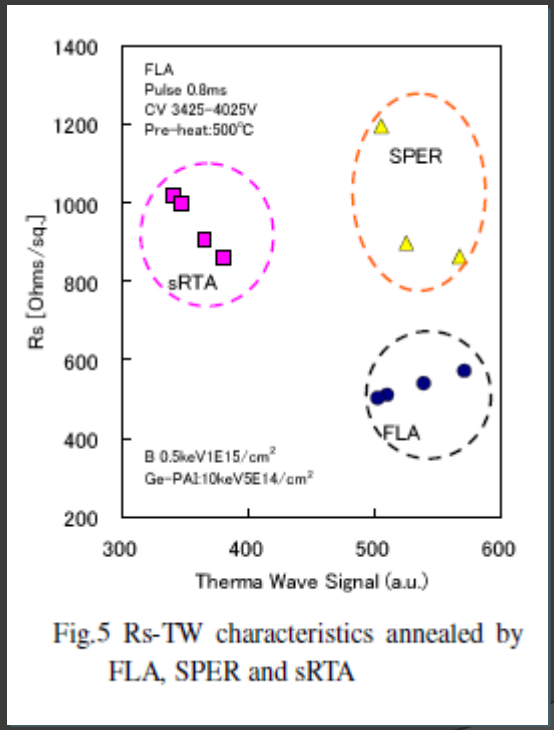
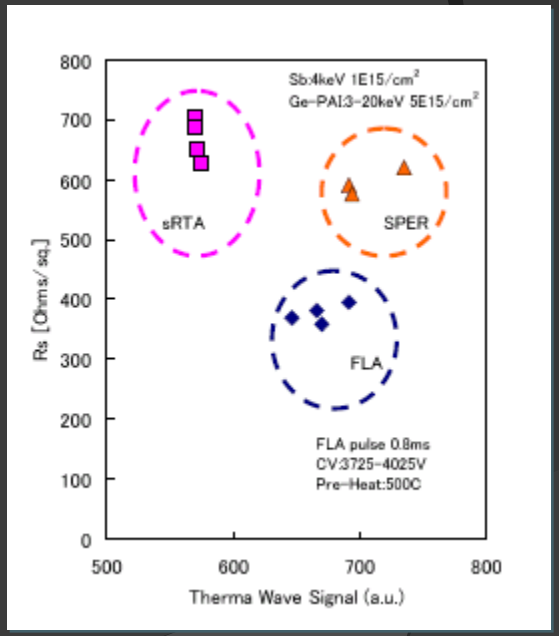


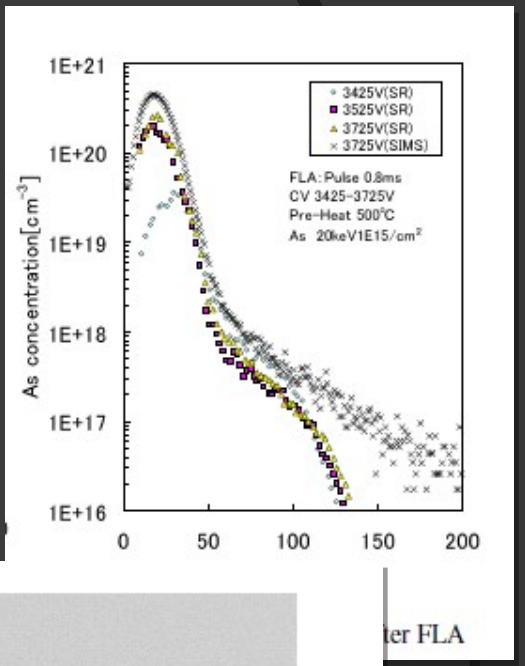

Fig.5 Rs-TW characteristics annealed by FLA, SPER and sRTA




Data from IWJT2007 Kato et al SELETE

# Amorphous layer study

- The amorphous layer decreases with increasing FLA power.
- As the amorphous layer crystallizes from a/c interface.
- Arsenic at amorphous layer is activated . The amorphous layer makes Rs high.



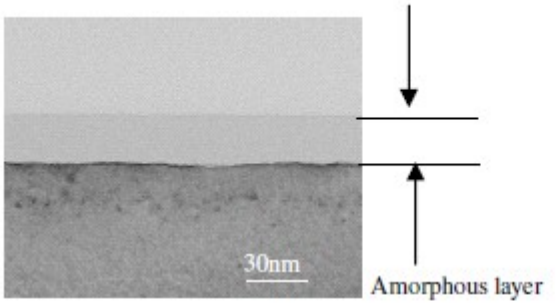




Fig.12-A TEM image of the n+/p junction region As(20keV) after FLA(3425V)

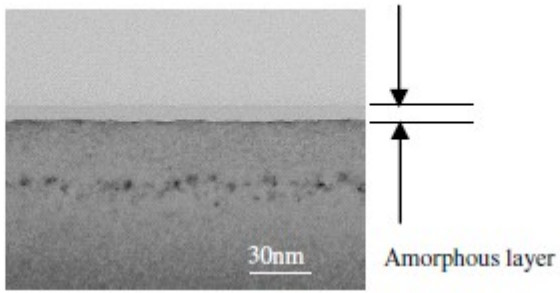



Fig12-B TEM image of the n+/p junction region As(20keV) after FLA(3525V)

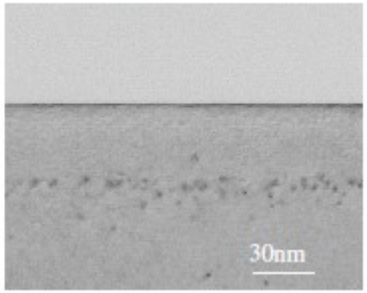
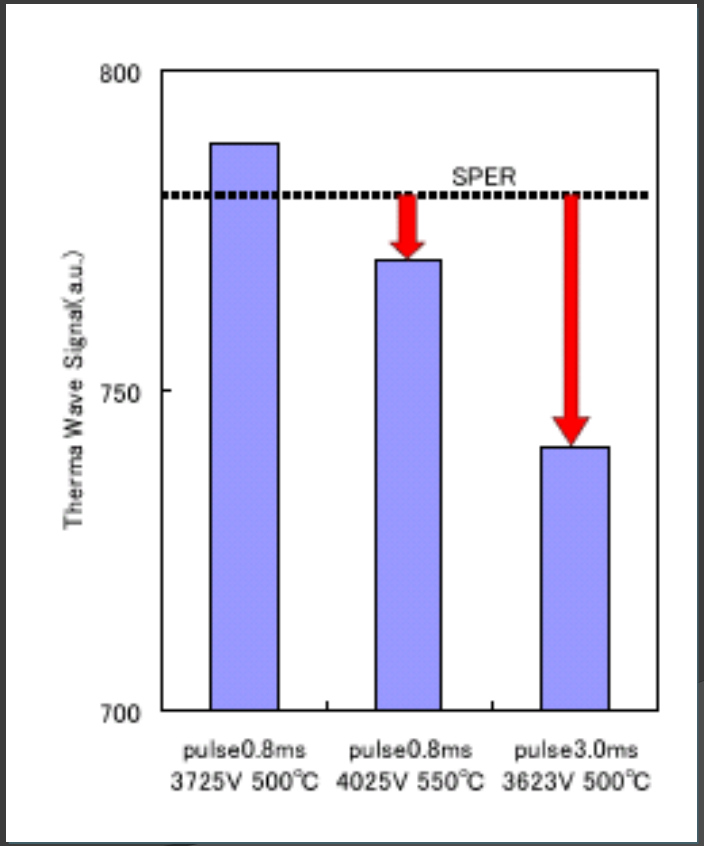



Fig12-C TEM image of the n+/p junction region As(20keV) after FLA(3725V)

Data from IWJT2007 Kato et al SELETE

# Longer Pulse and TW signal

- Higher Flash power or longer flash time shows better thermawave signal compared to SPE




Data from IWJT2007 Kato et al SELETE

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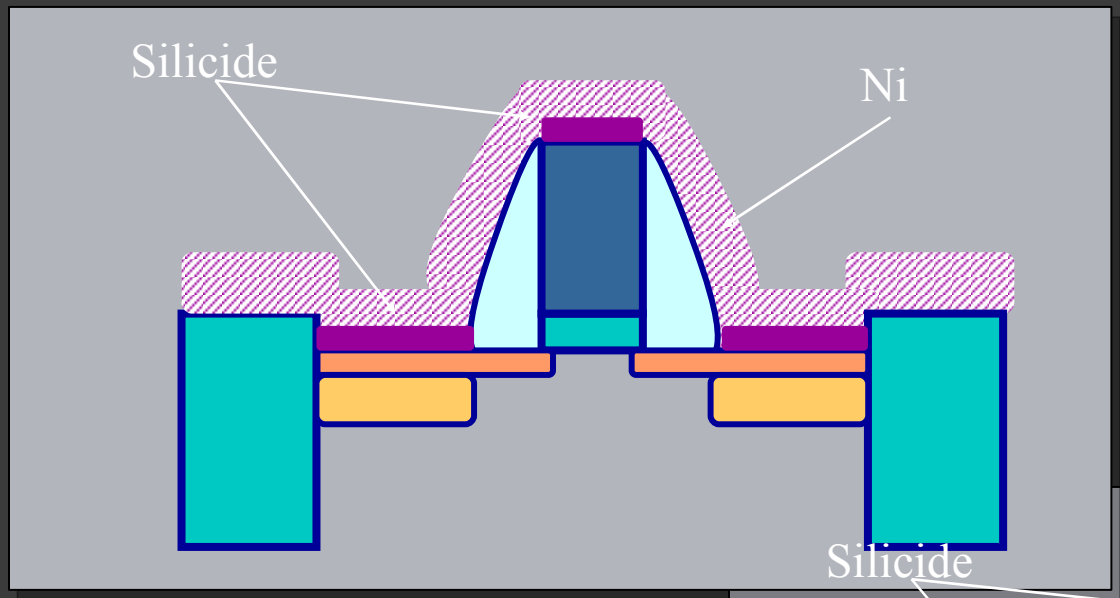
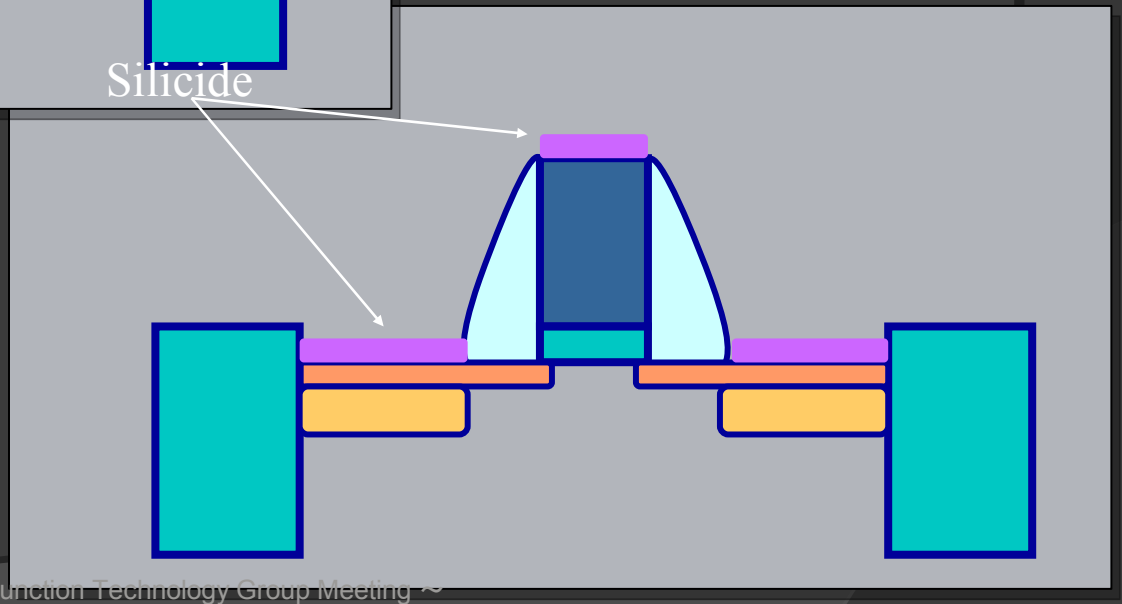
# Ni Silicide



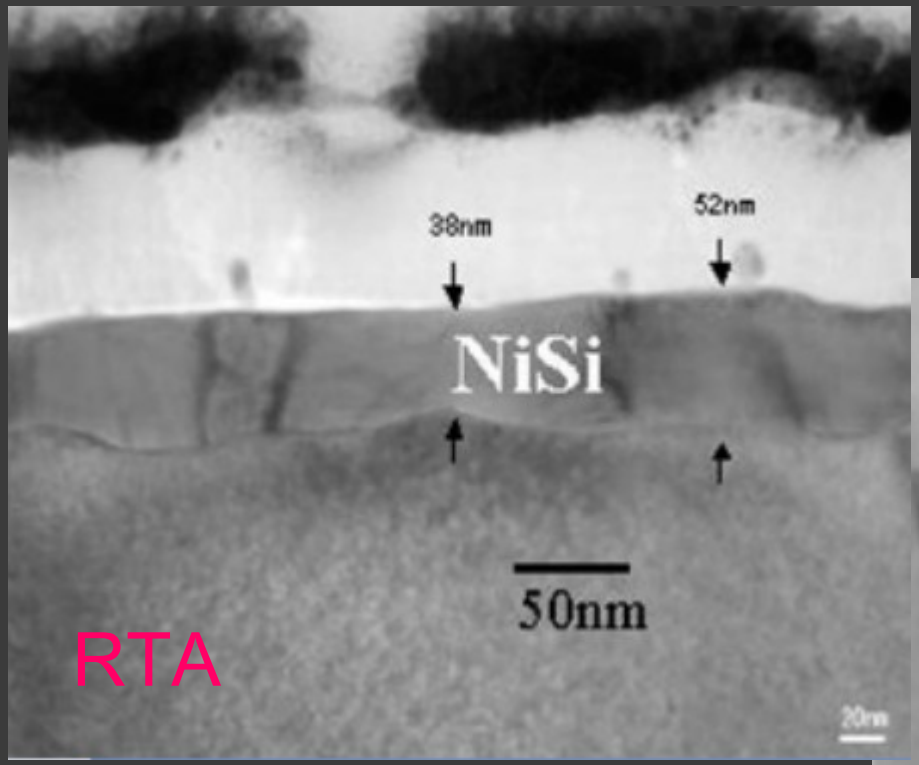
# NiSi reaction temperature

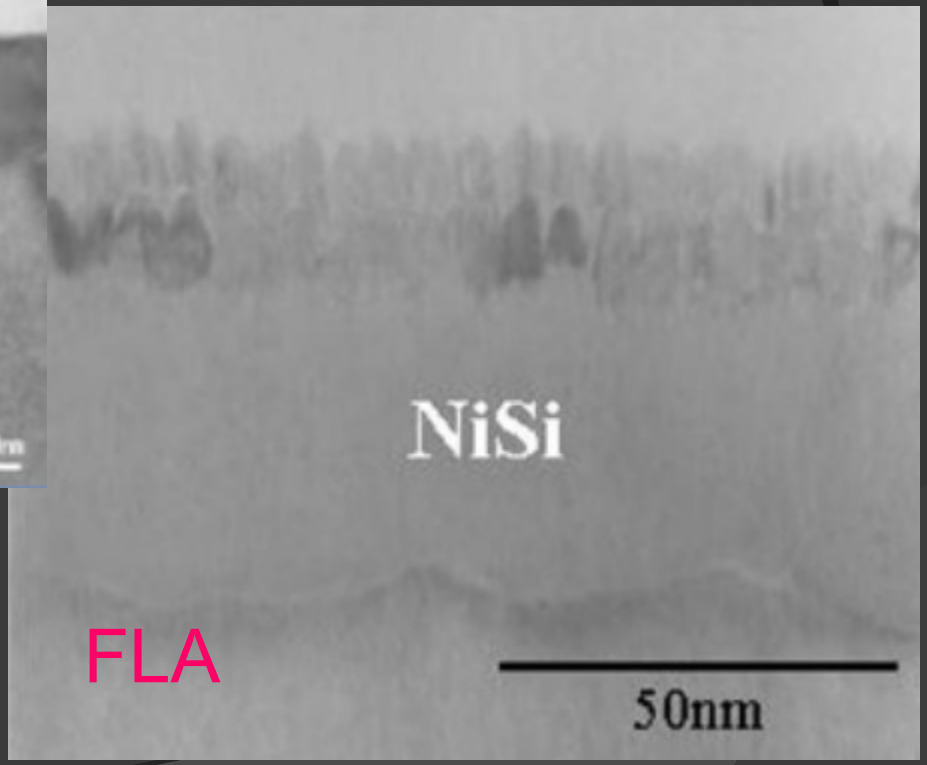
- NiSi reaction temperature is known as
  - $Ni_2Si$ : 200-300 c
  - NiSi : 320-600 c
  - $NiSi_2$ : over 600 c

- Ni start to react to $Ni_2Si$ at very low temperature.
- Over reaction of Ni will result in interface roughness and create the damage to device structure.
- To protect from over reaction of Ni, thermal budget control is very important.

# Ni Silicide

Using FLA, Si and NiSi interface became much smoother than that of RTP.

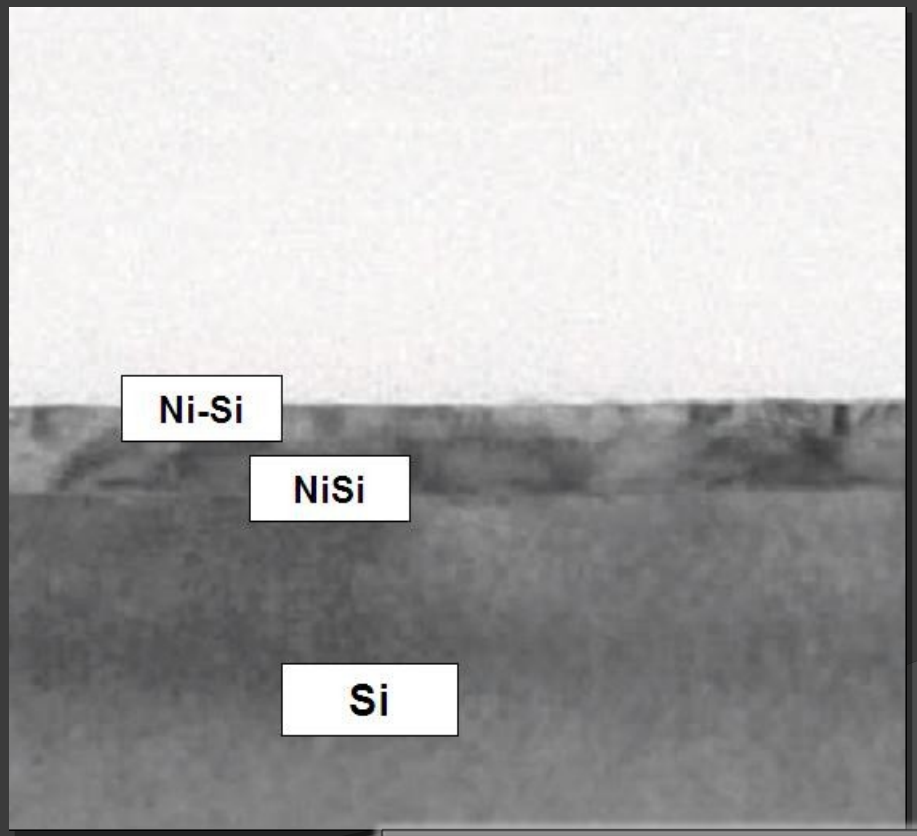



Data from SELETE 2004

# NiSi SEM Picture

NiSi formation by FLA.
Surface Ni remain as $Ni_xSi$

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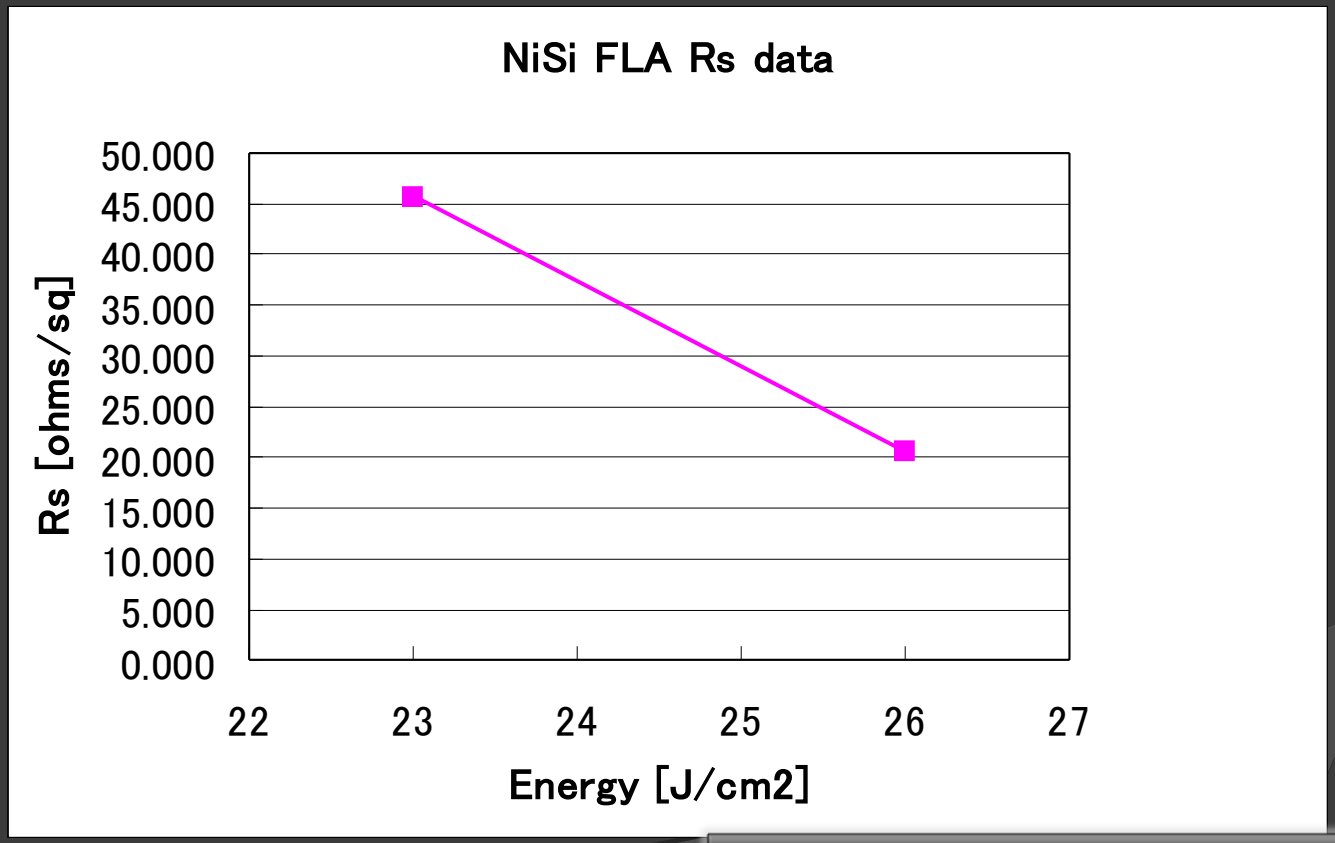
# Ni Silicide Rs Data

Higher flash power makes NiSi Rs go low.
Surface Ni and $Ni_xSi$ thickness decreases with higher flash power and NiSi thickness increases.

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# Silicidation

- FLA can create NiSi/Si interface much smoother than RTA because of its very short heating time.

- Flash time is millisecond order , but annealing time is enough for Ni-Si reaction.  Changing the flash power can control the process.

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- We have shown S/D activation capability of longer pulse. With longer pulse FLA we can realize no dopant diffusion and small thermal stress annealing.

- The Rs of Boron-implanted samples is reduced by Ge-PAI.
- The crystal grows from the a/c interface. The EOR defect remains near the a/c interface.
- The defects decrease with increasing FLA power or longer pulse.

- FLA is also available for silicide annealing method.

- FLA has a large capability to be a standard annealing technology for 45nm and future generation device manufacturing.